NTNU – Trondheim
Norwegian University of
Science and Technology

Design of Digital systems 1 TFE4141 - Assignment 1

Sindre Hansen Laurits Telle Riple

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Q1 What is $01000_2 + 01001_2$?

$01000_2 + 01001_2 = 10001_2 = 17$

Q2 Which number does 1111_2 represent

Q2a In 4-bit unsigned format?

$1111_2 = 15$

Q2b In 4-bit signed format (2's complement)?

To go from 2's complement to binary you invert every bit and add one. Thus, $1111_2 \rightarrow 0000_2 \rightarrow 0001_2$

Q3 What does "Dynamic range" in the context of number representation mean?

Dynamic range is the ratio between the largest and smallest values that a certain quantity can assume.

Q4 What has highest dynamic range of a 32 bit floating point number and a 32 bit fixed point number?

A floating point representation is similar to scientific notation, where you have a significand and an exponent. This allows you to have very large dynamic range.

Fixed point representation is less costly to implement than floating point, but you get a much smaller range of numbers.

Q5 How are floating point numbers and fixed point numbers spaced across the dynamic range?

With floating point numbers the numbers that can be represented is not uniformly spaced. They move further apart as the scale grows larger.

Fixed point numbers are evenly spaces across the range.

Q6 Add the numbers from Q1 in the same way as taught in school.

$$\begin{array}{r} {\scriptstyle 1} \\ 01000 \\ +01001 \\ \hline =10001 \end{array}$$

Q7 A boolean function can be constructed for computing the LSB in the addition of two fixed-point numbers (as done in Q6).

Q7a What is a boolean function?

A Boolean function is a function that returns either true or false (0 or 1).

Q7b Create a truth table for this Boolean function

A	B	S
0	0	0
0	1	1
1	0	1
1	1	0

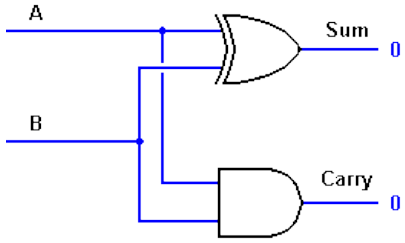
Q7c Create the Boolean function based on the truth table

A	B	S	SOP
0	0	0	$\overline{A}\overline{B}$
0	1	1	$\overline{A}B$
1	0	1	$A\overline{B}$
1	1	0	AB

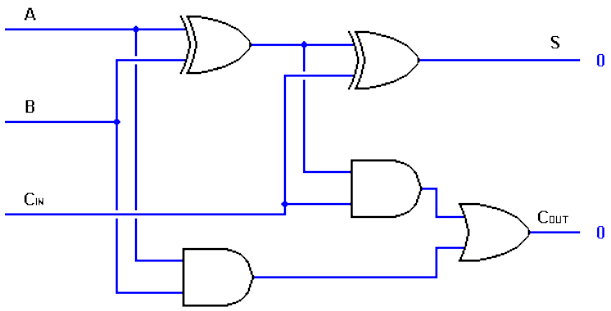
$\overline{A}\overline{B} + \overline{A}B + A\overline{B} + AB = A\overline{B} + \overline{A}B$

Q8 What is a half-adder and what is a full-adder?

A half adder takes two numbers, adds them and gives you the sum and any carry. It is easily implemented using an AND-gate and an XOR-gate.

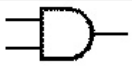
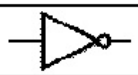
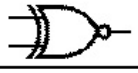


A full adder has three inputs, two numbers and a carry-in. It has two outputs, the sum and carry-out. This setup makes full-adders easy to chain together. We can implement the full-adder circuit using two half-adders.



Q9 Make something cool/useful out of full-adders and half-adders. Draw a diagram

Q10 Draw symbols for all the logic gates you can think of.

AND		$A \cdot B$
OR		$A + B$
NOT		$\overline{A}$
NAND		$\overline{A \cdot B}$
NOR		$\overline{A + B}$
XOR		$A \oplus B$
XNOR		$A \odot B$ or $\overline{A \oplus B}$

Q11 What is sequential logic?

Sequential logic is a type of logic circuit whose output depends not only on the present value of its input signals but on the sequence of past inputs, the input history.

Q12 What is combinational logic?

Combinational logic is a type of digital logic where the output is a function only of the present inputs.

Q13 D flip-flop

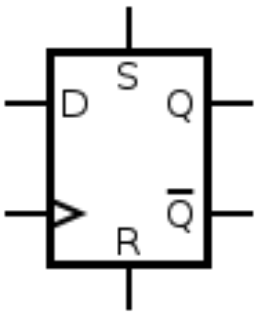
Q13a What is a D flip-flop?

The D flip-flop captures the value of the input at a spesific portion of the clock cycle. The captured value then becomes the output. The output is held at other parts of the clock cycle.

Truth table

Clock	D	Q_{next}
Rising edge	0	0
Rising edge	1	1
Non-rising	X	Q

Q13b Draw the symbol commonly used for representing a D flip-flop.



Q13c Find VHDL code for a D flip-flop with synchronous reset.

Here's VHDL code for a single positive edge triggered flip flop with synchronous reset from the module library.

```
1  library ieee;
2  use ieee.std_logic_1164.all;
3  use ieee.numeric_std.all;
4
5  entity dff_clr is
6    port (
7      clk : in std_logic;
8      reset_n : in std_logic;
9      d : in std_logic;
10     q : out std_logic);
11 end dff_clr;
12
13 architecture rtl of dff_clr is
14 begin
15   process(clk, reset_n)
16   begin
17     if (clk'event and clk='1') then
18       if(reset_n = '0') then
19         q <= '0';
20       else
21         q <= d;
22       end if;
23     end if;
24   end process;
25 end rtl;
```

Q14 Latch (The evil cousin of the D flip-flop)

Q14a What is latch?

A latch is basically an asynchronous storage element. It has no clock input. It differs from a flip-flop in that a flip-flop only changes its output in response to a clock edge. A latch can change its output in response to some other input regardless of the clock.

Q14b Try googling "unwanted latches".

There isn't really question here, but unwanted latches is what happens when there are some outputs that aren't assigned at every branch of the code. For

example if you specify the value in one condition but not in the other(s). For example,

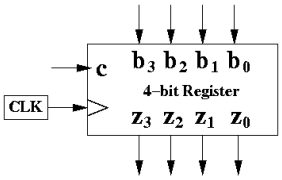
```
1 if a = '1' then
2     b(0) <= '1';
3 else
4     b(1 downto 0) <= "00";
5 end if;
```

Since the value of b(1) is not specified we would get an unwanted latch.

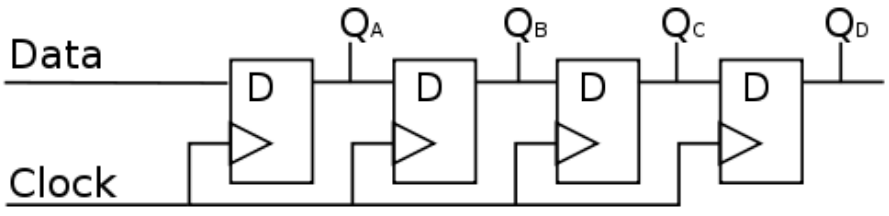
Q15 What is a register and how are registers related to D flip-flops?

A register is a form of low-level memory. It consists of a flip-flop for every bit it stores. There are several kinds of registers, but the simplest one is called a parallel load register.

Q16 Draw a 4-bit register



Q17 Draw a 4-bit shift-register

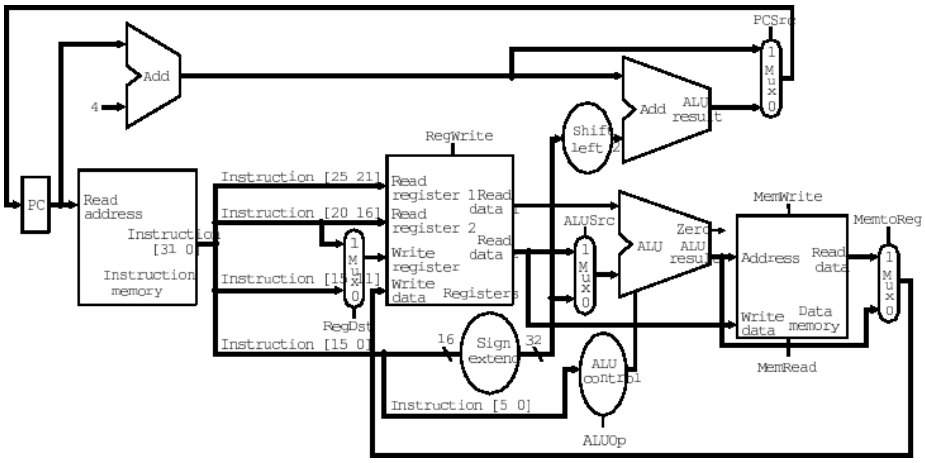


Q18 What is a Mux?

A multiplexer (or mux) is a device that selects one of several input signals and forwards the selected input into a single line.

Q19 Google "CPU datapath", print out one example Datapath and explain what we are looking at.

A CPU datapath shows how the functional units of a CPU work together. It typically consists of the program counter, the instruction register and data-/address memory register.



Q20 What is the purpose of pipelining in computing?

The purpose of pipelining is to increase throughput, typically in instructions per clock cycle.

Q21 What is logic synthesis?

Logic synthesis is a process by which an abstract form of desired circuit behavior is turned into a design implementation in terms of logic gates.

Q22 What is high-level synthesis?

High-level synthesis is an automated design process that interprets an algorithmic description of a desired behavior and creates digital hardware that implements that behavior.

Q23 What does EDA stand for in the context of digital design?

EDA stands for Electronic Design Automation.

Q24 What does "place & route" refer to?

In the context of FPGAs "place & route" refers to the placement and interconnection of logic elements on the grid of the FPGA.

Q25 What is static timing analysis (STA)?

Static timing analysis (STA) is a simulation method of computing the expected timing of a digital circuit without requiring a simulation of the full circuit.

Q26 Is negative slack a good thing?

Negative slack is not a good thing. It implies that a path is too slow and needs to be sped up if the whole circuit is to work at the desired speed.

Q27 What does "critical path" mean?

Critical path is the slowest logical path in the circuit, and determines the maximum possible clock rate.

Q28 What does the terms "setup-time" and "hold-time" for a flip-flop mean?

Setup time is the minimum amount of time the data input should be held steady before the clock event, so that the data is reliably sampled by the clock.

Hold time is the minimum amount of time the data input should be held steady after the clock event, so that the data is reliably sampled by the clock.

Q29 What does "design for testability" mean?

Designing for testability means to add testability features to the product design. The added features make it easier to develop and apply manufacturing tests to the designed hardware.

Q30 What is scan chain?

Scan chain is a technique used in design for testing. The objective is to make testing easier by providing a simple way to set and observe every flip-flop in a circuit.

Q31 What is formal verification?

Formal verification is when you prove or disprove an algorithm using formal methods of mathematics. It can be helpful in proving the correctness of systems such as cryptographic protocols and combinational circuits.

Q32 What is a state-machine and what role do they play in digital circuits?

A state-machine is a model used to design both computer programs and sequential logic circuits. A particular state-machine is defined by a list of its states, its initial state, and the triggering condition for transition.