NTNU – Trondheim
Norwegian University of
Science and Technology

Design of Digital systems 1 TFE4141 - Assignment 5

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Task 1: Draw a block diagram

Task 2: Simulate the circuit

The testbench gives the following inputs:

$$0x00000030000000200000001000000000 = 100925952$$
$$0x00000003000000020000000100000000 = 50462976$$

Which sums up to the following result:

$$0x00000033000000220000001100000000 = 151388928$$

Which look correct. So the adder is working!

Task 3: Count the number of flip flops that should be inferred during synthesis

Seems like the synthesised model is using 384 flipflops

Task 4: Synthesize the design and report the max clock frequency

We see that we get a negative slack og 1ns, but how does that transelate to 166Mhz? Ask the student assistent!

Task 5: Find the critical path in the design and improve timing

Task 6: Write RTL code, test and synthesize the new design