NTNU – Trondheim
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Design of Digital systems 1 TFE4141 - Assignment 4

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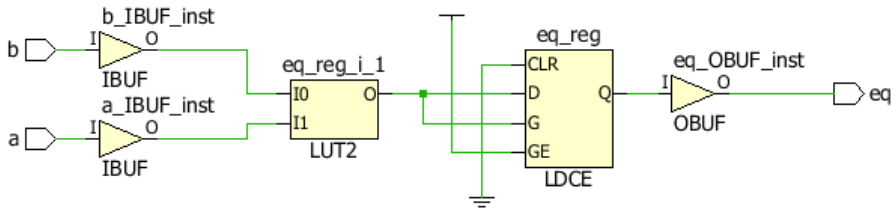
Task 1: Inferred latches

1.1



1.2

An example where a latch is unintentionally created is when you don't assign values to all output in every branch of an if-statement.

1.3

The way to make sure that latches are not generated from combinatorial processes is to always make sure that there are no incomplete branches, or incomplete signal assignments.

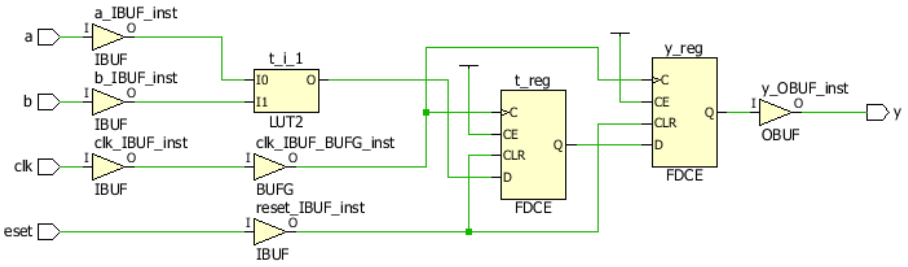
Task 2: Signals/variables and registers (flip-flops)

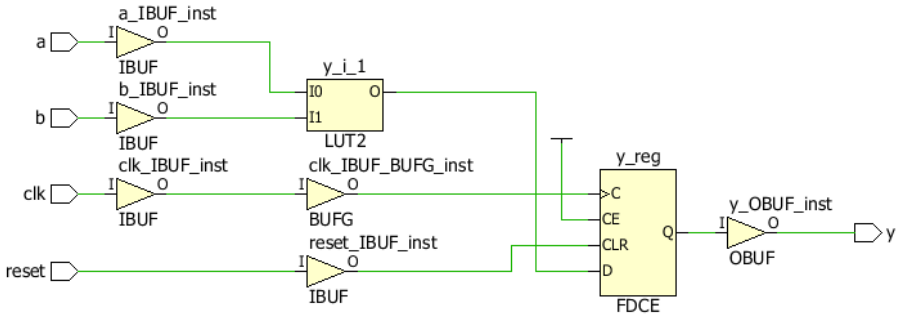
2.1

If we assume that on the first run the reset is held high then there's created a single flip-flop for 't' in both designs. However, if we on the next run assume that the reset is low, the difference in the two designs become clearer. Since design1 has the signal assignment before the variable assignment it needs to create another flip-flop for 't'. Therefore we end up with two flip-flops in the synthesis.

Design2 has the signal assignment after the variable assignment and therefore we end up with just one flip-flop in the synthesis.

2.2





2.3

There are two main requirements for a variable to be implemented as a register. One, it needs to be dependent of a clock and two, a variable needs to be assigned to a signal.

If you alter the variable after the last assignment to the signal a new register is created. It is this that happens in design1.

2.4

A variable is local to each process, its scope does not extend beyond the process. As such one can not read or write to it from another process. A signal is defined outside of the process and therefore it can safely be read from multiple processes. If one wishes to write to the signal you need to be careful with avoiding conflicts.

Task 3: Incomplete sensitivity lists

3.1

The reason that the process is not synthesizable is due to a security feature in Vivado. The reason for this security feature is to minimize differences between simulation and synthesis.

3.2

Yes, there is reason to suspect a difference between simulation and synthesization. The reason is that the synthesized circuit will be sensitive to signals that the simulation is not.

3.3

Make sure that every sensitivity list is updated with all signals it needs to react to.

Task 4: Combinational loops

4.1

A situation where oscillations from combinational loops are not discovered during simulation can occur if the signal that causes the oscillations is not included in the sensitivity list. E.g. if the signal b is not included in the sensitivity list in the following statement there would be no oscillation in the simulation, but there would be in the synthesis.

```
1 b <= a xor b;
2 y <= b;
```

4.2

It is permissible to have the same signal/variable on both sides of an assignment if ...