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NANOSCIENCE AND NANOTECHNOLOGY

PROJECT REPORT

FALL SEMESTER 2020

SLOT: C1

CNTFET AND GRAPHENE FET – STUDY OF CONSTRUCTION, WORKING, TYPES AND CHARACTERISTICS AND COMPARISON WITH CONVENTIONAL FET

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ABSTRACT

Carbon allotropes such as carbon nanotubes and graphene nanoribbons are of interest for use in solid state electronic devices. These structures have the potential for application in devices that require high performance and low power consumption. This paper addresses simulations that involve these two structures. Results of these simulations can be of use to experimentalists as well as manufacturers.

The Pz Orbital model is used to determine the band structure of graphene. Carbon nanotubes are briefly introduced as rolled strips of graphene, with orientation defined by a chiral vector. The Zone Folding Method is applied to single-layer graphene to provide a simulation model for plotting the band structure of carbon nanotubes in various orientations.

We demonstrated that the Pz Orbital model is sufficiently accurate for most carbon nanotubes. Graphene nanoribbons are also introduced, and are simulated using the Pz Orbital model. Edge states in graphene nanoribbons are addressed, including a discussion of why they are not observed in graphene.

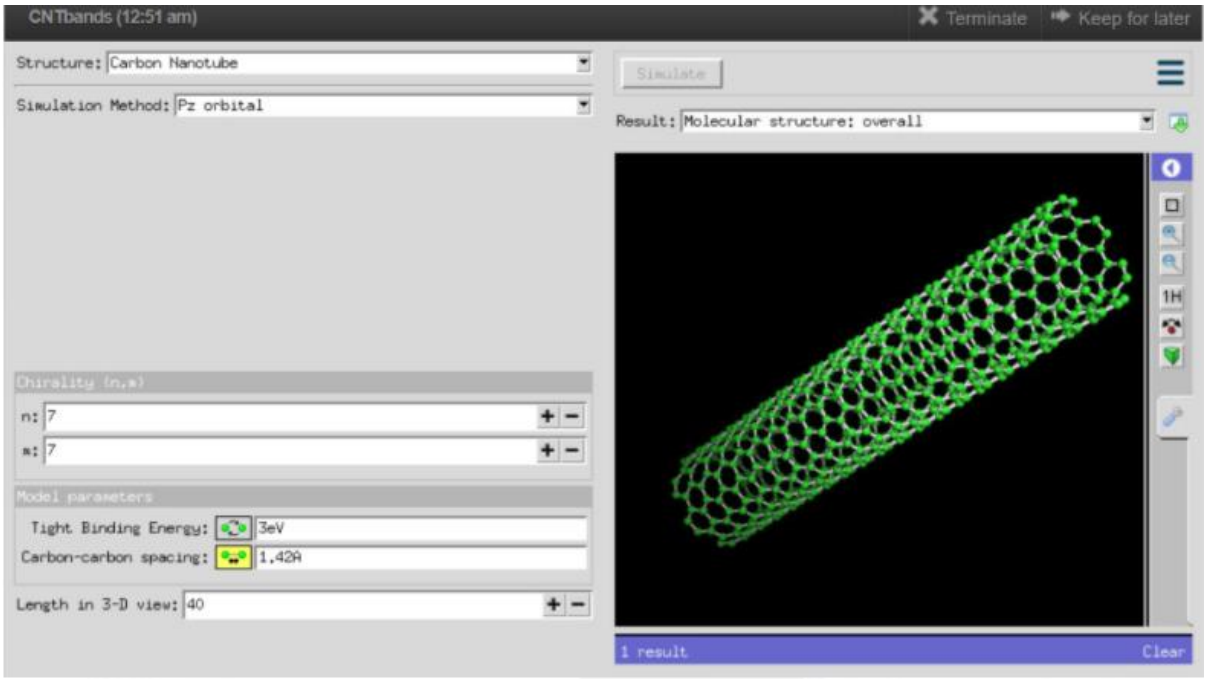
INTRODUCTION

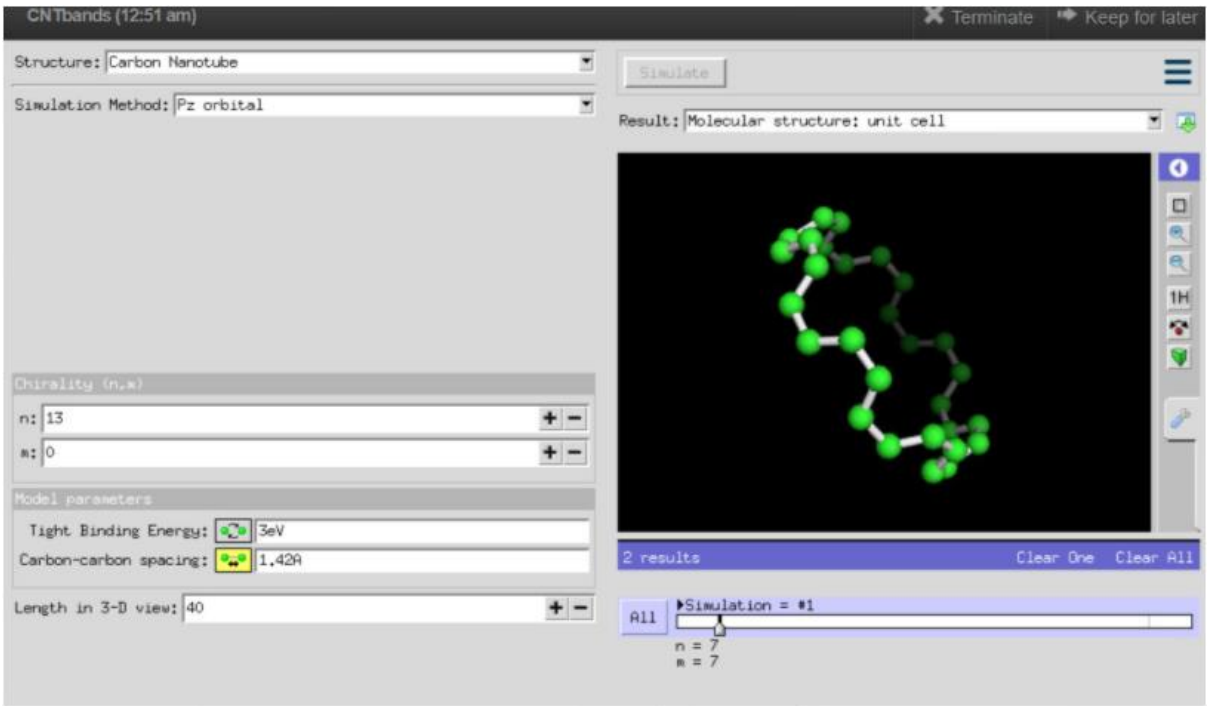
Carbon nanotubes (CNTs) are cylindrical molecules that consist of rolled-up sheets of single-layer carbon atoms (graphene). They can be single-walled (SWCNT) with a diameter of less than 1 nanometre (nm) or multi-walled (MWCNT), consisting of several concentrically interlinked nanotubes, with diameters reaching more than 100 nm. Their length can reach several micrometres or even millimetres.

Nanotubes can be formed in three different designs: Armchair, Chiral, and Zigzag. The design depends on the way the graphene is wrapped into a cylinder. For example, imagine rolling a sheet of paper from its corner, which can be considered one design, and a different design can be formed by rolling the paper from its edge. A single-walled nanotube's structure is represented by a pair of indices (n,m) called the chiral vector.

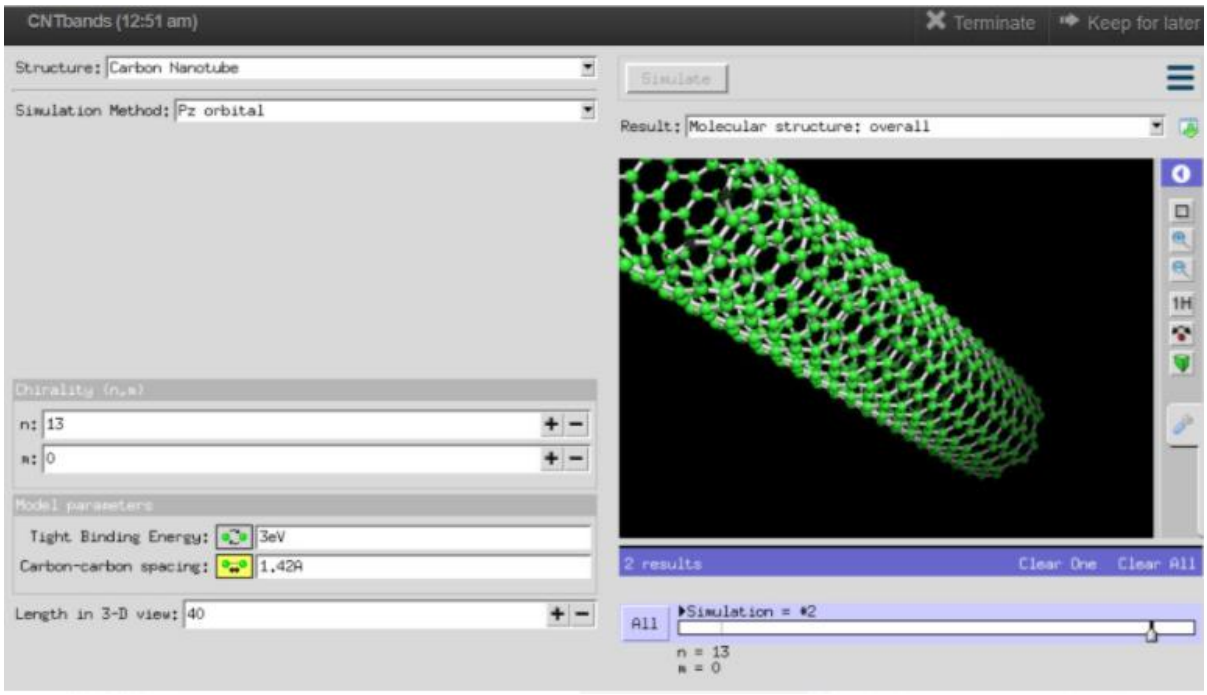
SIMULATIONS TO UNDERSTAND THE STRUCTURE OF CARBON NANOTUBE

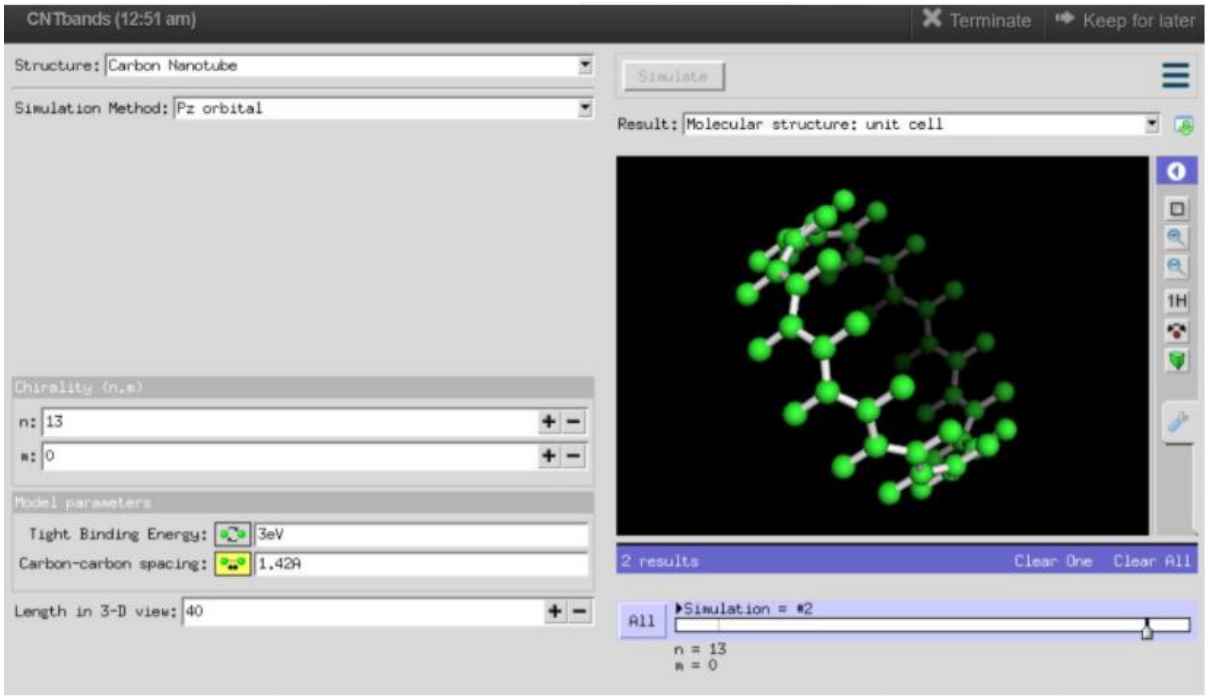
Armchair (n,m)=(5,5), θ=300 degree (metallic):



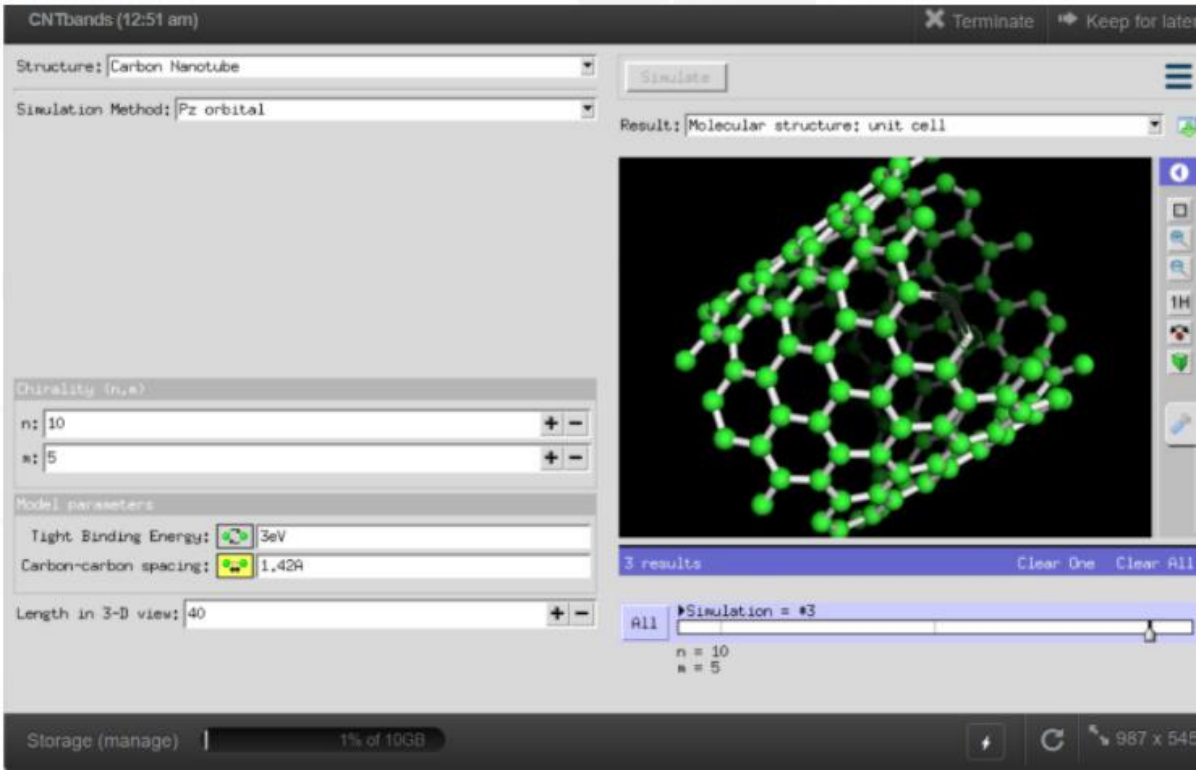


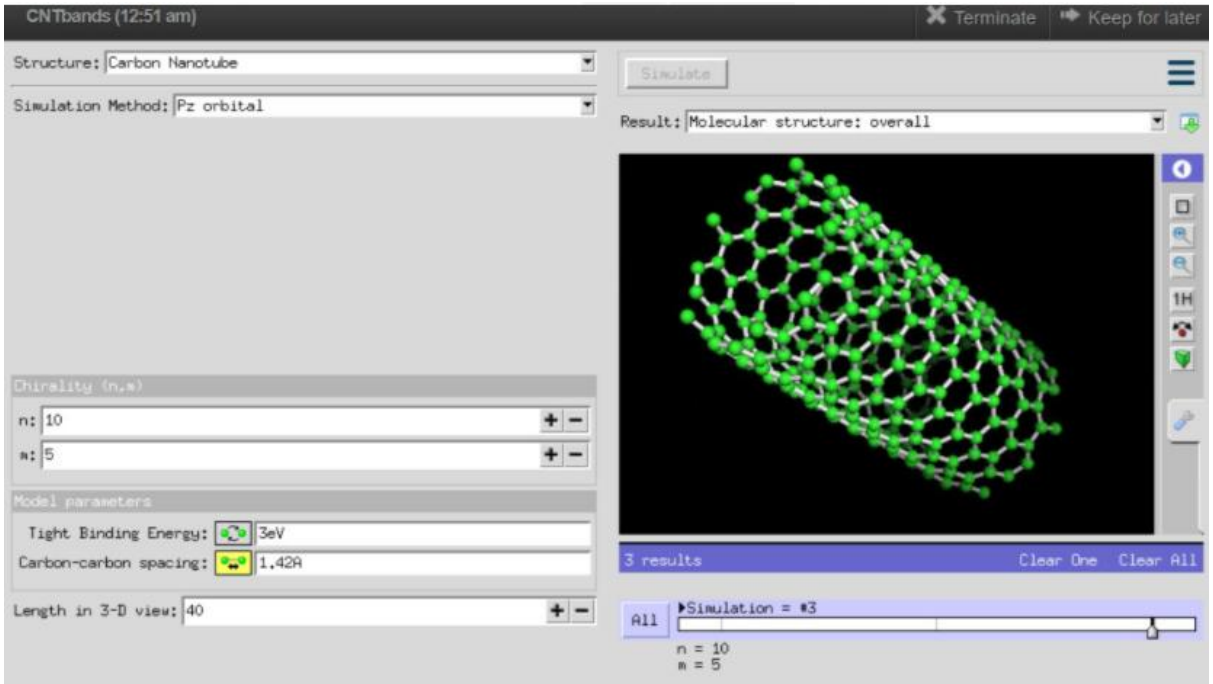
Zig Zag (n,m)=(9,0), θ=0 degree (semiconducting):





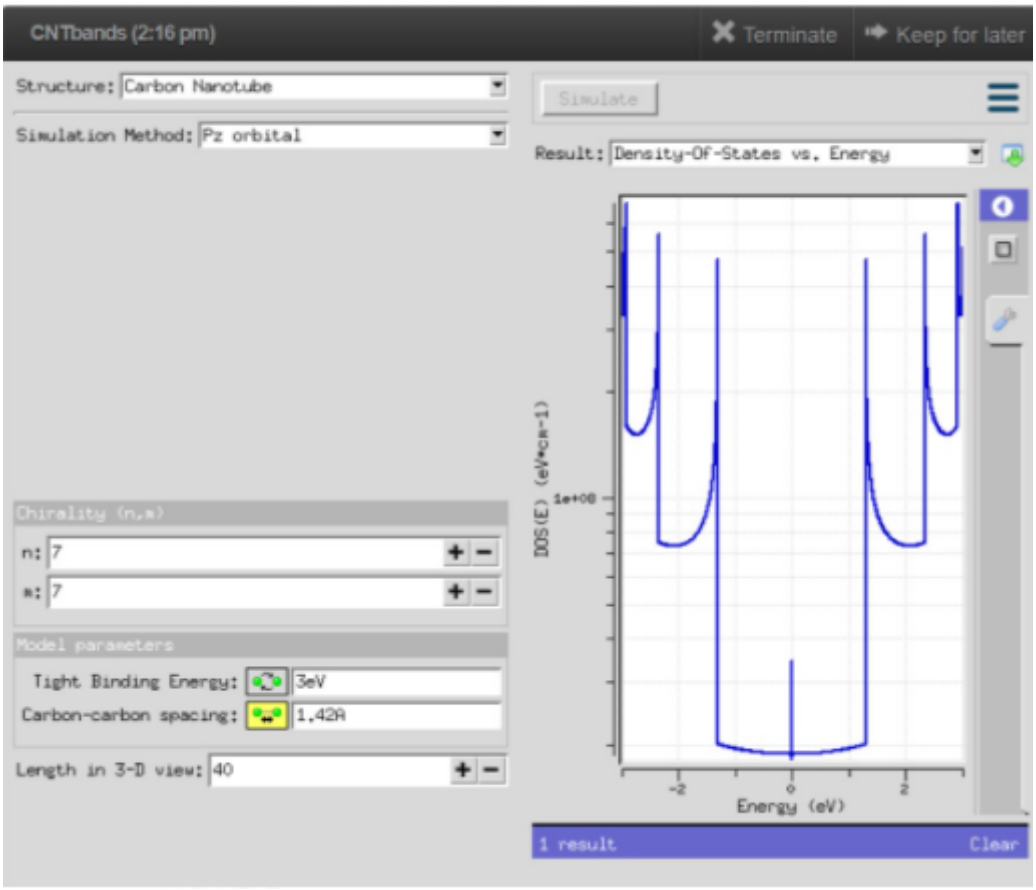
Chiral (n,m)=(10,5), 0 degree<θ :





CHARACTERISTIC ANALYSIS OF CNT ARMCHAIR (7,7)

DOS VS ENERGY:



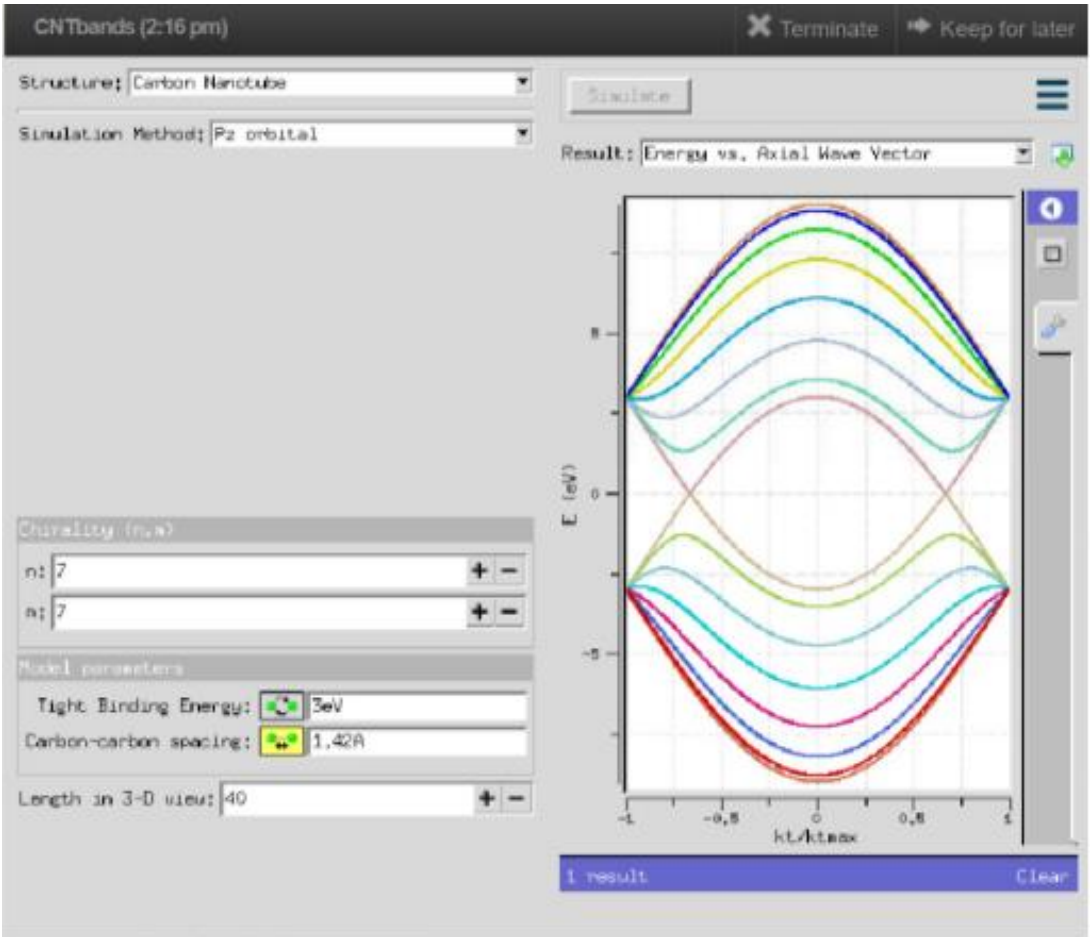
The DOS for the metallic carbon nanotubes (armchair) DOS may also be obtained but it is independent of their diameters as well as chirality because of the linear dispersion relations around the Fermi energy. The density of states (DOS) per unit length along the metallic carbon nanotube axis is constant given by $8/3\pi a_{c\text{-}c}t$.

It is observed that the DOS of PCNTs shows same typical features in one dimensional system. The DOS of semiconducting zigzag depends on the structure and diameter as shown in the graph. The continuous electronic density of states (DOS) in a CNT is divided into a series of spikes because of radial confinement of the wave function which is referred to as Van Hove singularities shown in the

wave. It may be seen in the graph that the universal relation for the armchair nanotubes has zero band gaps near the Fermi level.

At Fermi level the DOS between the two adjacent Van Hove singularities has some finite value for metallic tubes as shown in the graph while the DOS is zero at the Fermi level for semiconducting nature of zigzag tubes shown in graph. It may be noted that the zigzag tube (13, 0) is metallic in nature. It has been already verified through Scanning-Tunnelling Microscopy (STM) that the nanotubes that both metallic and semiconducting PCNTs possess DOS.

ENERGY VS AXIAL WAVE VECTOR:



In general (n, n) armchair carbon nanotubes yield 4n energy sub-bands by means of 2n conduction and 2n valence bands.

Out of these 2n bands, two are non-degenerate and n-1are doubly degenerate. The degeneracy comes from the two sub-bands with the same energy dispersion but with different ν - values. all armchair carbon nanotubes have band degeneracy between the highest valence and the lowest conduction band. Further it may be seen that for the tube of about the same diameter with different chirality shall have about the same band gap. Therefore, it is clear that the band gap of the semiconducting tubes depends inversely upon the diameter. The armchair (n, n) tubes band gap of the order of 0.011eV remain independent of diameter.

The bands in each armchair cross the Fermi level at $k = \pm 2\pi/3a$ thus they are considered to exhibit metallic behaviour. There is no energy gap of the order of $\approx$ 0.011 eV for armchairs.

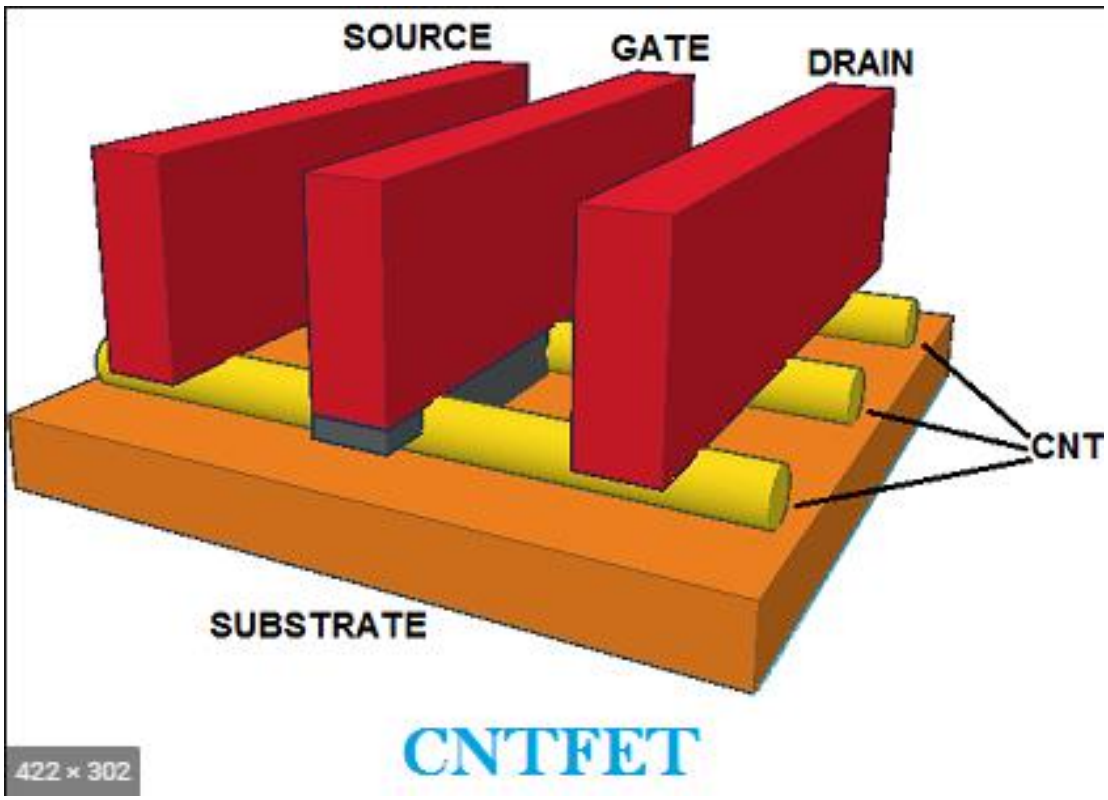
CNTFET (Carbon Nano-tube Field Effect Transistor)

CNTFETs (Carbon Nanotube Field Effect Transistors) are novel devices that are expected to sustain the transistor scalability while increasing its performance. One of the major differences between CNTFETs and MOSFETs is that the channel of the devices is formed by Carbon Nano-Tubes (CNTs) instead of silicon, which enables a higher drive current density, due to the larger current carrier mobility in CNTs compared to bulk silicon. In particular, with CNTs we obtain good operation even at very high frequencies.

A carbon nanotube field-effect transistor (CNTFET) refers to a field-effect transistor that utilizes a single carbon nanotube or an array of carbon nanotubes as the channel material instead of bulk silicon in the traditional MOSFET structure. Carbon Nano-tube Field Effect Transistors (CNTFET) are promising nano-scaled devices for implementing high performance very dense and low power circuits. The core of a CNTFET is a carbon nano-tube. Carbon nanotube field effect transistor (CNTFETs) uses semi conducting carbon nanotube as the channel.

The physical structure of CNTFETs is very similar to that of MOSFETs and their I-V characteristics and transfer characteristics are also very promising and they suggest that CNTFETs have the potential to be a successful replacement of MOSFETs in nanoscale electronics.

The first carbon nanotube field-effect transistors were reported in 1998. These were simple devices fabricated by depositing single-wall CNTs (synthesized by laser ablation) from solution onto oxidized Si wafers which had been prepatterned with gold or platinum electrodes. The electrodes served as source and drain, connected via the nanotube channel, and the doped Si substrate served as the gate.



Working principle:

Basic principle operation of CNTFET is the same as MOSFET where electrons are supplied by source terminal and drain terminal will collect these electrons. In other words, current is actually flowing from drain to source terminal. Gate terminal controls current intensity in the transistor channel and the transistor is in off state if no gate voltage is applied.

CNTFET TYPE:

- **Based on geometry**

1) **Top Gate**
2) **2) Back Gate**
3) **3) Coaxial Gate**

• Based on operation

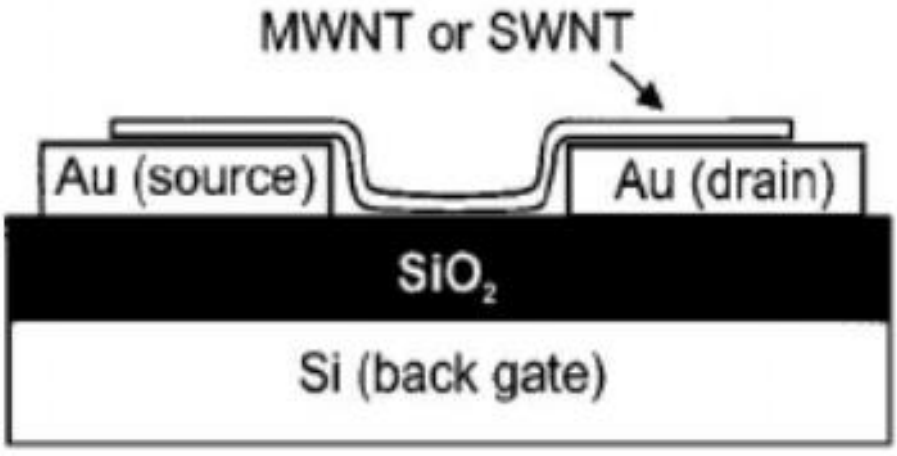
1) Schottky barrier

2) MOSFET

BACK-GATE CNTFET

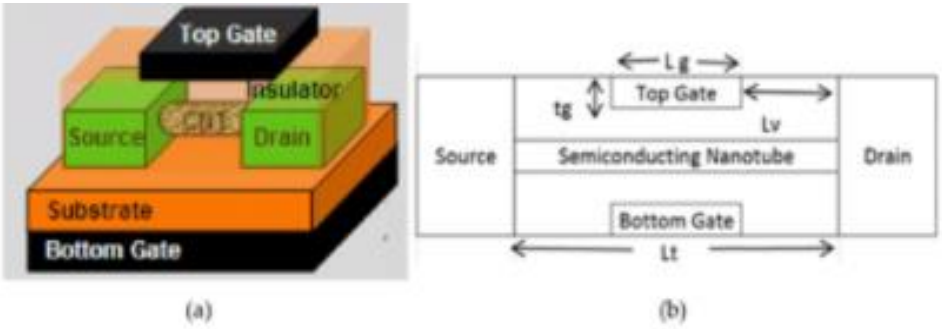
The earliest techniques for fabricating carbon nanotube (CNT) field-effect transistors involved pre-patterning parallel strips of metal across a silicon dioxide substrate, and then depositing the CNTs on top in a random pattern. The semiconducting CNTs that happened to fall across two metal strips meet all the requirements necessary for a rudimentary field-effect transistor. One metal strip is the "source" contact while the other is the "drain" contact. The silicon oxide substrate can be used as the gate oxide and adding a metal contact on the back makes the semiconducting CNT gate able. The devices displayed high on-state resistance of several MQ, low transconductance (-1,,) and no current saturation, and they required high gate voltages (several volts) to turn them on.

[6]



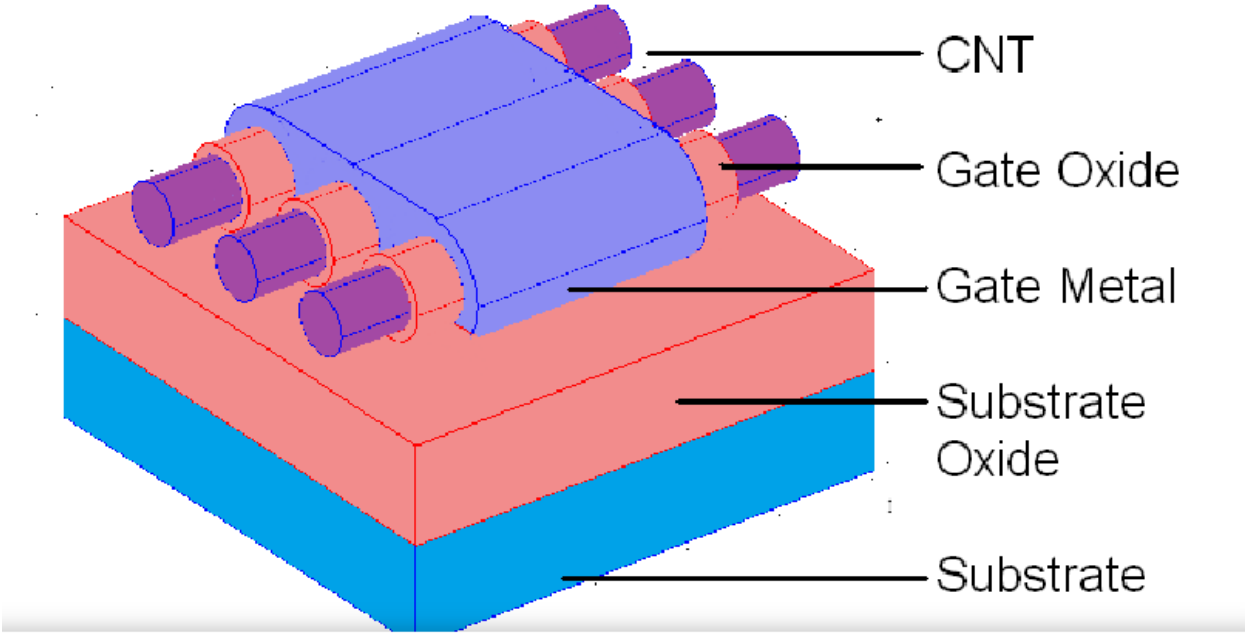
TOP GATE CNTFET

The next generation of CNTFET came in top-gate structure to improve the device performance. This structure gives better out-turn than early structure. The improvement comes from the scaling of the dimension and the adoption of better device geometry as well as the device performance.



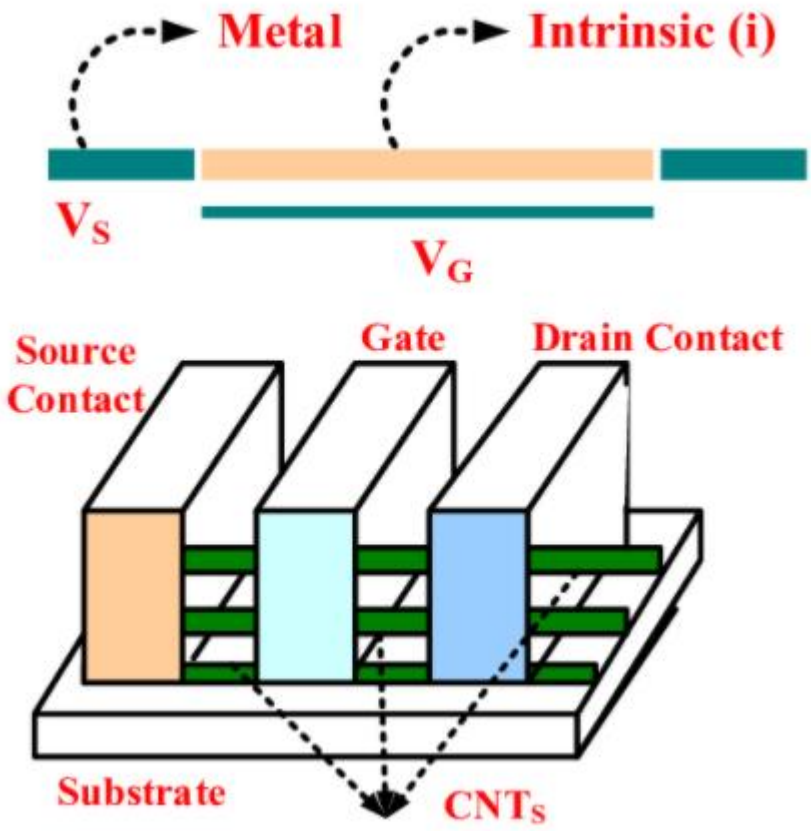
WRAP-AROUND GATE CNTFET

Wrap-around gate CNTFETs, also known as gate-all-around CNTFETs were developed in 2008, and are a further improvement upon the top-gate device geometry. In this device, instead of gating just the part of the CNT that is closer to the metal gate contact, the entire circumference of the nanotube is gated. This should ideally improve the electrical performance of the CNTFET, reducing leakage current and improving the device on/off ratio.



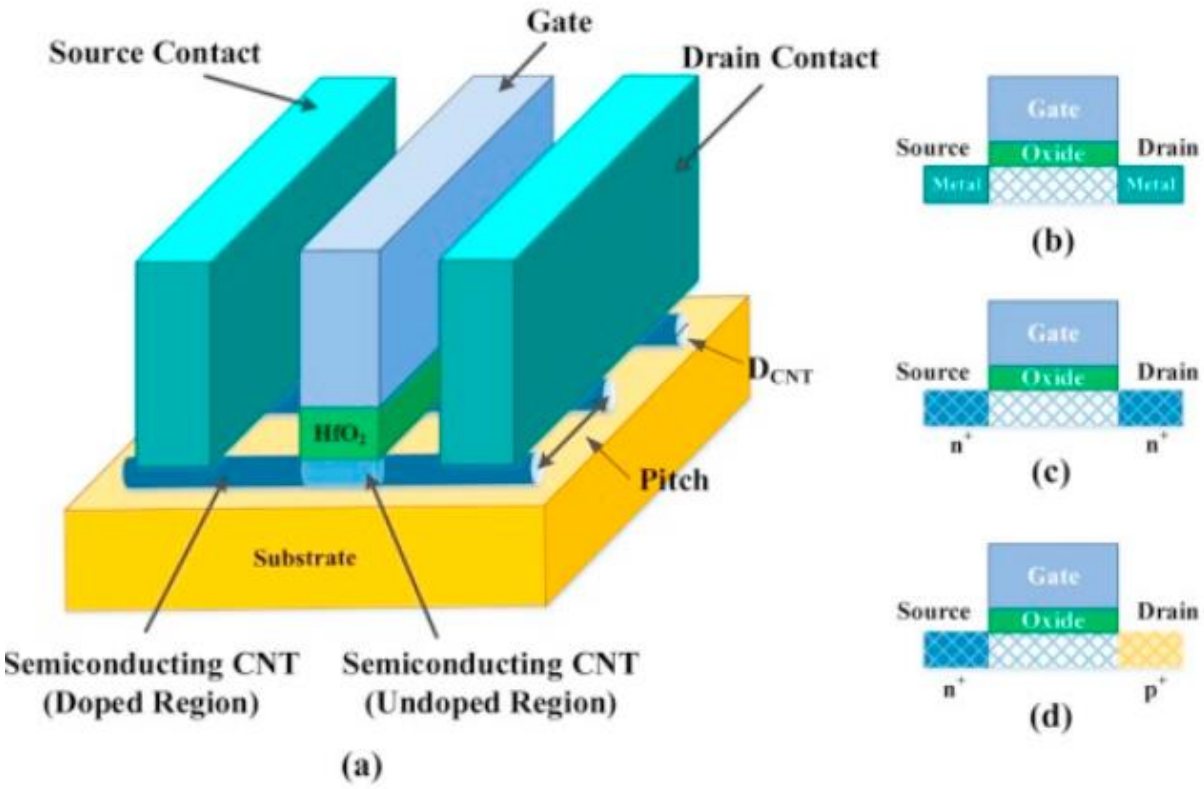
SCHOTTKY BARRIER CNTFET SB-CNFET

It works on the principle of direct tunnelling through the Schottky barrier at the source channel junction. The barrier width is controlled by the gate voltage and hence the trans conductance of the device depends on the gate voltage. At low gate bias, large barrier limits the current in the channel. As gate bias is increased, it reduces the barrier width, which increases quantum mechanical tunnelling through the barrier, and therefore increases current flow in transistor channel. In SBCNFET, the transistor action occurs by modulating the transmission coefficient of the device.



MOSFET like CNTFET

The structure of this device is slightly different than SB-CNTFET since it used heavily doped terminals instead of metal. This device operates on the principle of modulation of the barrier height by gate voltage application. The drain current is controlled by the charge that is induced in the channel by gate terminal.



What impacts on operation and performance of CNTFET?

♣ Contacts: Schottky barrier height depends on metal contact work function. Adhesion between metal and CNT also important since a tunnelling barrier forms that limits the current.

♣ Dielectric: Choosing a dielectric for CNTFETs is not related to Fermi level pinning or passivating surface states.

♣ The most common fabrication method for depositing high quality high-K dielectrics is atomic layer deposition (ALD)

♣ High-k dielectric materials can provide efficient charge injection to channel.

♣ Reduces direct tunnelling.

♣ Provides high gate capacitance.

CNTFET I-V CHARACTERISTICS

The Landauer Formula:

Landauer Formula is really useful in order to compute current in nanoscale devices. In nano-scale electronic devices, the wavelength of traveling electrons are of the order of the scale of device, so the electronic motion has to be considered with reflection and transmission concepts. The probability of an electron having energy E to transmit into the device is called as transmission probability T(E). Transmission spectrum is the name given to the function T(E) for the whole energy range. The number of electrons flowing through the device is given using quantum mechanical treatments. The electrons in the channel does not suffer any scattering mechanism, i.e. transport in the channel is ballistic, and that the electrons entering the reservoirs contacts are instantaneously in equilibrium with them. The current density (J) provided by the electrons injected into the nano scale device from left hand side is given by:

$$J = 2qn(k)v(k)T(k)dk$$

Where q is a charge of an electron, n(k) is the number of electrons with wave vector k and flowing from left to right, v(k) is velocity of electrons having wave vector k and flowing from left to right and T(k) is transmission probability of electrons traveling from to left hand side to right hand side of nano scale device.

$$J = 4\pi q\ h\ \mu 2 \int D(E)(f1(E) - f2(E))T(E)dE\ \mu 1$$

The above expression for current density is referred to be Landauer's formula and is used for the calculation of the current-voltage characteristics of the nano scale electronic devices.

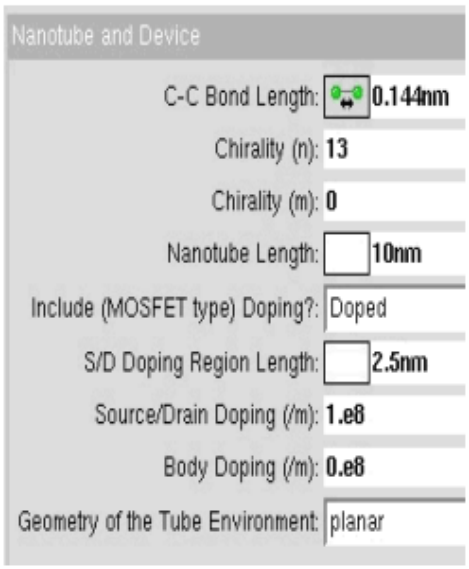
SIMULATION OF I-V CHARACTERISTICS OF PLANAR CNTFET

CNTFET lab tool calculates the ballistic I-V characteristics for the typical MOSFET design planar and coaxial CNTFET. The application is based on Non-Equilibrium Green's Function (NEGF) technique. We have varied the following parameters:

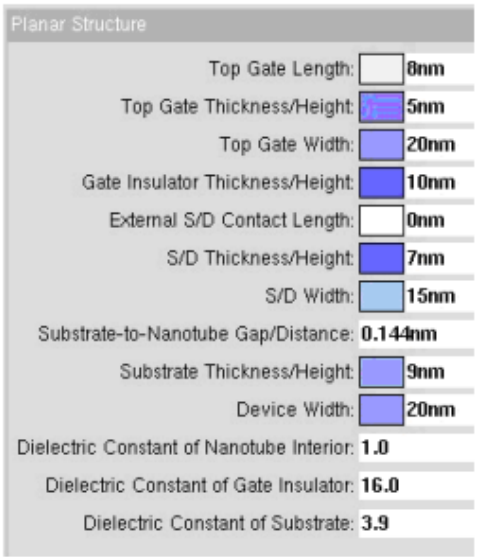
- **CNT Diameter**
- **Gate insulator material**

Gate thickness Software used:

- **CNTFET LAB tool**
- **FETTOY tool**
- **CNTBANDS 2.0 tool**



Parameters of CNT used in CNTFET



Parameters of planar CNTFET

CNTFET LAB tool Window

All the above tools are available on: www.nanohub.org

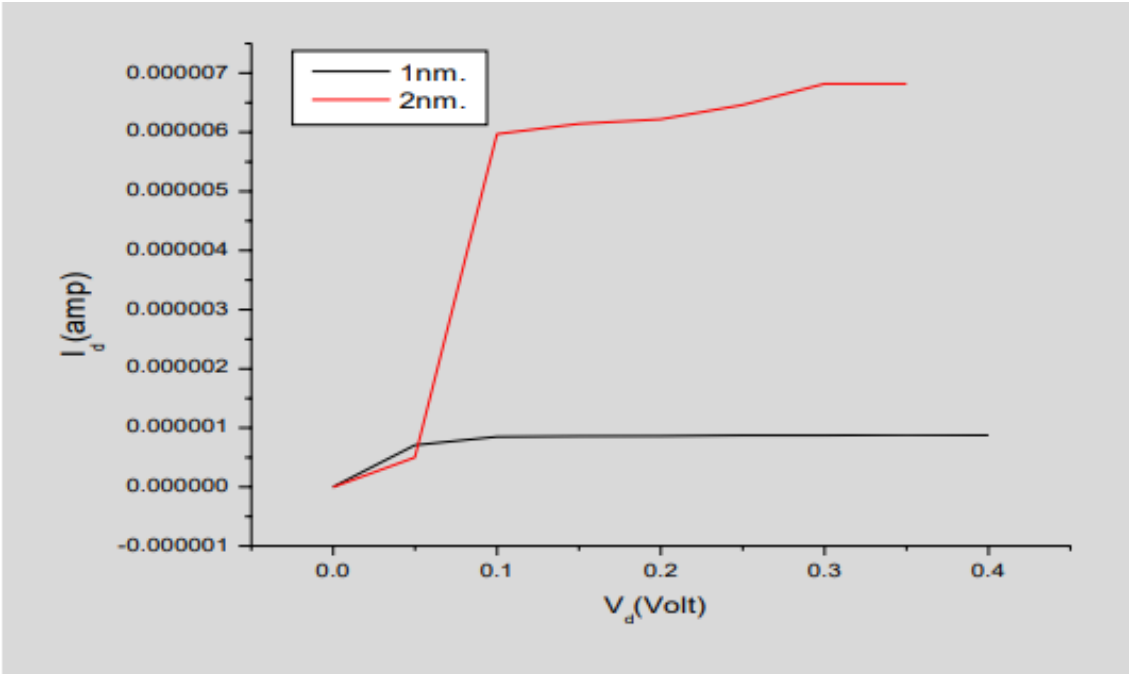
For variation in diameter (Chirality):

Diameter of CNT depends on the chirality of the CNT. It is given by:

$$d = \frac{a\sqrt{3(n^2 + mn + m^2)}}{\pi}$$

The doped CNT is used as a channel with gate insulator as Hafnium Dioxide(K=16) and oxide thickness is kept at 10nm. Here we have taken results for the following diameters by varying the chirality values:

- **1nm**
- **2nm**



Inference:

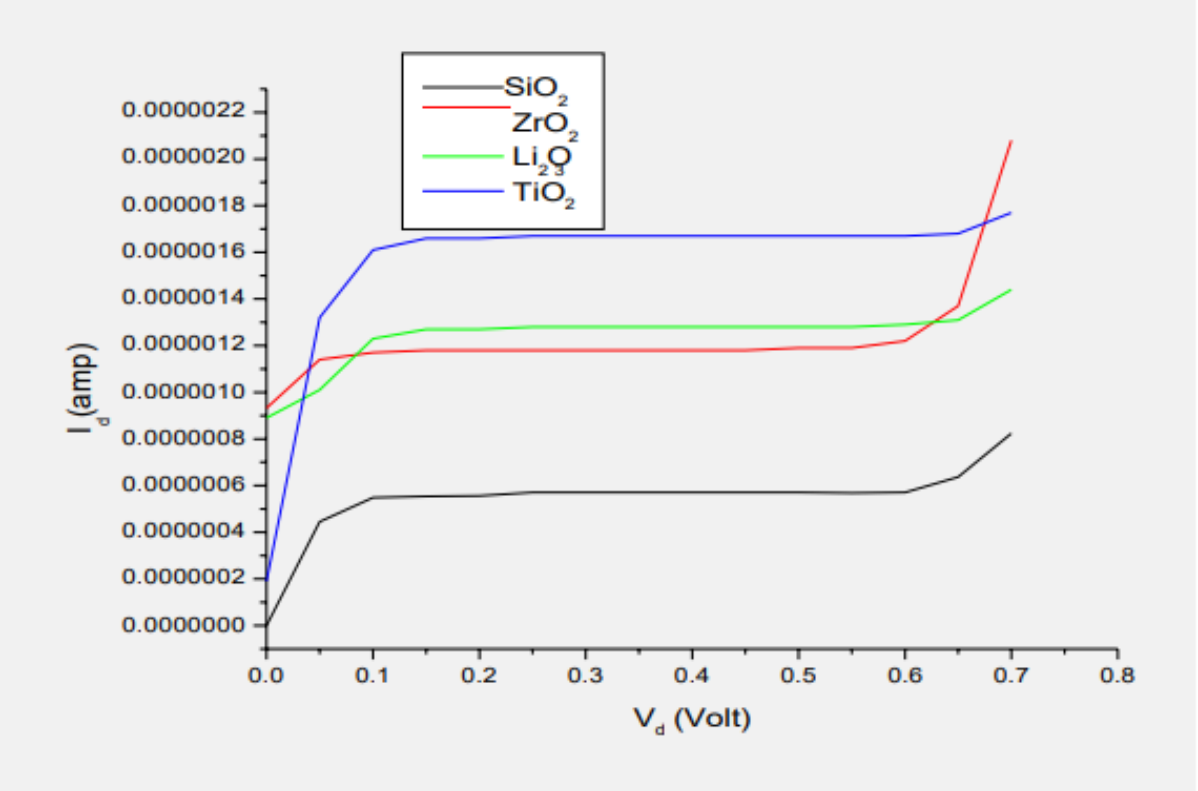
The current increases with increase in the value of diameter. Large diameter of CNT leads to smaller band gap, it will increase the current which leads to higher drain current and faster switching speed due to smaller band gap. Energy band gap is given by:

$$Eg = \frac{0.8eV}{d(nm)}$$

For variation in gate material:

Different gate materials with different dielectric constants have been taken. By keeping all other parameters such as diameter of CNT of 1nm and oxide thickness of 9nm constant, the graph has been plotted for the following dielectrics:

- **SiO2 (k=3.9)**
- **ZrO2 (k=25)**
- **Li2O3(k=30)**
- **TiO2 (k=80)**



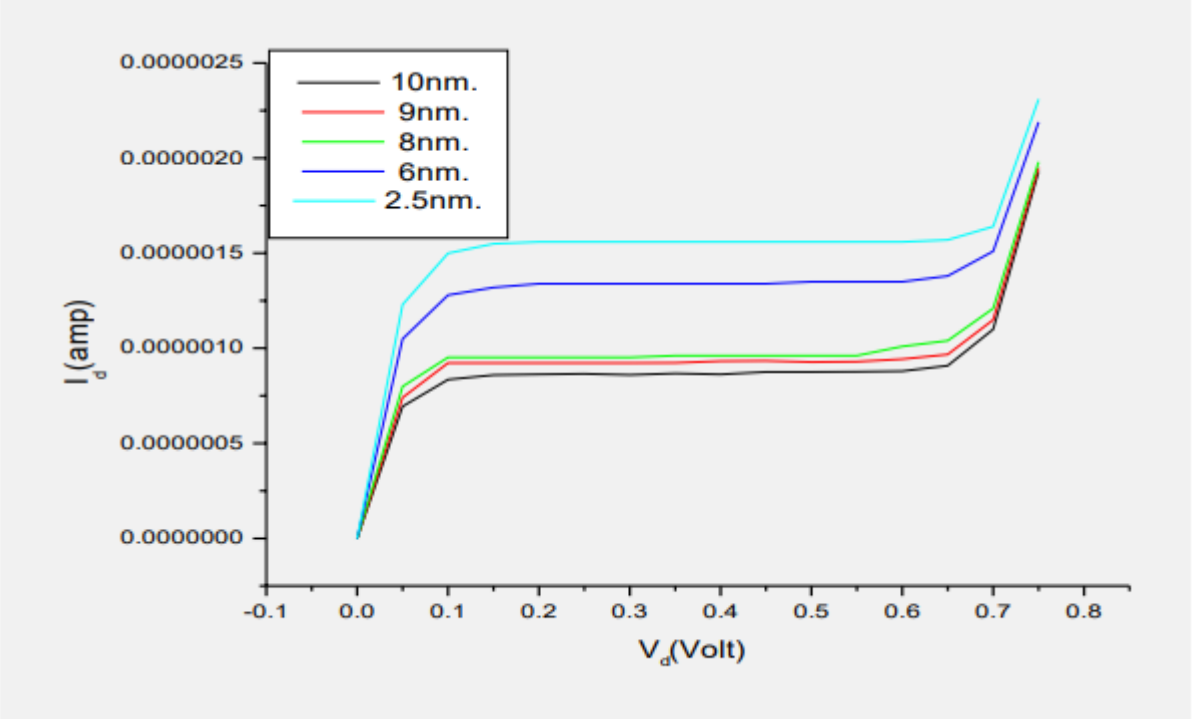
Inference:

Changing the dielectric constant has a vital effect on the output drain current. It is evident from the plot that the saturation current increases for increases for increasing dielectric constants. But degree of this positive effect reduces as we go for higher dielectric material. This means that we are going for higher and higher dielectric material the increment in drain current (Id) w.r.t. k reduces.

For variation in gate thickness:

By keeping all other parameters, gate insulator of HfO2(k=16) and diameter of 1nm constant we have plotted the I-V characteristics for the following gate insulator thicknesses:

- **2.5nm,**
- **6nm,**
- **8nm,**
- **9nm and**
- **10nm**

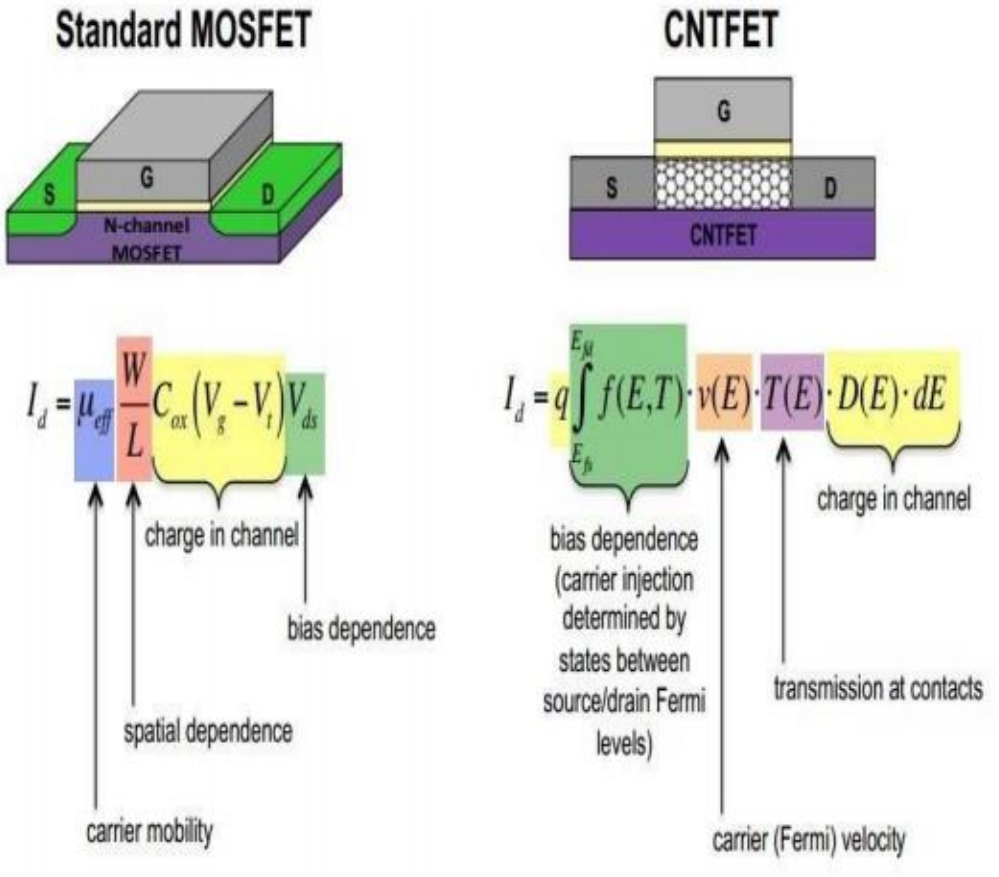


Inference:

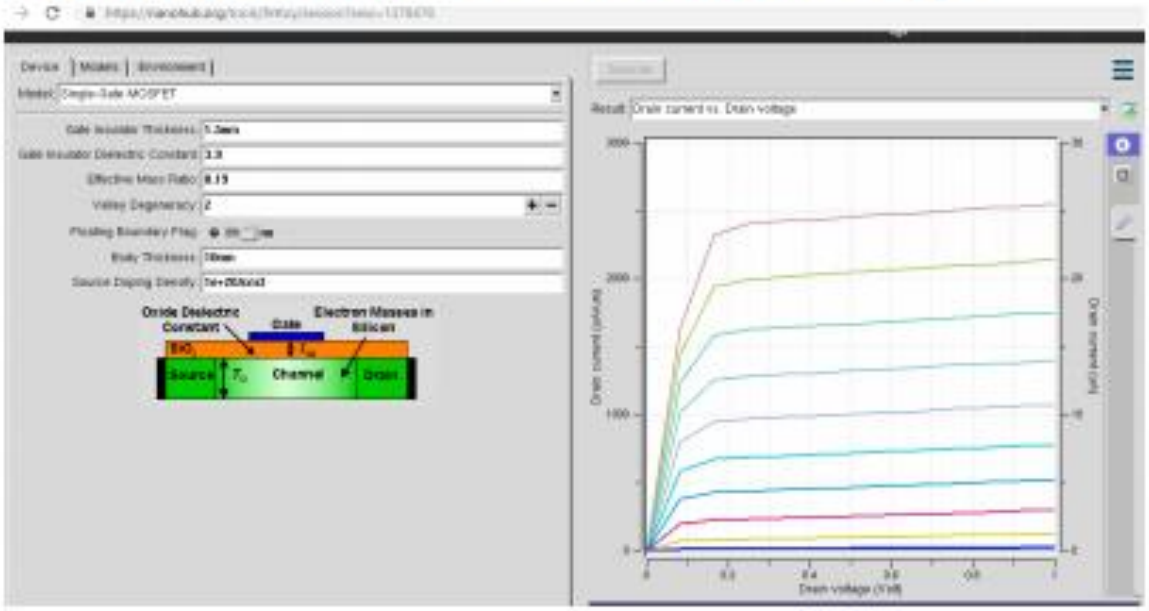
Lower the value of thickness of gate, higher will be the saturation current. It means that when we reduce the gate insulator thickness, the current capability of CNTFET enhances. This shows that the conductivity of CNTFET is inversely proportional to the thickness of gate insulator.

Comparison Between MOSFET and CNTFET

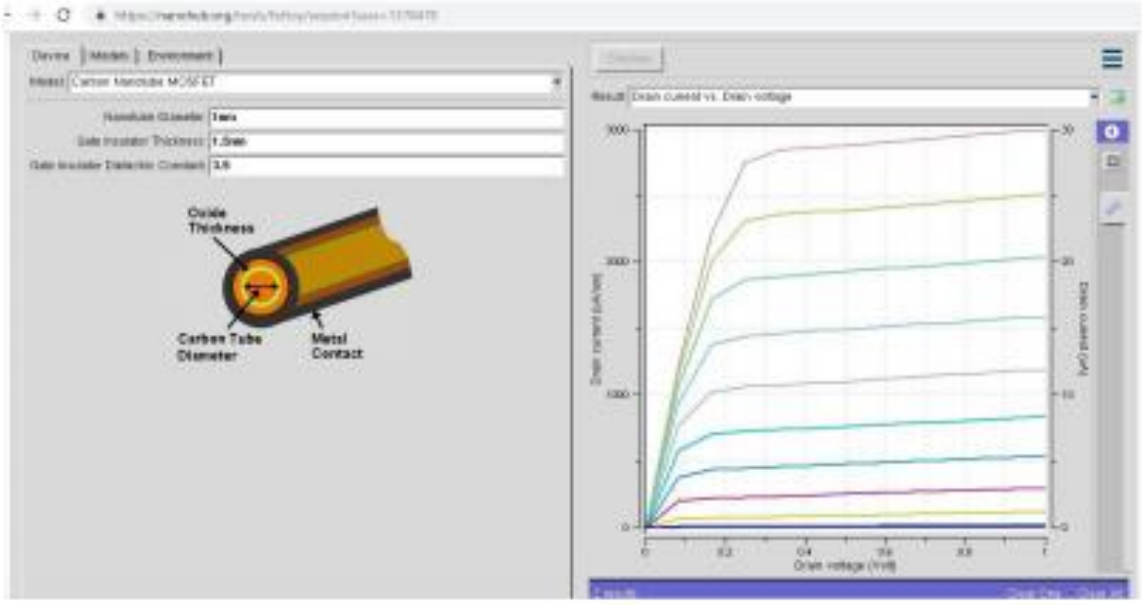
characteristics	Carbon nanotube MOSFET	Silicon nanowire MOSFET	Single gate MOSFET
I_D VS V_G	low	high	high
I_D VS V_D	Moderate slope	Minimum slope	Maximum slope
Mobile charge density VS V_G	low	high	high
Quantum capacitane VS V_G	minimum	high	high



I_d vs V_d GRAPH of MOSFET for different Gate Voltages



I_d vs V_d GRAPH of CNTFET for different Gate Voltages



Inference:

It is evident from the graph that the saturation currents for different gate voltages is more in CNTFET as compared to MOSFET. Hence CNTFET have current density.

Drawbacks of MOSFET:

• Short Channel Effects (Drain-Induced Barrier Lowering, Surface Scattering, Velocity Saturation, Impact Ionization, Hot Carrier Injection)

• High Leakage Current

• Excessive process variation

• Reliability issues

• As the size becomes smaller, scaling the silicon MOSFET becomes harder.

Advantages of CNTFET over MOSFET:

• High transconductance. This property determines the performance of any FET. A higher transconductance results in greater gain or amplification.

• Ballistic transport: The carbon nanotube is one-dimensional, which greatly reduces the scattering probability. As a result, the device may operate in ballistic regime. The nanotube conducts essentially on its surface where all the chemical bonds are saturated and stable. In other words, there are no dangling bonds which form interface states. Therefore, there is no need for careful passivation of the interface between the nanotube channel and the gate dielectric, i.e. there is no equivalent of the silicon/silicon dioxide interface. Negligible resistance. This property results in high speed devices.

• High current density

• Superior subthreshold slope. This property is very important for low power applications.

• Superior threshold voltage

$$C_{ox} = 2\pi\varepsilon \frac{L_g}{\ln(\frac{t_{ox} + r_{cnt}}{r_{cnt}})}$$

$t_{ox} = Gate\ dielectric\ thickness$

• High mobility

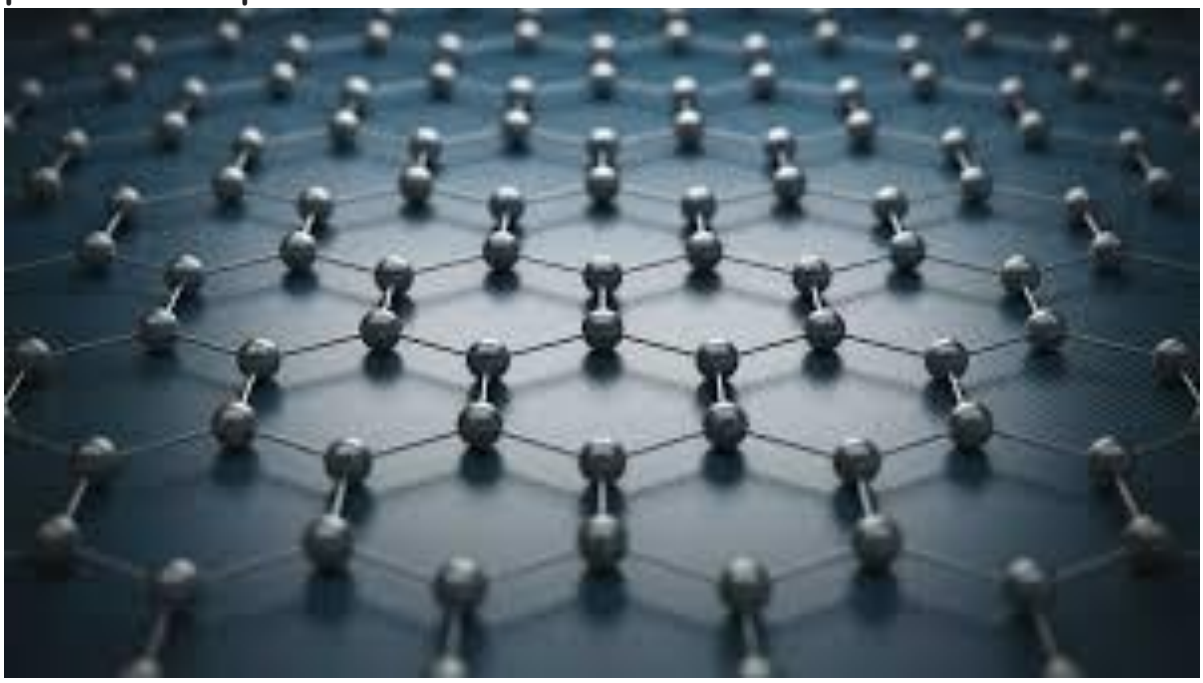
• High I_{on} / I_{off} current ratios • Have lesser quantum capacitance than MOSFETε=Dielectric constant, L_g=Gate length, r_{cnt} = nanotube diameter.

GRAPHENE:

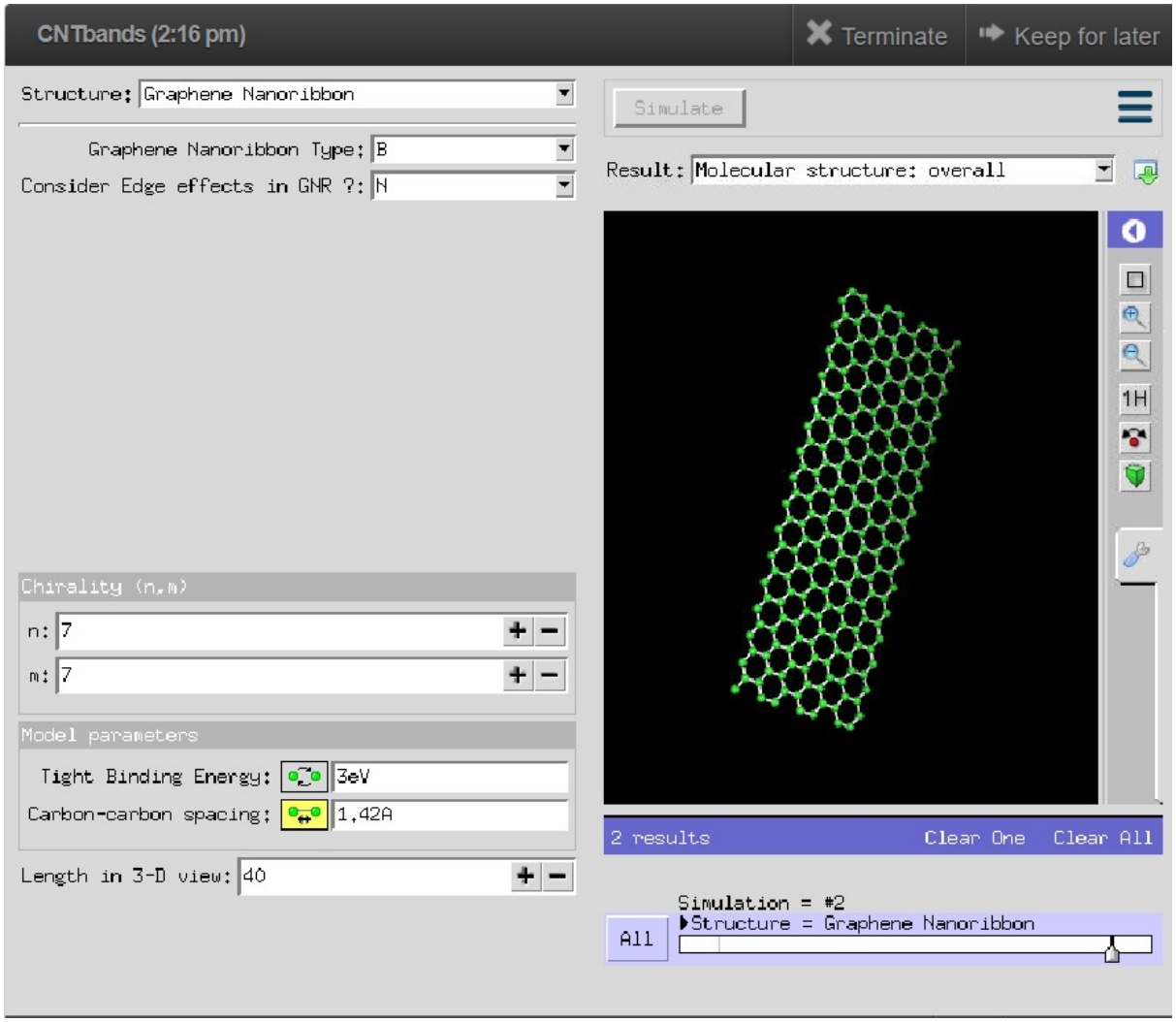
Graphene is a semimetal with small overlap between the valence and the conduction bands. It is an allotrope of carbon consisting of a single layer of carbon atoms arranged in a hexagonal lattice.

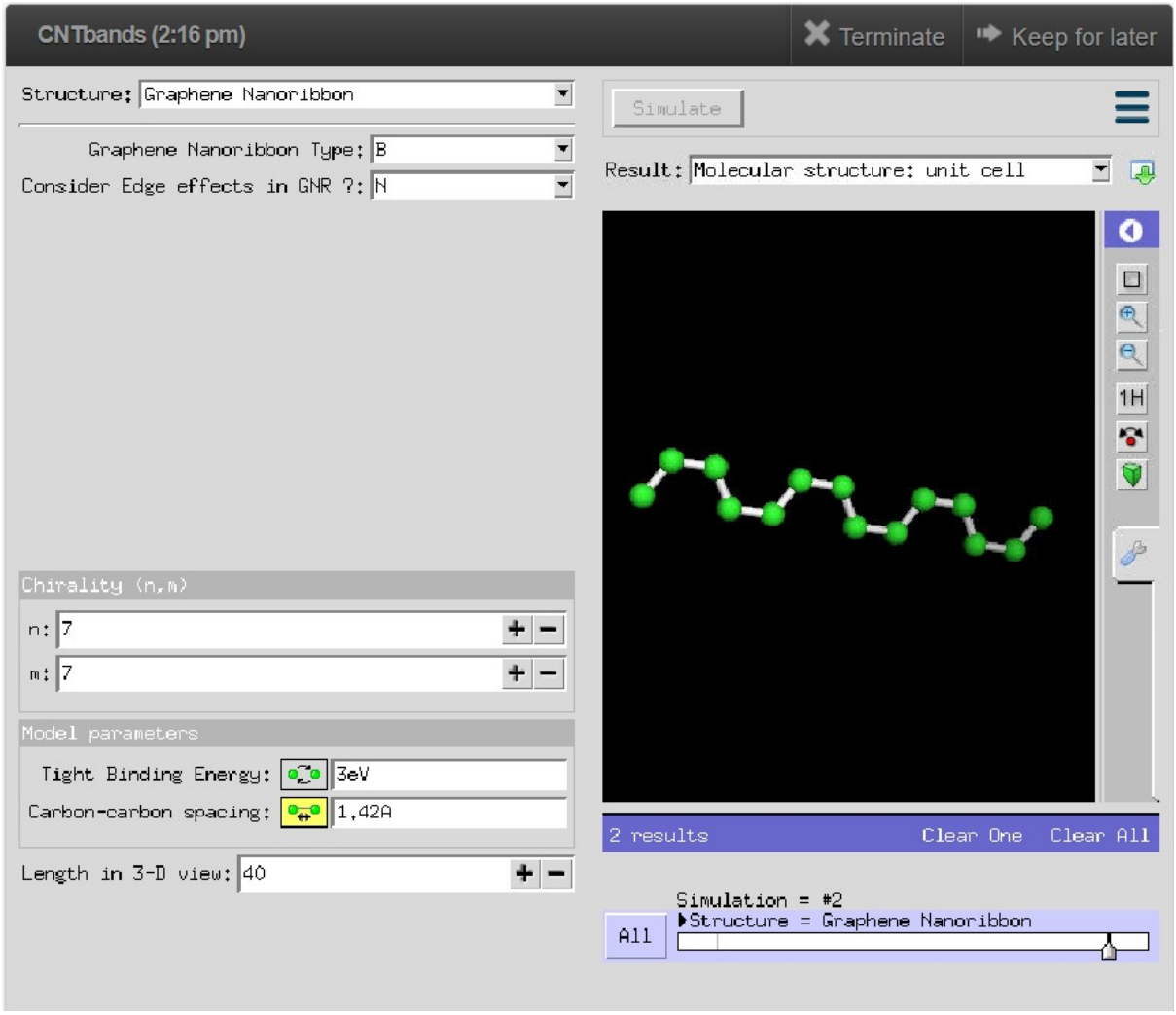
Graphene is the thinnest compound known to man at one atom thick, the lightest material known (with 1 square meter weighing

around 0.77 milligrams), the strongest compound discovered (between 100- 300 times stronger than steel), the best conductor of heat at room temperature and also the best conductor of electricity known. Other notable properties of graphene are its uniform absorption of light across the visible and near-infrared parts of the spectrum.



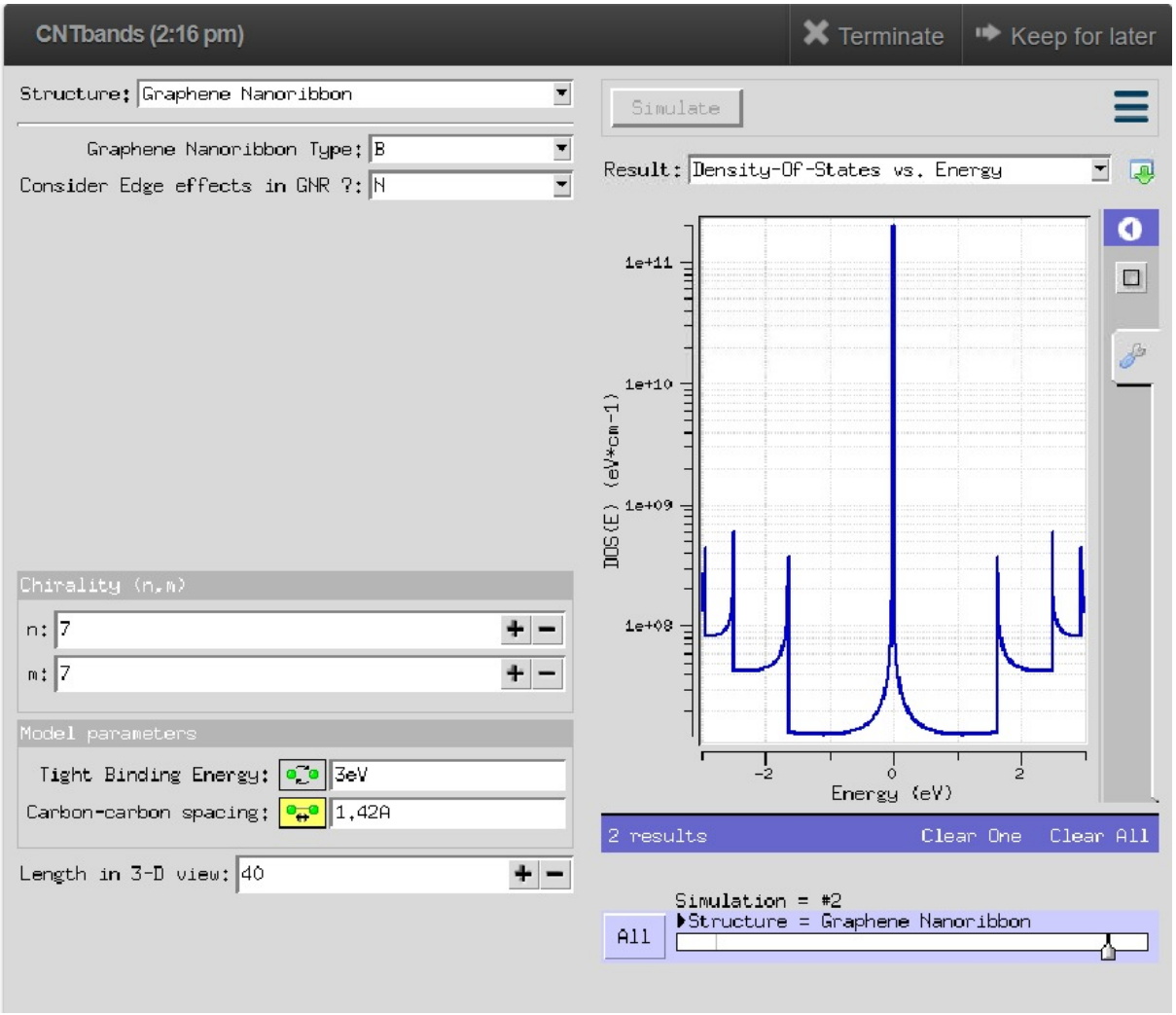
SIMULATIONS TO UNDERSTAND THE STRUCTURE OF CARBON NANOTUBE




CNTbands (2:16 pm)
Terminate
Keep for later
Structure: Graphene Nanoribbon
Graphene Nanoribbon Type: B
Consider Edge effects in GNR ?: N
Chirality (n,m)
n: 7
m: 7
Model parameters
Tight Binding Energy: 3eV
Carbon-carbon spacing: 1,42A
Length in 3-D view: 40
Simulate
Result: Molecular structure: unit cell
1H
2 results
Clear One
Clear All
Simulation = #2
Structure = Graphene Nanoribbon
All

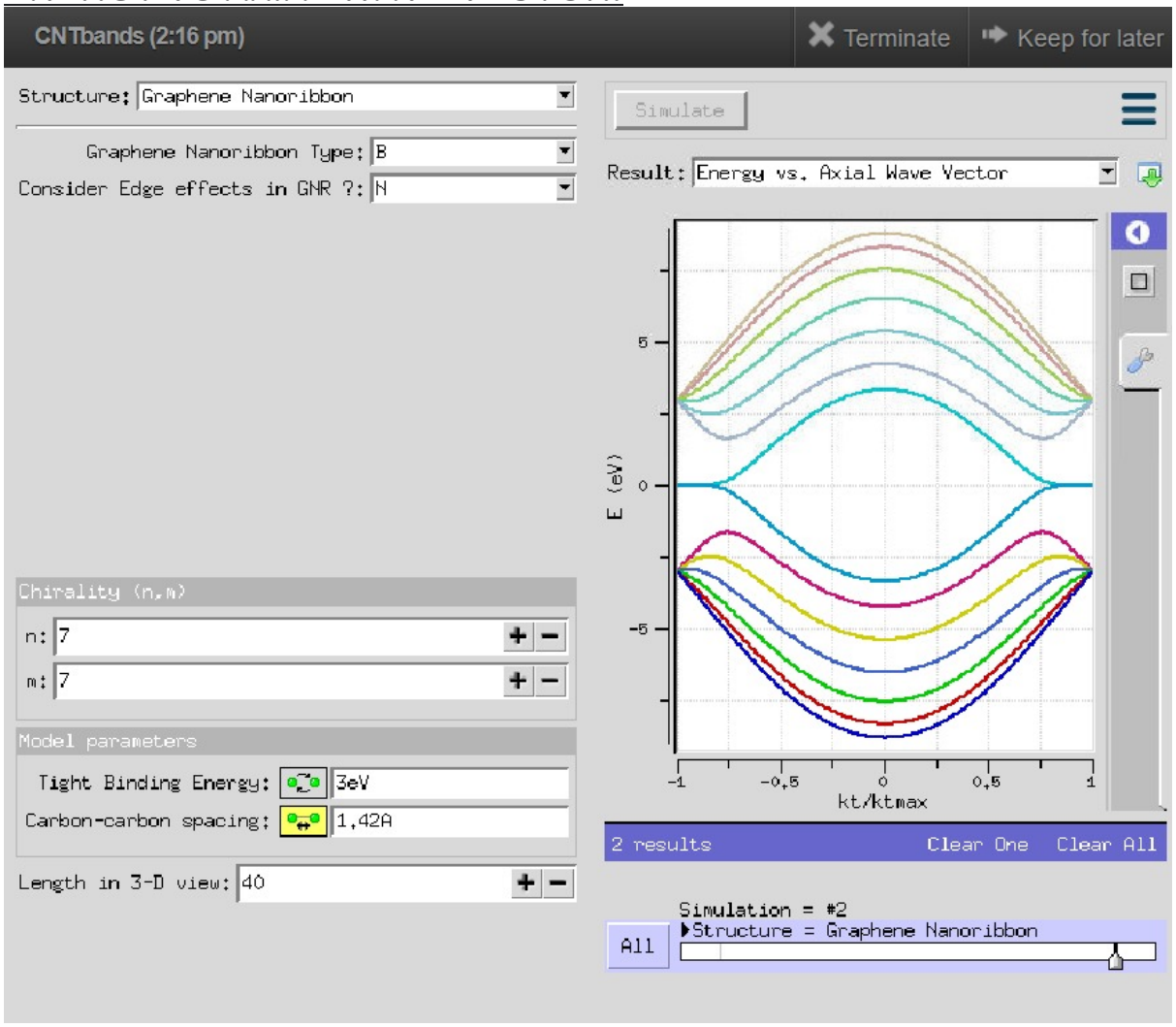
CHARACTERISTIC ANALYSIS OF CNT :

DOS vs ENERGY:



As can be seen in the DOS for a particular (n,n) armchair nanotube is the sum of the DOS of 1D electronic bands. As the nanotube diameter increases, the singularities move closer together. For larger diameter tubes the singularities merge, become smeared out, and the DOS approaches that of a graphene layer. On the other hand, for small diameter nanotubes as found in the present study, the 1D "spikes" in the electronic DOS are well separated especially near EF.

ENERGY VS AXIAL WAVE VECTOR:

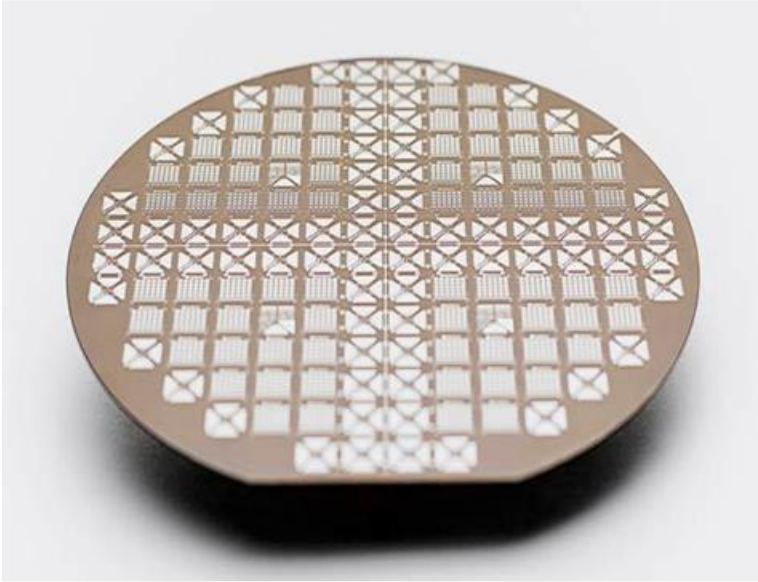


Types of Graphene:

There are two major types of graphene:

- **monocrystalline and**
- **polycrystalline.**

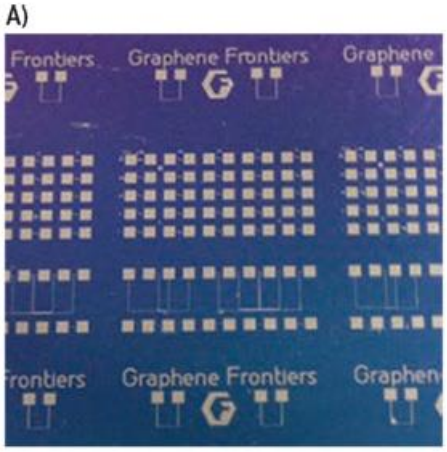
These two types have different applications. Polycrystalline graphene is crucial to manufacture some types of transistors and advanced composites, while monocrystalline graphene is used in more advanced applications. Despite the high demand for monocrystalline graphene, its methods of extraction do not allow large scale production. Up to date, monocrystalline graphene is produced through mechanical cleavage a technique in which graphene is extracted from graphite in single layer flakes.

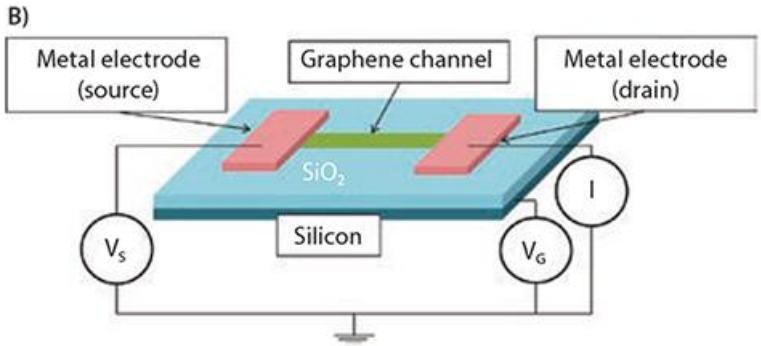


Graphene FET

Graphene has been revolutionizing electronics since October 2004 when it was first determined how to remove a single layer of carbon lattice from graphite. The production and research of today's graphene field effect transistors (GFETs) would not have been possible without the past two decades of research, and offer many benefits over traditional bipolar junction transistors. This is all thanks to the inherent qualities of graphene, which means GFETs can be used to good effect in a range of technologies, including biological

and chemical sensors. Graphene field-effect transistors (GFETs) take the typical FET device and insert a graphene channel tens of microns in size between the source and drain. Being graphene, a lattice of carbon atoms that is only one atom thick, the channels in GFETs have unprecedented sensitivity, which can be exploited on a wide variety of applications such as photo sensing, magnetic sensing and bio sensing.





Types of Graphene FET

Three typical configurations used in Graphene based Field Effect Transistors are-

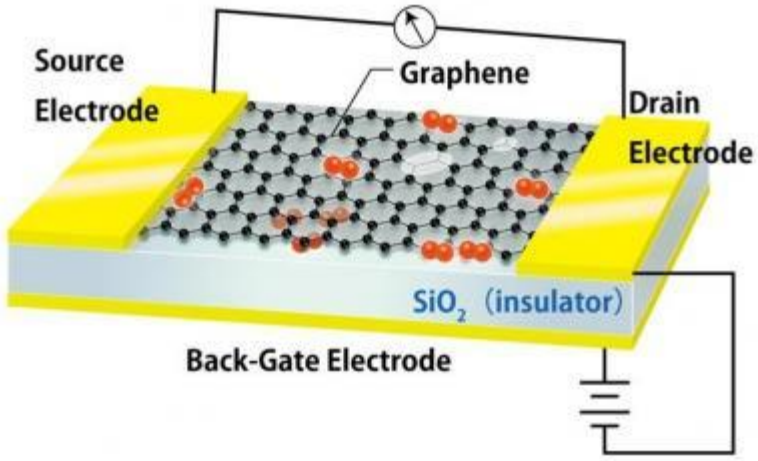
(i) back gate,

(ii) dual gate,

(iii) top gate

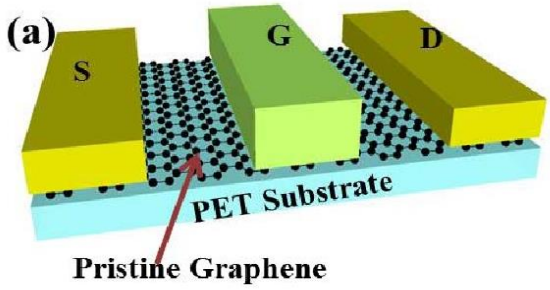
BACK GATE :

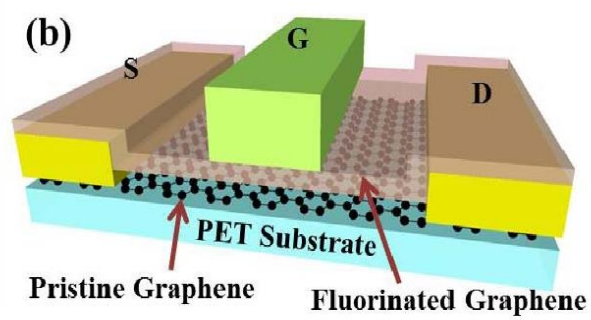
The back gate consists of a Silicon substrate on top of which lies SiO2 as the back gate dielectric, followed by layers of Graphene, Al, Al2O3 and finally nickel contacts for the gate and source & drain. On application of the gate voltages to this device, we can expect to observe accumulation of carriers in Graphene and hence a decrease in the resistance of the channel.



TOP GATE :

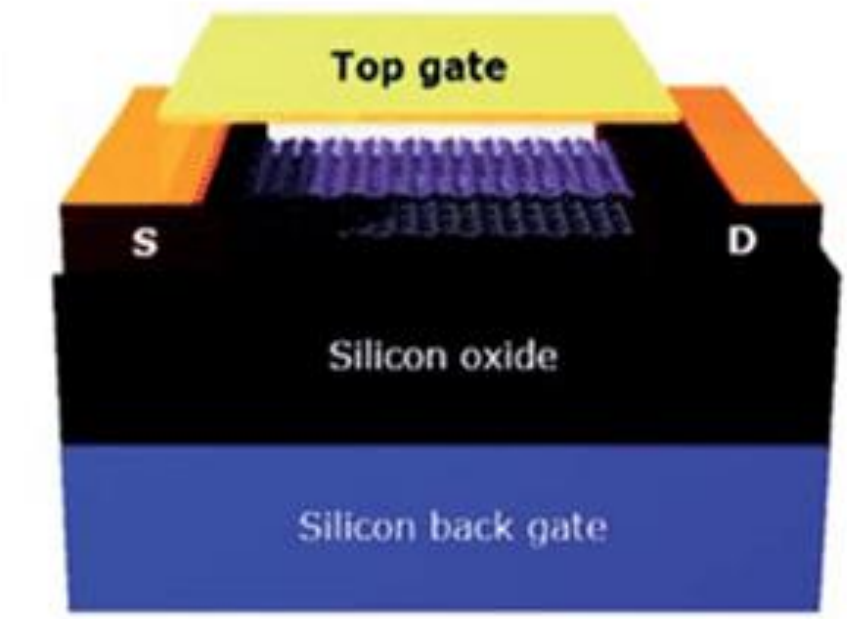
The top gate Graphene FET can be fabricated by growing epitaxial Graphene on top of a SiC layer. On top of the Graphene layer a dielectric layer is deposited (usually Al2O3) to form the top gate. Graphene grown on the C face of SiC has been shown to display higher values of mobility and can be used to make better devices although creating monolayer and bilayer on Silicon face is easier which makes it more suitable for commercial applications.





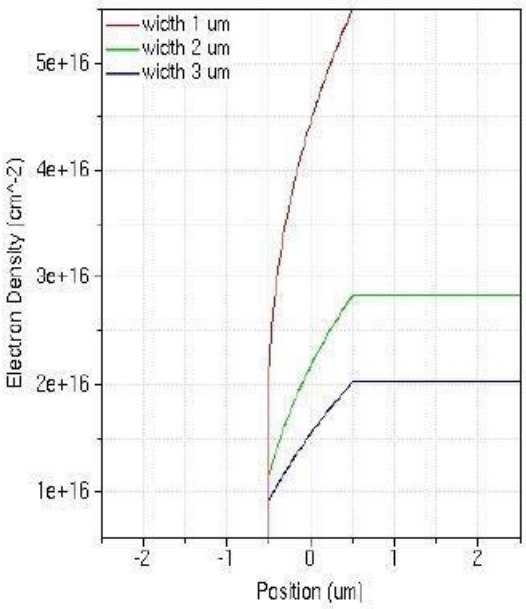
DUAL GATE :

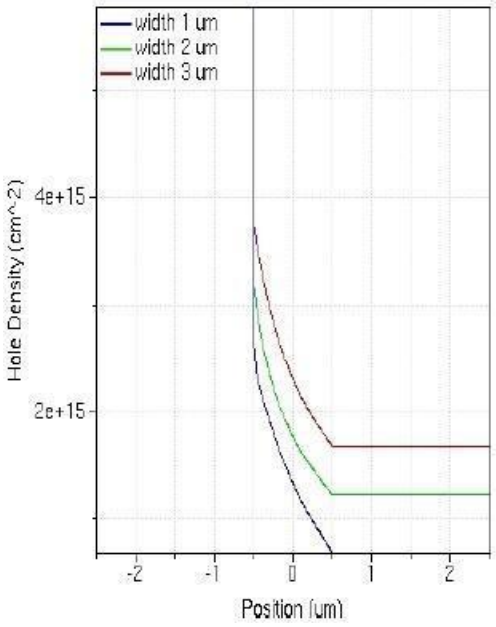
The dual gate configuration consists of a dielectric deposited on top of the flake to form another gate and thereby allowing both gates to control free carrier concentration in the channel.



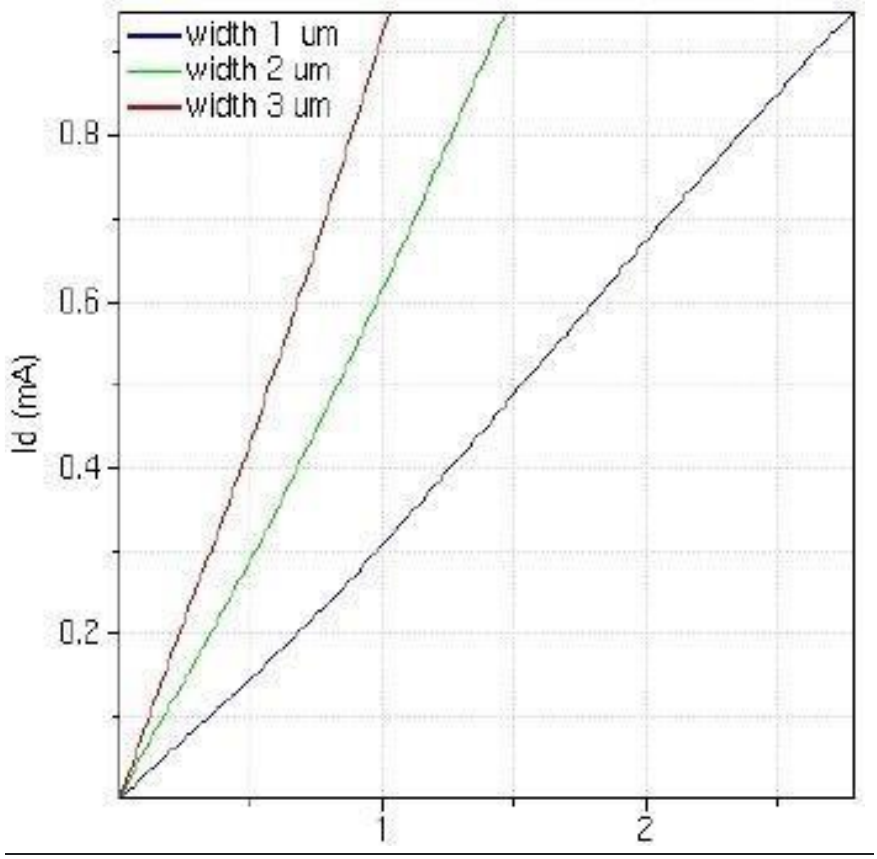
Electron density characteristics of GFET :

In the electron density characteristics of the GFET channel, it has been studied that, density of electrons increases linearly as proceeded through the channel from the centre position. But at certain position of the channel, the density of electrons become fixed. As, at the near end of the channel, the injected electrons become jammed and as a result, the total density of the electron from that certain position of the channel, become fixed. It has also been observed from this simulation curve that, for graphene channels of small width has large number of electron density at the channel end, but for graphene channel of large width, the electron density is less. In the following graphs the electron and hole densities of Graphene FET with channel width: 1 nm, 2 nm and 3 nm are observed.





Current voltage characteristics of GFET with varying channel width



<u>Inference</u>:

Slope of graph is more for greater value of channel width. It implies that the drain current is more for larger value of channel width for same value of drain voltage.

Benefits of Graphene transistors :

• Unprecedented Sensitivity

• The two-dimensional structure of graphene has a number of benefits over bulk semiconductors, such as silicon, used in standard FETs. Because most semiconductor transistor sensors are three-dimensional, electric charge changes at the surface of channel do not always penetrate deeper into the device. This can dramatically limit the response sensitivity of the device. On the other hand, as the graphene in a GFET is only one carbon atom thick, the entire channel is now on the surface, which directly exposes the channel to any molecules present in the nearby environment.

• Fewer Molecular Defects

• Semiconductors such as silicon are ineffective when produced to be as atomically thin as graphene. This is because surface defects, or dangling bonds, tend to dominate at these thicknesses, which limits the overall sensitivity of the device. Such bonds form additional defects in the sensor's semiconductor channel, and make non-specific binding possible, giving rise to false positives. This is unlike graphene which can be produced in a single layer with a high degree of accuracy and precision. Furthermore, a two-dimensional material such as graphene, produced efficiently, will have much less dangling surface bonds.

• Superior Conductivity

• GFETs also have a higher carrier mobility than traditional FETs

Methods to increase band gap in Graphene FET to increase its potential application:

Due to the zero band-gap in graphene band to band tunnelling is high and current saturation becomes difficult.
G-F ET Operation in a thermionic region is possible when VGS<VDS. In the case when VGS>VDS, band to band tunnelling starts and saturation become weak.

By creating a band gap in graphene, we can improve the drain current saturation up to some extent. But large area graphene is a zero-band gap material and for creating a band gap there is a need to cut the graphene in ribbon form which is quite difficult for large area fabrication.
The alternative way to improve the drain current saturation in graphene field effect transistor by keeping constant carrier concentration in the drain region. Therefore for more improvement and stable performance drain carrier concentrations should be constant throughout drain region and it is possible by selecting a suitable substrate which improves drain current saturation.

Use of graphene as supercapacitor:

Moore's law states that the number of transistors used in electronic circuitry will double every 2 years. The solution is to develop energy storage components such as either a supercapacitor or a battery that is able to hold a lot of energy and can be charged very quickly. Enhancing the capabilities of lithium ion batteries (by incorporating graphene as an anode) offer's much higher storage capacities with much better longevity and charge rate. Graphene based micro-supercapacitors are being developed for use in low energy applications. There is a recent outburst in research related to SQUID (superconducting quantum interference device. Six-layered vdW (Vander Waal material) heterostructures are fabricated by a standard polycarbonate assisted pick-up technique. Demonstration of helical edge modes in two graphene layers placed within a superconducting coherence length of each other represented the first step towards engineering topological superconductivity in graphene based heterostructures. By the reason of unprecedented electronic properties, two-dimensional (2D) crystals have brought chances for advancement in planar spintronic devices. Such circuits could help in developing bendable strainbased spin sensors, a great platform to find more about pure spin current based operations and low power flexible nanoelectronics. Spin transport signal measured in the spin valve geometry during the conduction of an experiment to learn more about such circuits displays switching between parallel (↑↑or ↓↓) and anti-parallel (↓↑ or ↑↓) configurations of the injector and detector electrodes.

WHERE IS TUNNELING EFFECT PRESENT IN MOSFETS-

The working principle of transistor is gate-controlled band to band tunnelling and its basic structure is a gated PIN diode. Compared to the MOSFET, it has numerous advantages like apt for low power applications due to lower outflow current, better immunity to short channel effects, greater operating speed due to tunnelling, the threshold voltage is much smaller, the current ratio is low off and higher on/off.

Scaling is a process which involves reducing the size of MOSFET and at the same time improving its performance. Each new generation has approximately doubled logic circuit density and increased performance by about 40% while the memory capacity has increased by four times. In ideal scaling, as the dimension and the operating voltage is reduced by a factor of 0.7, the area density doubles, switching delay decreases by a factor of 0.7 and the switching energy is halved

Tunnelling Effect:

Under normal conditions, in an operating or computational system integrated transistors are separated sufficiently enough so that operation of one transistor does not in any way affect the operation of another transistor. This separation is made by inserting a material that acts as a barrier between two transistors. However, the barriers are also scaling down along with the MOSFETs. So, there is a possibility of carriers from one MOSFET crossing over to another and distorting the performance. This effect increases exponentially as the barrier distance decreases.

MATLAB CODE FOR REPRODUCING TUNNELLING EFFECT-

```
close all;
clear all;
```

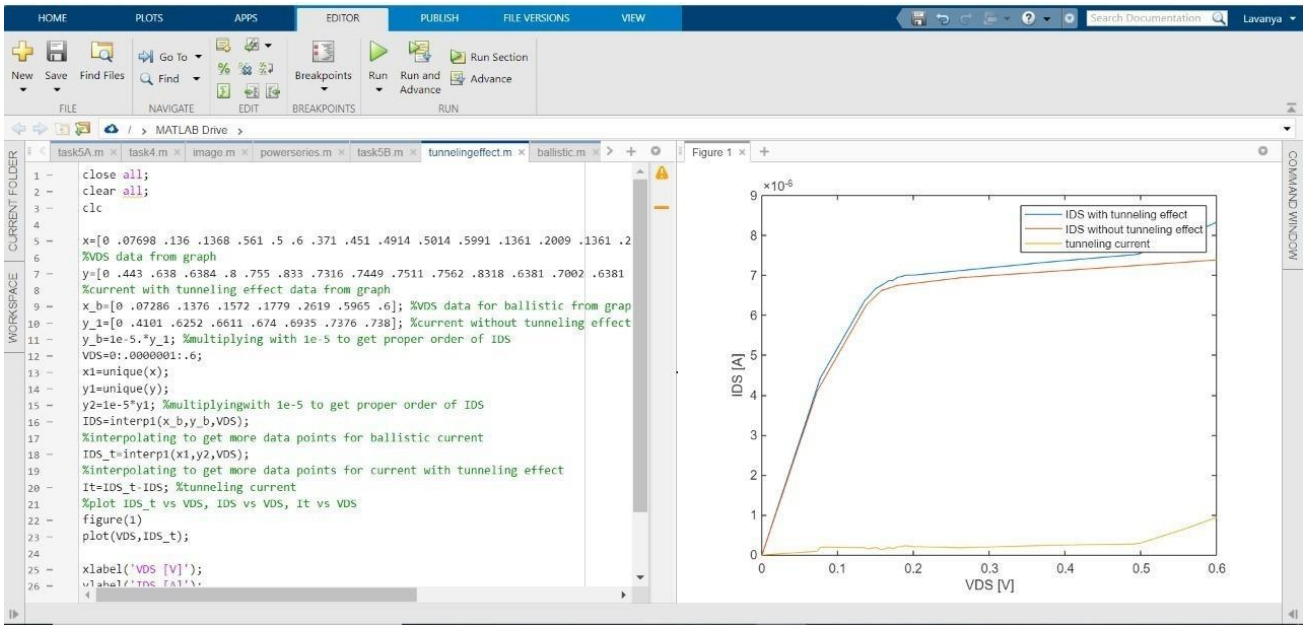
```
clc

x=[0 .07698 .136 .1368 .561 .5 .6 .371 .451 .4914 .5014 .5991 .1361
.2009 .1361 .2009 .15 .16052 .1671 .17237 .17895 .18552 .189473];
%VDS data from graph
y=[0 .443 .638 .6384 .8 .755 .833 .7316 .7449 .7511 .7562 .8318
.6381 .7002 .6381 .7002 .6666 .6777 .6861 .6866 .6944 .6972 .7];
%current with tunneling effect data from graph
x_b=[0 .07286 .1376 .1572 .1779 .2619 .5965 .6]; %VDS data for
ballistic from graph
y_1=[0 .4101 .6252 .6611 .674 .6935 .7376 .738]; %current without
tunneling effect data
y_b=1e-5.*y_1; %multiplying with 1e-5 to get proper order of IDS
VDS=0:.0000001:.6;
x1=unique(x);
y1=unique(y);
y2=1e-5*y1; %multiplyingwith 1e-5 to get proper order of IDS
IDS=interp1(x_b,y_b,VDS);
%interpolating to get more data points for ballistic current
IDS_t=interp1(x1,y2,VDS);
%interpolating to get more data points for current with tunneling
effect
It=IDS_t-IDS; %tunneling current
%plot IDS_t vs VDS, IDS vs VDS, It vs VDS
figure(1)
plot(VDS,IDS_t);


xlabel('VDS [V]');
ylabel('IDS [A]');
```

```
hold all;

plot(VDS,IDS)

plot(VDS,It)

legend('IDS with tunneling effect','IDS without tunneling
effect','tunneling current') ;
```

The resistance of short one-dimensional conductors depends neither on their composition nor on the length of the conductor. It depends only a function on the number of available conduction channels for example, one-dimensional sub bands, and the transmission at the contacts. This activity is known as the ballistic conduction, since electrons travel with zero scattering effect between two terminals. Although there is no scattering in the conduction channel or any back scattering of the electrons leaving the conductor, the resistance of a ballistic conductor is not zero.

Bandgap strain affects the drain current the most among the non-ballistic effects. Without strain effect, non-ballistic components deviate from the ideal behaviour by a very small amount. Tunnel control parameter maintains an inverse relation with channel length and chirality while it increases with temperature.

Matlab simulation:



INFERENCE-

It can be seen when compared to the ballistic results that, bandgap strain affects the performance of the CNTFET the most. Also, another interesting aspect is that tunnelling effect yields a higher current than ballistic effect. This is due to the fact that the tunnelling current is added to the drain current and increases the total drain current. However, this should be noted that tunnelling effect lowers the self-consistent potential and thus worsens the threshold characteristics of the CNTFET.

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