15ECE313/VLSI Design
VI Semester
Department of ECE
Amrita School of Engineering, Bengaluru

Chapter 7
Electronic Analysis of CMOS Logic Gates

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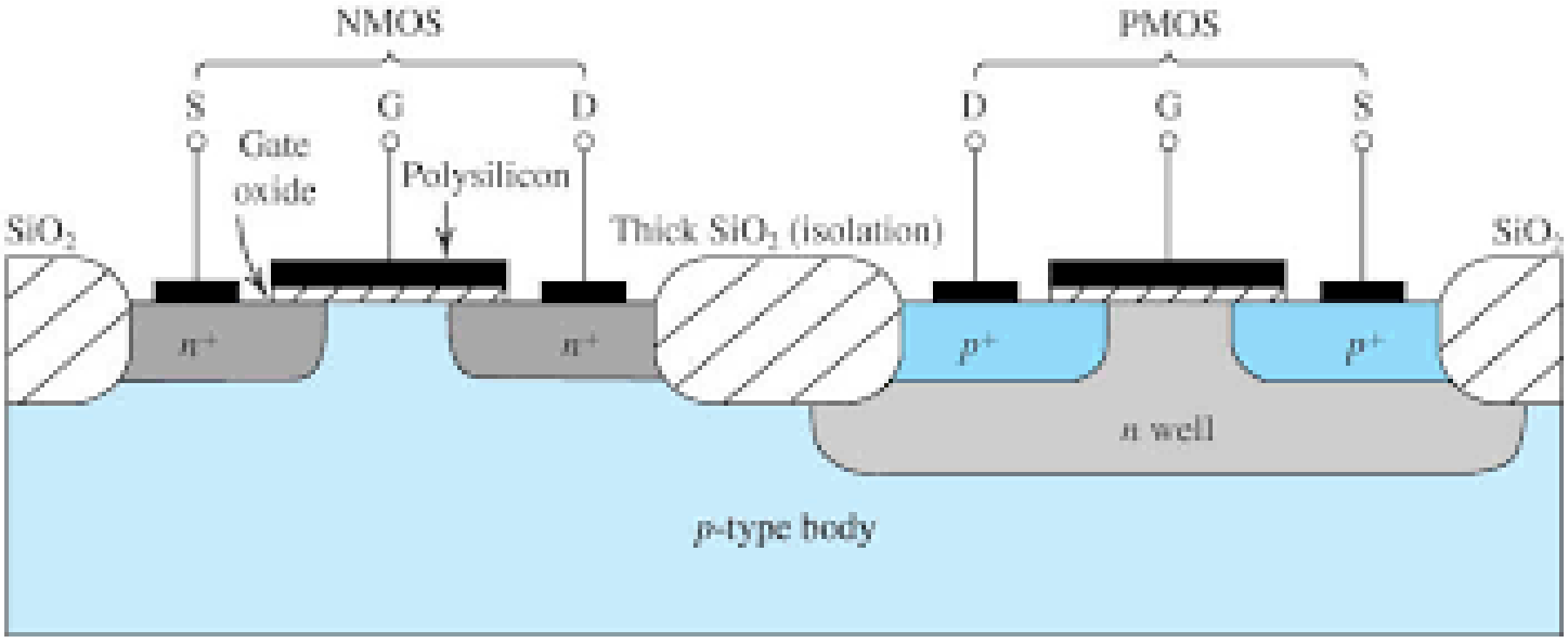
Electronic Analysis of CMOS Logic Gates

Goal

- Understand how to perform electronic analysis of CMOS logic gates. DC characteristics Noise margin
- Switching characteristics
- Power

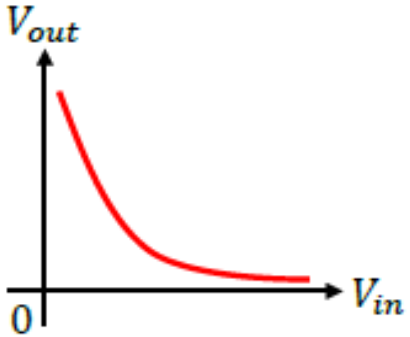
PMOS and NMOS Structure



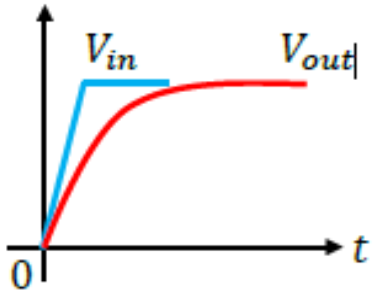
Region	NMOSFET		PMOSFET	
Cut Off	$V_{GS} < V_{Tn}$	$I_D = 0$	$V_{SG} < \lvert V_{Tp} \rvert$	$I_D = 0$
Linear Region (Resistive)	$V_{GS} > V_{Tn}$ $V_{DS} < V_{GS} - V_{Tn}$	$I_D = \mu_n C_{ox} \frac{W}{L} \{(V_{GS} - V_{Tn})V_{DS} - \frac{1}{2}{V_{DS}}^2\}$	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} < V_{SG} - \lvert V_{Tp} \rvert$	$I_D = \mu_p C_{ox} \frac{W}{L} \{(V_{SG} - \lvert V_{Tp} \rvert)V_{SD} - \frac{1}{2}{V_{SD}}^2\}$
Saturation Region	$V_{GS} > V_{Tn}$ $V_{DS} \geq V_{GS} - V_{Tn}$	$I_D = \frac{1}{2}\beta_n (V_{GS} - V_{Tn})^2$	$V_{SG} > \lvert V_{Tp} \rvert$ $V_{SD} \geq V_{SG} - \lvert V_{Tp} \rvert$	$I_D = \frac{1}{2}\beta_p (V_{SG} - \lvert V_{Tp} \rvert)^2$

Analysis

- DC Analysis
  - Vin vs. Vout = Voltage Transfer Characteristic (VTC)



- Transient (switching) analysis
  - Vin(t) vs. Vout(t)



The CMOS inverter gives the basic for calculating the electrical characteristic of logic gates

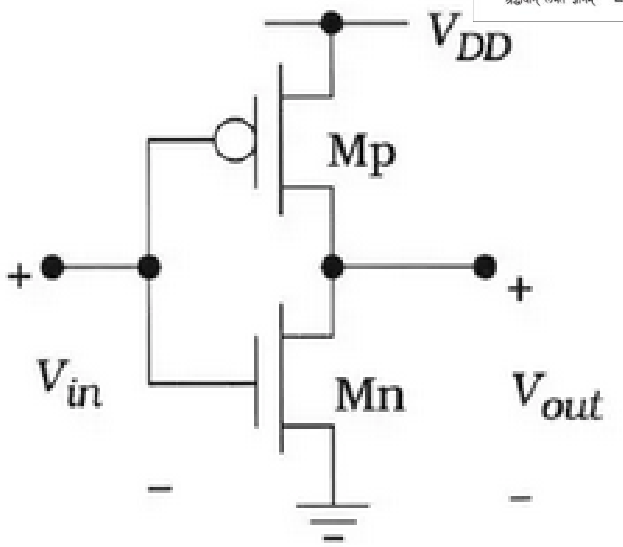
- The conduction states of M_n and M_p is determined by input voltage V_{in}
- Two types of calculations: *DC analysis* and *transient analysis*

DC analysis

- Provide a direct mapping of the input to the output, such that to determine V_{out}

Transient analysis

- The input voltage is an explicit function of time $V_{in}(t)$ corresponding to a changing logic value



pFET: $V_{Tp} < 0$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

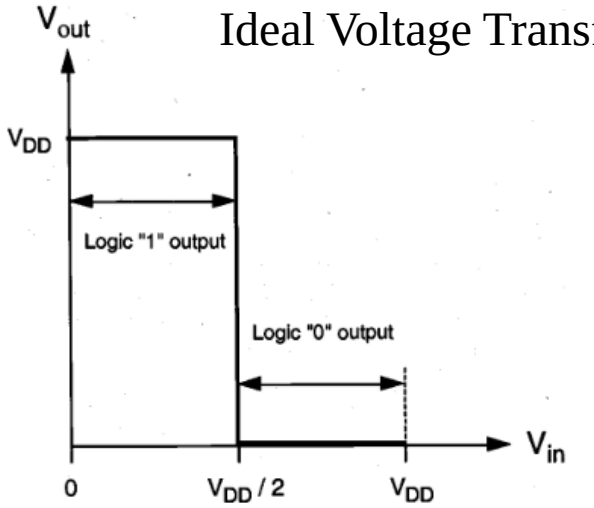
nFET: $V_{Tn} > 0$

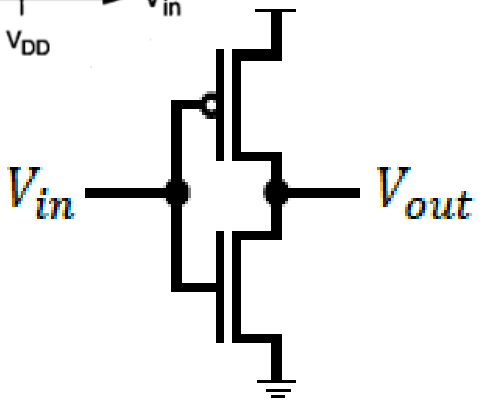
$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$

CMOS Inverter – DC Characteristics

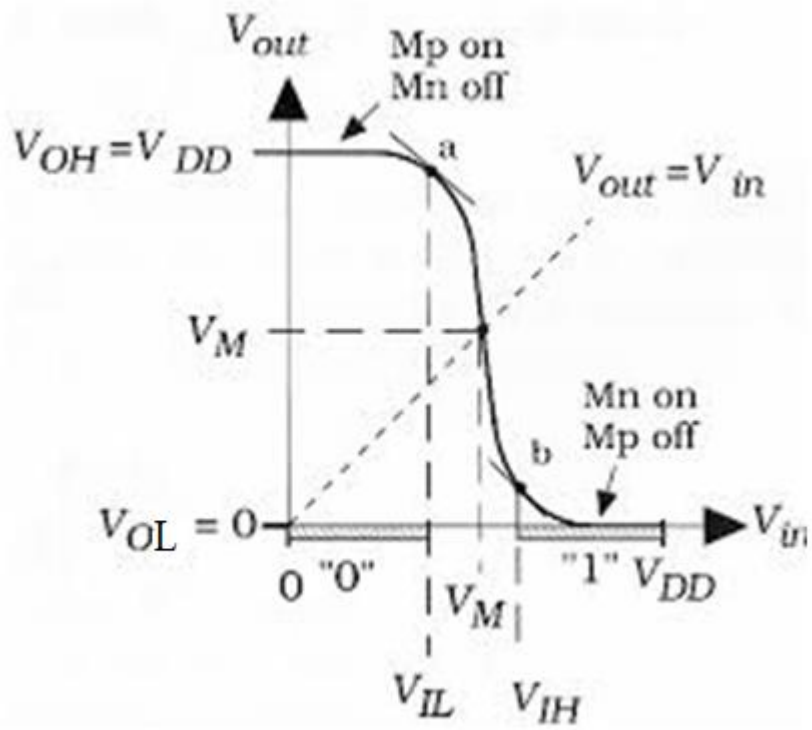
- Logic swing
  - When $V_{in} = 0$
    - $V_{out} = V_{DD}$
    - Output high voltage $V_{OH} = V_{DD}$
  - When $V_{in} = V_{DD}$
    - $V_{out} = 0$
    - Output low voltage $V_{OL} = 0$
  - Logic swing
    - $V_L = V_{OH} - V_{OL} = V_{DD}$

Ideal Voltage Transfer Characteristic (VTC)





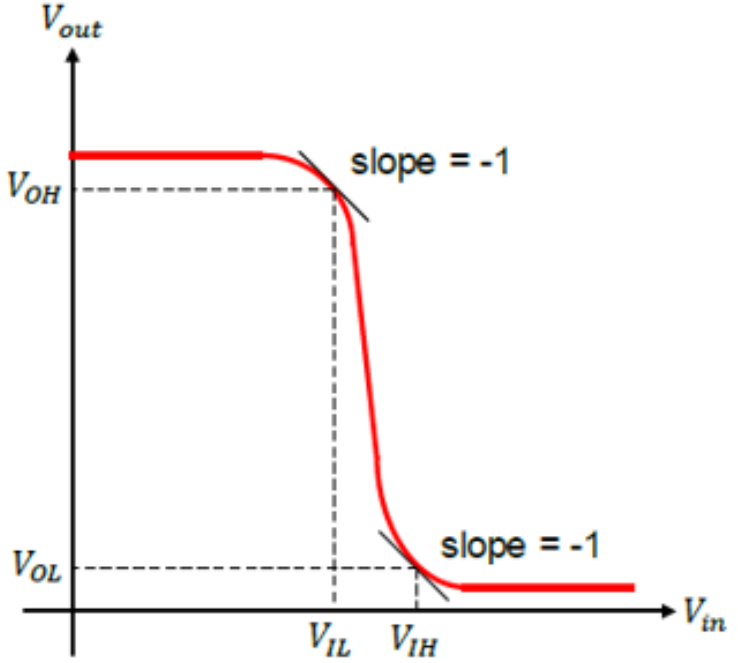
CMOS Inverter-VTC



CMOS Inverter Voltage Transfer Characteristic (VTC)

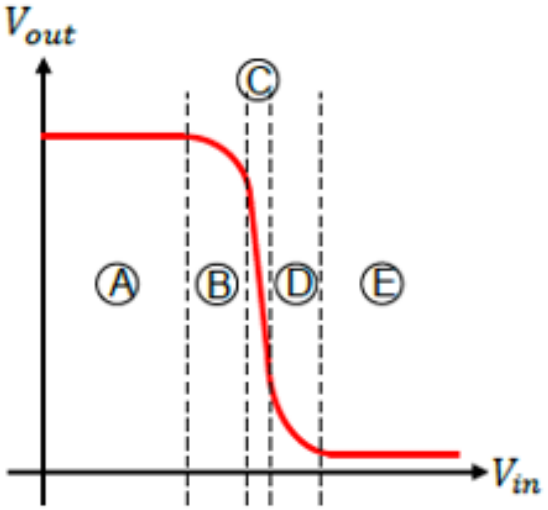
V_{IH}: Min. high input voltage
V_{IL}: Max. low input voltage
V_{OH}: Min. high output voltage
V_{OL}: Max. low output voltage

Logic '0' voltage : $0 \leq V_{in} \leq V_{IL}$
Logic '1' voltage : $V_{IH} \leq V_{in} \leq V_{DD}$

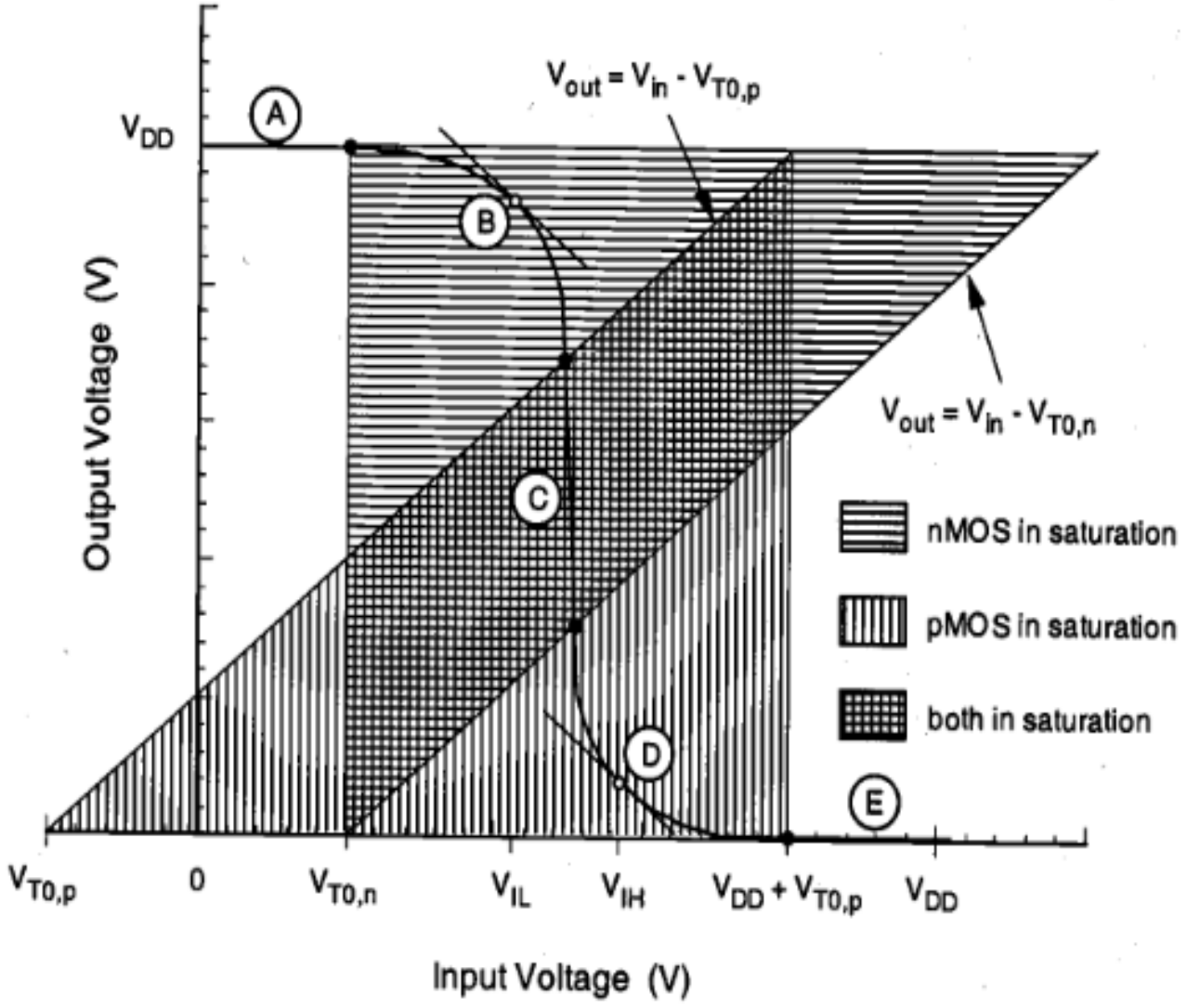


VIL and VIH are the two points at which Slope is equal to (dvout/dvin) = -1

CMOS Inverter-VTC

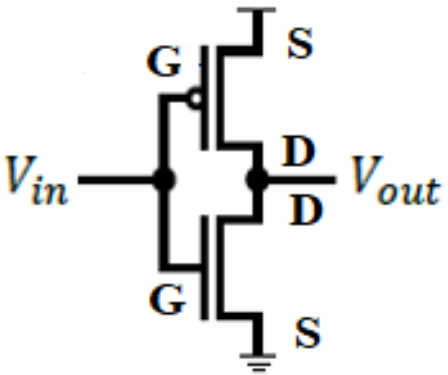


CMOS Inverter Voltage Transfer Characteristic (VTC)



NMOS		PMOS	
Condition	Remark	Condition	Remark
$V_{GS} > V_{Tn}$	If satisfied then ON otherwise OFF	$V_{SG} > \|V_{Tp}\|$	If satisfied then ON otherwise OFF
$V_{DS} \geq V_{GS} - V_{Tn}$	If satisfied then Saturation Region otherwise Linear region or Non-saturation region	$V_{SD} \geq V_{SG} - \|V_{Tp}\|$	If satisfied then Saturation Region otherwise Linear region or Non-saturation region

Finding Region of Operation of MOSFETs in various regions of VTC of CMOS Inverter

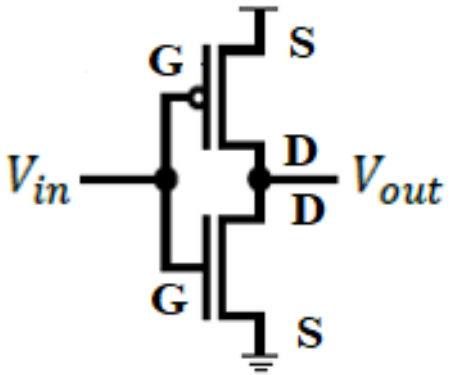


Region	Vin	Vout	NMOS Operating Region	PMOS Operating Region
A	< Vtn	VDD		
B	VIL	VOH ≈ VDD (HIGH)		
C	VM	VM		
D	VIH	VOL ≈ GND (LOW)		
E	VDD	GND		

For Region A on VTC

For NMOS	For PMOS
VG = (<Vtn) VS = 0 VGS = VG –VS = (<Vtn) – 0 = <Vtn Therefore, VGS < Vtn Therefore, NMOS is OFF	VG = (<Vtn) VS = VDD VSG = VS – VG = VDD – (<Vtn) ≈ VDD Therefore, VSG > |Vtp| Therefore, PMOS is ON To find the region of operation, VSD = VS – VD = VDD – VDD = 0 VSG -|Vtp| = VS – VG - |Vtp| = VDD – (<Vtn) -|Vtp| = +Ve value Therefore, VSD < VSG - |Vtp| So PMOS is in Linear Region of Operation

Region	Vin	Vout	NMOS Operating Region	PMOS Operating Region
A	< Vtn	VDD		
B	VIL	VOH ≈ VDD (HIGH)		
C	VM	VM		
D	VIH	VOL ≈ GND (LOW)		
E	VDD	GND		



CMOS Inverter-VTC Region of Operation for MOSFETs

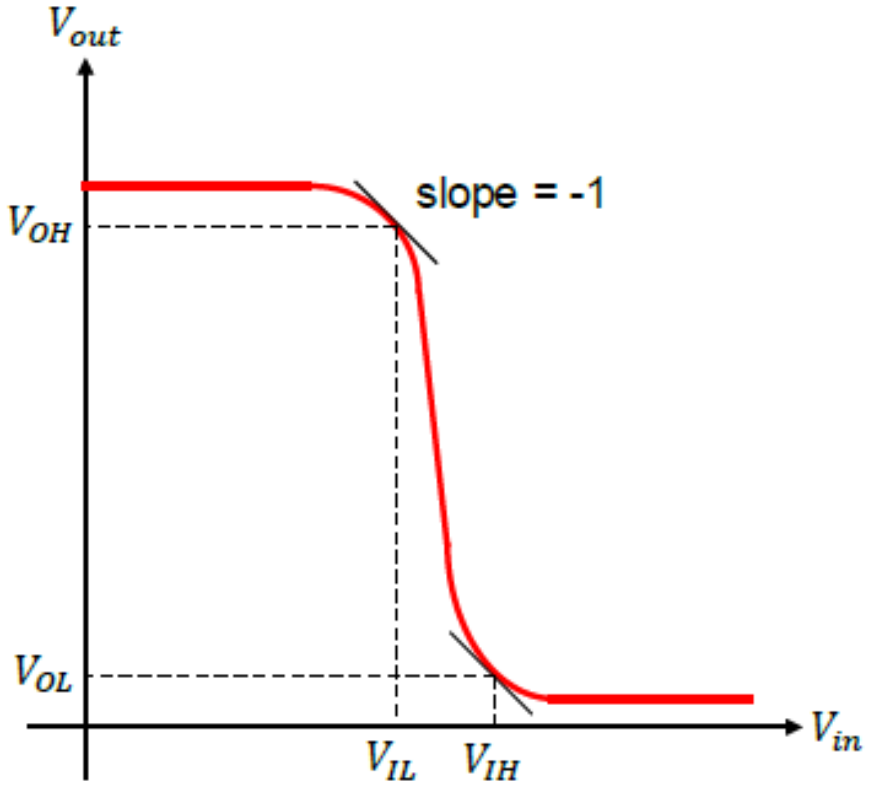
Region	Vin	Vout	NMOS Operating Region	PMOS Operating Region
A	< Vtn	VDD	Cut Off	Linear
B	VIL	VOH ≈ VDD (HIGH)	Saturation	Linear
C	VM	VM	Saturation	Saturation
D	VIH	VOL ≈ GND (LOW)	Linear	Saturation
E	VDD	GND	Linear	Cut off

CMOS Inverter – DC Characteristics

- Voltage noise margin
  - $VNM_H = V_{OH} - V_{IH}$
  - $VNM_L = V_{IL} - V_{OL}$

The noise margins give a quantitative measure of how stable the inputs are with respect to coupled electromagnetic signal interference.

- V_{IH}: Min. high input voltage
- V_{IL}: Max. low input voltage
- V_{OH}: Min. high output voltage
- V_{OL}: Max. low output voltage



Calculation of Mid Point Voltage V_M

- Switching threshold- Point on VTC where Vout = Vin is called *midpoint voltage*.
- At midpoint voltage Vin = Vout = V_M
- Point is found in C region of VTC
- In this C region , both NMOS and PMOS are ON and found to be getting operated in Saturation region of operation.

For nFET

$V_{GSn} = V_G - V_S = V_{in} - V_S = V_M$

$V_{DSn} = V_D - V_s = V_{out} - V_S = V_M$

$V_M > (V_M - V_{Tn})$

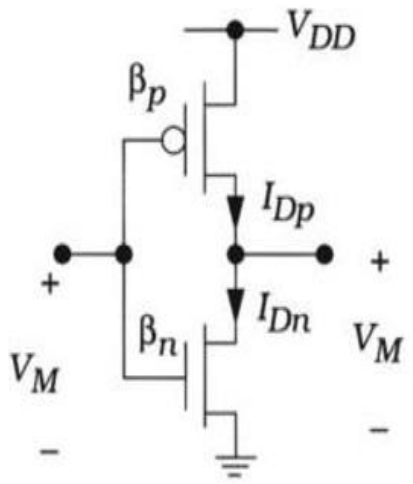
So $V_{DSn} > (V_{GSn} - V_{Tn})$

For pFET

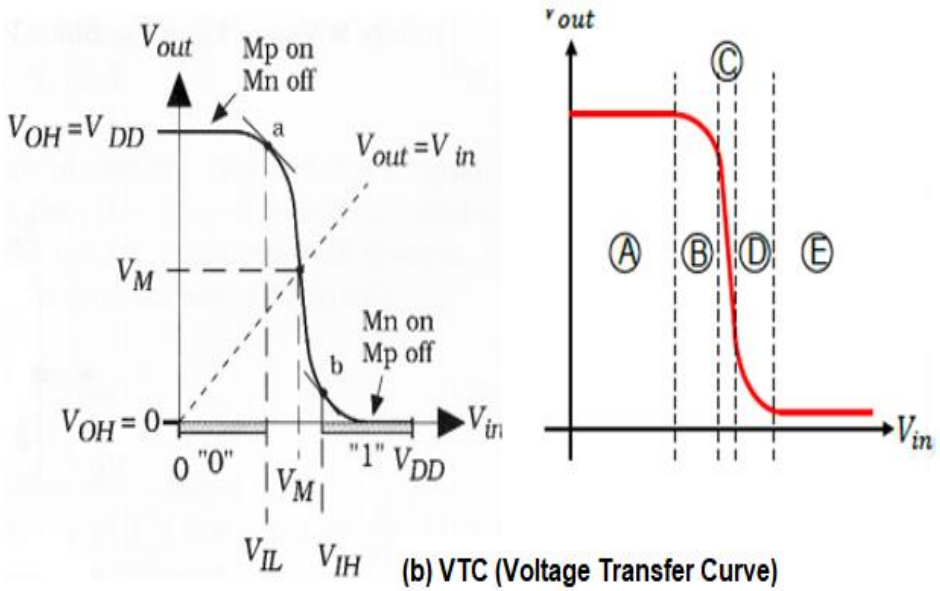
$V_{SGp} = V_S - V_G = V_{DD} - V_M$

$V_{SDp} = V_S - V_D = V_{DD} - V_M$

So $V_{SDp} > (V_{SGp} - |V_{Tp}|)$



(a) CMOS Inverter



(b) VTC (Voltage Transfer Curve)

Calculation of Mid Point Voltage V_M

- In an Inverter

$$I_{Dn} = I_{Dp}$$

Solve equation for V_M

$$I_{Dn} = \frac{\beta_n}{2}(V_{GSn} - V_{tn})^2 = \frac{\beta_p}{2}(V_{SGp} - |V_{tp}|)^2 = I_{Dp}$$

- express in terms of V_M

$$\frac{\beta_n}{2}(V_M - V_{tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{tp}|)^2 \quad \Rightarrow \quad \sqrt{\frac{\beta_n}{\beta_p}}(V_M - V_{tn}) = V_{DD} - V_M - |V_{tp}|$$

- solve for V_M

$$V_M = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

The equation shows that V_M is set by the nFET-to-pFET ratio $\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p}$

Calculation of Mid Point Voltage V_M

- If nFET and pFET are of same size then

  $(W/L)_n = (W/L)_p$

  $C_{OXn} = C_{OXp}$ (always)

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{oxn}\left(\frac{W}{L}\right)_n}{\mu_p C_{oxp}\left(\frac{W}{L}\right)_p} = \frac{\mu_n}{\mu_p} \cong 2 or 3$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r = \text{mobility ratio}$$

Symmetrical Inverter

- A symmetrical inverter VTC is one that has equal “0” and “1” input voltage ranges.
- This can be achieved by choosing

$$V_M = \frac{1}{2} V_{DD}$$

We know $I_{Dn} = I_{Dp}$

$$\frac{\beta_n}{2}(V_M - V_{tn})^2 = \frac{\beta_p}{2}(V_{DD} - V_M - |V_{tp}|)^2$$

After substituting $V_M = \frac{1}{2} V_{DD}$

$$\frac{\beta_n}{\beta_p} = \frac{\left(\frac{1}{2}V_{DD} - |V_{Tp}|\right)^2}{\left(\frac{1}{2}V_{DD} - V_{Tn}\right)^2}$$

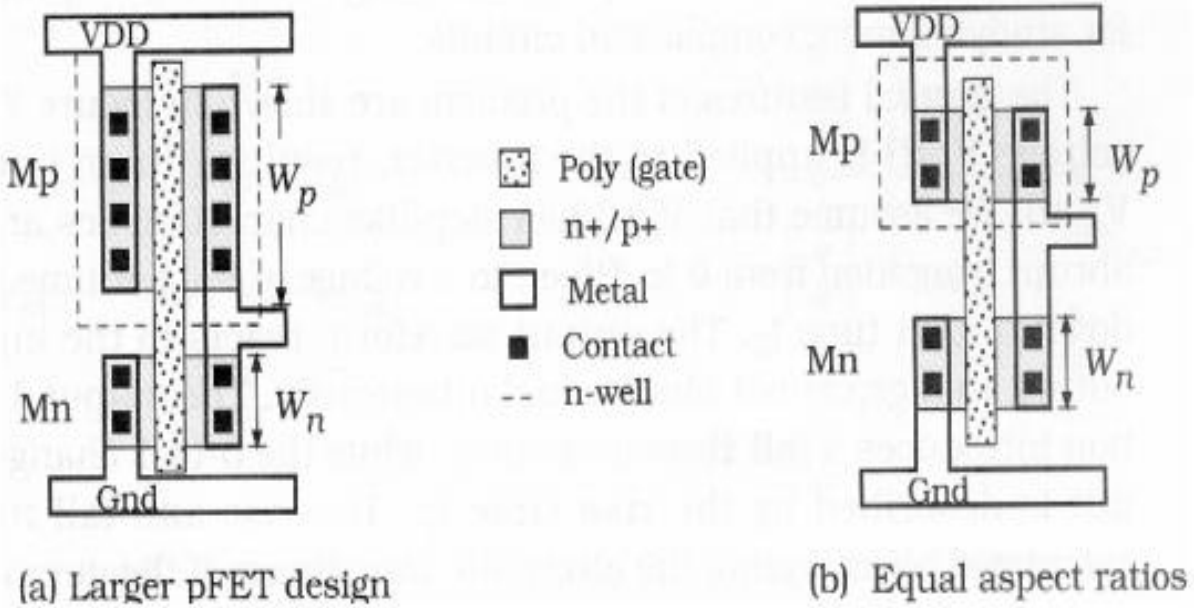
If $V_{Tn} = |V_{Tp}|$

Then $\beta_n = \beta_p$

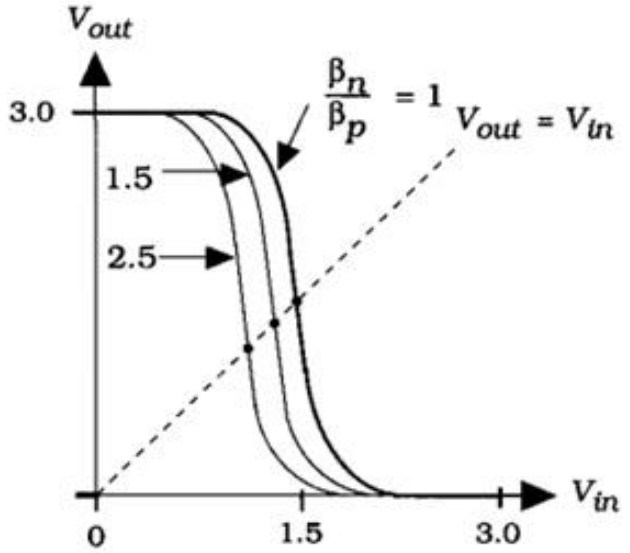
$$\mu_n C_{oxn}\left(\frac{W}{L}\right)_n = \mu_p C_{oxp}\left(\frac{W}{L}\right)_p$$

$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$$

Dependence of V_M on Device Ratio



(a) Larger pFET design (b) Equal aspect ratios



transition pushed lower as beta ratio increases

$$V_M = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$

Solved Problem

Example 7.1 Consider a CMOS process with the following parameters-

$k'_n = 140\ \mu A/V^2$, $V_{Tn} = 0.70V$, $k'_p = 60\ \mu A/V^2$, $V_{Tp} = -0.7\ V$, $V_{DD} = 3.0V$. Find-

(a) The relative sizes of nFET and pFET for symmetrical inverter.

(b) Midpoint voltage for the inverter with same aspect ratio.

Solution:

Consider the case where $\beta_n = \beta_p$. We can verify that this is a symmetrical design by calculating

$$V_M = \frac{3 - 0.7 + \sqrt{1}(0.7)}{1 + \sqrt{1}} = 1.5\ V$$

so that V_M is one-half the value of the power supply voltage. To achieve this design, we must choose the device aspect ratios such that

$$\frac{\beta_n}{\beta_p} = \frac{k'_n\left(\frac{W}{L}\right)_n}{k'_p\left(\frac{W}{L}\right)_p} = 1$$

where we recall that the process transconductance parameters k' are given by $k' = \mu_n C_{ox}$, and are set by the processing. For the present case, we rearrange the expression to read

$$\left(\frac{W}{L}\right)_p = \frac{k'_n}{k'_p}\left(\frac{W}{L}\right)_n$$

so that

$$\left(\frac{W}{L}\right)_p = \left(\frac{140}{60}\right)\left(\frac{W}{L}\right)_n = 2.33\left(\frac{W}{L}\right)_n$$

This shows that the pFET must be about 2.33 times larger than the nFET.

Let us now examine the case where the nFET and the pFET have the same aspect ratio $(W/L)_n = (W/L)_p$. With the values provided in the problem statement,

$$\frac{\beta_n}{\beta_p} = \frac{k'_n}{k'_p} = 2.33$$

so that the midpoint voltage is given by

$$V_M = \frac{3 - 0.7 + \sqrt{2.33}\ (0.7)}{1 + \sqrt{2.33}} = 1.33\ V$$

Assignment 1

1. A CMOS inverter is built in a process where $k'_n = 100\ \mu A/V^2$, $V_{Tn} = 0.70$ V, $k'_p = 42\ \mu A/V^2$, $V_{Tp} = -0.8$ V, $V_{DD} = 3.3$V. Find the midpoint voltage if $(W/L)_n = 10$ and $(W/L)_p = 14$. (1.48 V)

2. Find the ratio (β_n / β_p) needed to obtain an inverter midpoint voltage of 1.3 V with a power supply of 3 V. Assume that $V_{Tn} = 0.60$ V and $V_{Tp} = -0.82$ V. What would be the relative device sizes if $k'_n = 110\ \mu A/V^2$ and the mobility values are related by $\mu_n = 2.2\ \mu_p$? (1.58, (W/L)p = 1.39(W/L)n)

3. State whether the following statements are true or false for the VTC of CMOS inverter shown in figure. (Give proper explanations, prove the statement if necessary).

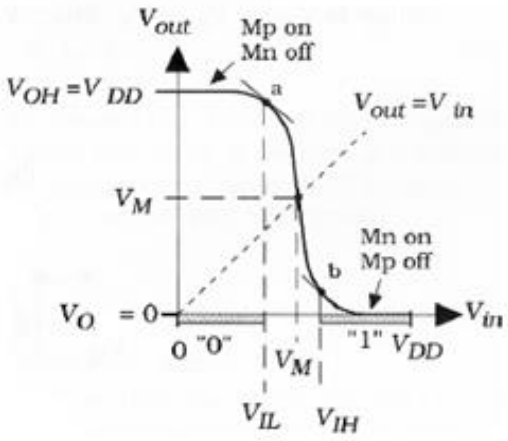
a). The mid-point voltage(V_M) depends on the threshold voltage of PMOS and NMOS transistors.

b). At V_M both the transistors are in triode region.

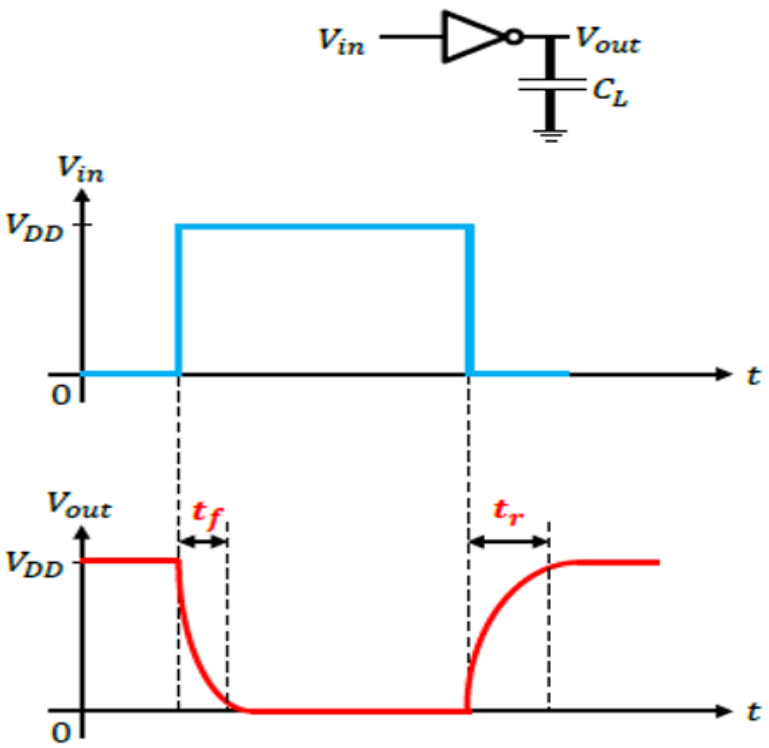
c). Increasing the threshold voltage of NMOS would decrease the voltage noise margin ($V_{NML} = V_{IL} - V_{OL}$).

d). Increasing the size (W/L) of PMOS would move the midpoint voltage upwards.

e). For a symmetrical inverter, which has equal "0" and "1" input voltage ranges, $V_M = 0.5\ V_{DD}$



CMOS Inverter Transient(Switching) Characteristics-



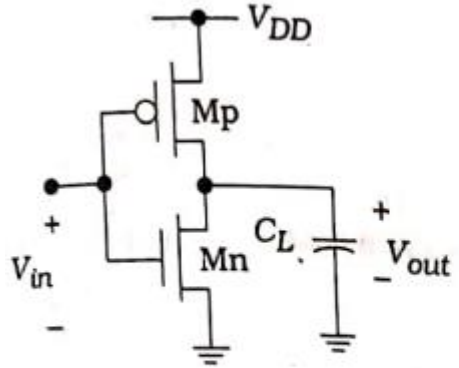
C_L: load capacitance

t_r: rise time

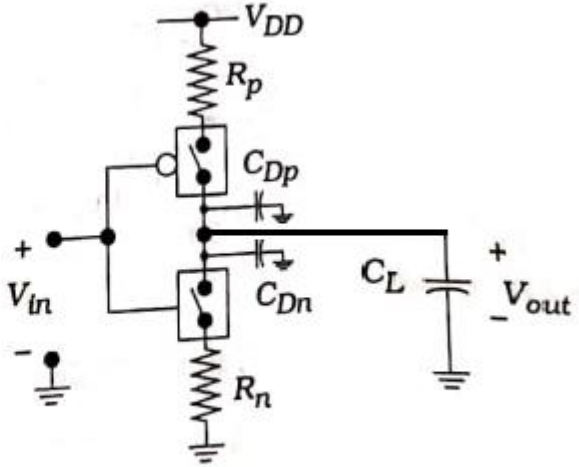
t_f: fall time

CMOS Inverter Transient(Switching) Characteristics-

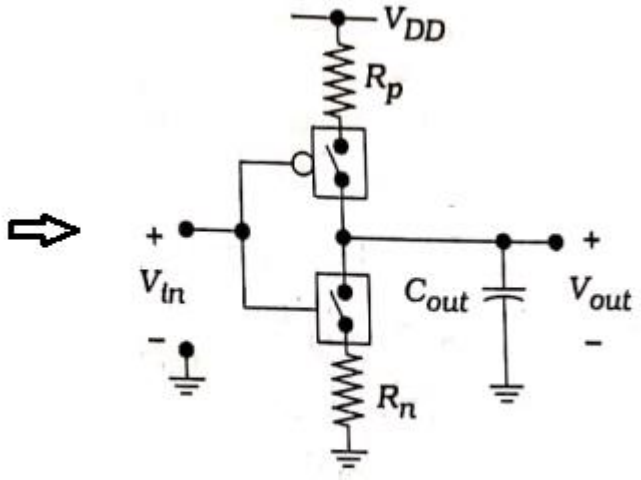
- The rise and fall time delays are due to the parasitic resistance and capacitances of the transistors.



(a) FET Circuit



(b) RC switch model equivalent



(c) Complete switching model

C_{FET}: FET capacitance

- $C_{FET} = C_{Dn} + C_{Dp}$
  - » $C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2}C_{ox}L'W_n + C_{Jn}A_n + C_{Jswn}P_n$
  - » $C_{Dp} = C_{GSp} + C_{DBp} = \frac{1}{2}C_{ox}L'W_p + C_{Jp}A_p + C_{Jswp}P_p$

C_L: load capacitance

C_{out}: total output capacitance

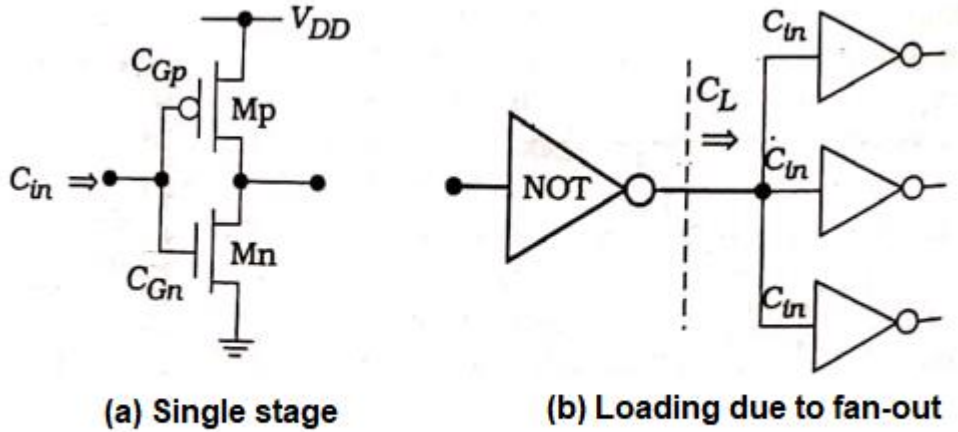
- $C_{out} = C_{FET} + C_L$

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$$

$$R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}$$

CMOS Inverter Transient(Switching) Characteristics-

- Load capacitance C_L
- In a logic chain, every logic gate must drive another or set of logic gates which is known as fan-out of the circuit.
- The fan-out gates act as a load to the driving circuit because of their input capacitance.



(a) Single stage (b) Loading due to fan-out

Input capacitance and load effects

$C_{in} = C_{Gp} + C_{Gn}$ Where $C_G = C_{OX}WL'$

$C_L = 3C_{in}$

CMOS Inverter Transient(Switching) Characteristics-

Fall time

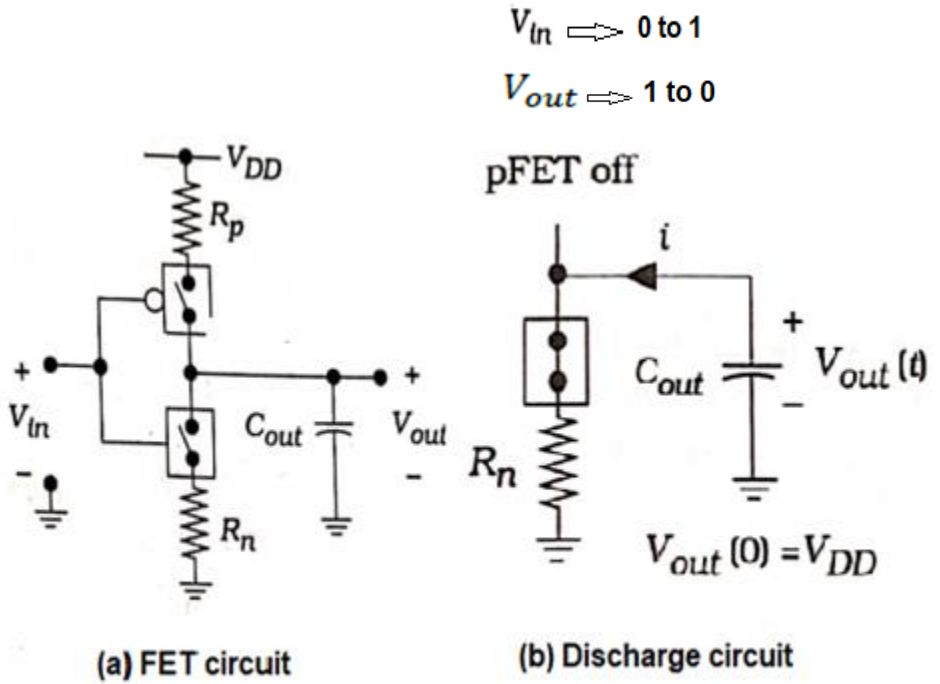
- From $V_{out} = 0.9V_{DD}$ to $V_{out} = 0.1V_{DD}$

- Fall time calculation
  - Discharging (Natural response)
  - $i = -C_{out}\frac{dV_{out}}{dt} = \frac{V_{out}}{R_n}$
    - $R_n = \frac{1}{\beta_n(V_{DD}-V_{Tn})}$

$$i = -C_{out}\frac{dv_{out}}{dt} = \frac{v_{out}}{R_n}$$

$$\int_{v_{out}(0)=V_{DD}}^{v_{out}(t)} \frac{dv_{out}}{v_{out}} = -\int_0^t \frac{dt}{R_n C_{out}}$$

$$\ln(v_{out}(t)) - \ln(V_{DD}) = -t/R_n C_{out}$$



CMOS Inverter Transient(Switching) Characteristics-

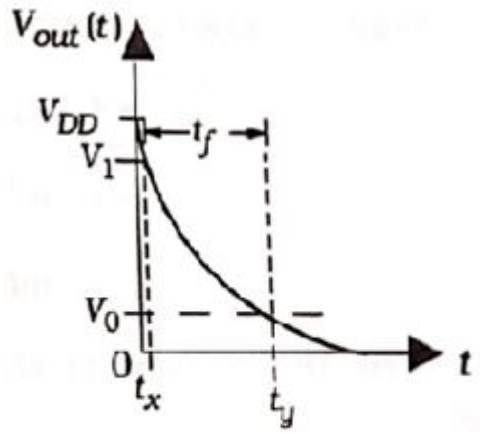
$$\ln\left(\frac{V_{out}(t)}{V_{DD}}\right) = -t/R_n C_{out}$$

$$\frac{V_{out}(t)}{V_{DD}} = e^{-t/R_n C_{out}}$$

$$\therefore \boxed{V_{out}(t) = V_{DD} e^{-t/R_n C_{out}}}$$

- $V_{out}(t) = V_{DD} e^{-\frac{t}{\tau_n}}$
  - $\tau_n = R_n C_{out}$ (time constant)
- $t = \tau_n \ln\left(\frac{V_{DD}}{V_{out}}\right)$

90% value $[V_1, t_x]$ to 10% value $[V_0, t_y]$



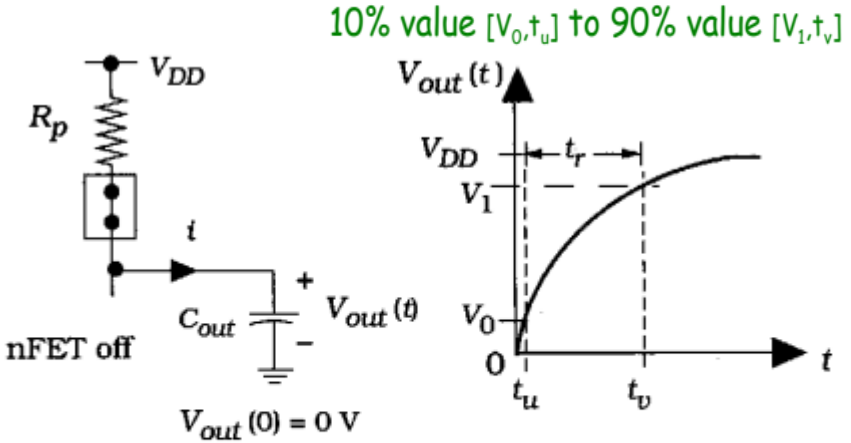
Output waveform

$t_f = t_y - t_x$

- $t_f = t(V_{out} = 0.1V_{DD}) - t(V_{out} = 0.9V_{DD}) = \tau_n\left(\ln 10 - \ln\frac{10}{9}\right) = \tau_n \ln 9$
- $\boxed{t_f \approx 2.2\tau_n = 2.2\, R_n C_{out} \approx 2.2R_n(C_{FET} + C_L) = t_{f0} + 2.2R_n C_L}$
- $t_{HL} = t_f$
  - t_{HL}: high-to-low time

CMOS Inverter Transient(Switching) Characteristics-

- Rise time
  - From $V_{out} = 0.1V_{DD}$ to $V_{out} = 0.9V_{DD}$
- Rise time calculation
  - Charging (Step response)
  - $i = C_{out}\frac{dV_{out}}{dt} = \frac{V_{DD}-V_{out}}{R_p}$
    - $R_p = \frac{1}{\beta_p(V_{DD}-|V_{Tp}|)}$
  - $V_{out}(t) = V_{DD}\left(1 - e^{-\frac{t}{\tau_p}}\right)$
    - $\tau_p = R_pC_{out}$ (time constant)
  - $t = \tau_p \ln\left(\frac{V_{DD}}{V_{DD}-V_{out}}\right)$
  - $t_r = t(V_{out} = 0.9V_{DD}) - t(V_{out} = 0.1V_{DD}) = \tau_p\left(\ln 10 - \ln\frac{10}{9}\right) = \tau_p \ln 9$
  - $t_r \approx 2.2\tau_p \approx 2.2\,R_pC_{out} \approx 2.2R_p(C_{FET} + C_L) = t_{r0} + 2.2R_pC_L$
  - $t_{LH} = t_r$
    - t_{LH}: low-to-high time



(a) Charge circuit (b) Output waveform

Rise time calculatiom

CMOS Inverter Transient(Switching) Characteristics-

- **Maximum Signal Frequency**

➢ This is the largest frequency that can be applied to the gate and still allow the output to settle to a definable state.

$$f_{max} = \frac{1}{t_{HL}+t_{LH}} = \frac{1}{t_f+t_r} = \frac{1}{2.2\,(\tau_n+\tau_p)}$$

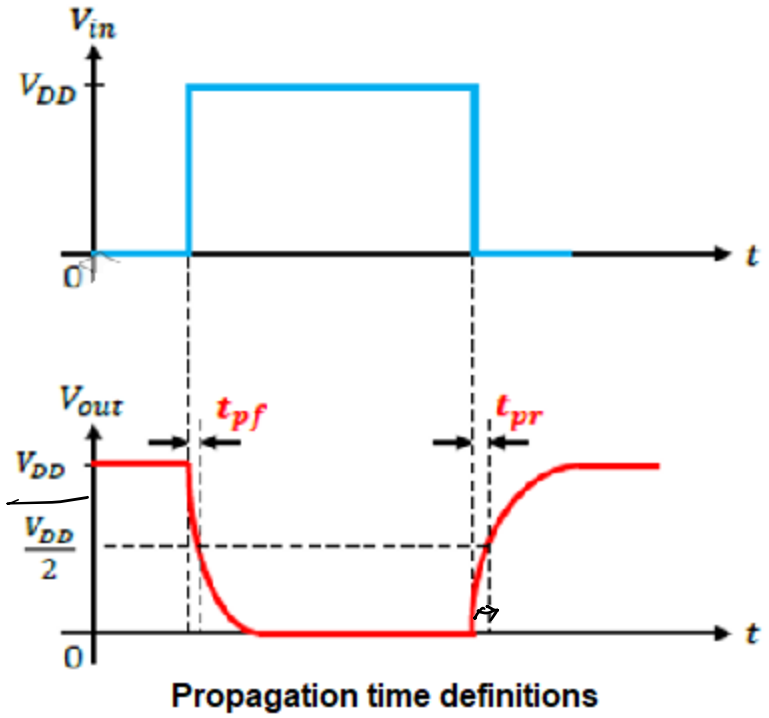
- **The Propagation Delay**

➢ Reaction time delay from input to output

– $t_p = \frac{t_{pf}+t_{pr}}{2}$

  - t_{pf}: output fall time $(V_{DD} \rightarrow \frac{V_{DD}}{2})$
    - $t_{pf} = \tau_n \ln 2$
  - t_{pr}: output rise time $(0 \rightarrow \frac{V_{DD}}{2})$
    - $t_{pr} = \tau_p \ln 2$

– $t_p = 0.35(\tau_n + \tau_p)$

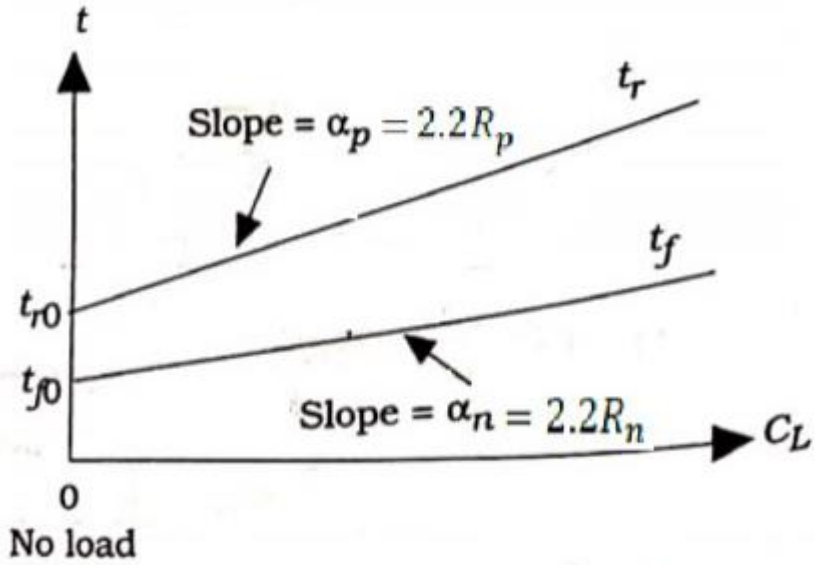


Propagation time definitions

CMOS Inverter-General Analysis

- Output capacitance
  - $C_{out} = C_{FET} + C_L$
- Rise time
  - $t_r = \tau_p \ln 9 \approx 2.2R_p(C_{FET} + C_L) = t_{r0} + 2.2R_pC_L$
    - $R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}$
- Fall time
  - $t_f = \tau_n \ln 9 \approx 2.2R_n(C_{FET} + C_L) = t_{f0} + 2.2R_nC_L$
    - $R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$
- Speed vs. area
  - $\beta \uparrow \Rightarrow R \downarrow \Rightarrow t \downarrow$
    - Area goes up, but the logic is faster.

$$C_{FET} = C_{Dn} + C_{Dp}$$
$$\gg C_{Dn} = C_{GSn} + C_{DBn} = \frac{1}{2}C_{ox}L'W_n + C_{jn}A_n + C_{jswn}P_n$$
$$\gg C_{Dp} = C_{GSp} + C_{DBp} = \frac{1}{2}C_{ox}L'W_p + C_{jp}A_p + C_{jswp}P_p$$



General behavior of the rise and fall times

----*Fast circuits consume more area than slow circuits* ---

CMOS Inverter-General Analysis

- Normal CMOS Inverter

If $\left(\frac{W}{L}\right)_n = \left(\frac{W}{L}\right)_p$

$\beta_n > \beta_p$ (since $\mu_n > \mu_p$)

$R_n < R_p$ ($R \alpha \frac{1}{\beta}$)

So $t_r > t_f$ ($t_r \alpha R_p$ and $t_f \alpha R_n$)

$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{Tp}|)}$$

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{Tn})}$$

- For Symmetrical Inverter

If $\beta_n = \beta_p$

$\left(\frac{W}{L}\right)_p = r \left(\frac{W}{L}\right)_n$ where $r = \frac{\mu_n}{\mu_p}$

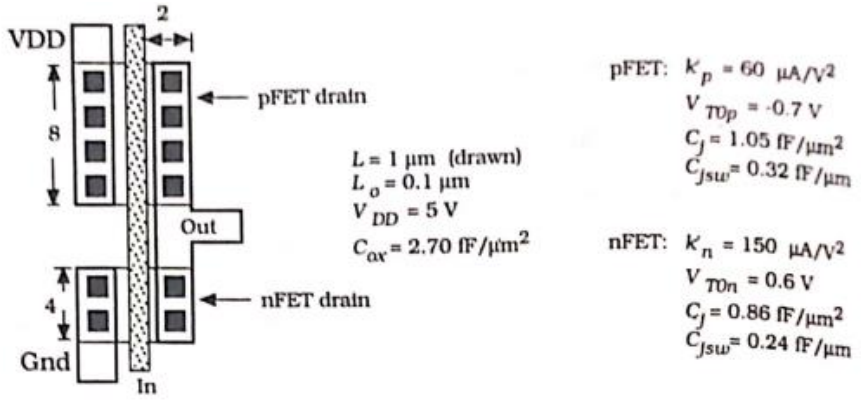
If $V_{Tn} = |V_{Tp}|$

$R_n = R_p$

So $t_r = t_f$

Solved Problems

Example 7.2. Find the output capacitance in the NOT gate shown in Figure.



Solution :

First we will find the gate capacitances using

$$C_{Gp} = (2.70)(1)(8) = 21.6 \text{ fF} = C_{OX} W_p L'$$
$$C_{Gn} = (2.70)(1)(4) = 10.8 \text{ fF} = C_{OX} W_n L'$$

Next, note that the overlap distance L_o is specified as 0.1 μm, which should be included in the area and perimeter factors in the junction capacitances. For the pFET, the p+ capacitance is

$$C_p = C_j A_{bot} + C_{jsw} P_{sw}$$

so

$$C_p = (1.05)(8)(2.1) + (0.32)2(8 + 2.1) = 24.10 \text{ fF}$$

The total capacitance at the pFET drain is therefore given by

$$C_{Dp} = \frac{21.6}{2} + 24.10 = 34.9 \text{ fF}$$

The nFET drain is analyzed using the same approach. The n+ junction capacitance is

$$C_n = (0.86)(4)(2.1) + (0.24)(2)(4 + 2.1) = 10.15 \text{ fF}$$

so that

$$C_{Dn} = \frac{10.8}{2} + 10.15 = 15.55 \text{ fF}$$

is the total capacitance at the drain of the nFET. Adding gives

$$C_{FET} = C_{Dp} + C_{Dn}$$
$$= 34.9 + 15.55$$
$$= 50.45 \text{ fF}$$

as the total internal FET capacitance. The total capacitance at the output is

$$C_{out} = 50.45 + C_L$$

in fF, where C_L is the external load (also in fF).

Solved Problems

Example 7.3. Consider an inverter circuit that has FET aspect ratio of $(W/L)_n = 6$ and $(W/L)_p = 8$ in a process where $k'_n = 150\ \mu A/V^2$, $V_{Tn} = 0.7V$, $k'_p = 62\ \mu A/V^2$, $V_{Tp} = -0.85$ V, $V_{DD} = 3.3$ V. The total output capacitance is estimated to be $C_{out} = 150$ fF. Compute rise time, fall time and maximum signal frequency.

Solution :

Consider first the fall time. The pFET resistance is given by

$$R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)} = \frac{1}{(62\times10^{-6})(8)(3.3-0.85)} = 822.9\ \Omega$$

The time constant for the charging event is computed using the RC product R_pC_{out} to find

$$\tau_p = (822.9)(150\times10^{-15}) = 123.43 \text{ ps}$$

where 1 ps (picosecond) is 10^{-12} sec. The rise time is

$$t_r = 2.2\tau_p = 271.55 \text{ ps}$$

The fall time is calculated in a similar manner. First, we find the nFET resistance

$$R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})} = \frac{1}{(150\times10^{-6})(6)(3.3-0.70)} = 427.35\ \Omega$$

so that the discharge time constant is

$$\tau_n = (427.35)(150\times10^{-15}) = 64.1 \text{ ps}$$

The fall time is

$$t_f = 2.2\tau_n = 141.0 \text{ ps}$$

Combining these results, the maximum signal frequency is

$$f_{max} = \frac{1}{t_r + t_f} = \frac{1}{271.55 + 141.0 \times10^{-12}} = 2.42 \text{ GHz}$$

Assignment 2

1. An inverter uses FETs with $\beta_n = 2.1$ mA/V^2 and $\beta_p = 1.8$ mA/V^2. The threshold voltages are given as $V_{tn} = 0.6$ V and $V_{tp} = -0.7$V and the power supply has a value of $V_{DD} = 5$ V. The parasitic FET capacitance at the output node is estimated as $C_{FET} = 74$ fF.

(a) Find the midpoint voltage. (2.378 V)
(b) Find the values of R_n and R_p. (108.23 ohm, 129.2 ohm)
(a) Calculate the rise time and fall times at the output when $C_L = 0$. (21.03ps, 17.62ps)
(b) Calculate the rise time and fall time when an external load of value $C_L = 115$ fF is connected to the output. (53.72ps, 45ps)
(e) Plot rise time and fall time as functions of C_L.

2. A CMOS inverter is designed with $\beta p = 80\ \mu A/V^2$, $\beta n = 0.25$ mA/V^2, $V_{tn} = |V_{tp}| = 0.5$ V and VDD = 2.5 V. The total capacitance at the output is 50fF.

(a) Using general expression for MOSFET resistance in saturation, what is the resistance for each transistor? ($R_n = 2$ Kohm, $R_p = 6.25$ Kohm)
(b) What is the rise time of this circuit? (685.5ps)
(c) What is the fall time of this circuit? (220ps)
(d) What is the high-to-low propagation delay for this inverter? (69.3ps)
(e) What is the low-to-high propagation delay for this inverter? (217ps)

3. Consider the NOT gate shown in figure of example 1 when an external load of $C_L = 80$fF is connected to the output. The electrical channel length is $L = 0.8\ \mu$m.

(a) Find the input capacitance of the circuit. (32.4 fF) Hint : $C_{in} = C_{Gp} + C_{Gn}$ Where $C_G = C_{ox}WL'$
(b) Find the values of R_n and R_p. (303.03 ohm, 387.6 ohm)
(c) Calculate rise and fall times for the inverter. (111.24ps, 87.04ps)

CMOS Inverter- Power Dissipation

- The current I_{DD} flowing from power supply to ground gives a dissipated power of-

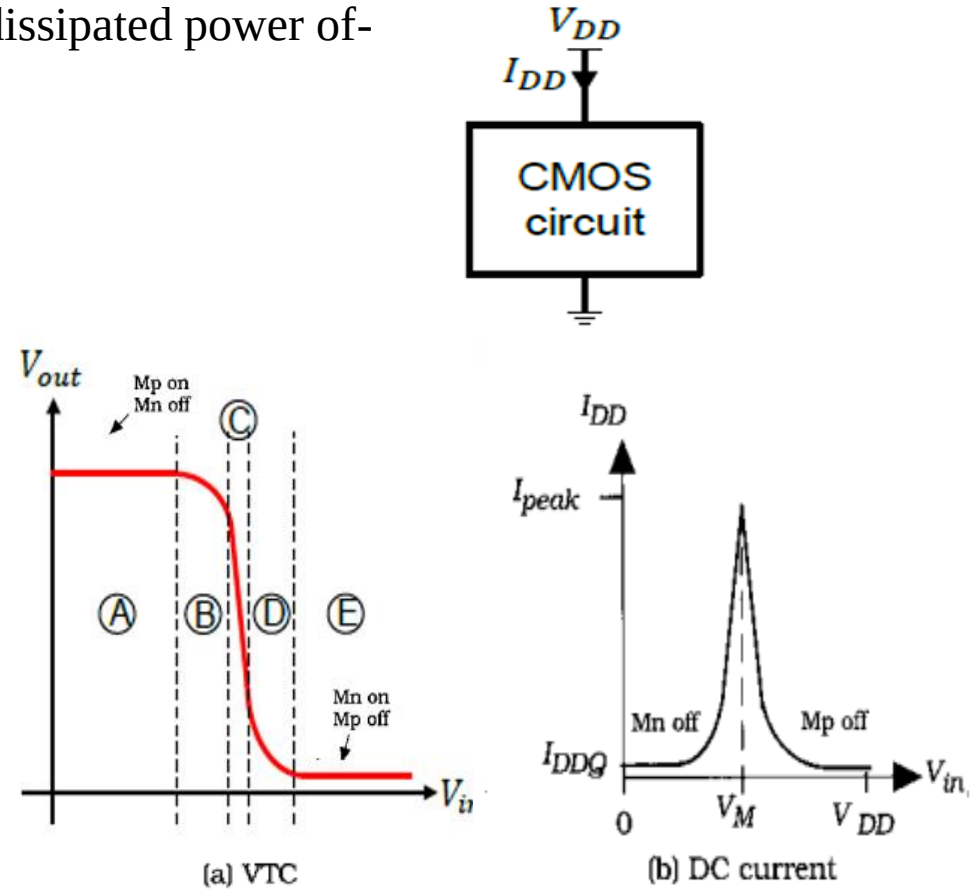
$$P = V_{DD}I_{DD}$$

- The current is divided into DC and dynamic contributions so

$$P = P_{DC} + P_{dyn}$$

DC Power P_{DC} (Static power) –

- When the input voltage V_{in} stable at logic "0" or logic "1".
- Region A, E: $I_{DD} = 0$
  - Actually, there is leakage current I_{DDQ}.
    - » I_{DDQ}: quiescent leakage current
  - $P_{DC} = V_{DD}I_{DDQ}$



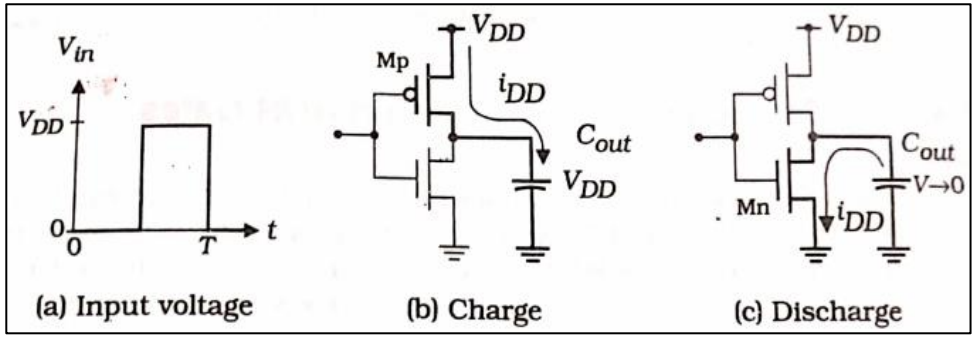
CMOS Inverter- Power Dissipation

Dynamic Power Dissipation P_{dyn} (Switching Power)-

- When the input is switching the **power dissipated** is called **dynamic power dissipation**.
- A complete cycle of input voltage effectively creates a path for the current to flow from the power supply to the ground.
- During the first half cycle of input voltage-

➢ Stored electric charge on the capacitor

$$Q_e = C_{out} V_{DD}$$



- During the second half cycle same amount of charge is lost.
- The average power dissipated over a single cycle, of input voltage $V_{in,}$ with a period T is-

$$P_{av} = V_{DD} I_{DD} = V_{DD} (Q_e/T)$$

$$\boxed{P_{dyn} = C_{out} V^2_{DD} f} \qquad \text{where } f = 1/T$$

Total power

$$\boxed{P = V_{DD} I_{DDQ} + C_{out} V^2_{DD} f}$$

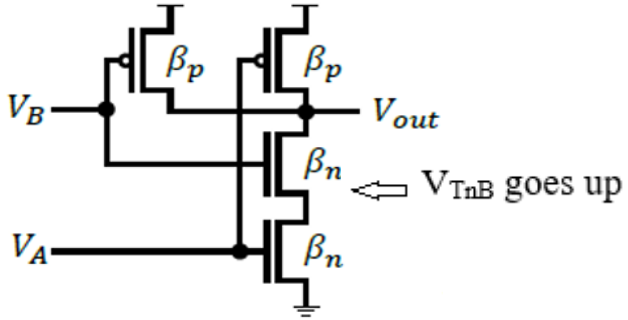
Power increases with Cout and frequency, and strongly with VDD

"A fast circuit dissipates more power than a slow circuit"

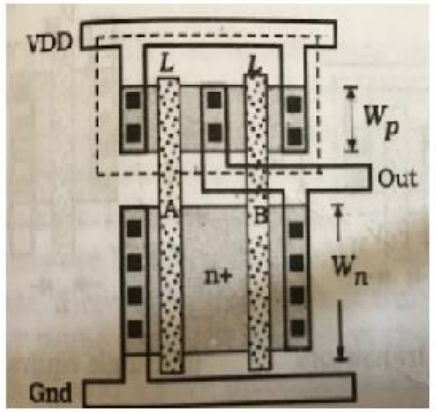
DC Characteristics – NAND Gate

- **NAND Analysis**

➢ Both the pFETs are described by β_p and both nFETs have same β_n.



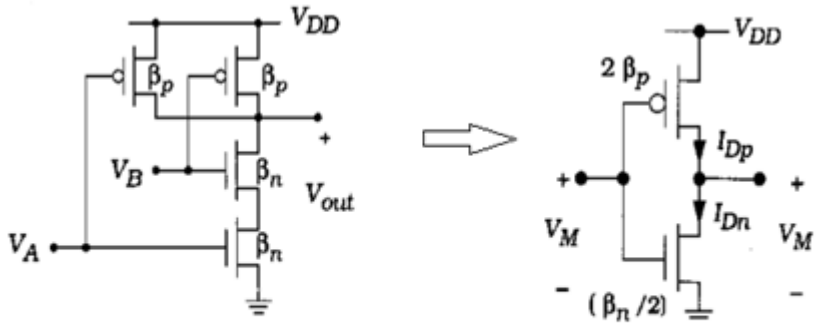
NAND2 logic circuit



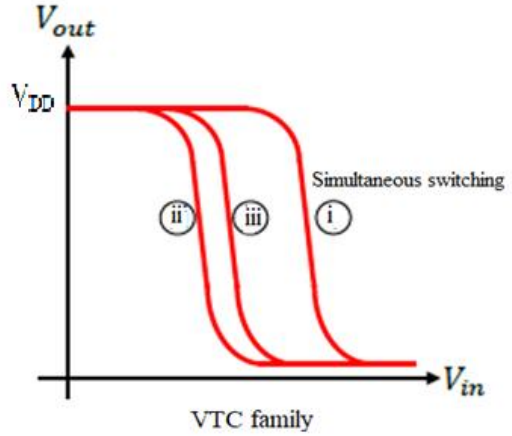
NAND2 Layout

	V_A	V_B	V_{out}
(i)	0	0	V_{DD}
(ii)	0	V_{DD}	V_{DD}
(iii)	V_{DD}	0	V_{DD}
	V_{DD}	V_{DD}	0

Transition Table



Simplified V_M circuit for the NAND2 gate (Simultaneous switching)



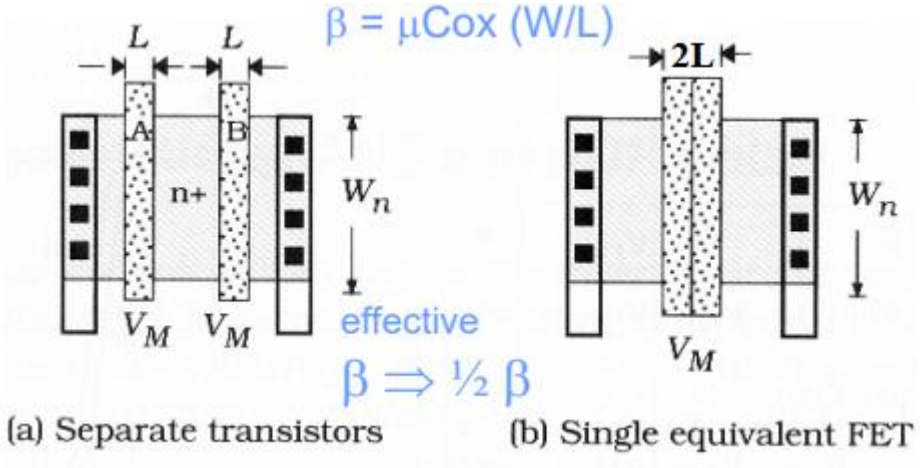
VTC family

DC Characteristics – NAND Gate

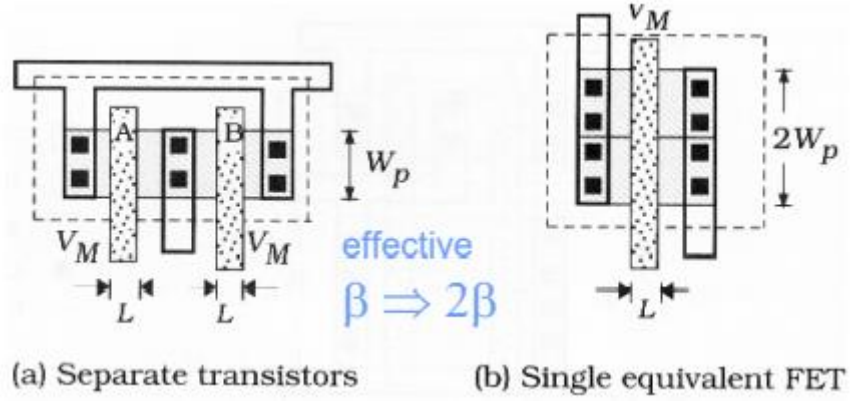
- **Series/Parallel Equivalent Circuits-**

➢ Inputs must be at the same value/voltage

Series transistors – increases effective length



Parallel transistors – increases effective width



DC Characteristics – NAND Gate

Midpoint voltage for simultaneous switching condition-

- V_M $(V_{in} = V_{out} = V_M)$
  - nFET network: $\frac{\beta_n}{2}$
  - pFET network: $2\beta_p$
- Both nFET and pFET are in saturation region

$$I_{DSn} = \frac{(\frac{\beta_n}{2})}{2}(V_M - V_{Tn})^2$$

$$I_{SDp} = \frac{(2\beta_p)}{2}(V_{DD} - V_M - |V_{Tp}|)^2$$

Solve $I_{DSn} = I_{SDp}$

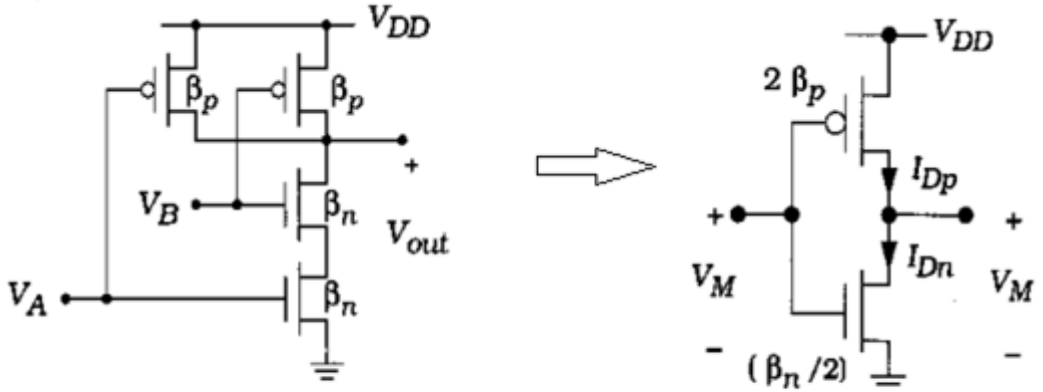
$$\frac{\left(\frac{\beta_n}{2}\right)}{2}(V_M - V_{Tn})^2 = \frac{(2\beta_p)}{2}(V_{DD} - V_M - |V_{Tp}|)^2$$

$$\Rightarrow \frac{1}{4}\frac{\beta_n}{\beta_p}(V_M - V_{Tn})^2 = (V_{DD} - V_M - |V_{Tp}|)^2$$

Taking Square root -

$$\Rightarrow \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}(V_M - V_{Tn}) = (V_{DD} - V_M - |V_{Tp}|)$$

$$\Rightarrow V_M\left(1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}\right) = V_{DD} - |V_{Tp}| + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}V_{Tn}$$



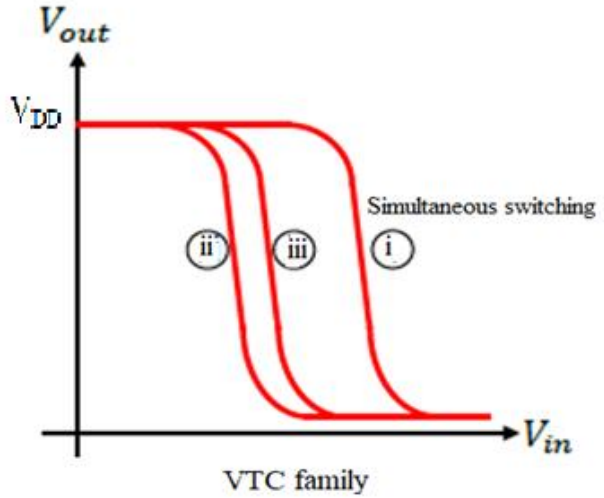
Simplified V_M circuit for the NAND2 gate (Simultaneous switching)

DC Characteristics – NAND Gate

For 2-Input NAND Gate

$$V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{2} V_{Tn} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{2}\sqrt{\frac{\beta_n}{\beta_p}}}$$

For Inverter- $$V_M = \frac{VDD - |V_{tp}| + V_{tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$



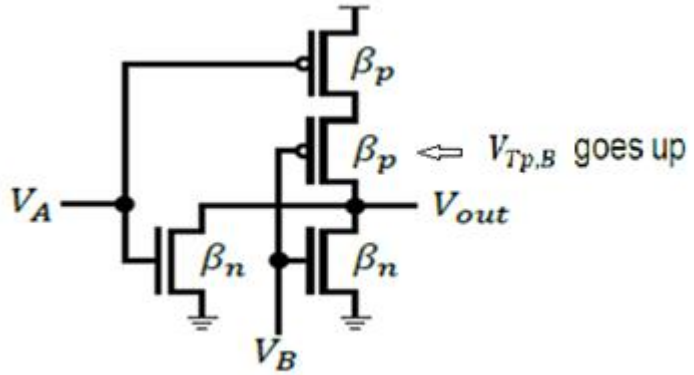
- For NAND*k*

$$V_M = \frac{V_{DD} - |V_{Tp}| + \frac{1}{k} V_{Tn} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \frac{1}{k}\sqrt{\frac{\beta_n}{\beta_p}}}$$

DC Characteristics – NOR Gate

- **NOR Analysis**

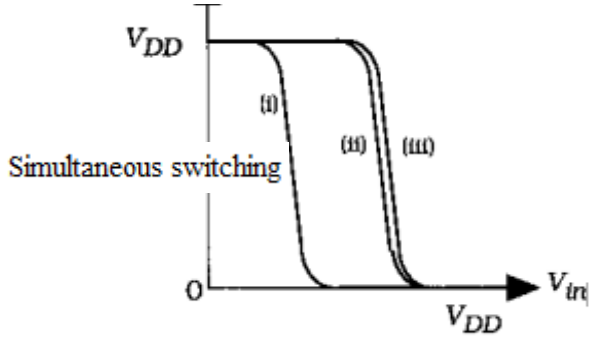
➢ Both the pFETs are described by β_p and both nFETs have same β_n.



NOR2 logic circuit

	V_A	V_B	V_{out}
	0	0	V_{DD}
(iii)	0	V_{DD}	0
(ii)	V_{DD}	0	0
(i)	V_{DD}	V_{DD}	0

Transition table



VTC family

- The substrate Fermi potential ϕF is negative in NMOS, positive in pMOS
- The substrate bias coefficient γ is positive in nMOS, negative in pMOS
- For pFET-

$$V_{TP} = V_{TP}(V_{SB}=0) - \gamma_p\left(\sqrt{2\phi_n - V_{SB}} - \sqrt{2\phi_n}\right)$$

DC Characteristics – NOR Gate

Midpoint voltage for simultaneous switching condition-

- V_M $(V_{in} = V_{out} = V_M)$
  - nFET network: $2\beta_n$
  - pFET network: $\frac{\beta_p}{2}$

- Both nFET and pFET are in saturation region

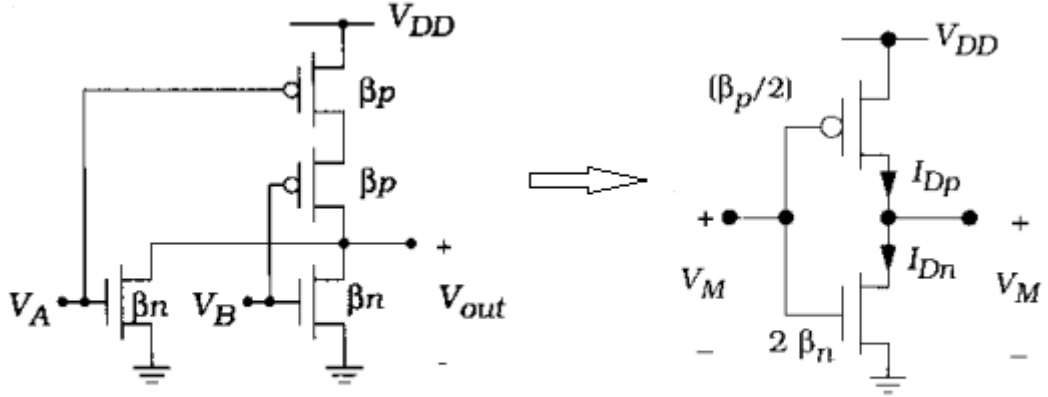
$$I_{DSn} = \frac{2\beta_n}{2}(V_M - V_{Tn})^2$$

$$I_{SDp} = \frac{(\frac{\beta_p}{2})}{2}(V_{DD} - V_M - |V_{Tp}|)^2$$

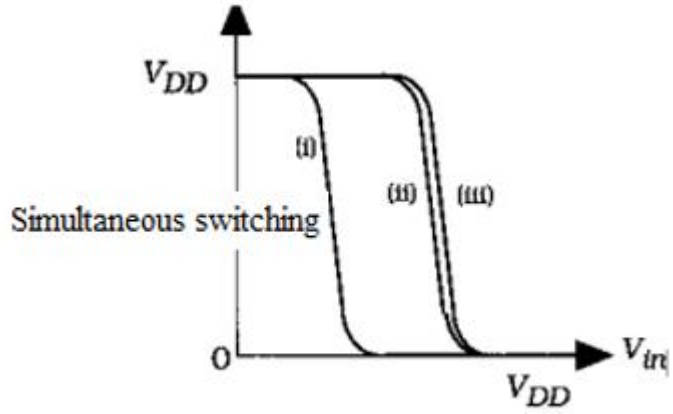
Solve $I_{DSn} = I_{SDp}$.

$$V_M = \frac{V_{DD} - |V_{Tp}| + 2V_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + 2\sqrt{\frac{\beta_n}{\beta_p}}}$$

- For NORk
  - $V_M = \frac{V_{DD} - |V_{Tp}| + kV_{Tn}\sqrt{\frac{\beta_n}{\beta_p}}}{1 + k\sqrt{\frac{\beta_n}{\beta_p}}}$



Simplified V_M circuit for the NOR2 gate (Simultaneous switching)



VTC family

Assignment-3

1. A CMOS NAND2 is designed using identical nFETs with a value of $\beta_n = 2\beta_p$; the pFETs are the same size. The power supply is chosen to be
   V_{DD} = 5 V and the device threshold voltages are given as V_{Tn} = 0.6 V and V_{Tp} = -0.7 V.
   (a) Find the midpoint voltage V_M for the case of simultaneous switching. (2.77 V)
   (b) What would be the midpoint voltage for an inverter made with the same β specifications? (2.13 V)

2. A CMOS NOR2 gate is designed using nFETs with a value of β_n. The pFETs are both described by $\beta_p = 2.2\ \beta_n$. Find the value of V_M for the case of simultaneous switching if V_{DD} = 3.3 V, V_{Tn} = 0.65 V and V_{Tp} = - 0.80 V. (1.47 V)

3. A NAND3 gate uses identical nFETs with an aspect ratio of 4. The nFET process transconductance is 120 $\mu A/V^2$, and the threshold voltage is 0.55 V. A power supply of 5 V is chosen for the circuit.
   Find the value of the pFET β_p needed to create a gate where the case of simultaneous switching gives a midpoint voltage of V_M = 2.4 V, Assume that V_{Tp} = -0.90 V and r = 2.4. (63.16 $\mu A/V^2$)

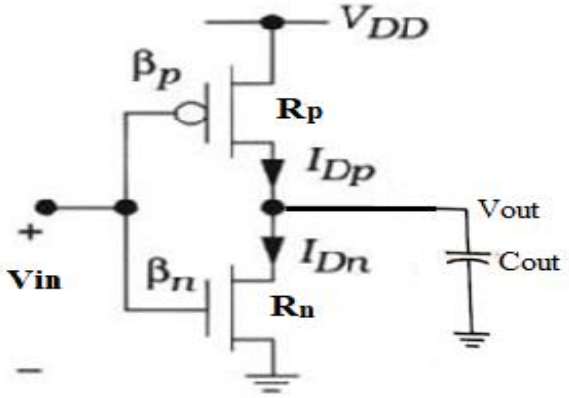
Gate Design for Transient Performance

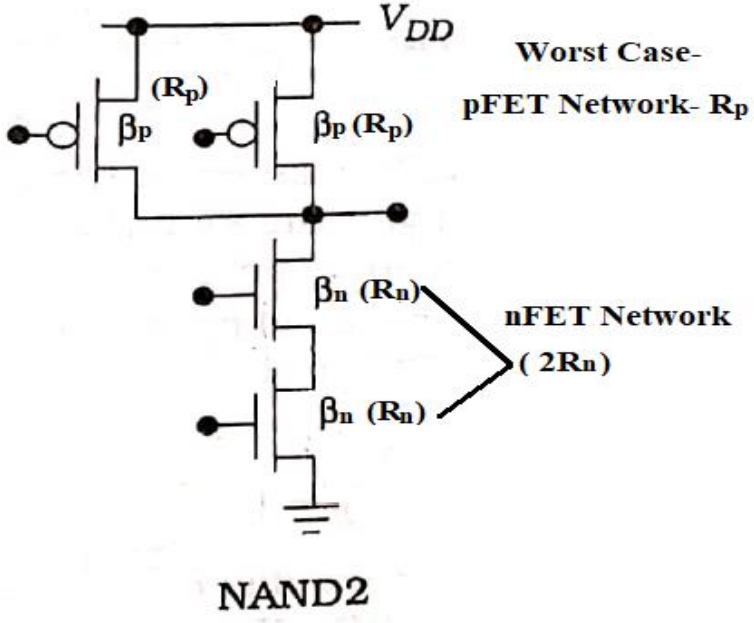
- **Why Logic Gate Sizing ?**

➢ High Speed Circuits are limited by the switching time of individual gates.

➢ Aspect Ratios – Critical Design Parameters for both DC and transient switching times.

➢ Inverter is used as a reference and then attempt to design other gates that have approximately the same switching times.





$t_r = 2.2\ R_p\ C_{out}$ $\qquad$ $t_f = 2.2\ R_n\ C_{out}$

$t_r\ \alpha\ R_p$ $\qquad$ $t_f\ \alpha\ R_n$

Gate Design for Transient Performance

- **Non Symmetrical Inverter**

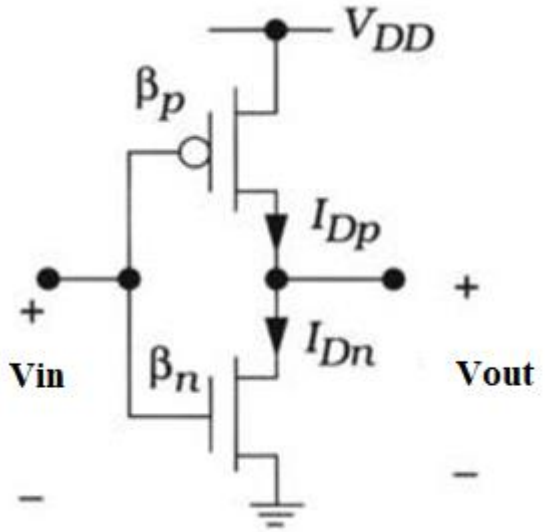
➢A non Symmetrical Inverter uses equal size of transistor. Where βn > βp

$(W/L)_n = (W/L)_p$

$C_{OXn} = C_{OXp}$ (always)

$$\frac{\beta_n}{\beta_p} = \frac{\mu_n C_{oxn}\left(\frac{W}{L}\right)_n}{\mu_p C_{oxp}\left(\frac{W}{L}\right)_p} = \frac{\mu_n}{\mu_p} \cong 2or3$$

$$\frac{k'_n}{k'_p} = \frac{\mu_n}{\mu_p} = r = \text{mobility ratio}$$



pFET: $V_{Tp} < 0$

$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

nFET: $V_{Tn} > 0$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$

Gate Design for Transient Performance

- **Symmetrical Inverter**

➢Generally Symmetrical Inverter (Unit Size Inverter) is used as a sizing reference in designing any logic function.

For Symmetrical Inverter

$$\beta_n = \beta_p$$

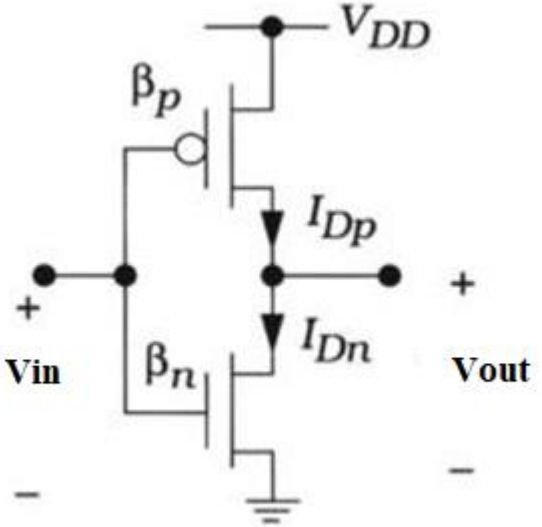
That requires, Vtn = |Vtp| and

$$\left(\frac{W}{L}\right)_p = r\left(\frac{W}{L}\right)_n$$

$$r = \frac{k'_n}{k'_p}$$ Where K' = μ Cox

$$\mathbf{R_n = R_p \Longrightarrow t_r = t_f}$$

$$R_p = \frac{1}{\beta_p(V_{DD} - |V_{Tp}|)}, \qquad R_n = \frac{1}{\beta_n(V_{DD} - V_{Tn})}$$



pFET: $V_{Tp} < 0$

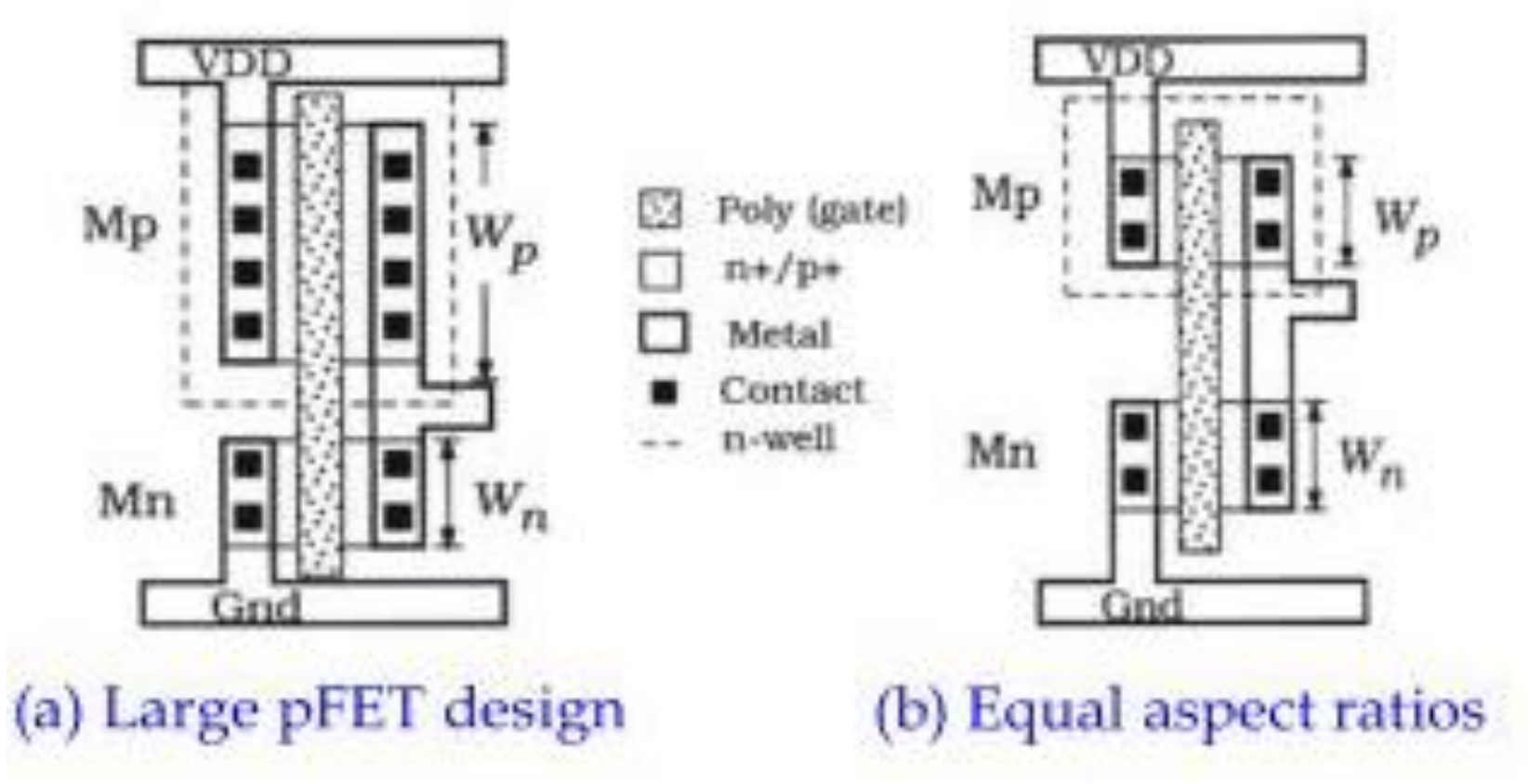
$$\beta_p = k'_p \left(\frac{W}{L}\right)_p$$

nFET: $V_{Tn} > 0$

$$\beta_n = k'_n \left(\frac{W}{L}\right)_n$$

Gate Design for Transient Performance

- Identify Symmetrical and Non Symmetrical CMOS Inverter



(a) Large pFET design

(b) Equal aspect ratios

Gate Design for Transient Performance

- **Symmetrical NAND2 Sizing**

➢Consider parallel pFETS- Worst case

$$\beta_P = \beta_p$$

➢Series-connected nFETs-

$$R = R_N + R_N \quad \text{where} \quad R_N = \frac{1}{\beta_N(V_{DD} - V_{Tn})}$$

Using the inverter as a reference, we set

$$R = R_n = 2R_N$$

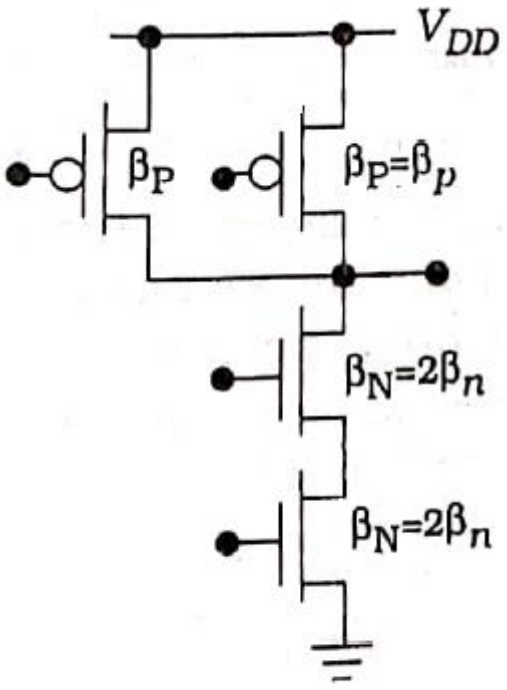
Substituting,

$$\frac{1}{\beta_n(V_{DD} - V_{Tn})} = \frac{2}{\beta_N(V_{DD} - V_{Tn})}$$

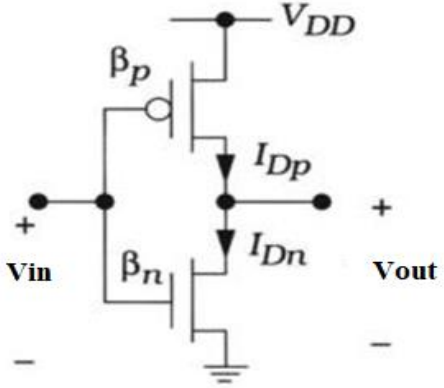
which has the solution

$$\beta_N = 2\beta_n$$

$$\left(\frac{W}{L}\right)_N = 2\left(\frac{W}{L}\right)_n$$



NAND2



Gate Design for Transient Performance

- **Symmetrical NOR2 Sizing**

➢For parallel nFETs- worst case

$$\beta_N = \beta_n$$

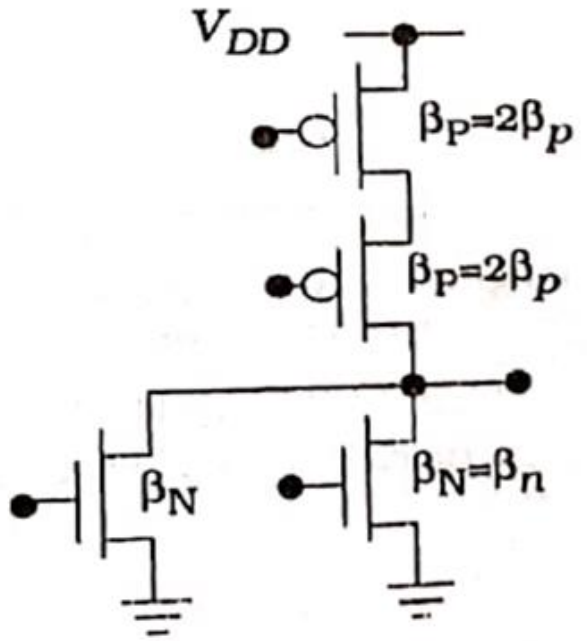
➢For series connected pFETs-

$$R = R_p = 2R_P$$

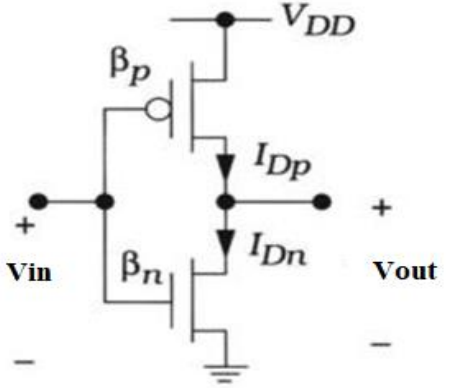
$$\frac{1}{\beta_p(V_{DD}-|V_{Tp}|)} = \frac{2}{\beta_P(V_{DD}-|V_{Tp}|)}$$

$$\beta_P = 2\beta_p$$

$$\left(\frac{W}{L}\right)_P = 2\left(\frac{W}{L}\right)_p$$

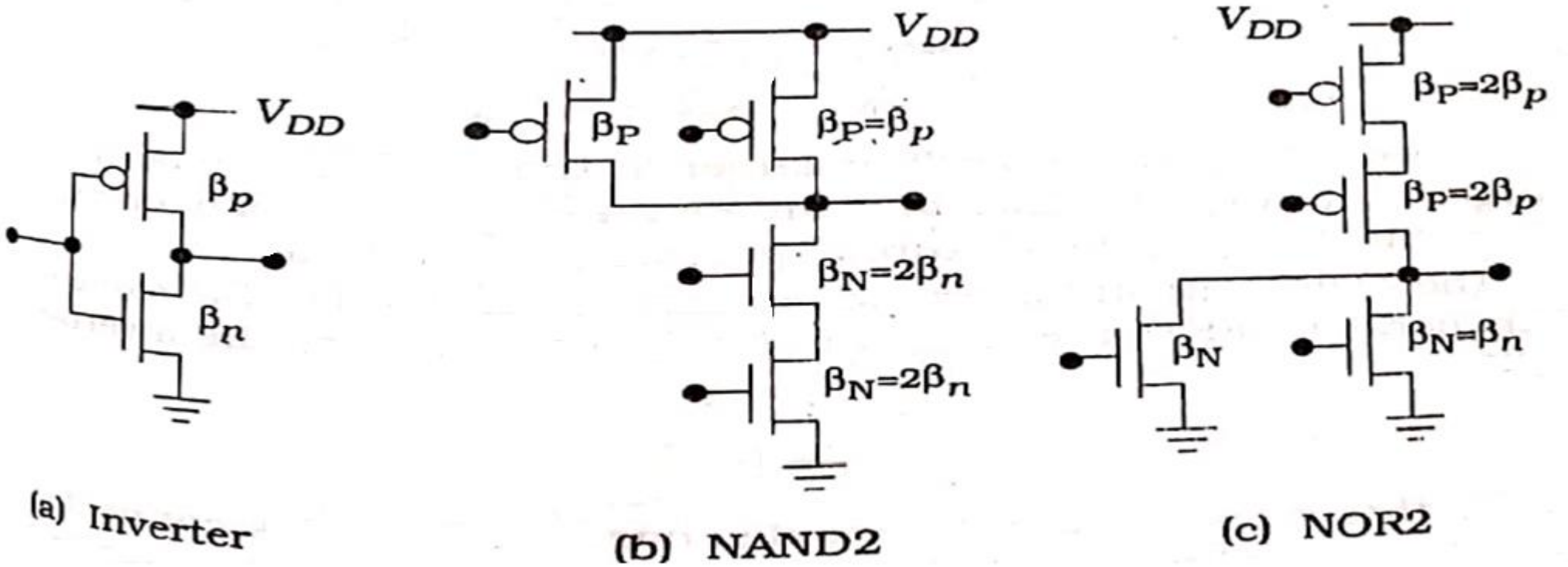


NOR2



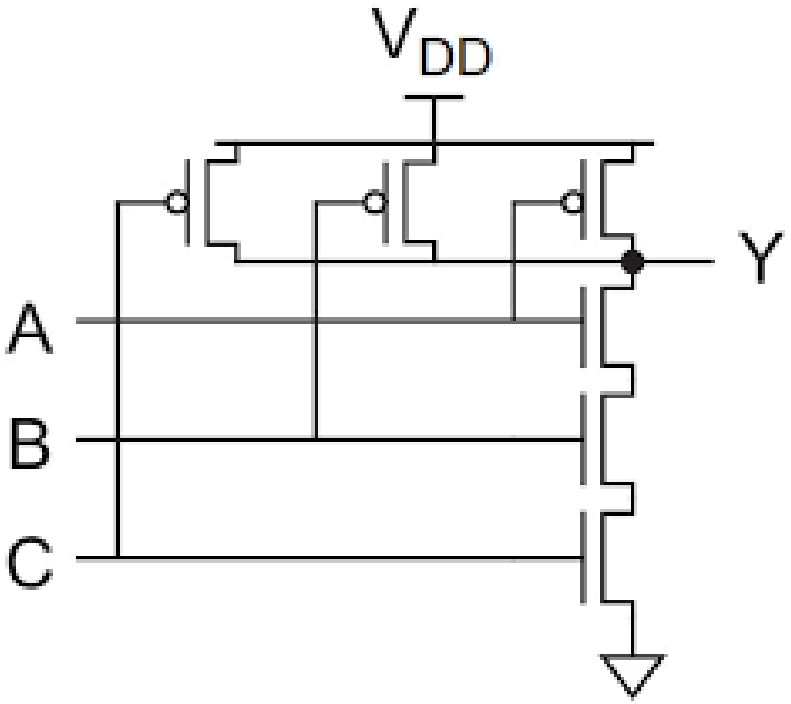
Gate Design for Transient Performance

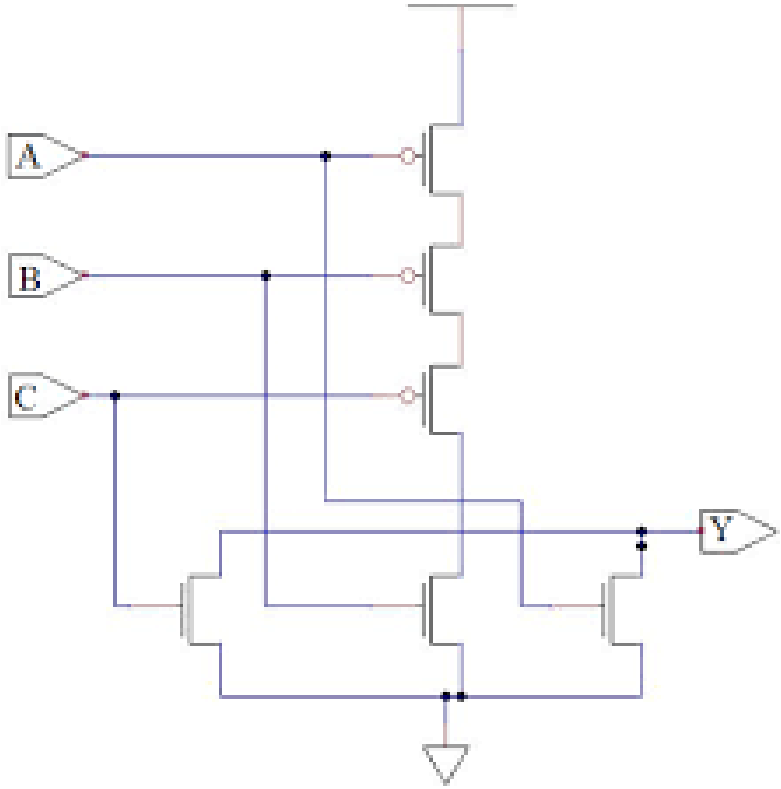
- **Summary**



Gate Design for Transient Performance

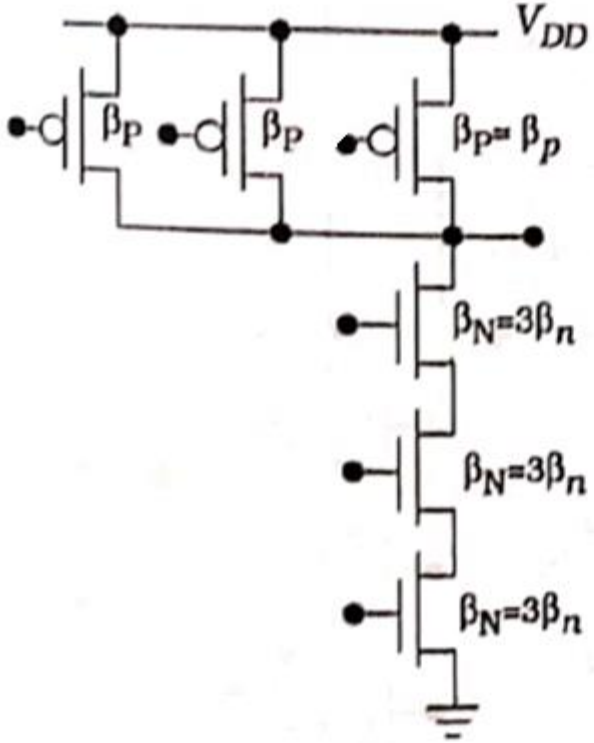
- **Sizing of 3-Input gates**



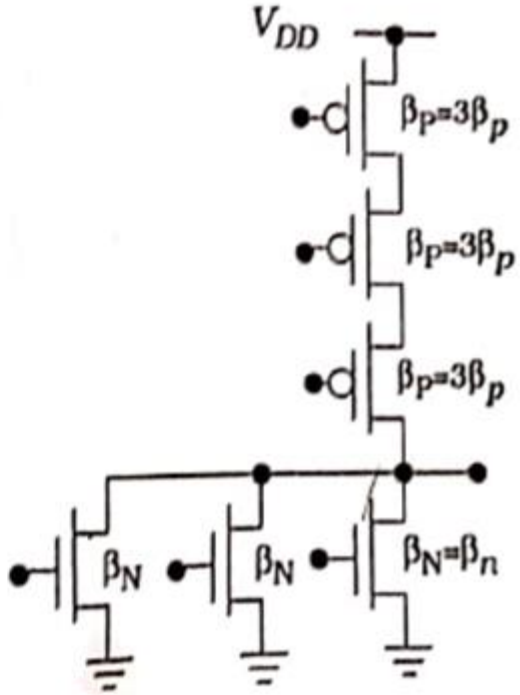


Gate Design for Transient Performance

- **Answer-**



(a) NAND3



(b) NOR3

Gate Design for Transient Performance

- **Sizing of Complex function**

A CMOS logic gate that implements the function

$$f = \overline{(a \cdot b + c \cdot d) \cdot x}$$

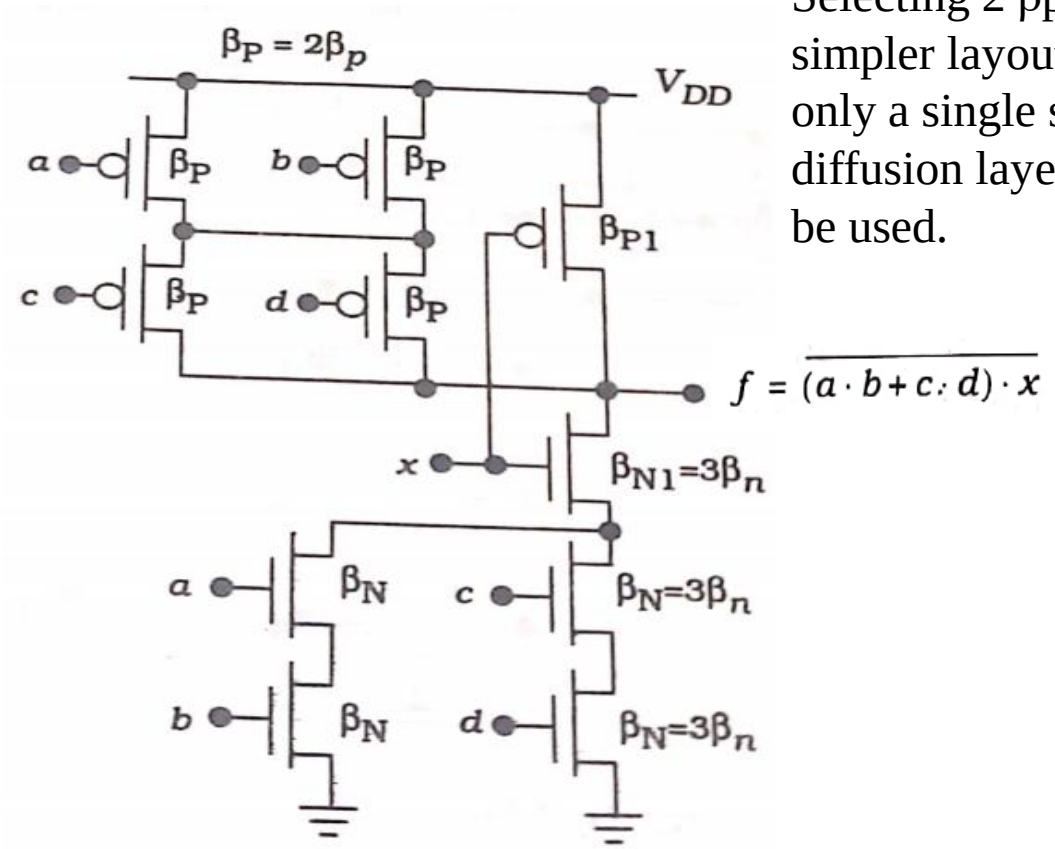
(a) Design the logic circuit.

(b) An inverter with $\beta_n = \beta_p$ is used as sizing reference. Find the device sizes needed to equalize the nFET and pFET resistances.

Ans. $\beta_N = \beta_{N1} = 3\ \beta_n = 3\beta_p$
$\beta_P = 2\beta_p$
$\beta_{P1} = 2\beta_p$ or β_p

(c) An inverter with $\beta_n = 1.5\beta_p$ is used as sizing reference. Find the device sizes needed to equalize the nFET and pFET resistances.

Ans. $\beta_N = \beta_{N1} = 3\ \beta_n = 4.5\beta_p$
$\beta_P = 2\beta_p$
$\beta_{P1} = 2\beta_p$ or β_p



$\beta_{P1} = 2\ \beta p$ or βp
Selecting 2 βp leads to simpler layout since only a single size P+ diffusion layer would be used.

Assignment-4

1. A CMOS logic gate that implements the function

$$F = \overline{x.(y+z) + x.w}$$

(a) Design the logic circuit.

(b) An inverter with $\beta_n = \beta_p$ is used as sizing reference. Find the device sizes needed to equalize the nFET and pFET resistances.

2. A CMOS logic gate that implements the function

$$F = \overline{(a+b).(b+c).d}$$

(a) Design the logic circuit.

(b) An inverter with $\beta_n = 1.5\ \beta_p$ is used as sizing reference. Find the device sizes needed to equalize the nFET and pFET resistances.

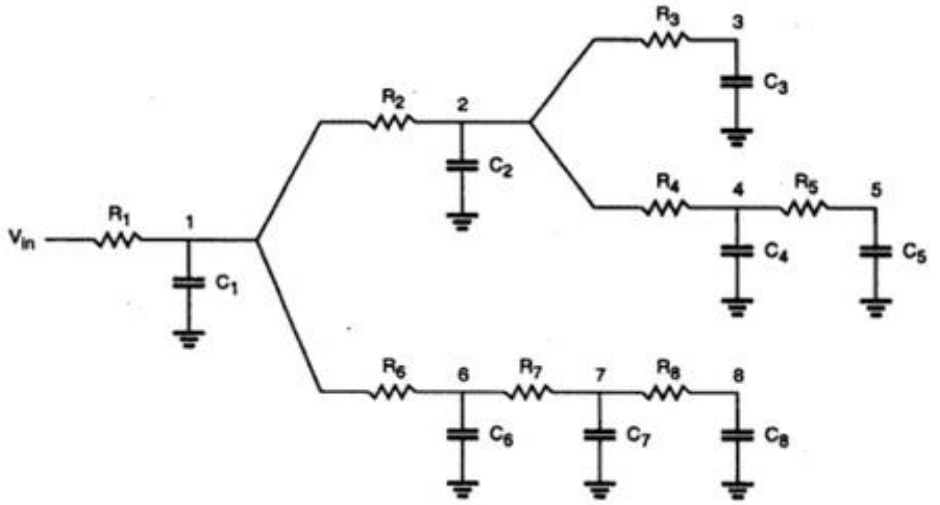
Elmore Delay Calculation

- Consider a general RC tree network,

  i) There are no resistor loops in this circuit

  ii) All of the capacitors in an RC tree are connected between a node and the ground

  iii) There is one input node in the circuit. Also notice that there is a unique resistive path, from the input node to any other node in the circuit.

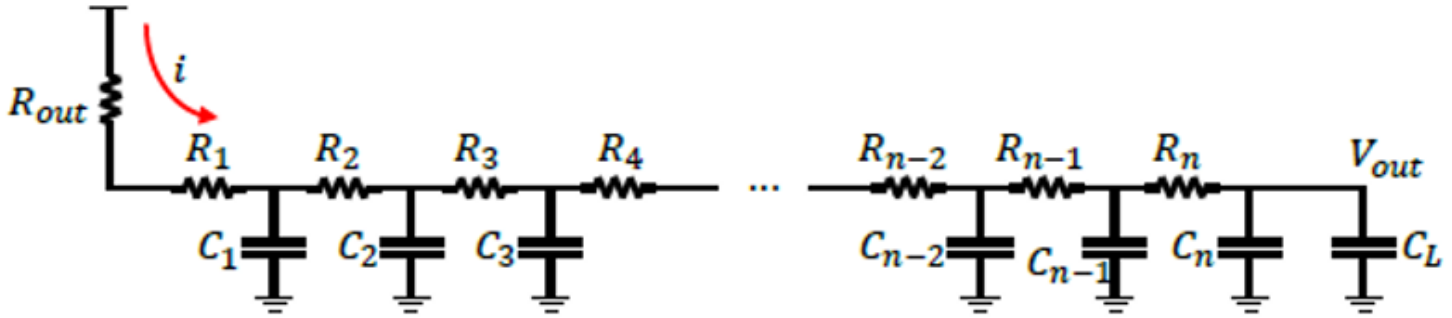


- Inspecting the general topology of this RC tree network, we can make the following path definition:
  - Let Pi denote the unique path from the input node to node i, i = 1,2,3,…..,N
  - Let Pij = Pi ∩ Pj denote the portion of the path between the input and the node i, which is common to the path between the input and node j.
  - Assuming that the input signal is a step pulse at time t = 0, the Elmore delay at node i of this RC tree is given by the following expression.

$$\tau_{Di} = \sum_{j=1}^{N} Cj \sum_{for\ all\ k \in Pij} Rk$$

Elmore Delay Calculation

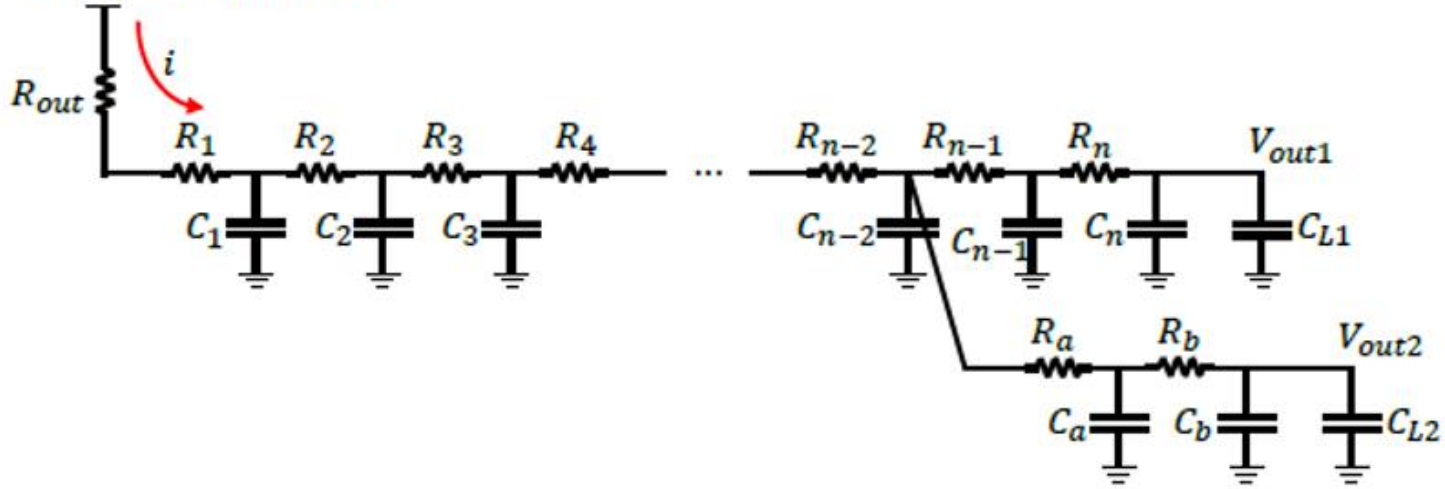
- How to estimate delay in general RC networks.
  - How to
    - Start at the target sink node.
    - Traverse the RC network toward the source.
    - Whenever there is a resistor, multiply its resistance and its downstream capacitance and add it to the total delay.
  - For two-pin nets



$$\tau = R_n(C_n + C_L) + R_{n-1}(C_{n-1} + C_n + C_L) + R_{n-2}(C_{n-2} + C_{n-1} + C_n + C_L) + \ldots + R_3(C_3 + \cdots + C_n + C_L) + R_2(C_2 + \cdots + C_n + C_L) + R_1(C_1 + \cdots + C_n + C_L) + R_{out}(C_1 + \cdots + C_n + C_L)$$

Elmore Delay Calculation

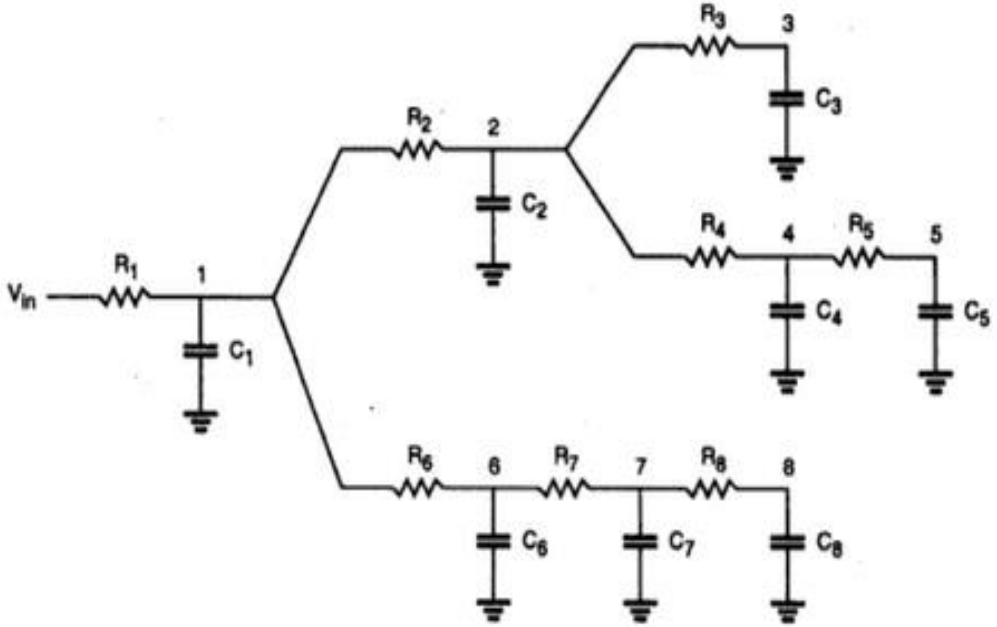
- How to estimate delay in general RC networks.
  - For multi-pin nets



$$\tau(V_{out1}) = R_n(C_n + C_{L1}) + R_{n-1}(C_{n-1} + C_n + C_{L1}) +$$
$$R_{n-2}(C_{n-2} + C_{n-1} + C_n + C_{L1} + C_a + C_b + C_{L2}) +$$
$$\ldots + R_3(C_3 + \cdots + C_n + C_{L1} + C_a + C_b + C_{L2}) +$$
$$R_2(C_2 + \cdots + C_n + C_{L1} + +C_a + C_b + C_{L2}) + R_1(C_1 + \cdots + C_n + C_{L1} + C_a + C_b + C_{L2}) +$$
$$R_{out}(C_1 + \cdots + C_n + C_{L1} + +C_a + C_b + C_{L2})$$

Elmore Delay Calculation

- **Example**



Elmore Delay at node 7 can be calculated as

$$\tau_{D7} = R_7(C_7 + C_8) + R_6(C_6 + C_7 + C_8) + R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8)$$

$$\tau_{D7} = R_1C_1 + R_1C_2 + R_1C_3 + R_1C_4 + R_1C_5 + (R_1 + R_6)C_6 + (R_1 + R_6 + R_7)C_7 + (R_1 + R_6 + R_7)C_8$$

Elmore Delay at node 5 can be calculated as

$$\tau_{D5} = R_5C_5 + R_4(C_4 + C_5) + R_2(C_2 + C_3 + C_4 + C_5) + R_1(C_1 + C_2 + C_3 + C_4 + C_5 + C_6 + C_7 + C_8)$$

$$\tau_{D5} = R_1C_1 + (R_1 + R_2)C_2 + (R_1 + R_2)C_3 + (R_1 + R_2 + R_4)C_4 + (R_1 + R_2 + R_4 + R_5)C_5 + R_1C_6 + R_1C_7 + R_1C_8$$

Elmore Delay Calculation

- **Example**

Assume N = 8 and solve if R1 = R2 = ……= R8 = 1 K Ohm, and C1 = C2 = …..= C8 = 2 pF. Find delay at node 8.