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# Operating System:

## GATE PYQ – Virtual Memory

By: Vishvadeep Gothi

# VISHVADEEP GOTHI SIR

## AIR- 19, 119, 440, 682 in GATE

**ME from IISc Bangalore**
**Mtech BITS Pilani in Data Science**

14+ Years of Teaching Experience,
10+ Years in GATE/IES

**Subjects Taken:**
Computer Organization & Architecture, data structure, operating system, C-Programming, Data science, Machine Learning, Python, coding interview problems,


# Vishvadeep Gothi

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- GATE AIR-19, 119, 440, 682 - ME from IISc, - MTech BITS Pilani (Data Science) - 14 years experience

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Starts on Aug 11, 2021 • 3:00 PM

In this session Vishvadeep Gothi will provide practice questions to students on subject operating system. And will solve those questions to make students learn how to solve questions.


**11 Aug 2021**
**3:00PM – 5:30PM**

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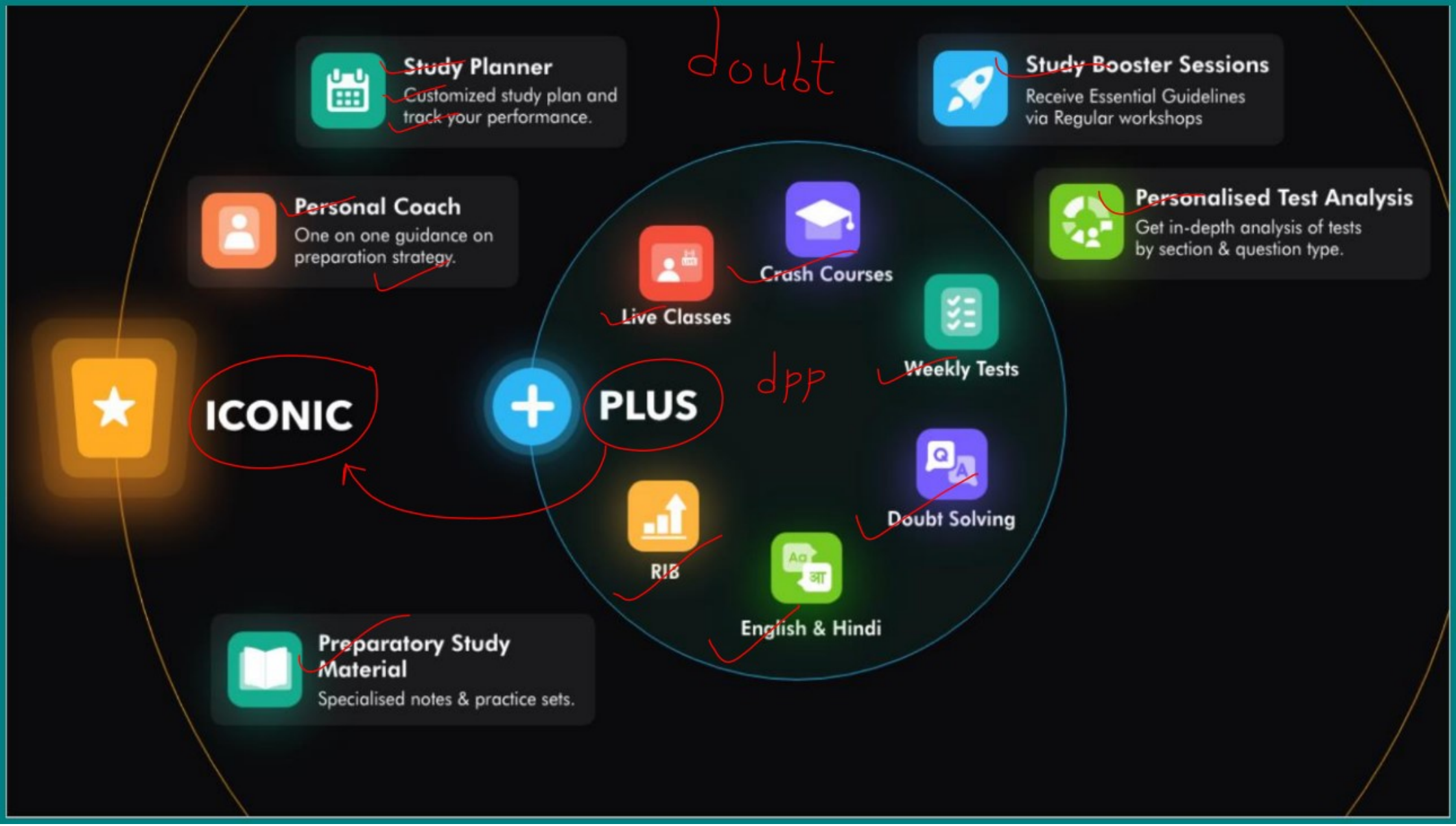
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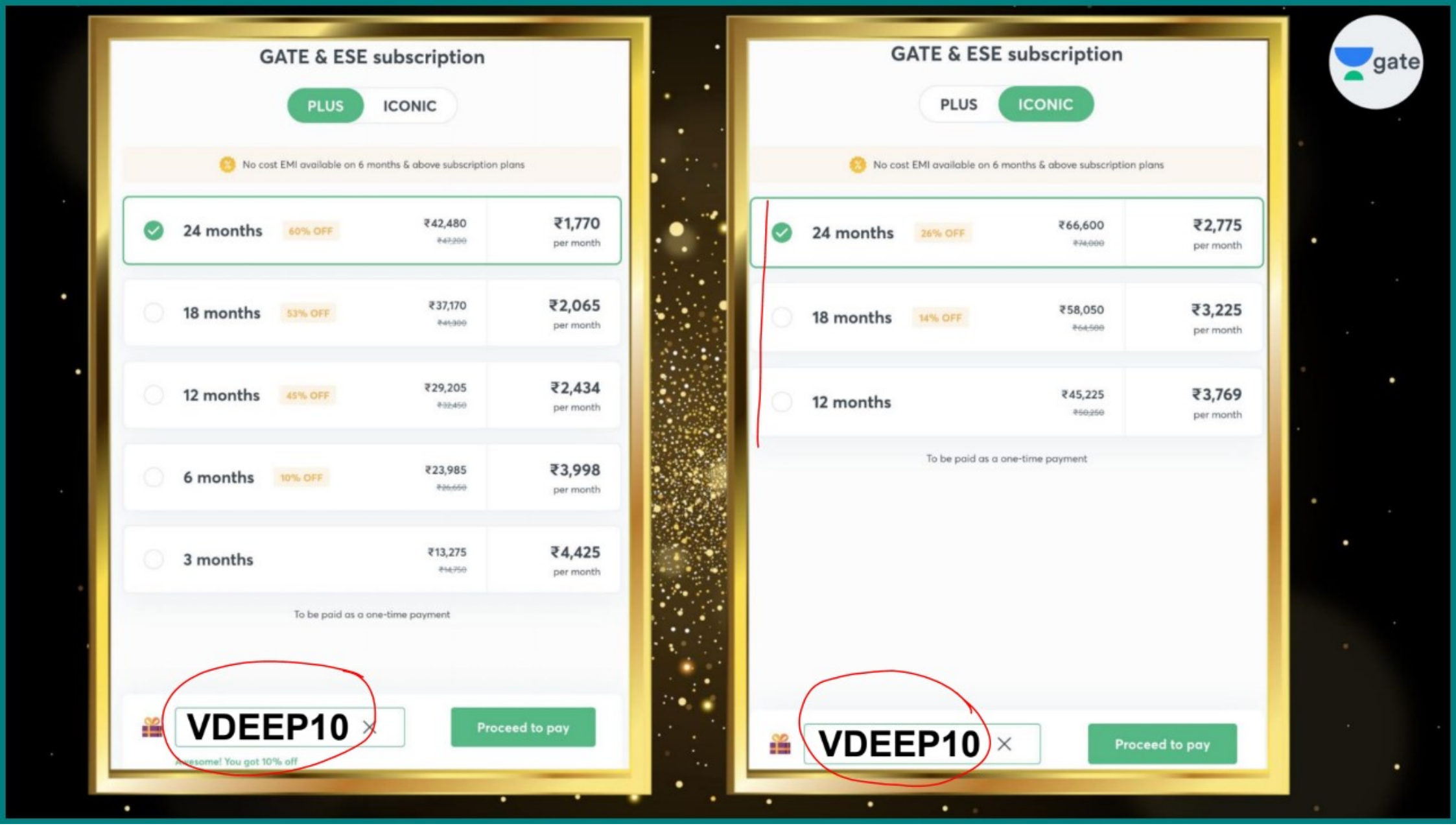
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# Are You Ready??

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# GATE 1999

A multi-user, multi-processing operating system cannot be implemented on hardware that does not support

A. Address translation
B. DMA for disk transfer
C. At least two modes of CPU execution (privileged and non-privileged)
D. Demand paging

# GATE 2000

$10 * 10^{-3}$ Sec

Suppose the time to service a page fault is on the average 10 milliseconds, while a memory access takes 1 microsecond. Then a 99.99% hit ratio results in average memory access time of

A. 1.9999 milliseconds
B. 1 millisecond
C. 9.999 microseconds
D. 1.9999 microseconds

$(0.9999 * 1 + 0.0001 * 10000)$ μs

$= 0.9999 + 1$

$= 1.9999$ μSec

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# GATE 2001

Where does the swap space reside?

A. RAM
B. Disk
C. ROM
D. On-chip cache

# GATE 2001

Which of the following statements is false?

A. Virtual memory implements the translation of a program's address space into physical memory address space
B. Virtual memory allows each program to exceed the size of the primary memory
C. Virtual memory increases the degree of multiprogramming
D. Virtual memory reduces the context switching overhead → false

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# GATE 2001

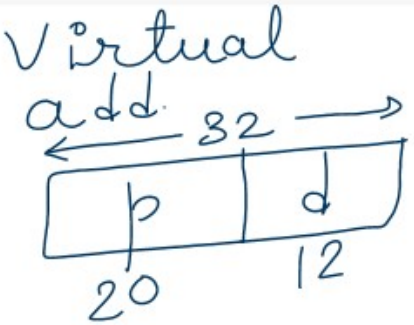
Page size = 4KB = $2^{12}$ B $\Rightarrow$ d = 12-bits

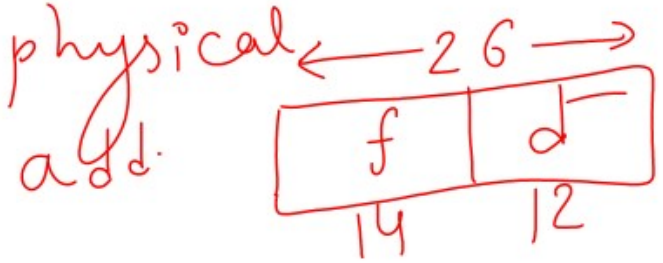
Consider a machine with 64 MB physical memory and a 32-bit virtual address space. If the page size is 4 KB, what is the approximate size of the page table?

A. 16 MB
B. 8 MB
C. 2 MB
D. 24 MB

page table size = no. of pages * 1 entry size

$= 2^{20} * 14\text{-bits} \cong 2MB$

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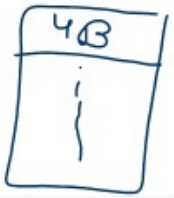
# GATE 2001

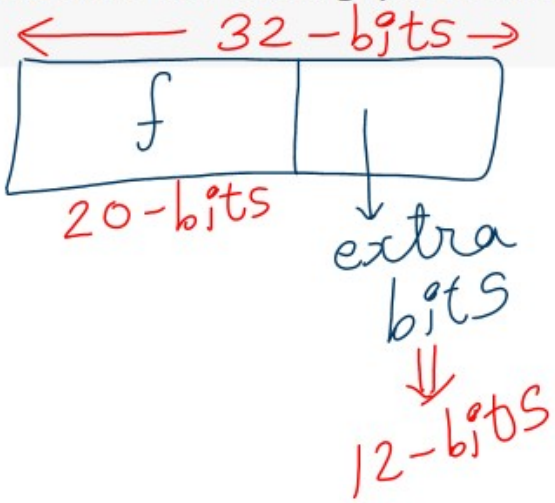


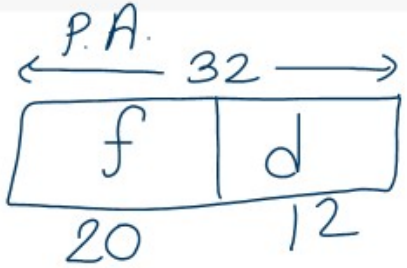

no. of entries in a page $= \frac{4KB}{4B} = 1K = 2^{10}$

A computer uses $32-bit$ virtual address, and $32-bit$ physical address. The physical memory is byte addressable, and the page size is 4 kbytes. It is decided to use two level page tables to translate from virtual address to physical address. An equal number of bits should be used for indexing first level and second level page table, and the size of each table entry is 4 bytes.

A. Give a diagram showing how a virtual address would be translated to a physical address.
B. What is the number of page table entries that can be contained in each page? $2^{10} = 1K = 1024$
C. How many bits are available for storing protection and other information in each page table entry? → 12-bits

P.T. entry

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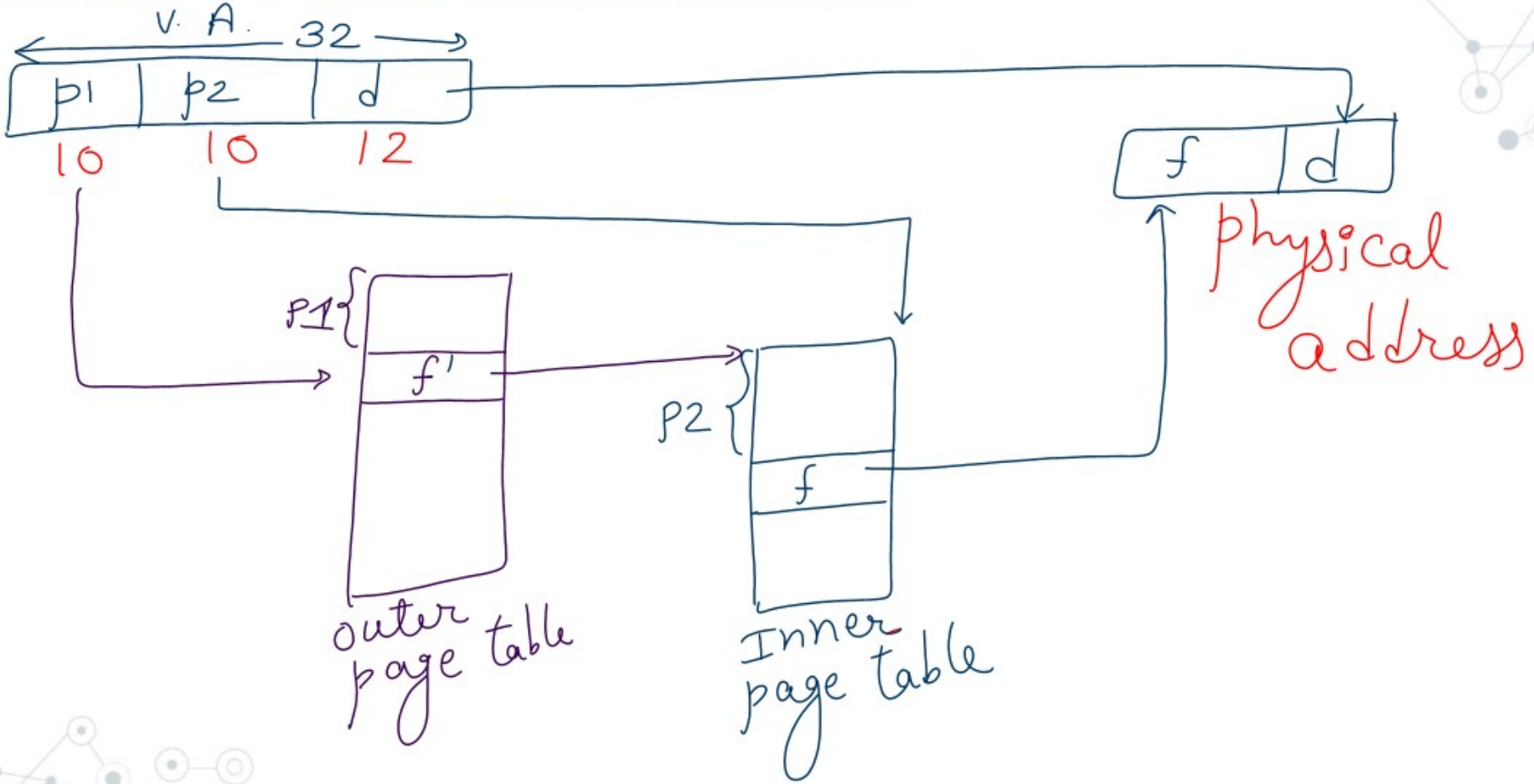
# GATE 2001 Solution

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# GATE 2003

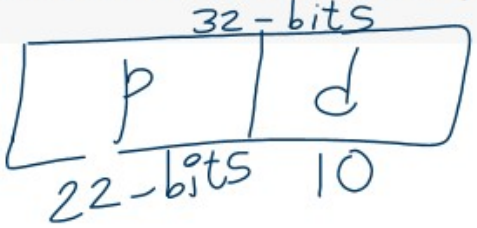
$2^{10} \Rightarrow d = 10\text{-bits}$

In a system with $32$ bit virtual addresses and $1$ KB page size, use of one-level page tables for virtual to physical address translation is not practical because of

A. the large amount of internal fragmentation
B. the large amount of external fragmentation
C. the large memory overhead in maintaining page tables
D. the large computation overhead in the translation process

22

Virtual add




no. of pages = 2

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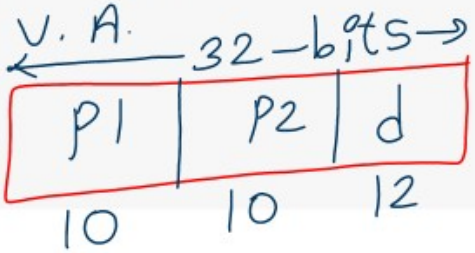
# GATE 2003

A processor uses $2-level$ page tables for virtual to physical address translation. Page tables for both levels are stored in the main memory. Virtual and physical addresses are both $32$ bits wide. The memory is byte addressable. For virtual to physical address translation, the $10$ most significant bits of the virtual address are used as index into the first level page table while the next $10$ bits are used as index into the second level page table. The $12$ least significant bits of the virtual address are used as offset within the page. Assume that the page table entries in both levels of page tables are $4$ bytes wide. Further, the processor has a translation look-aside buffer (TLB), with a hit rate of $96\%$. The TLB caches recently used virtual page numbers and the corresponding physical page numbers. The processor also has a physically addressed cache with a hit rate of $90\%$. Main memory access time is $10$ ns, cache access time is $1$ ns, and TLB access time is also $1$ ns.

Assuming that no page faults occur, the average time taken to access a virtual address is approximately (to the nearest $0.5$ ns)

A. $1.5$ ns
B. $2$ ns
C. $3$ ns
D. $4$ ns

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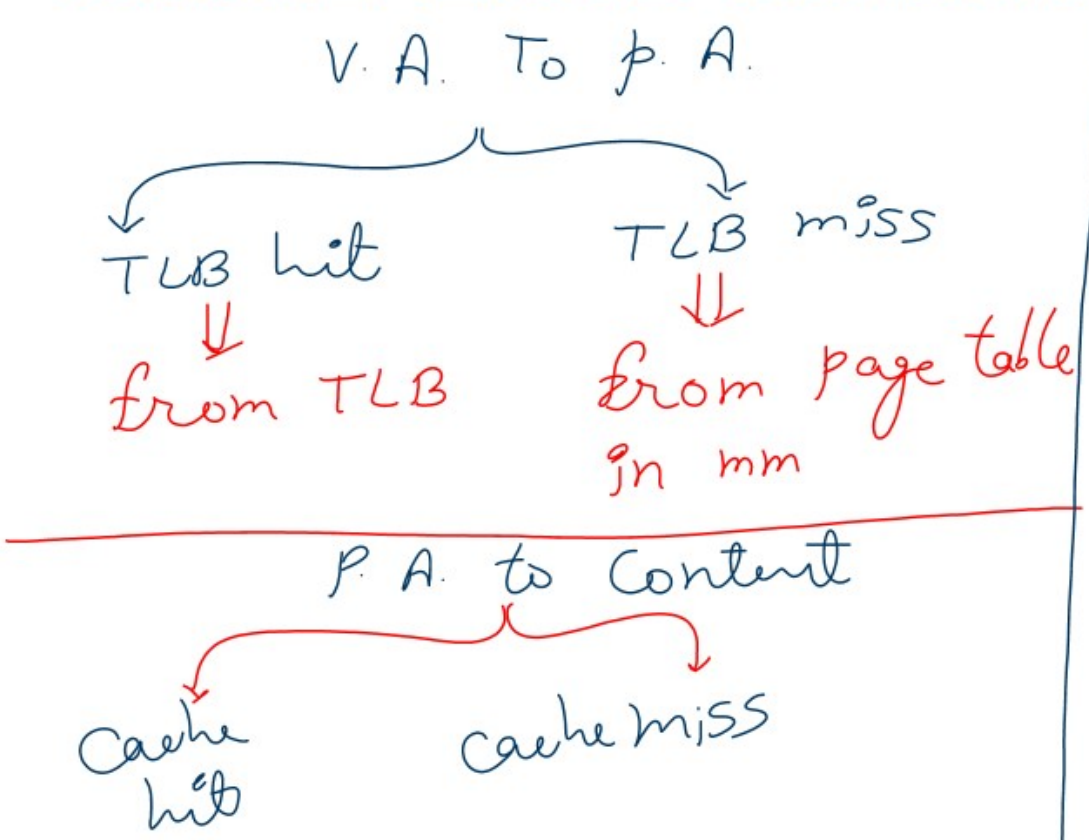
# GATE 2003 Solution



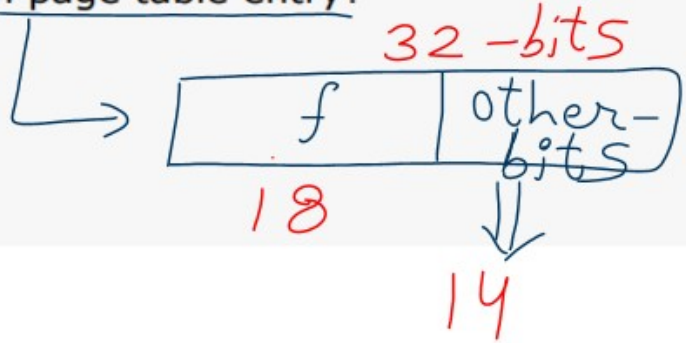

$$= 0.96\left[1ns + 0.9(1) + 0.1*(1+10)\right] + 0.04\left[1 + 2*10 + 0.9*1 + 0.1*(1+10)\right]$$

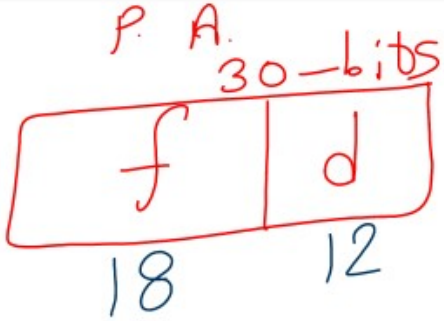
$$\cong 4\ nsec$$

# GATE 2004

In a virtual memory system, size of the virtual address is 32-bit, size of the physical address is 30-bit, page size is 4 Kbyte and size of each page table entry is 32-bit. The main memory is byte addressable. Which one of the following is the maximum number of bits that can be used for storing protection and other information in each page table entry?

A. 2
B. 10
C. 12
D. 14

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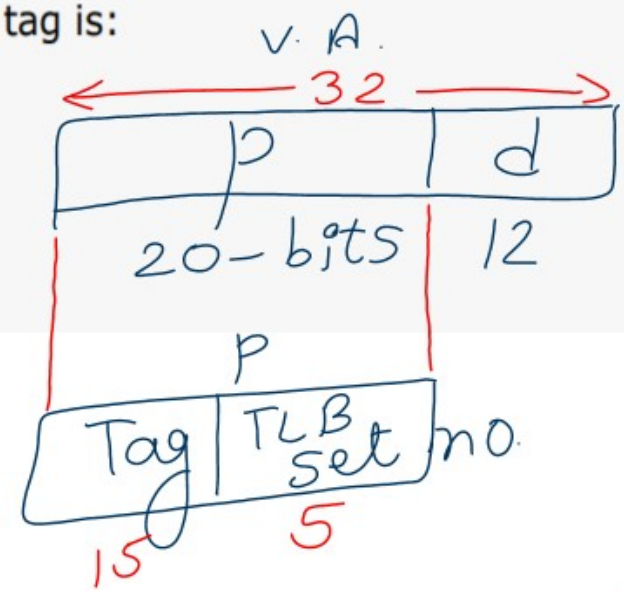
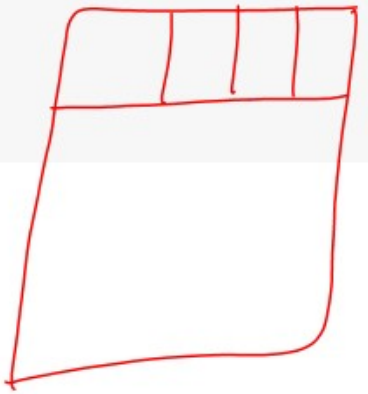
# GATE 2006

$2^{12}$ B $\Rightarrow$ d = 12-bits

A CPU generates 32-bit virtual addresses. The page size is 4 KB. The processor has a translation look-aside buffer (TLB) which can hold a total of 128 page table entries and is 4-way set associative. The minimum size of the TLB tag is:

A. 11 bits
B. 13 bits
C. 15 bits ✓
D. 20 bits



no. of sets in TLB $= \frac{128}{4} = 2^5$

Set no. = 5-bits

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# GATE 2006

A computer system supports 32-bit virtual addresses as well as 32-bit physical addresses. Since the virtual address space is of the same size as the physical address space, the operating system designers decide to get rid of the virtual memory entirely. Which one of the following is true?

A. Efficient implementation of multi-user support is no longer possible
B. The processor cache organization can be made more efficient now
C. Hardware support for memory management is no longer needed
D. CPU scheduling can be made more efficient now

# GATE 2008

A paging scheme uses a Translation Look-aside Buffer (TLB). A TLB-access takes $10$ ns and the main memory access takes $50$ ns. What is the effective access time(in ns) if the TLB hit ratio is $90\%$ and there is no page-fault?

A. $54$
B. $60$
C. $65$
D. $75$

$$= 0.9(10+50) + 0.1(10+50+50)$$

$$= 65 \text{ nsec}$$

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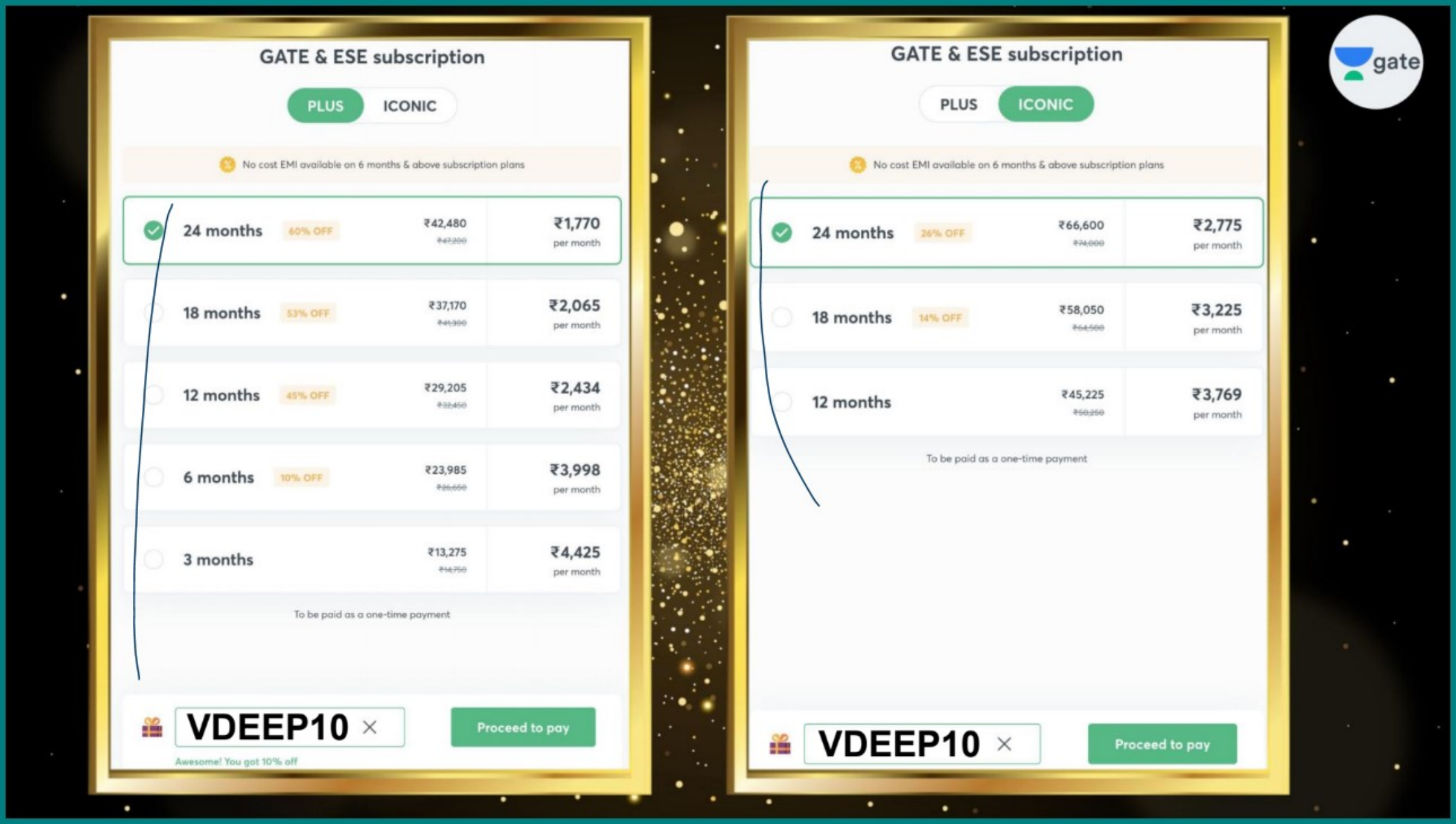
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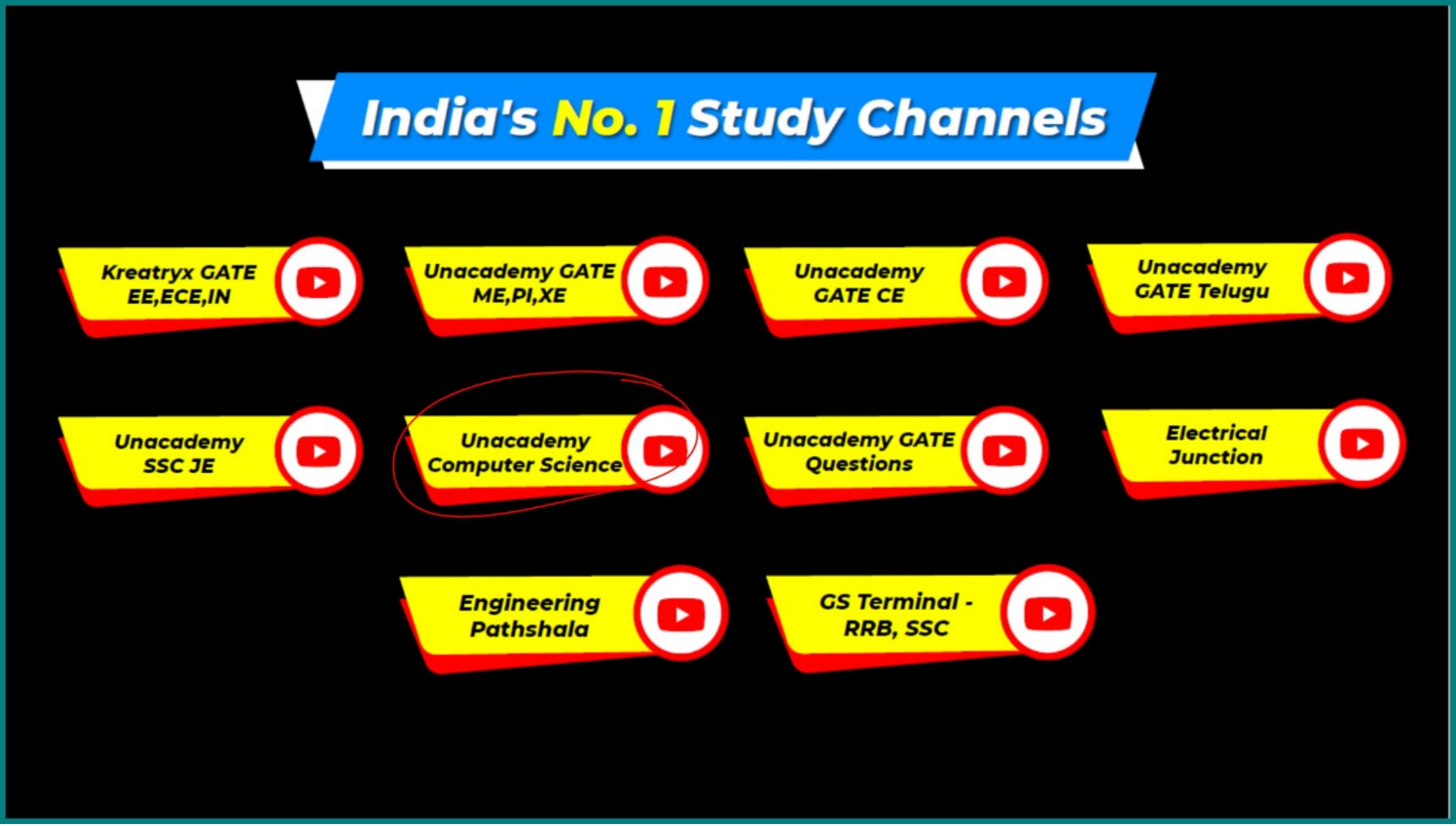
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