

# MANZIL

For JEE Aspirants



Lecture No.1

Semiconductors

*Legend*



By- Rajwant Singh

# TOPICS TO BE COVERED

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- 1.** Complete Semiconductors
- 2.** Questions
- 3.**
- 4.**

How to take Max benefit from this batch.

1. Only write Important points & formula (either new )  
(PCM)  
or  
Important
2. Solve Questions
3. After class Work.



## What to do after the lecture



- Solve your Left over questions and report the answer
- After half an Hour download the PDF from PW APP from Manzil Legend Batch
- Revise the theory and make formula and important point sheet in 1 hour
- Solve the DPP and Remaining PYQ

“Topic”: Logic Gates ✓

Zener Diode ✓

Diode Biasing ✓

Application of Diodes ✓

Transistor



# ENERGY BAND THEORY



Isolated atom  $\rightarrow$  fix Energy shells.

atoms  $\rightarrow$  Lattice

Valence shell  $\rightarrow$  Interact

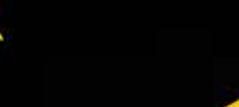


Energy Change



all Valence  $e^-$  bands of Energies permissible energy levels in isolated Si atom

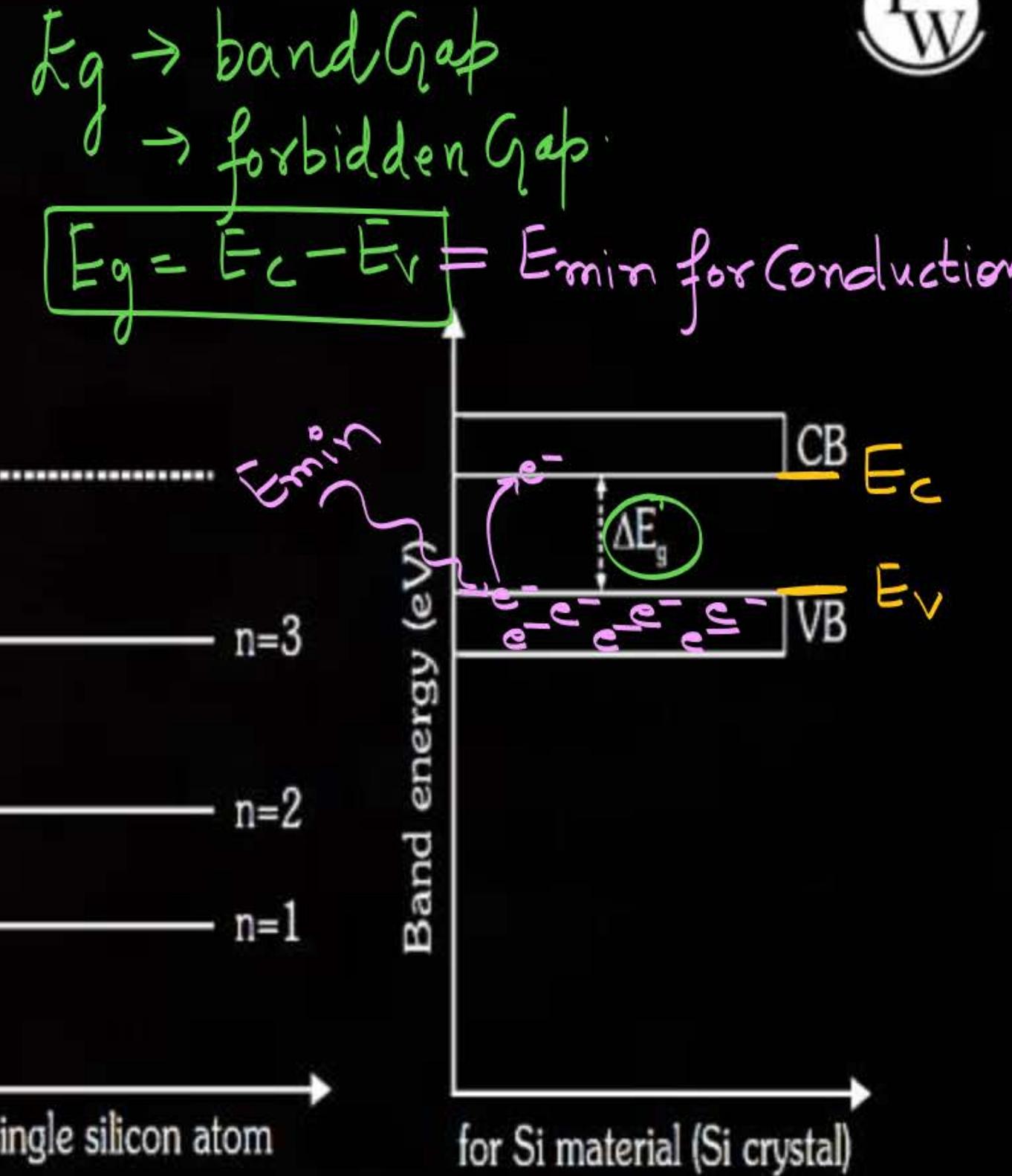
$e^-$



V.B

CB

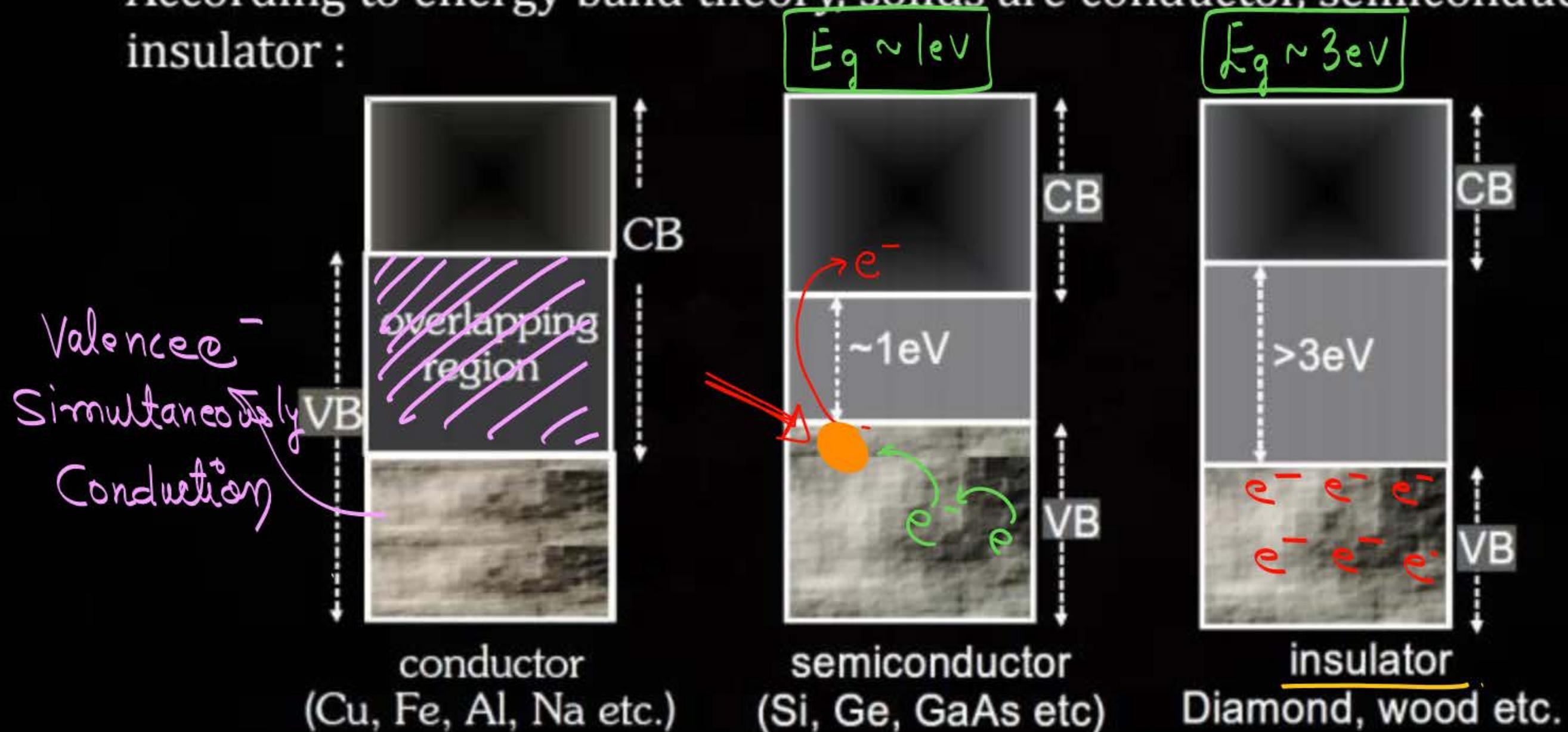
permissible energy levels in isolated Si atom





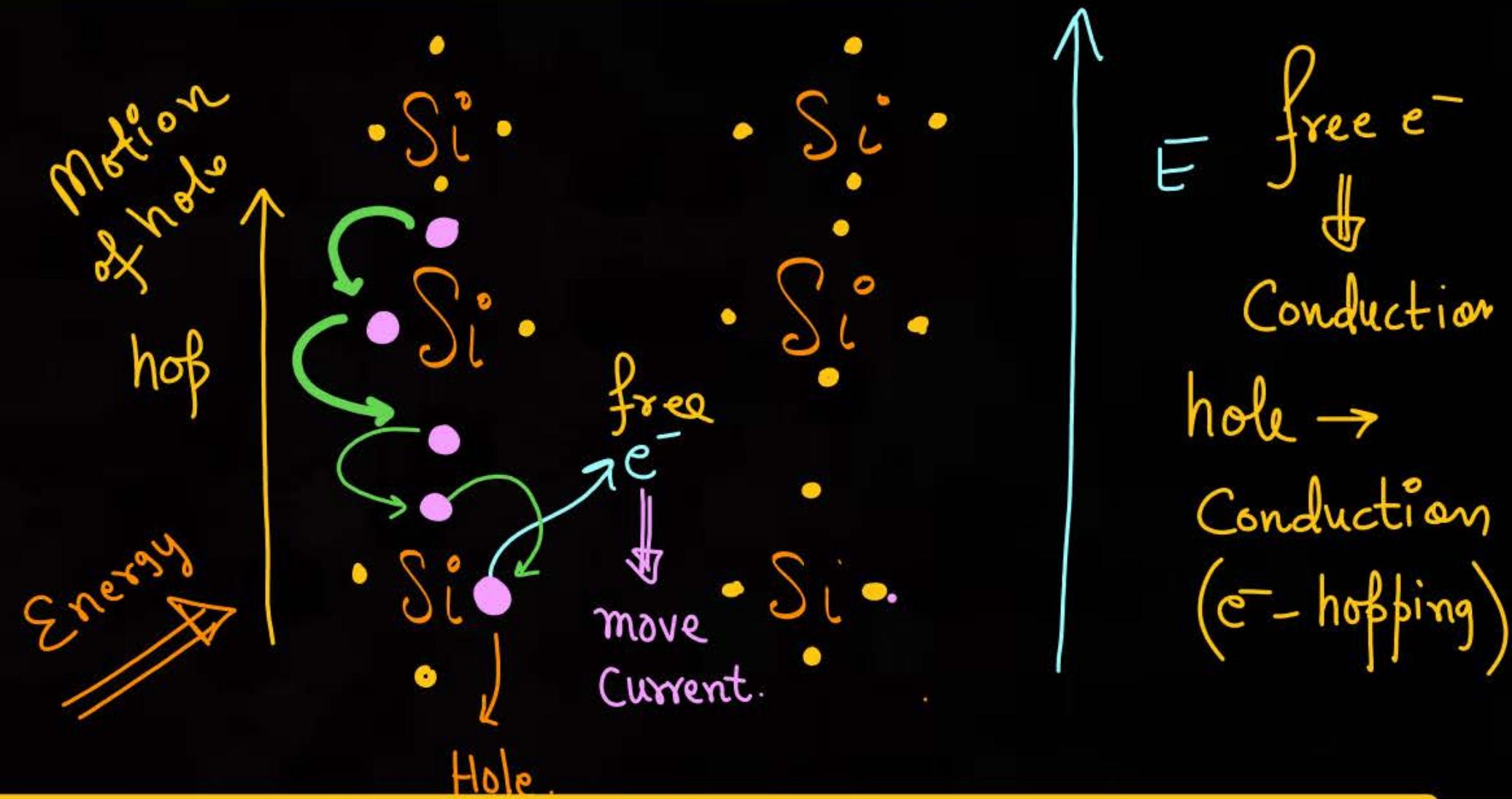
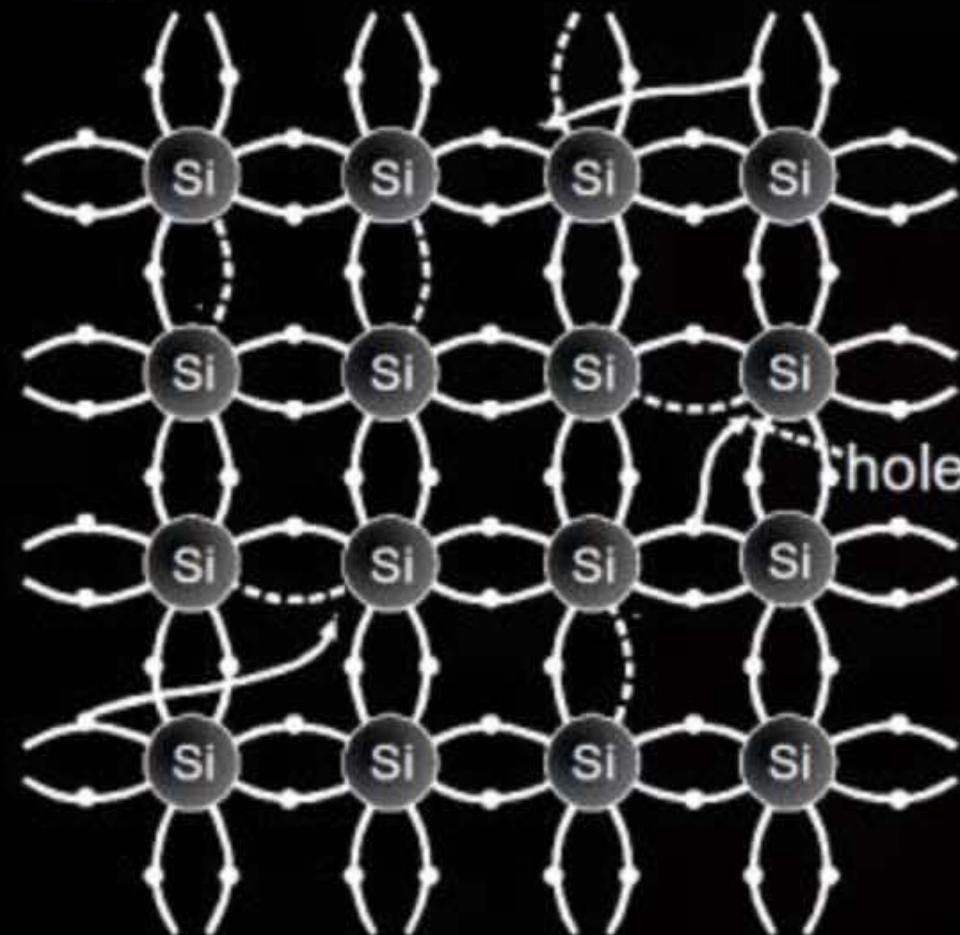
# CLASSIFICATION OF SOLIDS ACCORDING TO ENERGY BAND THEORY

According to energy band theory, solids are conductor, semiconductor and insulator:





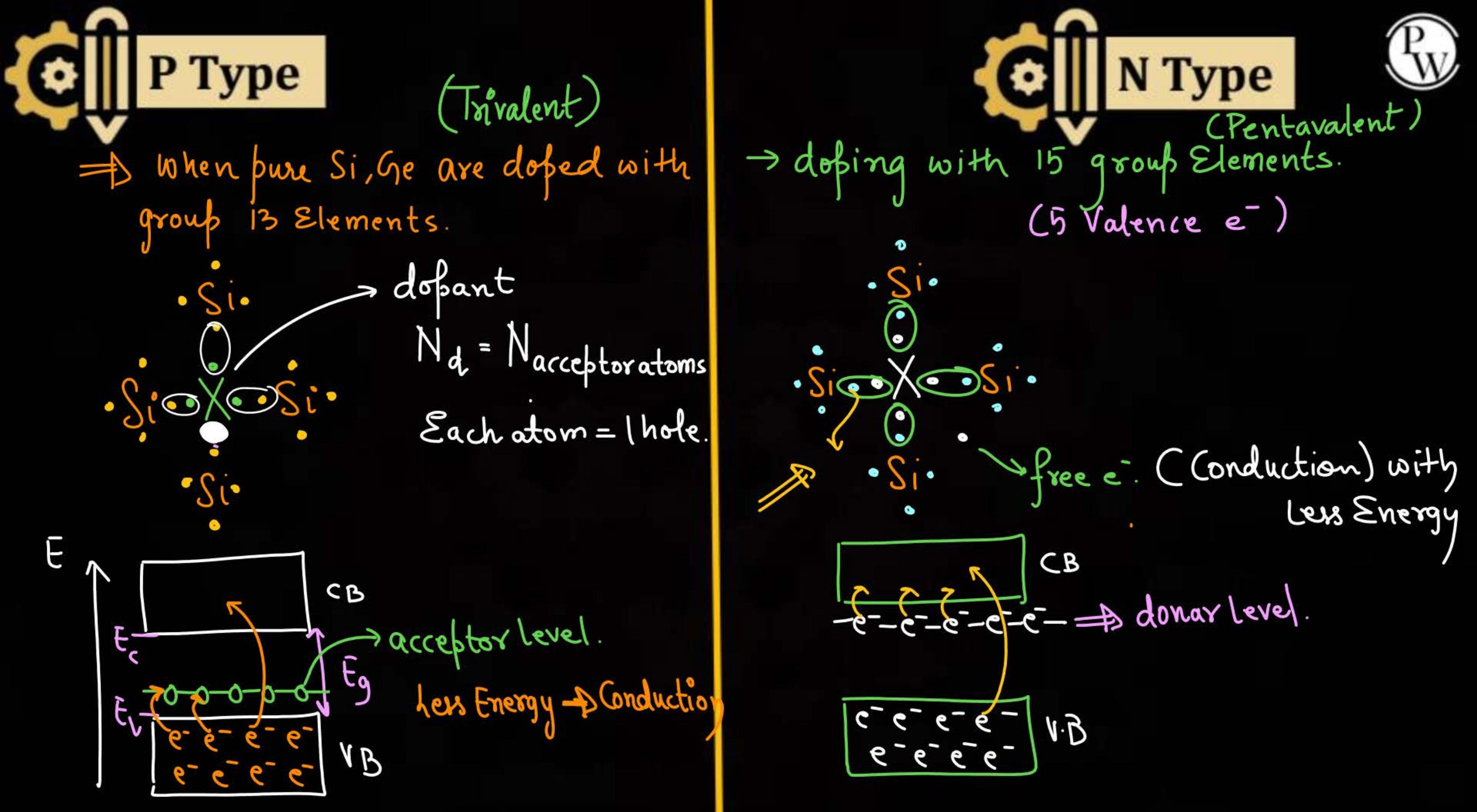
# CONCEPT OF "HOLES" IN SEMICONDUCTORS



- ❖ It is missing electron in valence band.
- ❖ Its effective mass is more than electron.

- ❖ It acts as positive charge carrier.
- ❖ Its mobility is less than electron.

*Hole acts as virtual charge, although there is no physical charge on it.*





# EFFECT OF IMPURITY IN SEMICONDUCTOR



Doping is a method of addition of "desirable" impurity atoms to pure semiconductor to increase their conductivity. CLASSIFICATION OF SEMICONDUCTOR

## CLASSIFICATION OF SEMICONDUCTOR

Intrinsic semiconductor	Extrinsic semiconductor (Doped semiconductor)	
	N-type	P-type
(pure form of Ge, Si) $n_e = n_h = n_i$ $n_e = n_h = n_i^0$	pentavalent impurity (P, As, Sb) donor impurity ( $N_D$ ) $n_e >> n_h$ $n_e >> n_i^0$	trivalent impurity (B, In, Al) acceptor impurity ( $N_A$ ) $n_h >> n_e$ $n_h >> n_i^0$

Intrinsic Semiconductor	N-type (Pentavalent impurity)	P-type(Trivalent impurity)
1.		
2.		
3. Current is due to both electrons and holes	Mainly due to electrons $I_T \approx I_e$	Mainly due to holes $I_T \approx I_h$
4. $n_e = n_h = n_i$	$n_e >> n_h (N_D \approx n_e)$	$n_h >> n_e (N_A \approx n_h)$
5. $I = I_e + I_h$	$I \approx I_e$	$I \approx I_h$
6. Entirely neutral	Entirely neutral	Entirely neutral
7. Quantity of electrons and holes are equal	Majority - Electrons Minority - Holes	Majority - Holes Minority - Electrons



## MASS ACTION LAW

$$n_e n_h = n_i^2$$

after doping  $n_i^2 = N_h N_e$

$n_i^2$  = Intrinsic Carrier density

**Q.**

Statement I : By doping silicon semiconductor with pentavalent material, the electrons density increases. (*True*) *15<sup>th</sup> group*

Statement II : The n-type semiconductor has net negative charge. (*False*)

In the light of the above statements, choose the most appropriate answer from the options given below :

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**A**

Statement - I is true but Statement - II is false. *Ans*

**B**

Statement - I is false but Statement - II is true.

**C**

Both Statement I and Statement II are true.

**D**

Both Statement I and Statement II are false.



# Conduction in Semiconductor



Semi  $\rightarrow$  ( $e^-$  + holes)

$$I = neA\upsilon_d$$

$$I_T = I_e + I_h$$

$$= n_e e A \upsilon_e + n_h e A \upsilon_h$$

$$I = (n_e e A \mu_e + n_h e A \mu_h) E$$

$$\frac{I}{A} = J = (n_e \mu_e + n_h \mu_h) E$$

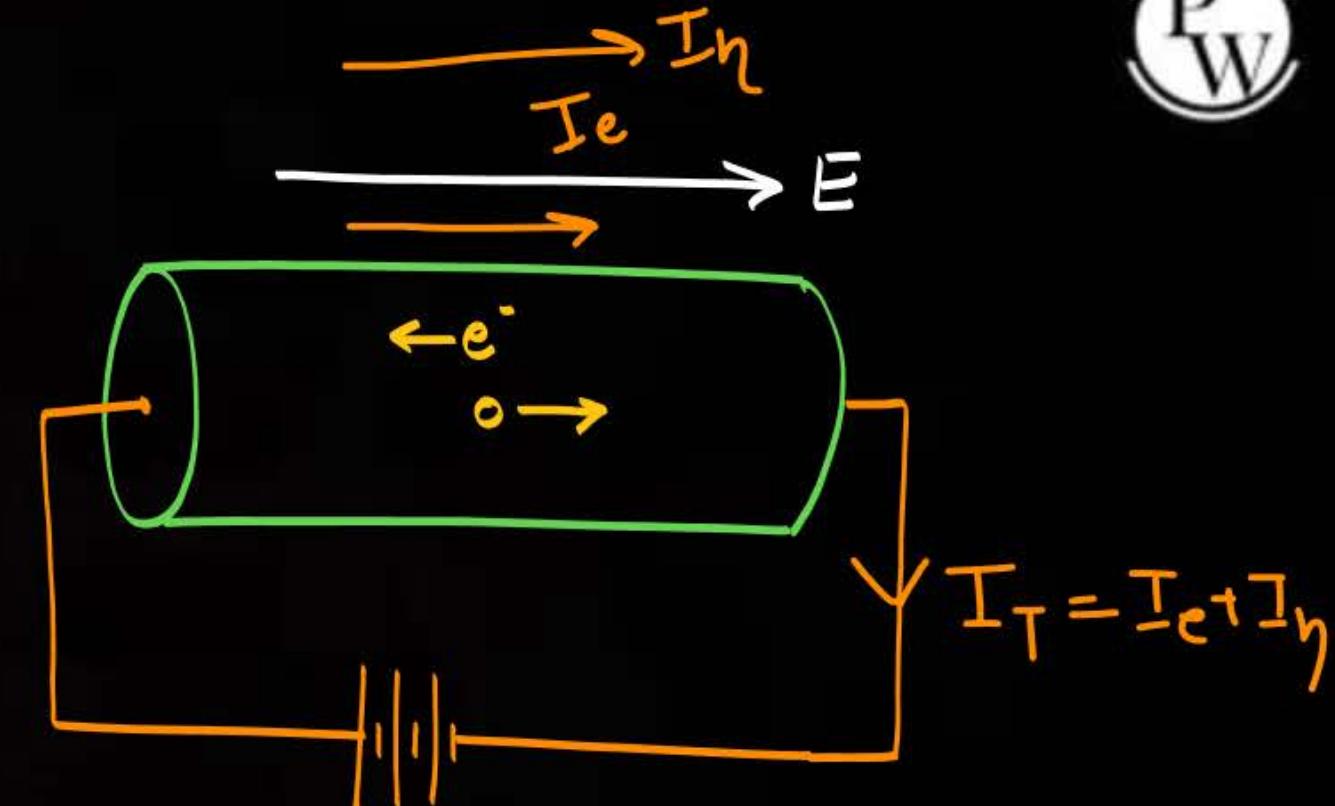
$$\mu = \frac{\upsilon_d}{E}$$

$$\upsilon_d = \mu E$$

$$\bar{J} = \sigma E$$

$$\sigma = \text{Const} = n_e \mu_e + n_h \mu_h$$

$$\sigma = \frac{1}{\rho}$$



## Intrinsic semiconductor

$$n_e = n_h$$

$$J = ne [v_e + v_h]$$

$$\sigma = \frac{1}{\rho} = en [\mu_e + \mu_h]$$

## P - type

$$n_h \gg n_e$$

$$J \approx e n_h v_h$$

$$\sigma = \frac{1}{\rho} \approx e n_h \mu_h$$

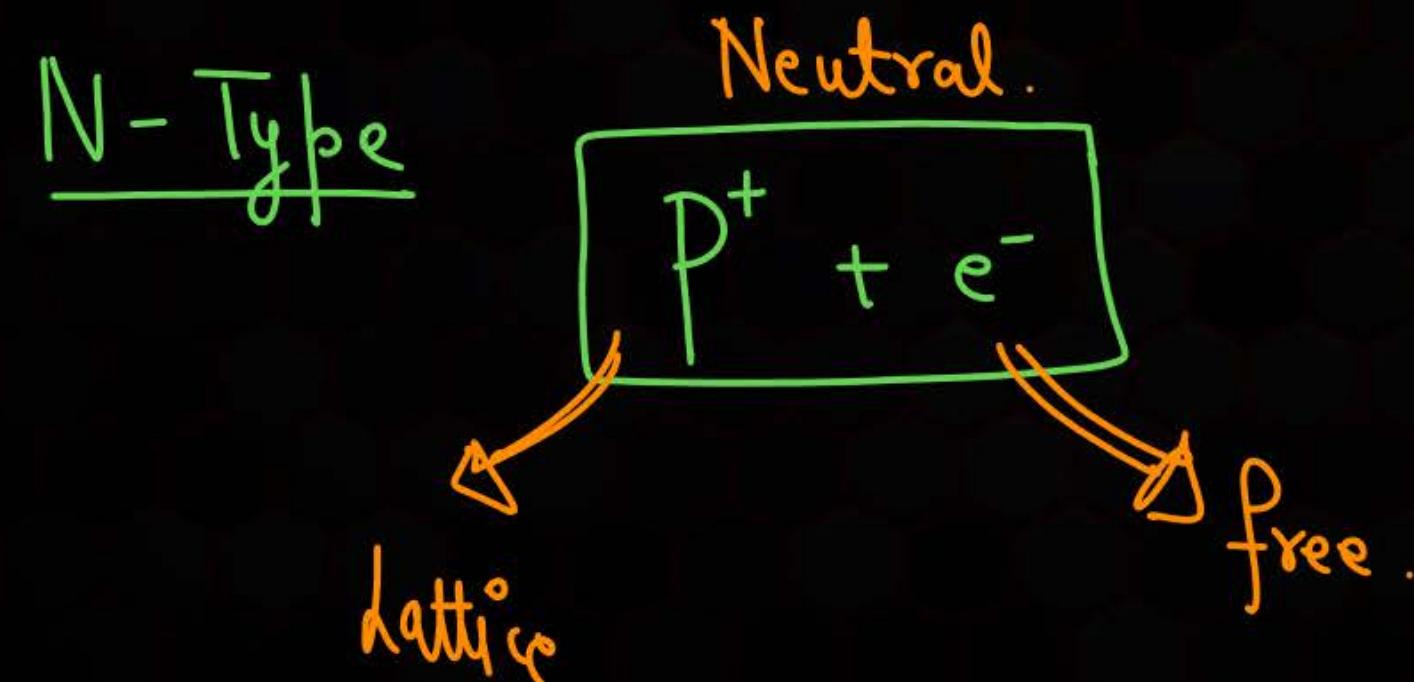
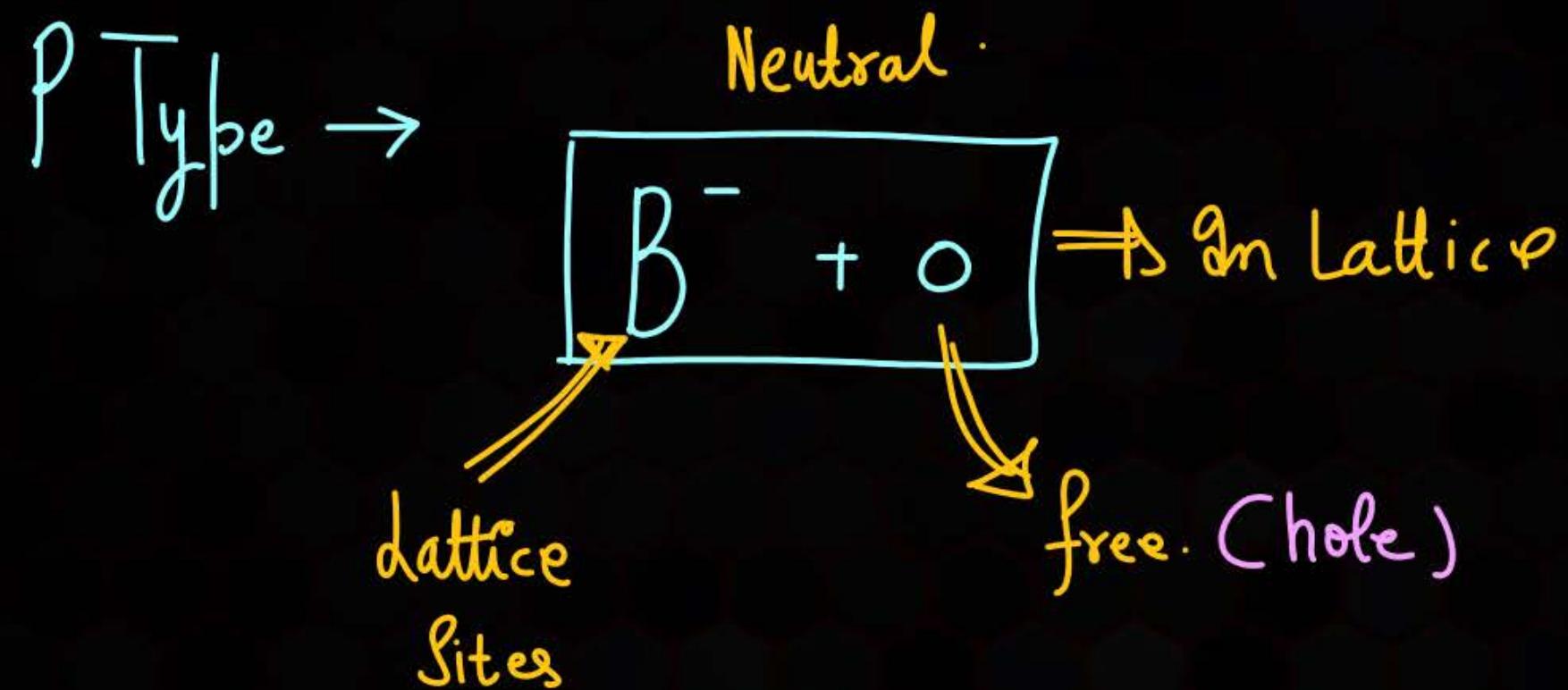
## N - type

$$n_e \gg n_h$$

$$J \approx e n_e v_e$$

$$\sigma = \frac{1}{\rho} \approx e n_e \mu_e$$

Intrinsic semiconductor	P - type	N - type
$n_e = n_h$	$n_h \gg n_e$	$n_e \gg n_h$
$J = ne [v_e + v_h]$	$J \approx e n_h v_h$	$J \approx e n_e v_e$
$\sigma = \frac{1}{\rho} = en [\mu_e + \mu_h]$	$\sigma = \frac{1}{\rho} \approx e n_h \mu_h$	$\sigma = \frac{1}{\rho} \approx e n_e \mu_e$

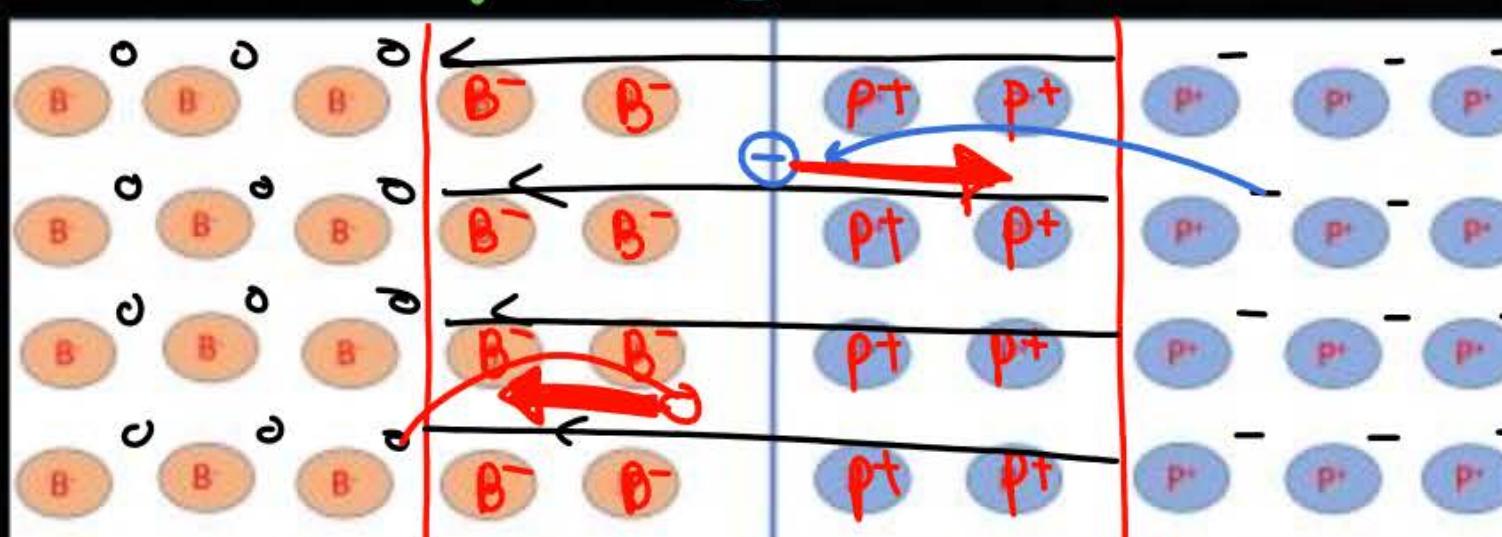
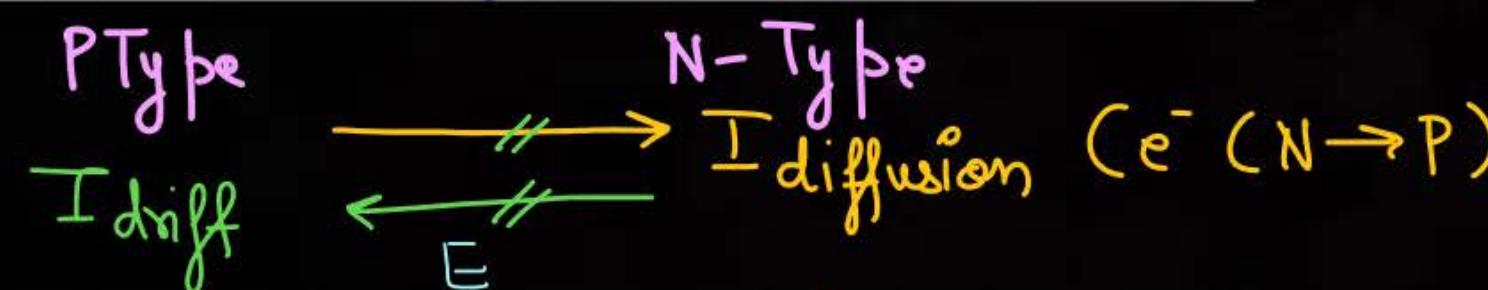
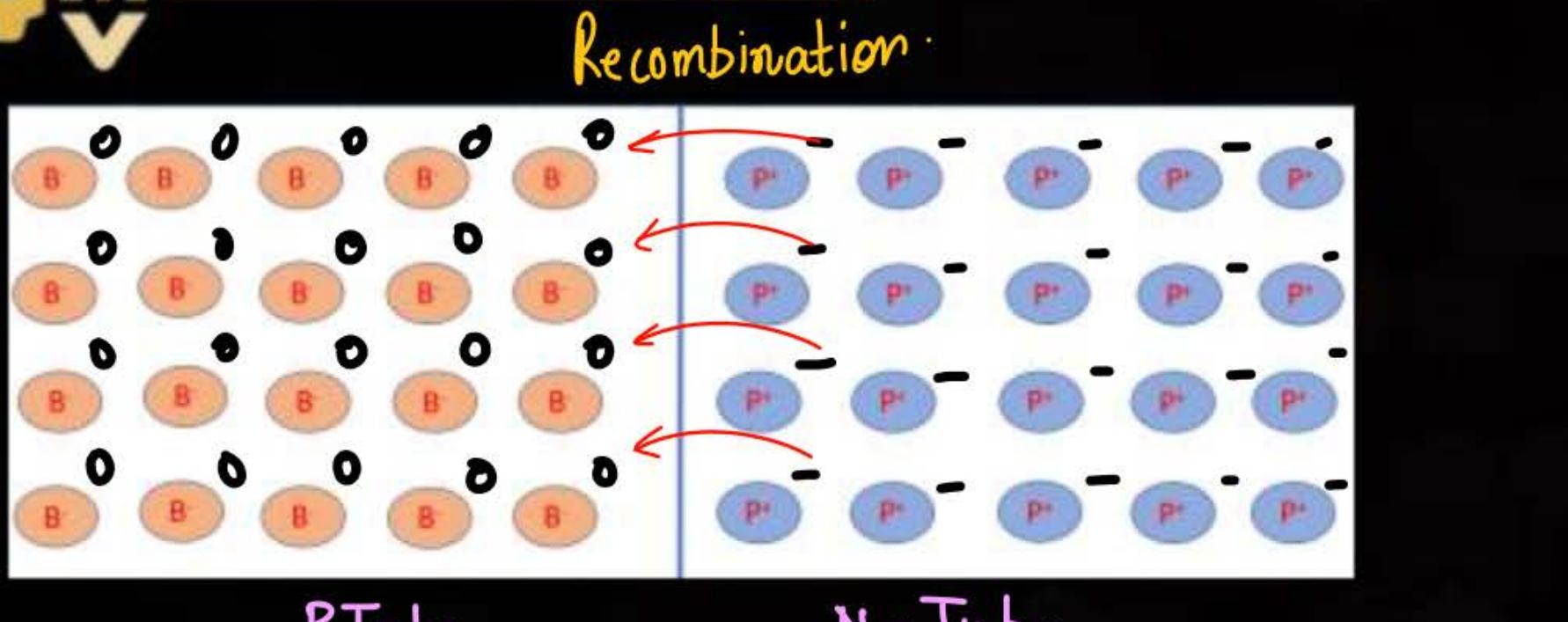




# P-N JUNCTION

P  
W

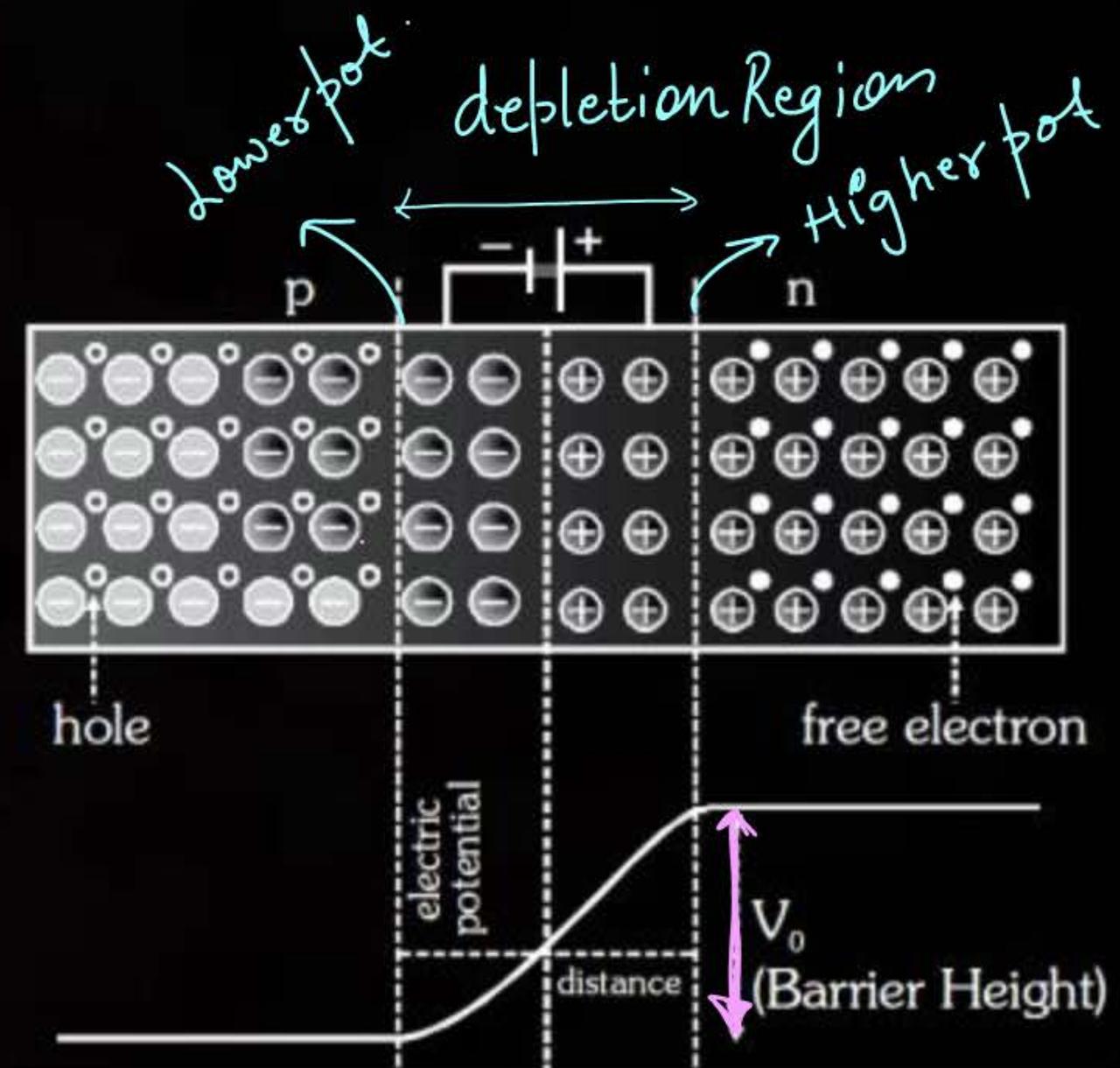
1.



$P\text{-Type}$

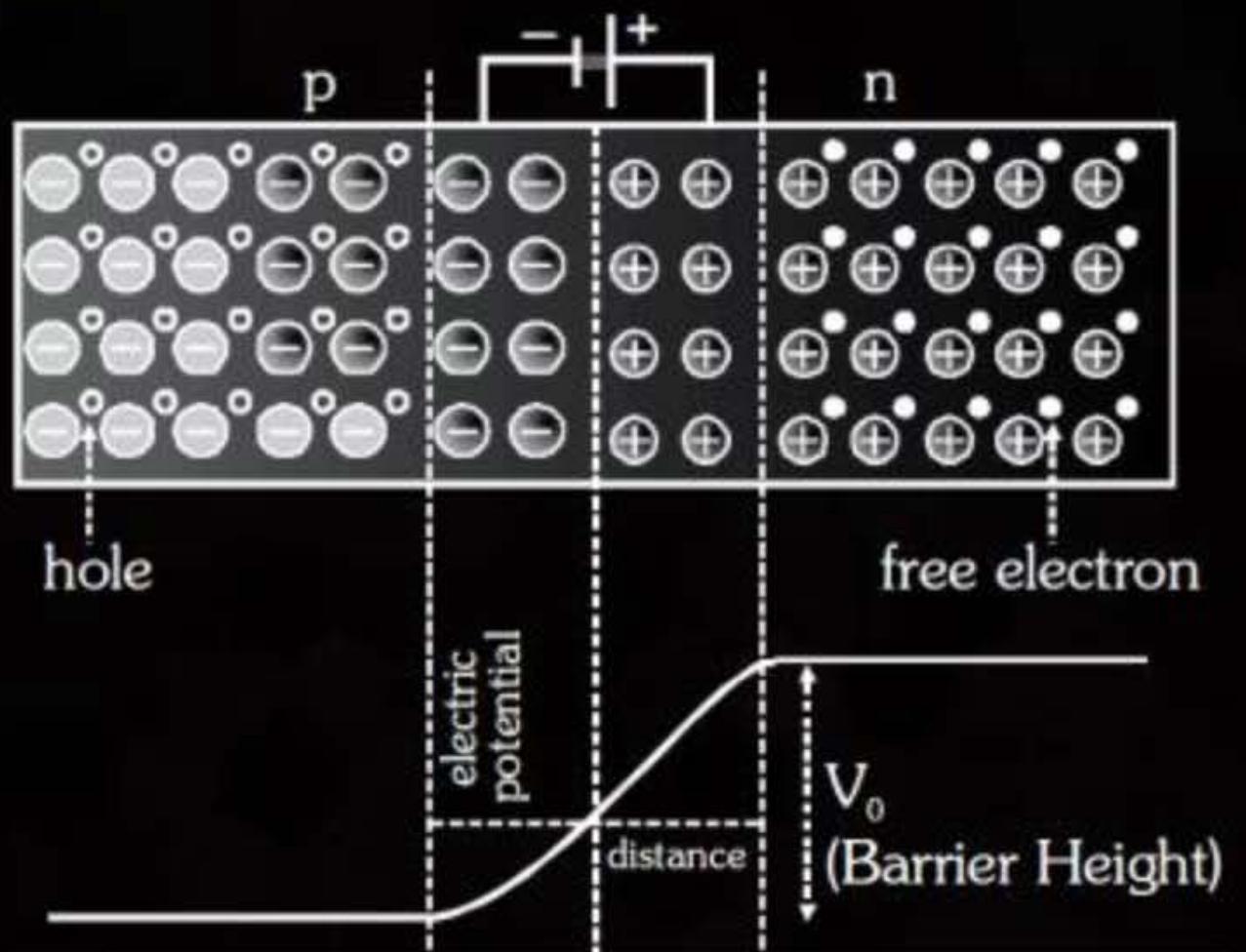
$N\text{-Type}$

$$\frac{I}{I_T} = 0$$





# P-N JUNCTION



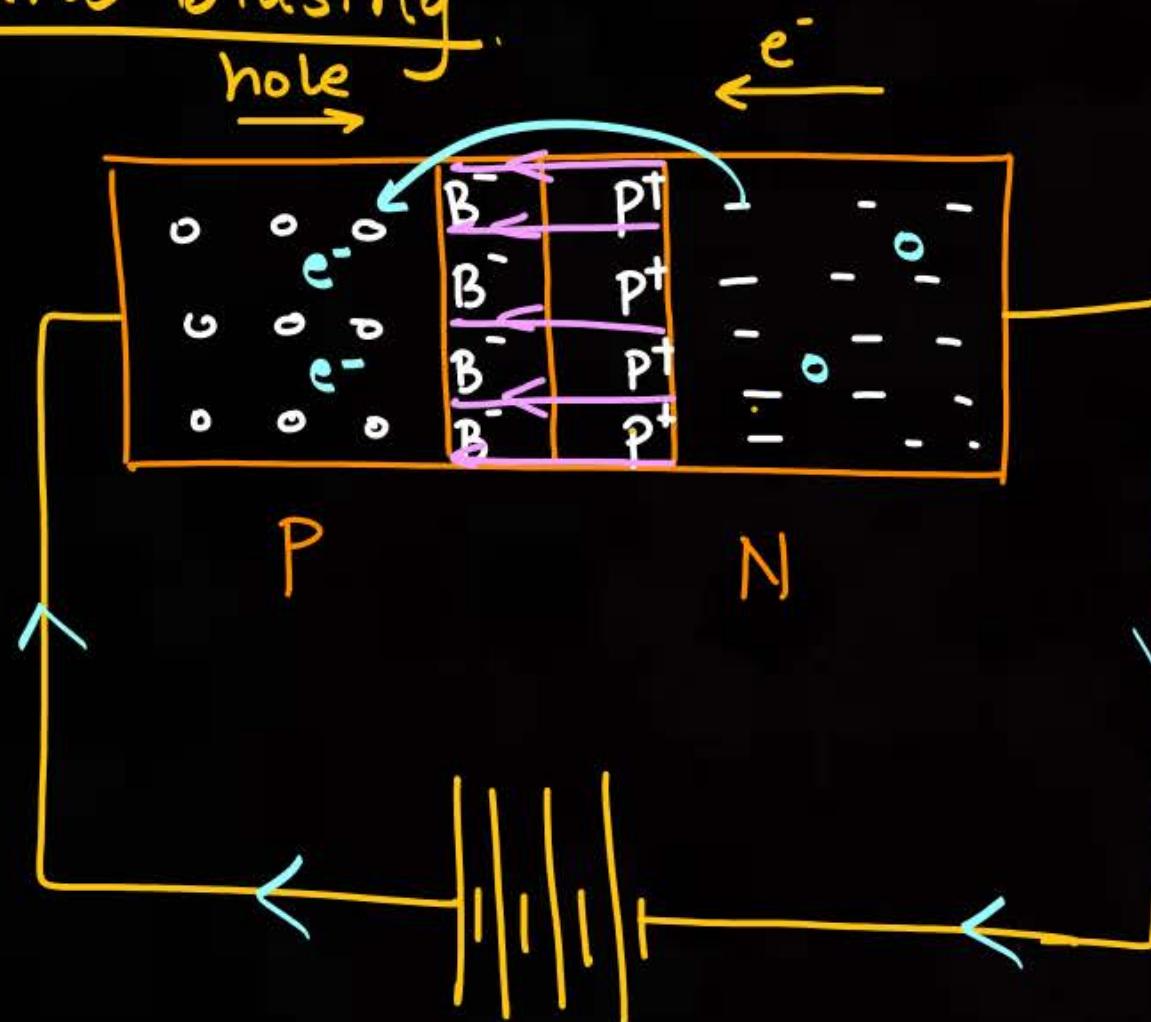


# Biasing

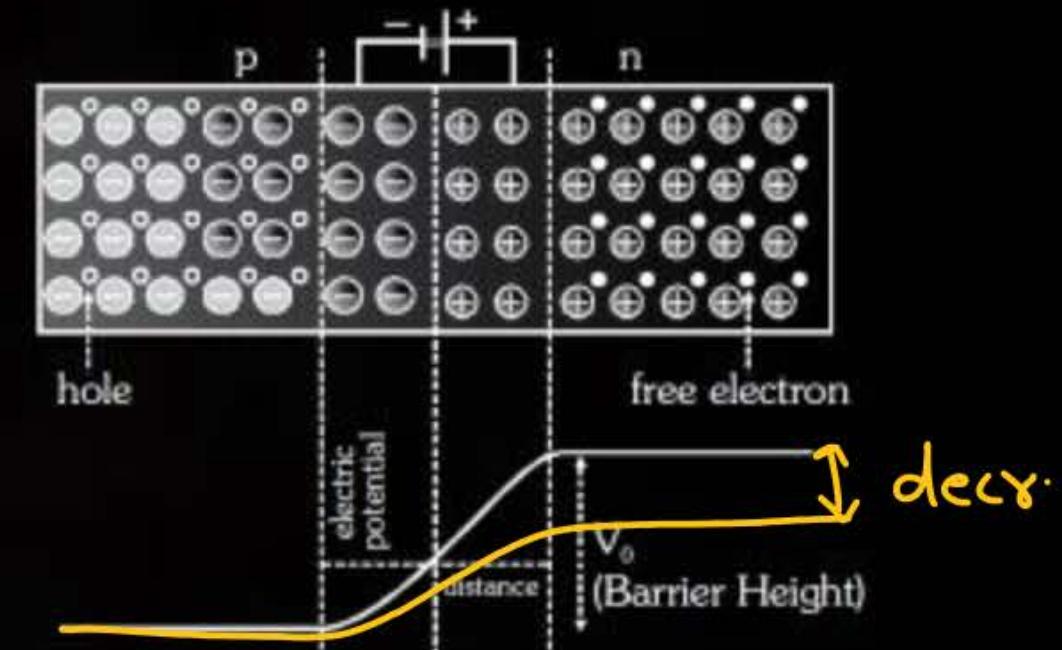
→ Application of  $V_{ext}$  to PN Junction



## a) Forward Biasing



⇒ Majority Carrier Jump depletion  
⇒ Current → forward current (mA)

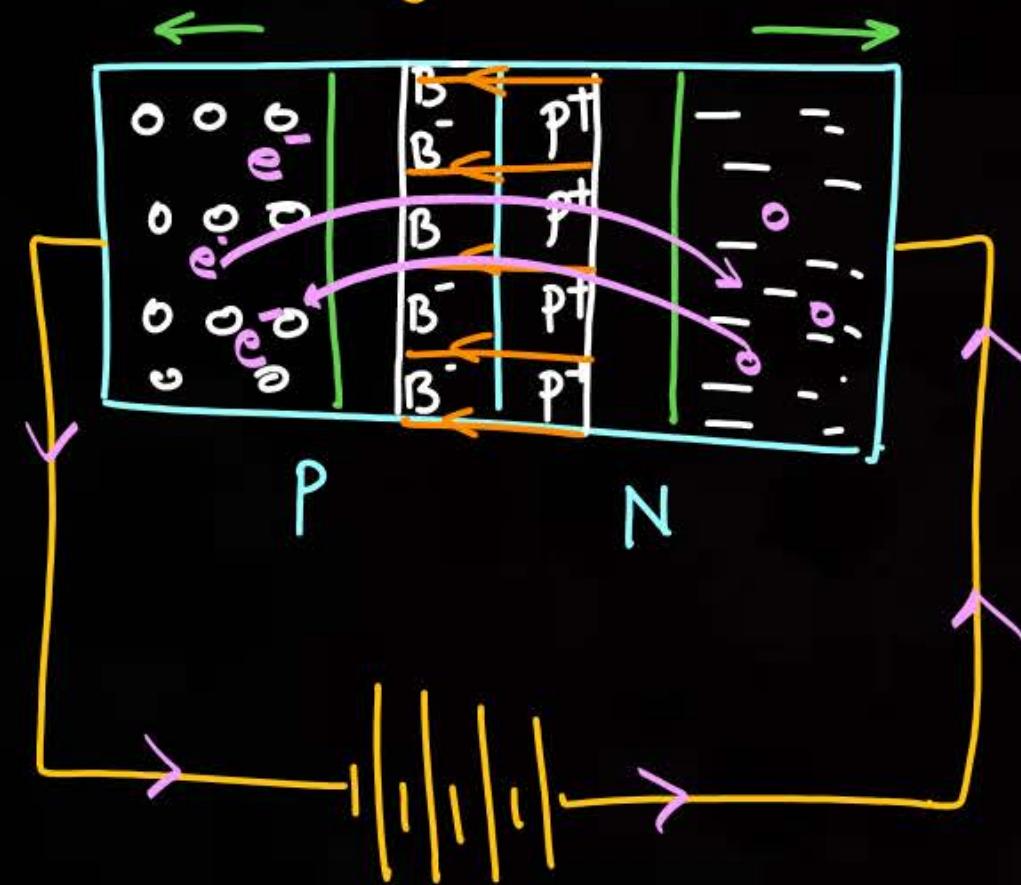


- \* depletion layer decr.
- \* F.B.  $P \rightarrow$  higher Pot.  
 $N \rightarrow$  lower Pot.
- \* Pot barrier  $\rightarrow$  dec.

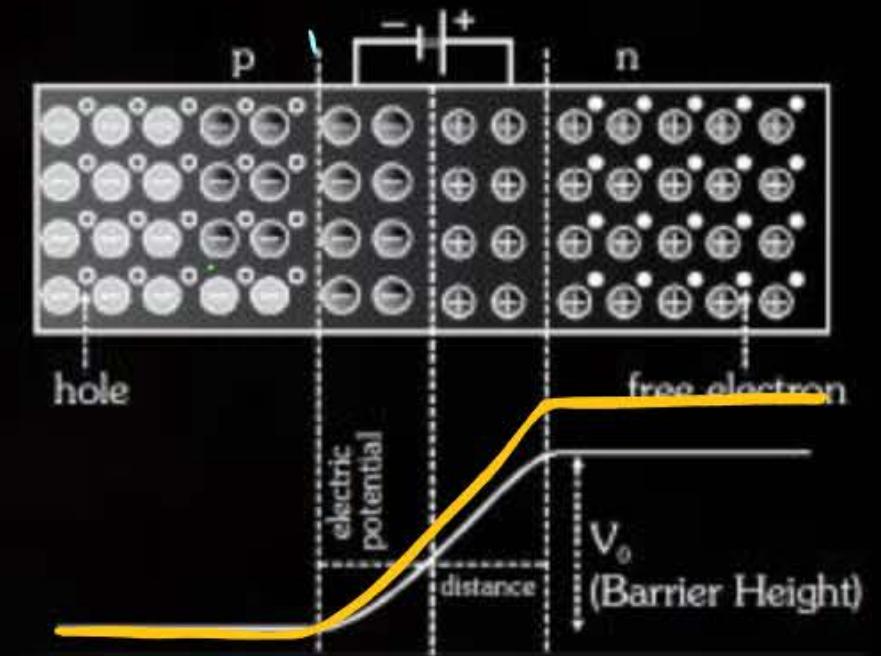


# Biasing

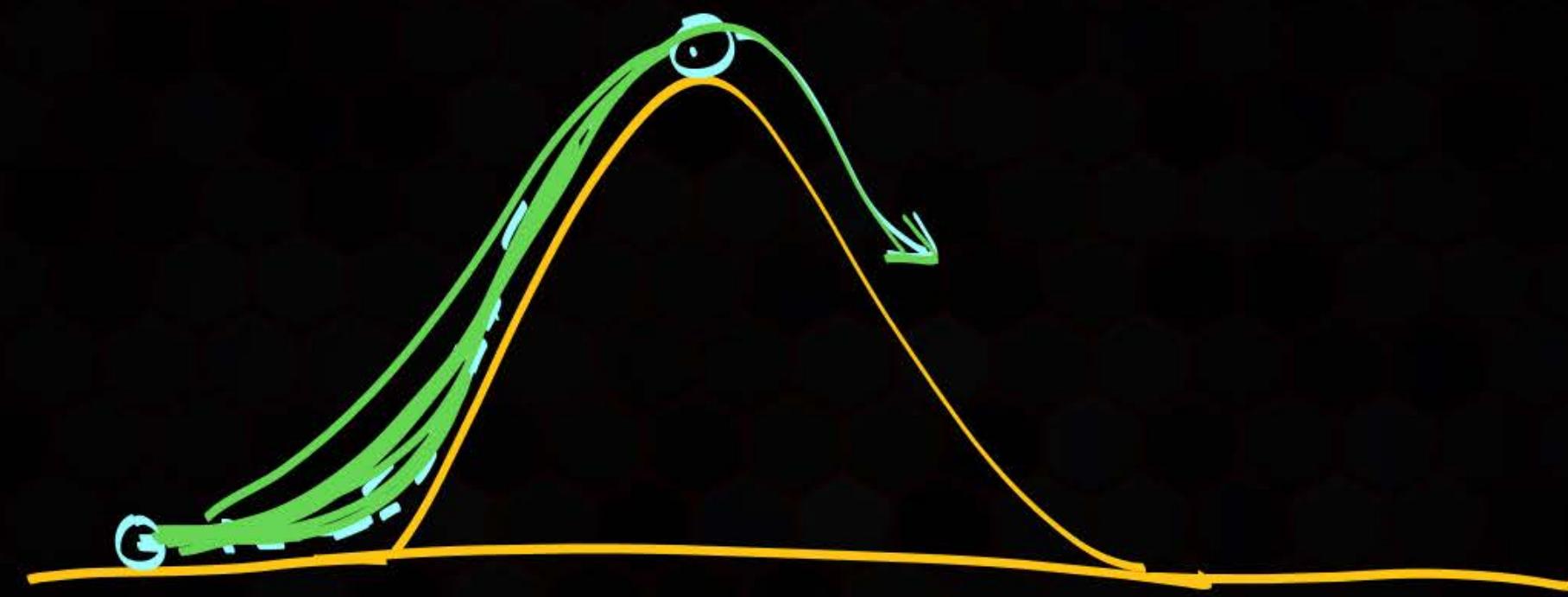
b) Reverse biasing.



→ Minority Carrier Jump.  
→ Reverse Current  $\rightarrow (nA, uA)$



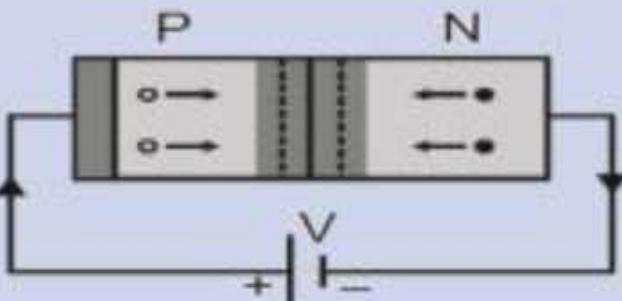
- ⊗ P  $\rightarrow$  lower  
N  $\rightarrow$  Higher.
- ⊗ depletion layer  $\uparrow$
- ⊗ Pot barrier  $\uparrow$



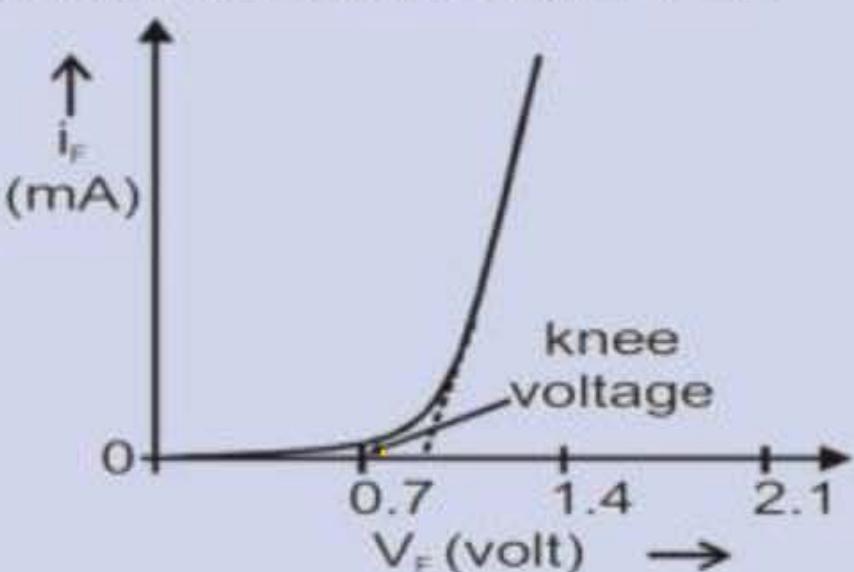
**Forward Bias**

P → positive  
N → negative

Higher  
Lower

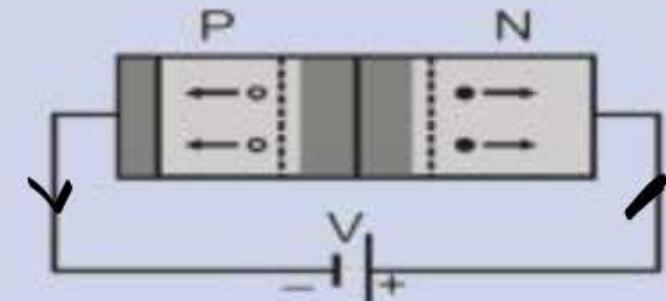


1. Potential Barrier reduces.
2. Width of depletion layer decreases.
3. P-N Junction provides very small resistance.
- 4 Forward current flow in circuit.
5. Order of forward current is milli ampere.
6. Mainly majority current flows.
7. Forward characteristic curve

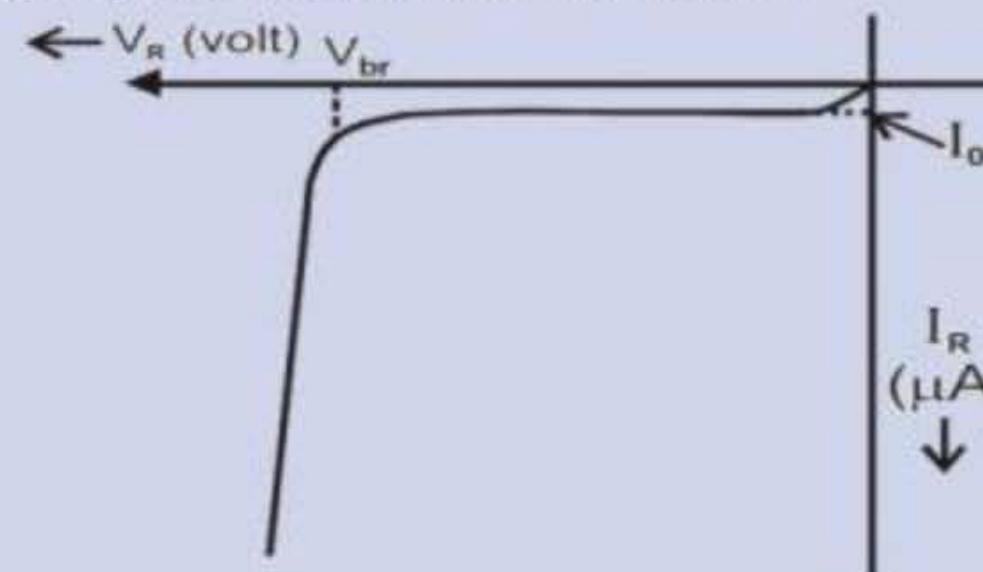
**Reverse Bias**

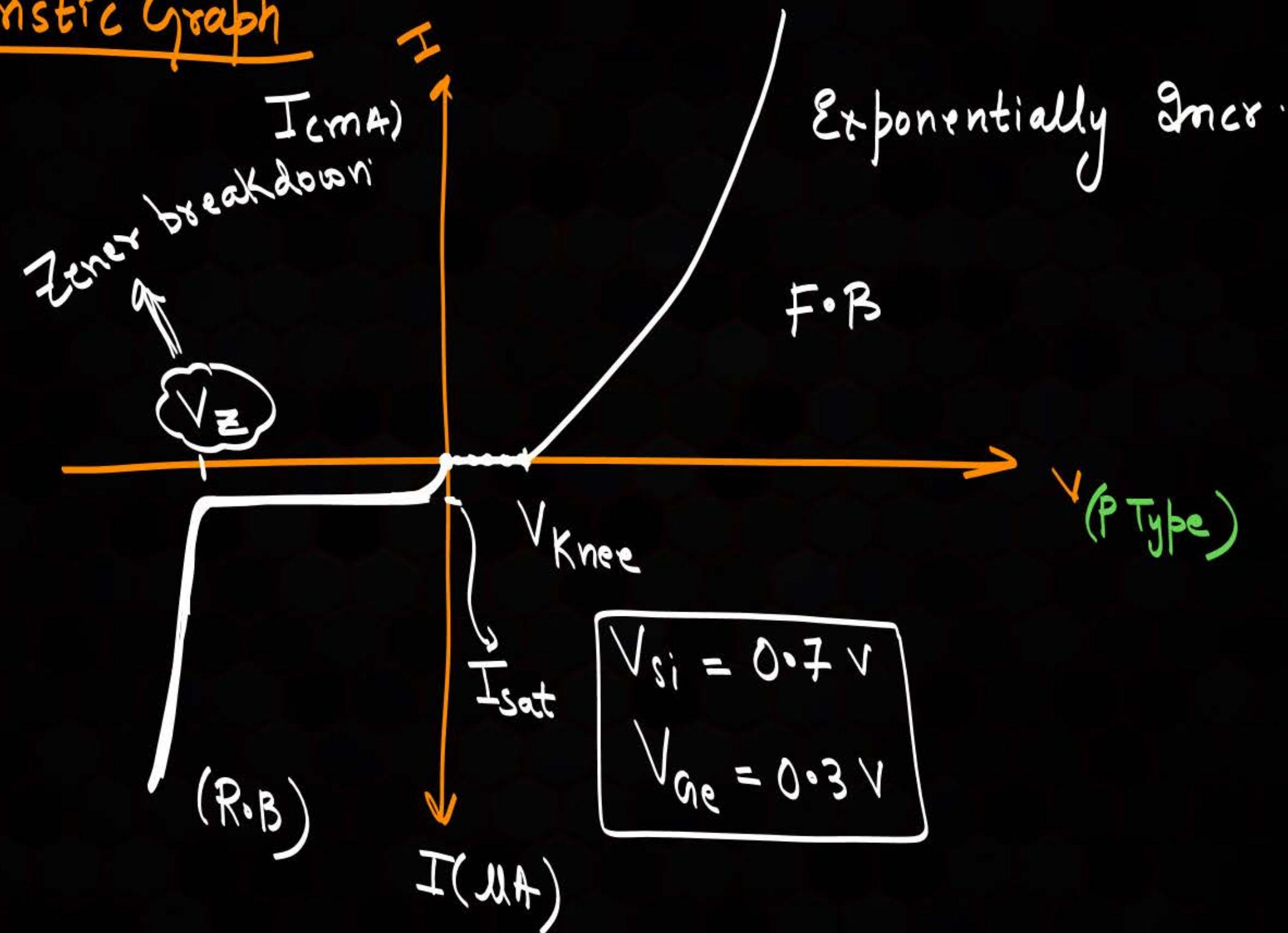
P → negative  
N → positive

Lower  
Higher

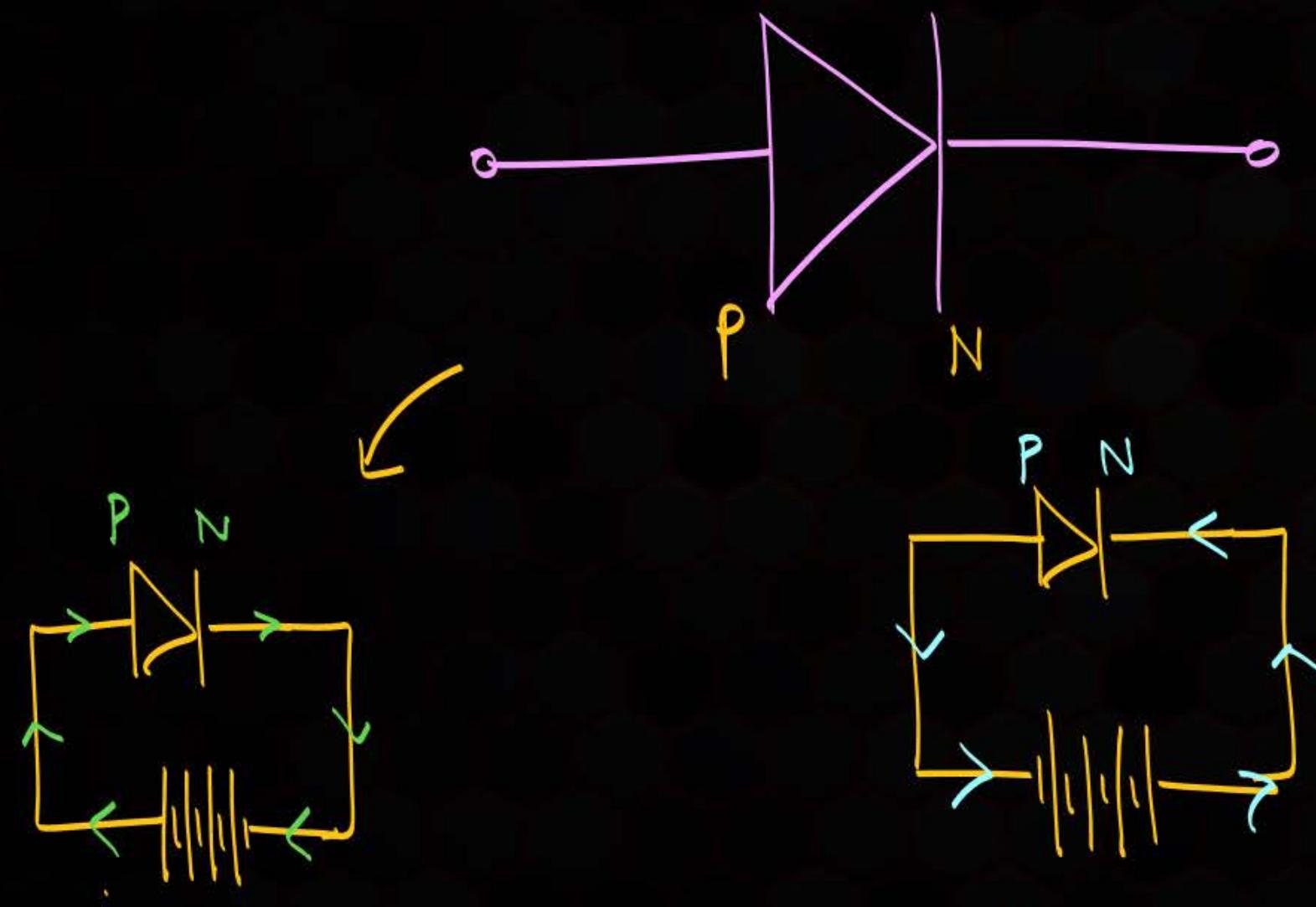


1. Potential Barrier increases.
2. Width of depletion layer increases.
3. P-N Junction provides high resistance.
- 4 Reverse current flow in circuit.
5. Order of current is micro ampere (Ge) or Nano ampere (Si).
6. Mainly minority current flows.
7. Reverse characteristic curve



Characteristic Graph

## Representation of PM Junction diode

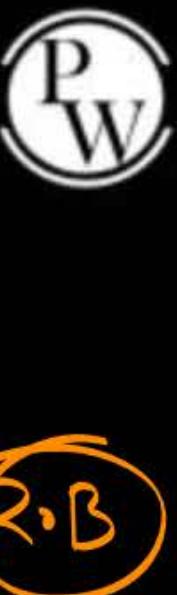


Current allowed  
(mA)

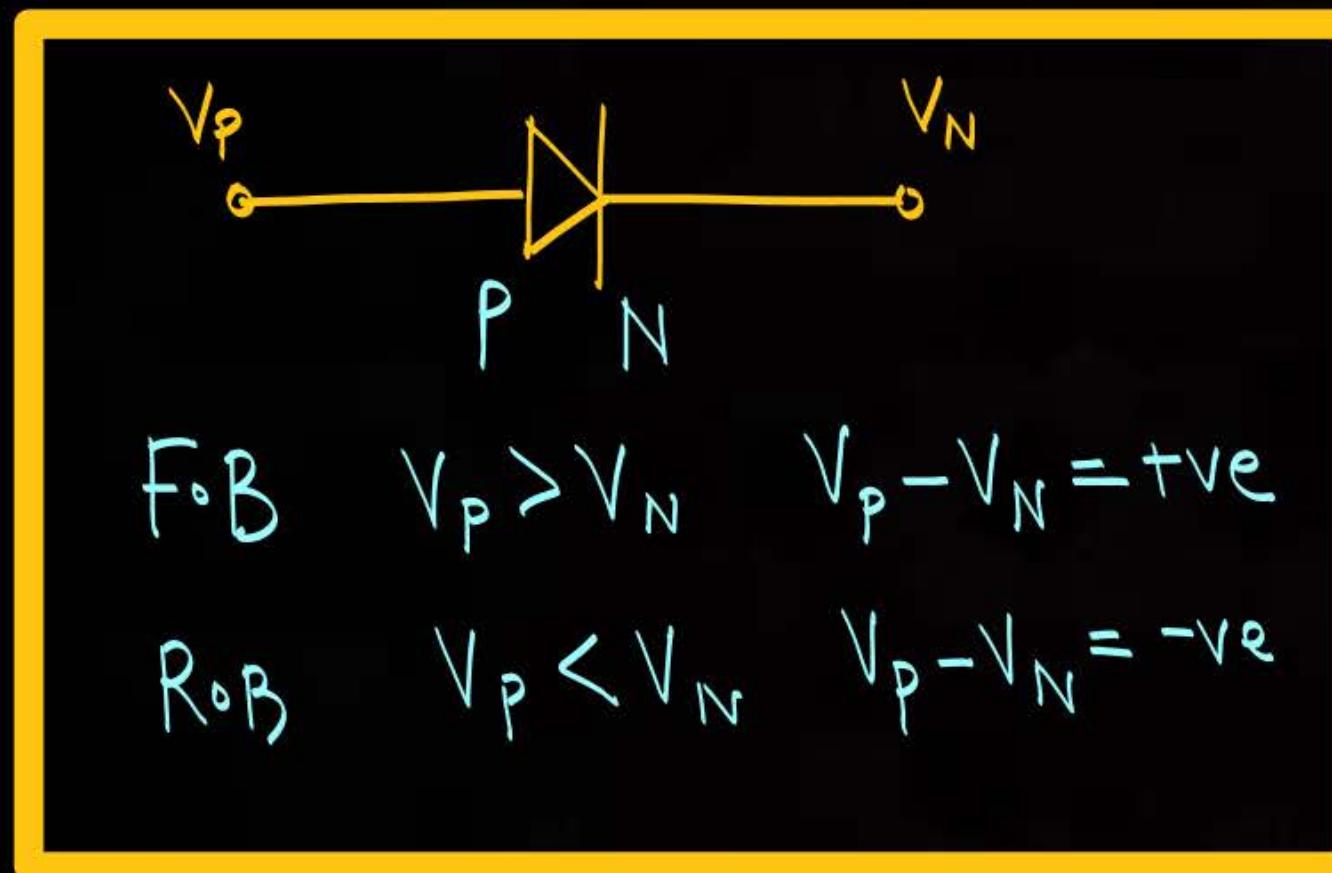
Reverse. (mA)



# PN Junction diode in electrical circuit



a) Checking of Biasing:



- a)  $\mathcal{E}_x$        $5V$        $10V$        $\Rightarrow 5 - 10 = -5$   $\textcircled{R \cdot B}$
- b)  $0V$        $-2V$        $\Rightarrow 0 - (-2) = 2$   $\textcircled{F \cdot B}$
- c)  $6V$        $3V$        $\Rightarrow 6 - 3 = 3$   $\textcircled{F \cdot B}$
- d)  $-2V$        $-5V$        $\Rightarrow -2 - (-5) = 3$   $\textcircled{F \cdot B}$

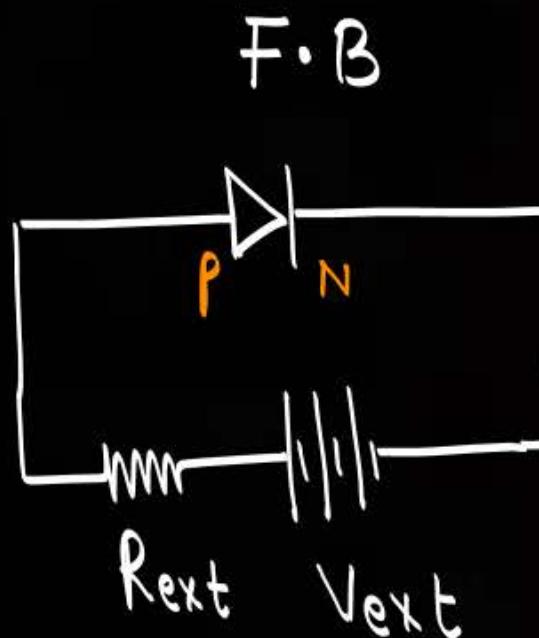


# PN Junction diode in electrical circuit



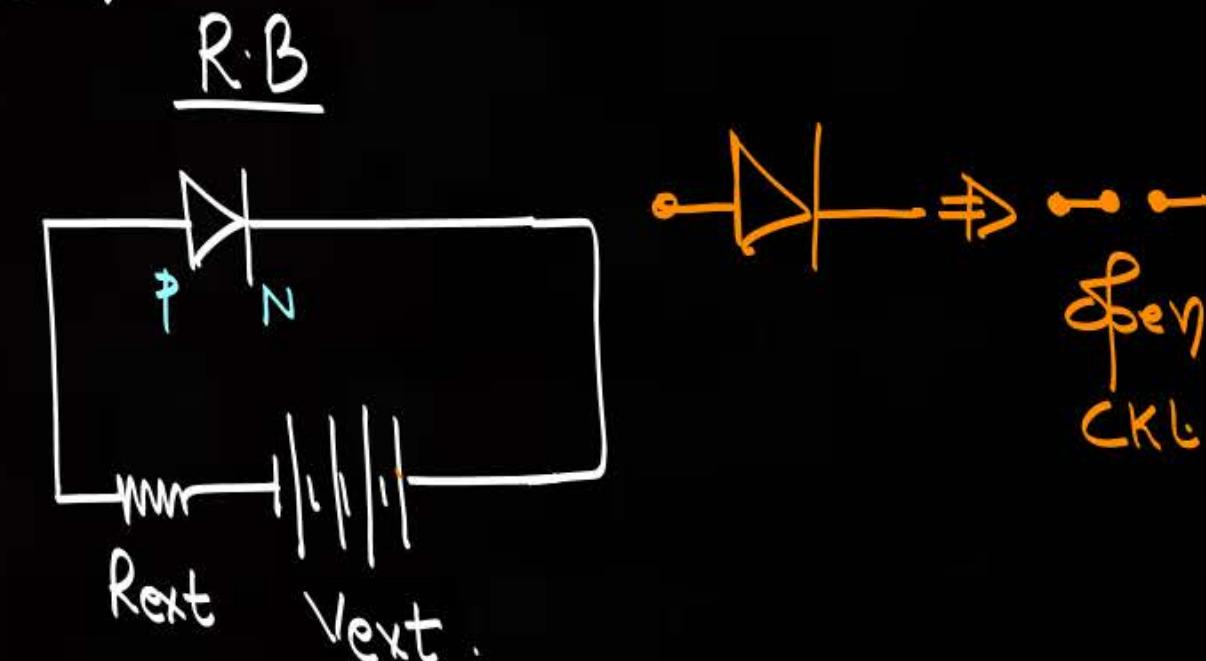
behaviour in CKt.

- a) Ideal Diode
- Resistance = 0 (F·B) (Short CKt)
  - Resistance =  $\infty$  (R·B) (open CKt)
  - $V_{knee} = 0$ .



F·B

$$\rightarrow \text{Diode} = \text{---}$$



$I = \frac{V_{ext}}{R_{ext}}$

$R_{ext}$   $V_{ext}$

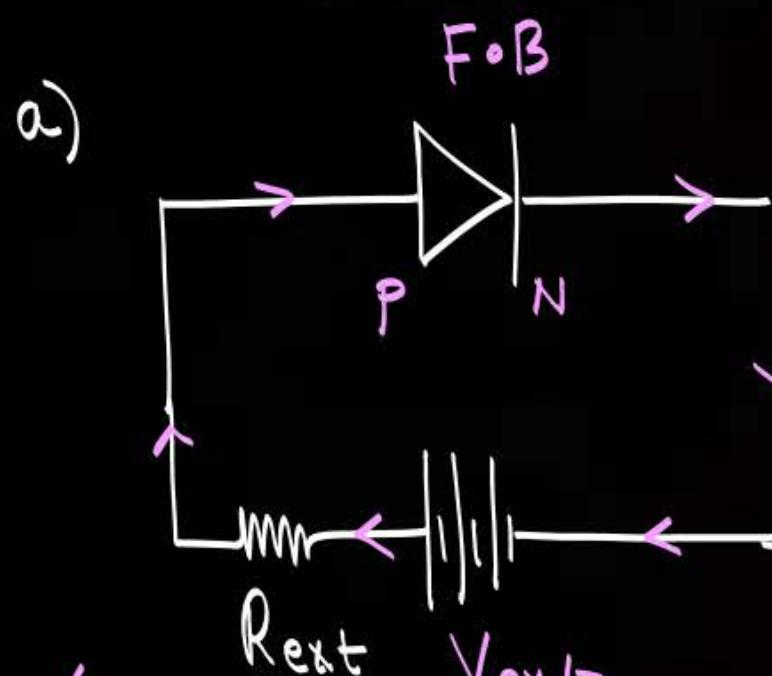
$R_{ext}$   $V_{ext}$



# PN Junction diode in electrical circuit



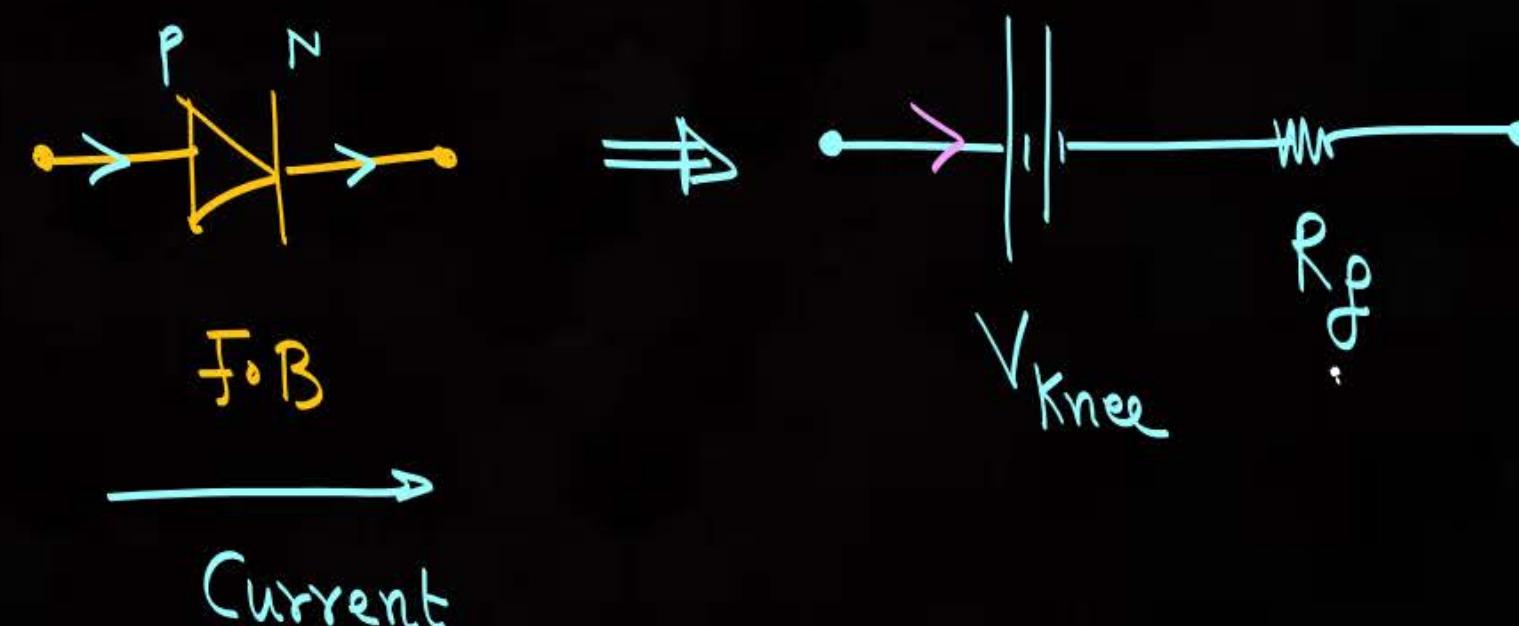
Real diodes



$$\begin{aligned} \text{Si} &\Rightarrow V_{\text{knee}} = 0.7, R_f = \checkmark \\ \text{Ge} &\Rightarrow V_{\text{knee}} = 0.3, R_R = \checkmark \end{aligned}$$

$V_{\text{knee}}$  is Given in Ques.  
Resistance  $\rightarrow f \checkmark$   
 $\rightarrow R \checkmark$

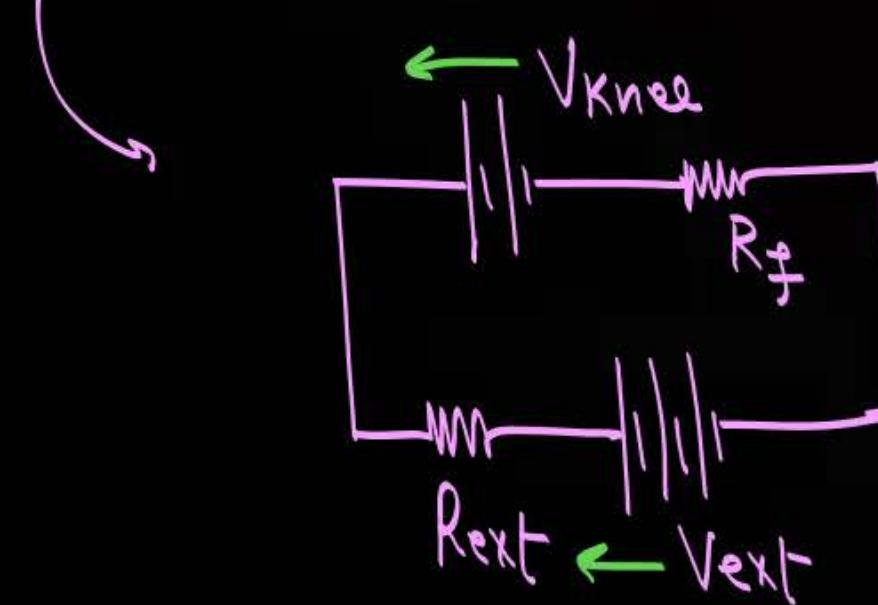
If Resistance Not given  
dont take tension of it.



$$I = \frac{V_{\text{ext}} - V_{\text{knee}}}{R_{\text{ext}} + R_f}$$

$R_f$  = forward R

$R_R$  = Reverse Resis.



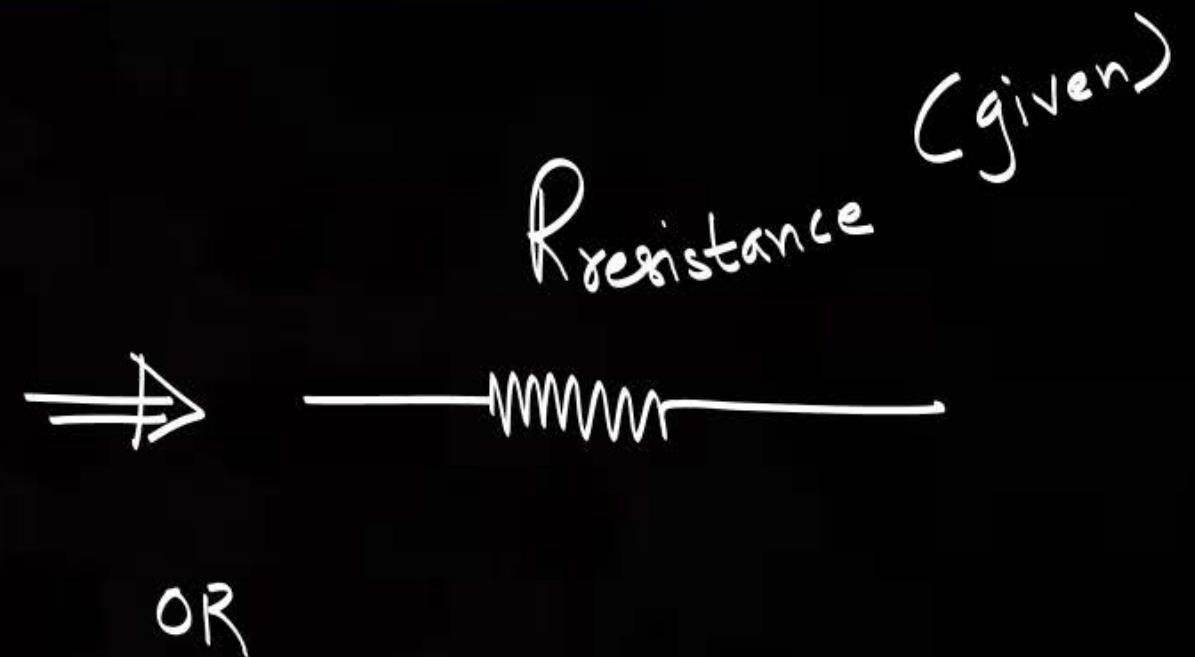
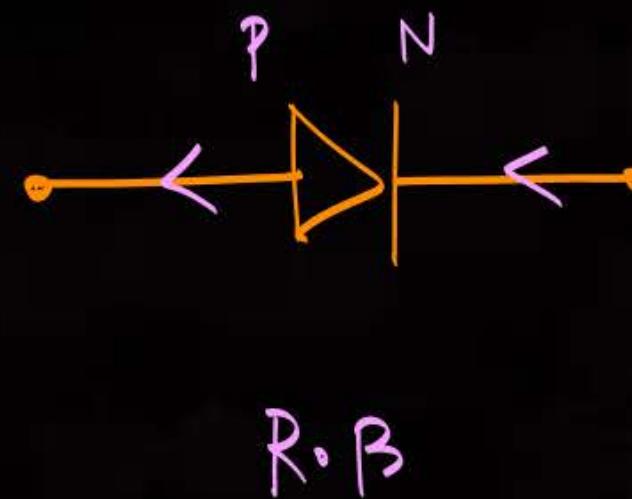
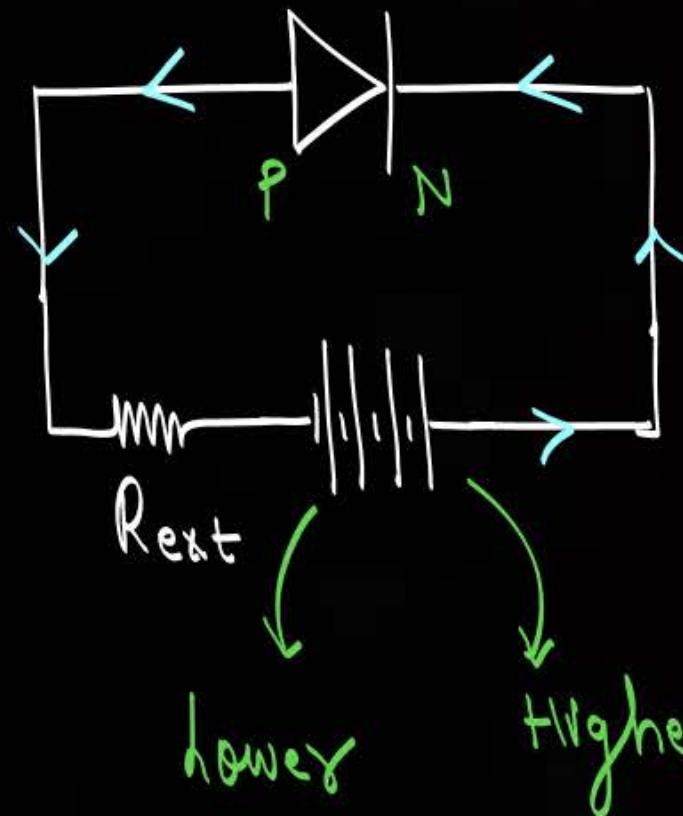


# PN Junction diode in electrical circuit



Real diodes

a)



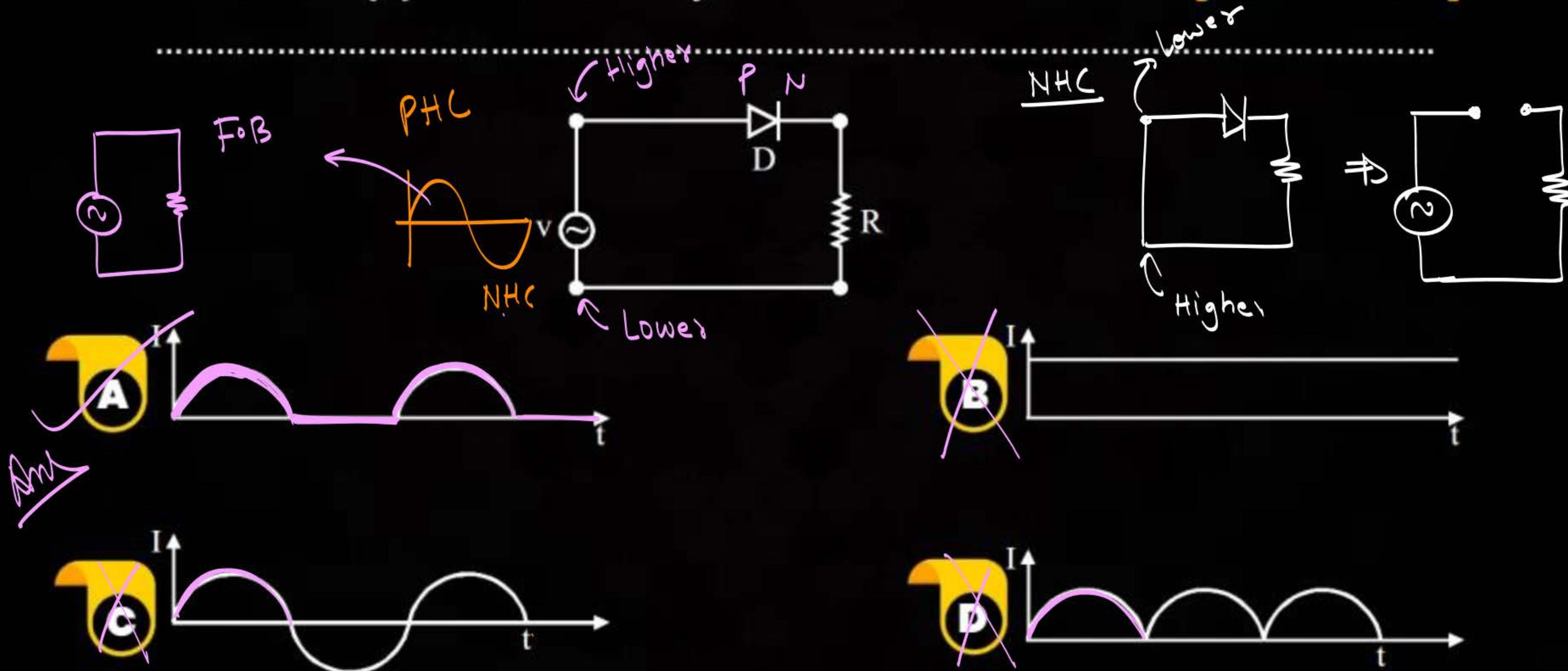
$$R_{Reve} = \infty$$

$R \cdot B$

Q.

A p-n junction diode (D) shown in the figure can act as a rectifier. An alternating current source ( $V$ ) is connected in the circuit. The current ( $I$ ) in the resistor ( $R$ ) can be shown by :-

[AIEEE - 2009]



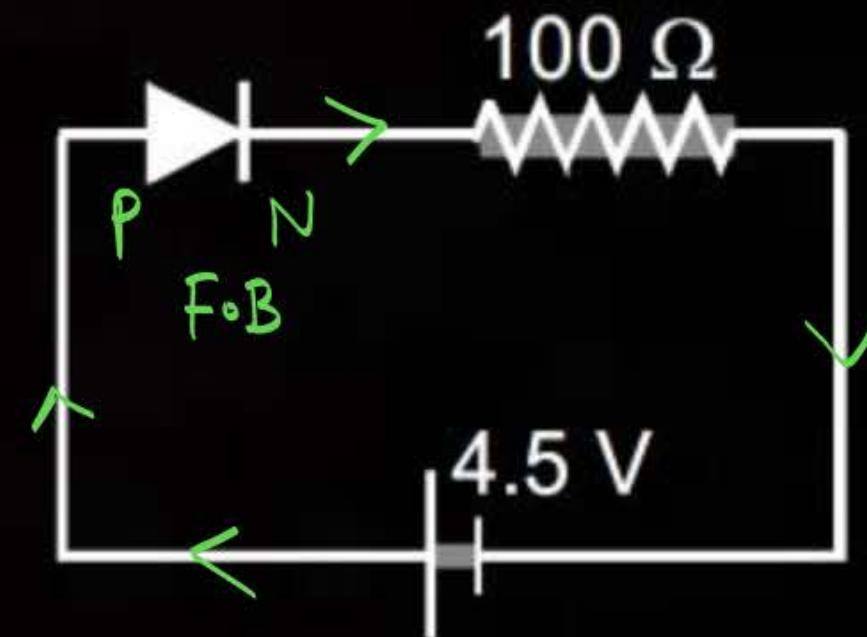
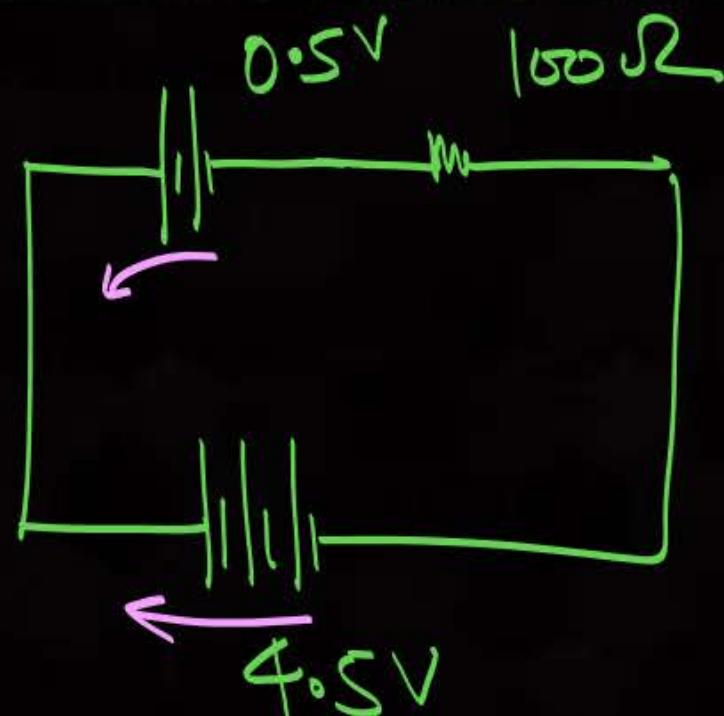
**Q.**

Figure shows a diode connected to an external resistance and an e.m.f. Assuming that the barrier potential developed in diode is 0.5 V, obtain the value of current in the circuit in millampere.

P  
W

V<sub>Knee</sub>

opb battery



$$I = \frac{4.5 - 0.5}{100}$$

$$\therefore \frac{4}{100} = 40 \text{ mA}$$

What is the value of current I in given circuits

Q.

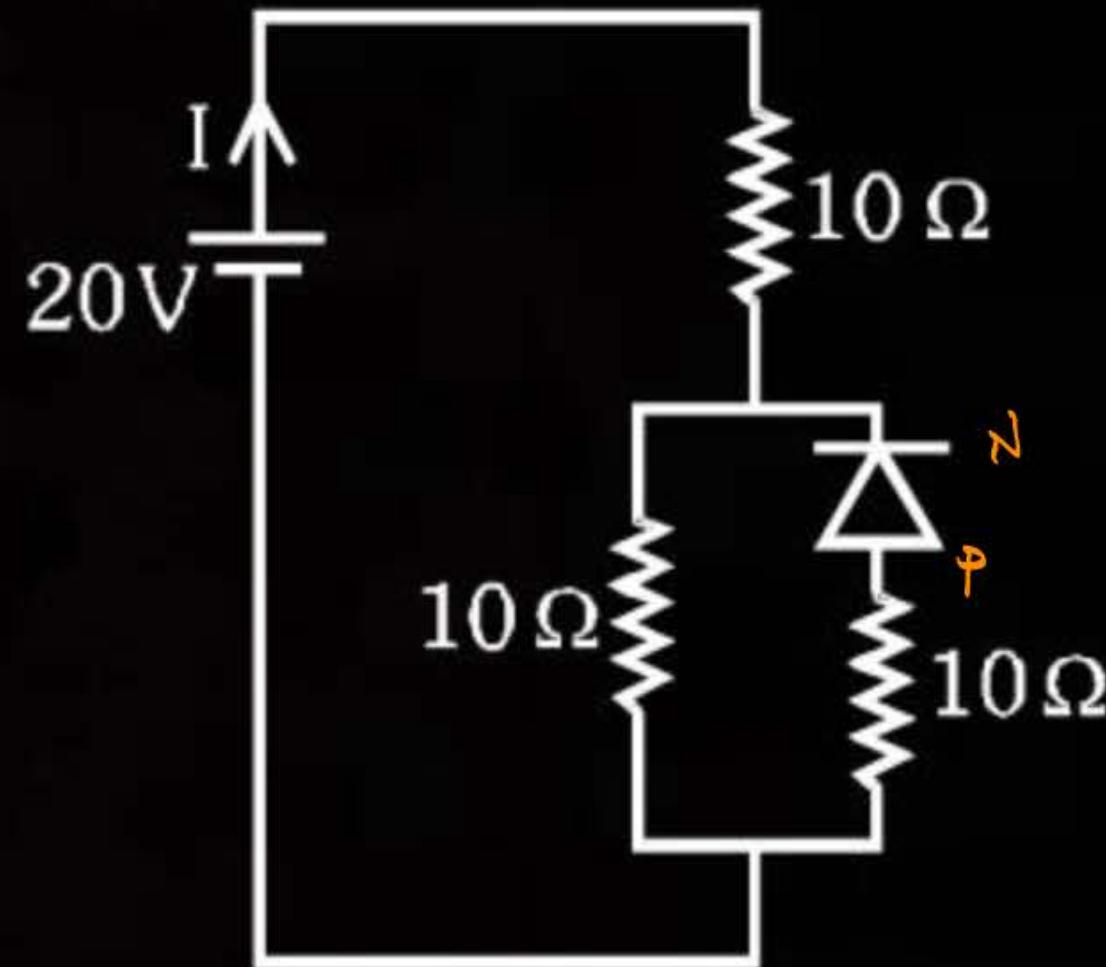
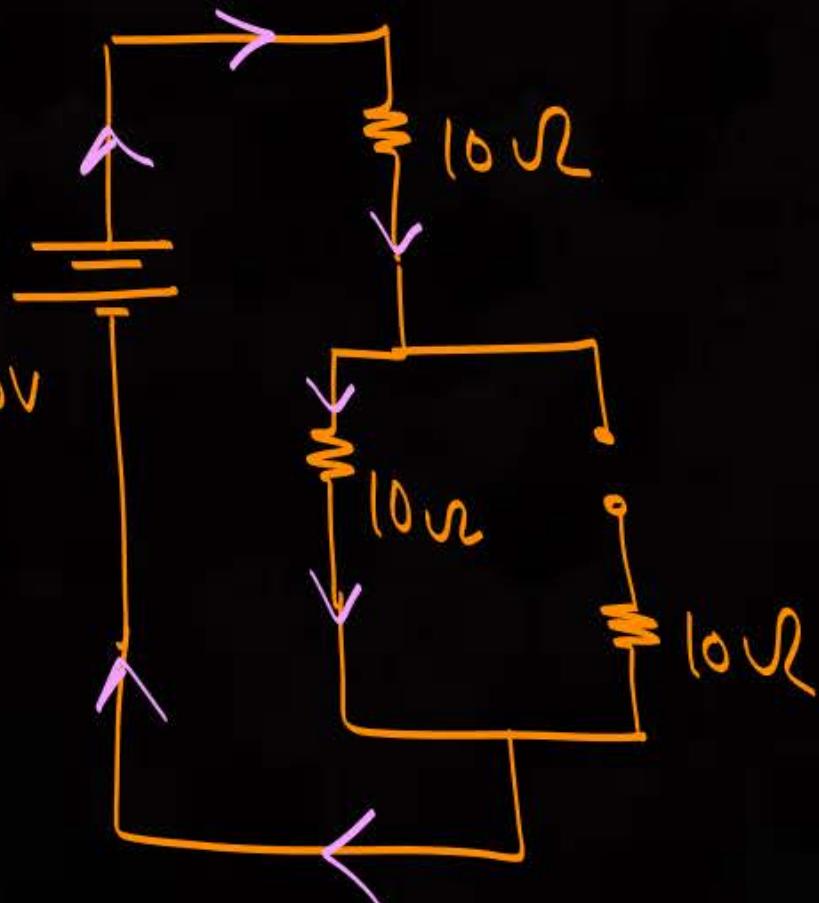
(Ideal)

Reverse



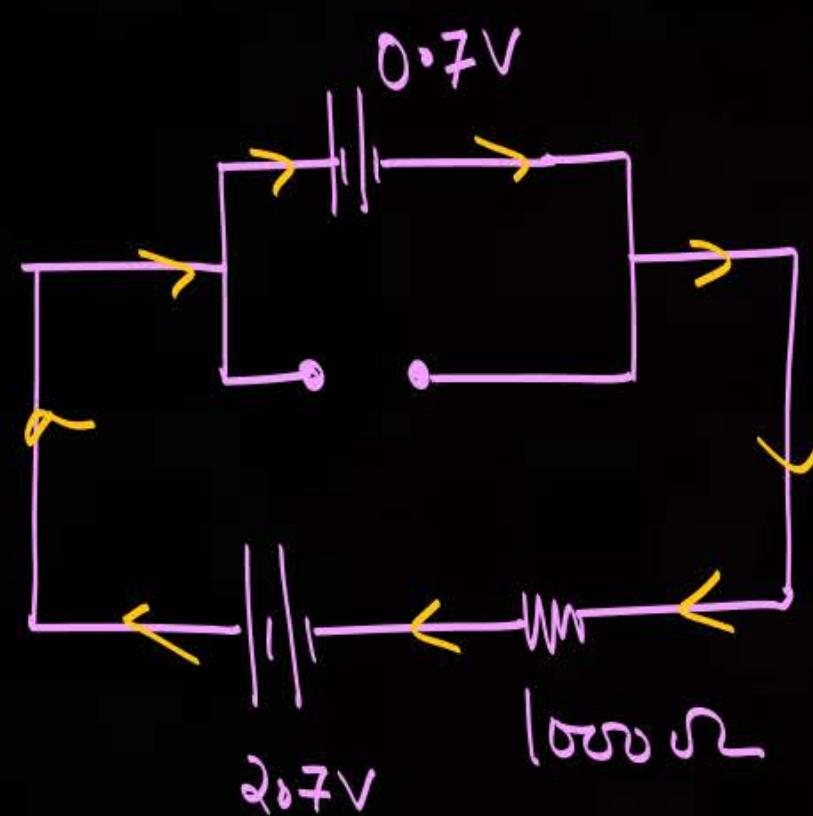
$$I = \frac{V_T}{R_T} = \frac{20}{20}$$

$$= 1A, 20V$$



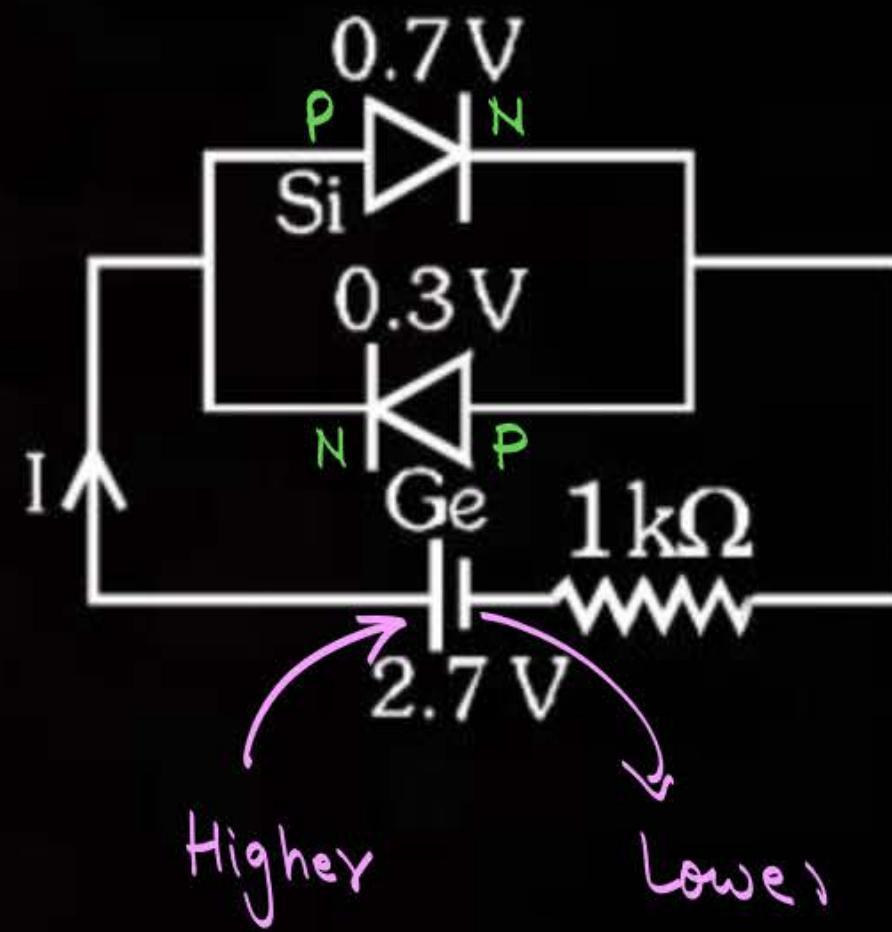
What is the value of current I in given circuits

Q.



$$Si \rightarrow F \cdot B$$

$$Ge \rightarrow R \cdot B$$



$$I = \frac{2.7 - 0.7}{100\Omega} = 2mA_{II}$$

Q.

In the given figure, each diode has a forward bias resistance of  $30\Omega$  and infinite resistance in reverse bias. The current  $I_1$  will be :

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A 3.75 A

B 2.35 A

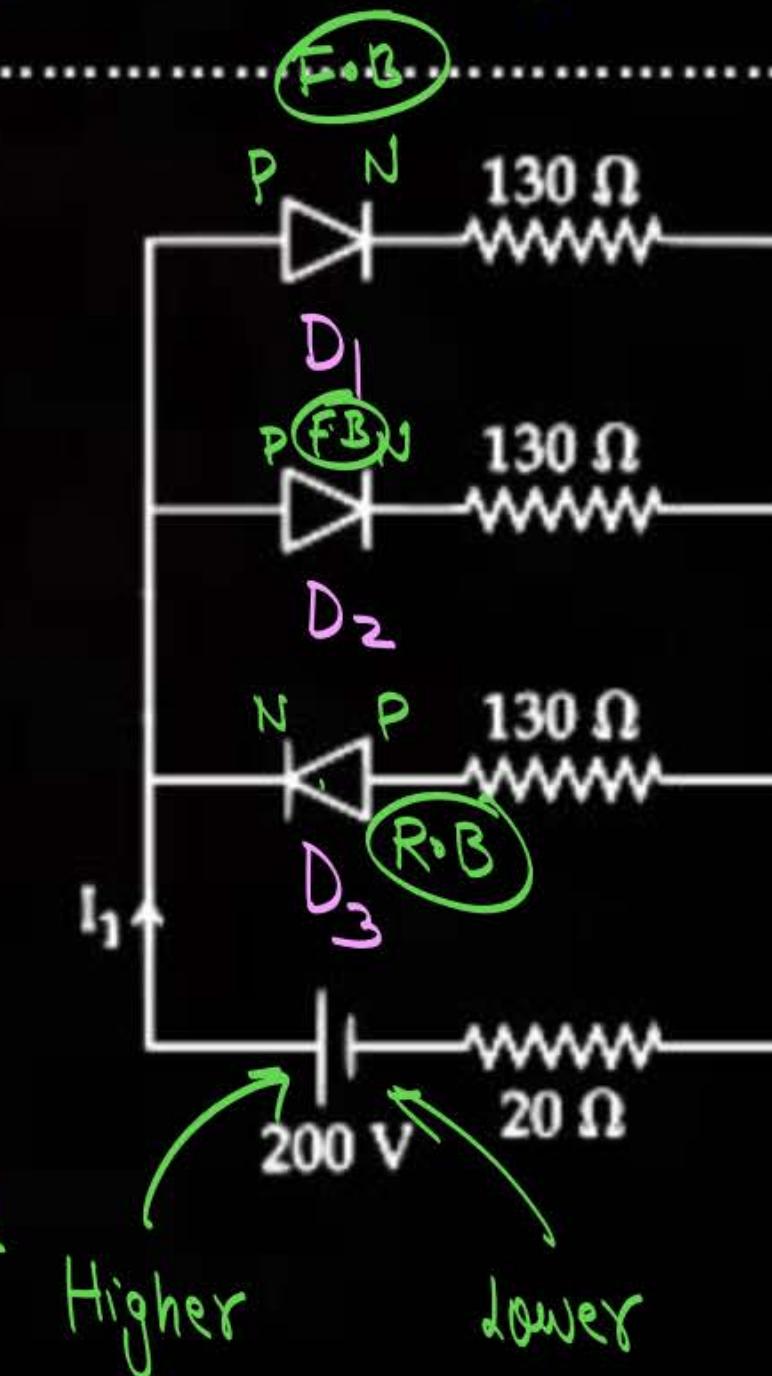
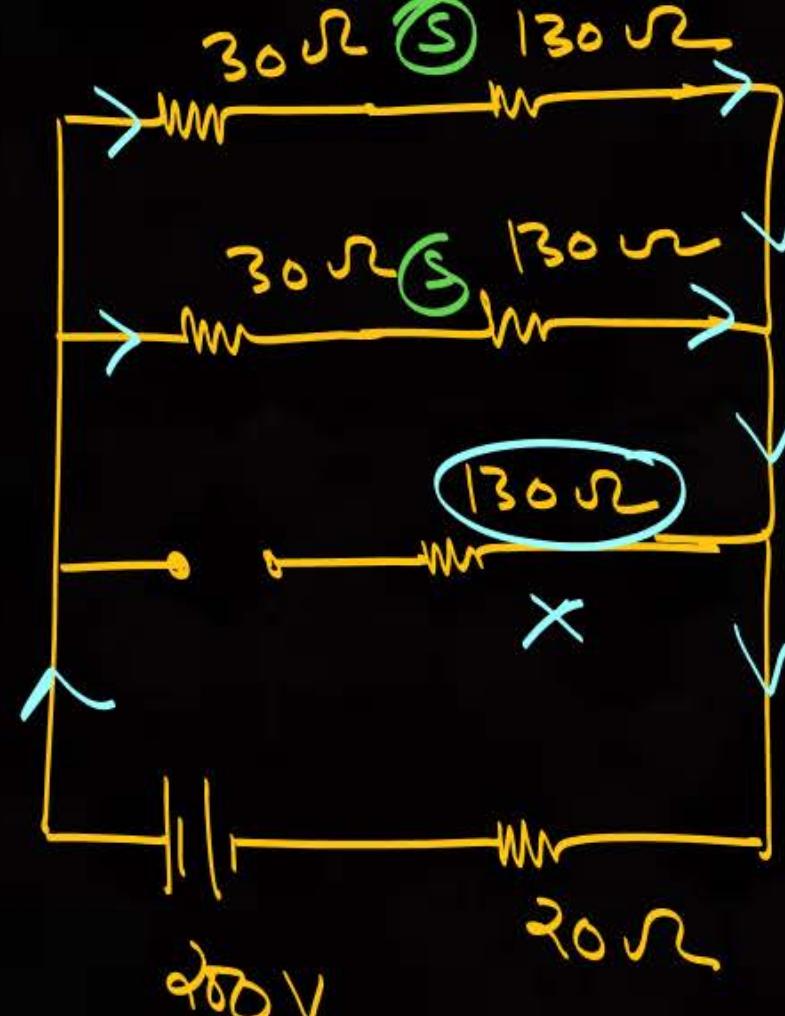
C 2 A

D 2.73 A

*Ans*

$$I = \frac{V}{R} = \frac{200}{100} = 2 \text{ A}$$

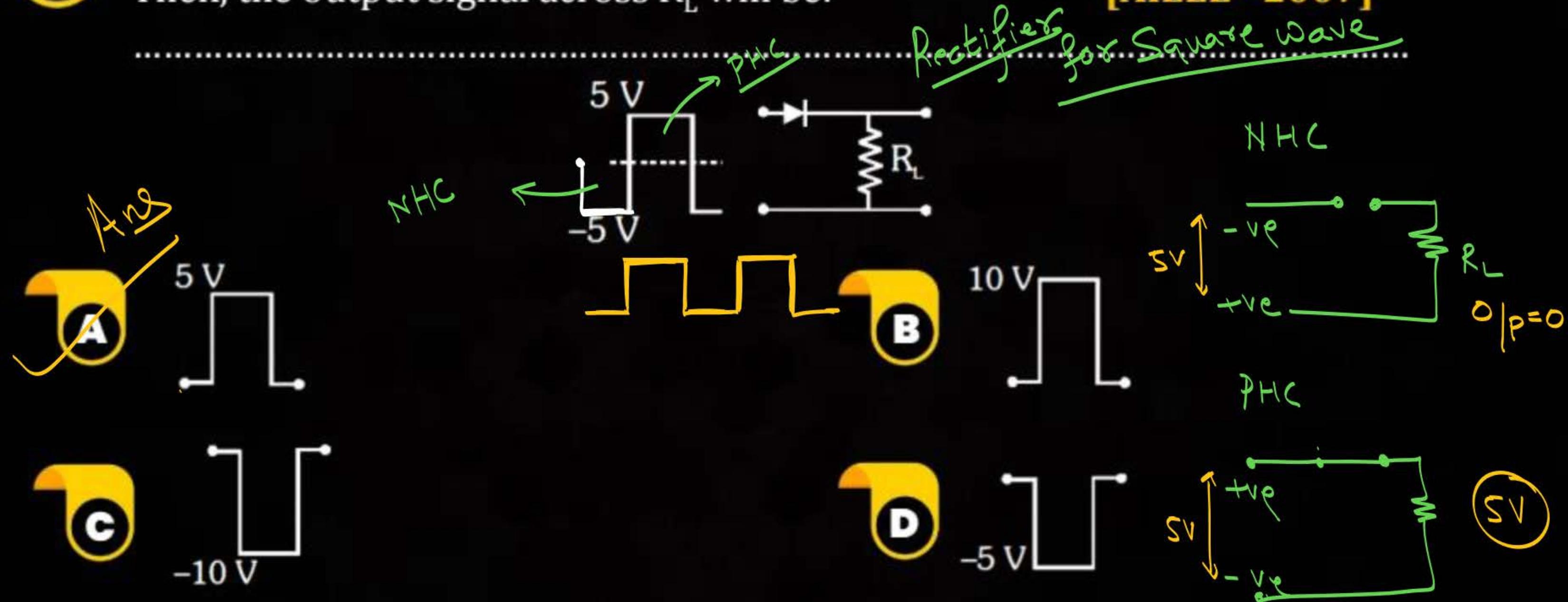
$$R_T = 80 + 20 = 100\Omega$$



Q.

If in a p-n junction diode, a square input signal of 10 V is applied as shown.  
 Then, the output signal across  $R_L$  will be:

[AIEEE - 2007]



Q.

When a diode is forward biased, it has a voltage drop of  $0.5\text{ V}$ . The safe limit of current through the diode is  $10\text{ mA}$ . If a battery of emf  $1.5\text{ V}$  is used in the circuit, the value of minimum resistance to be connected in series with the diode so that the current does not exceed the safe limit is

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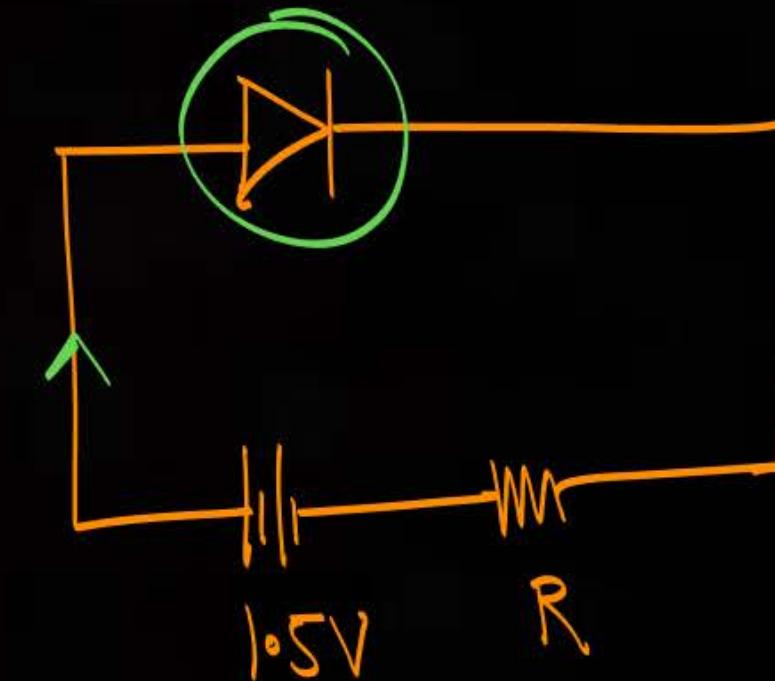
A  $50\Omega$ B  $200\Omega$ C  $30\Omega$ D  $100\Omega$ 

$$I = 10\text{ mA}$$

$$V_{\text{knee}} = 0.5\text{ V}$$

$$R = \frac{1.5 - 0.5}{10 \times 10^{-3}}$$

I



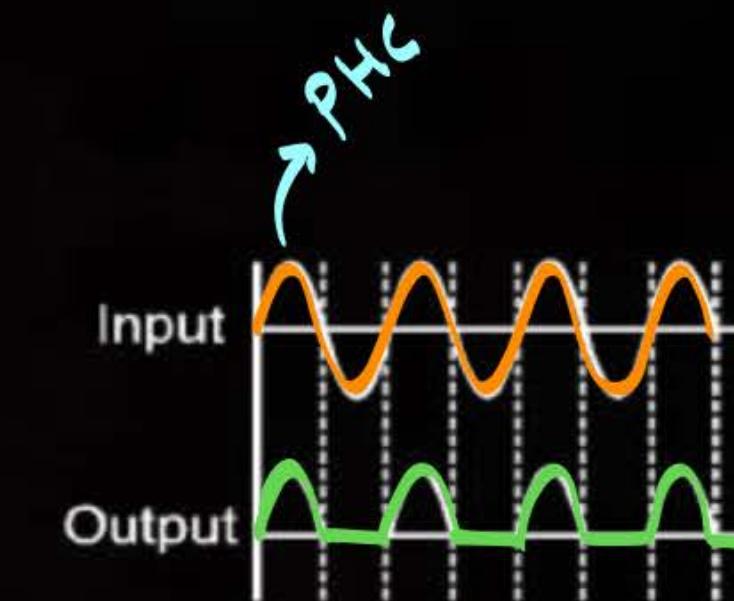
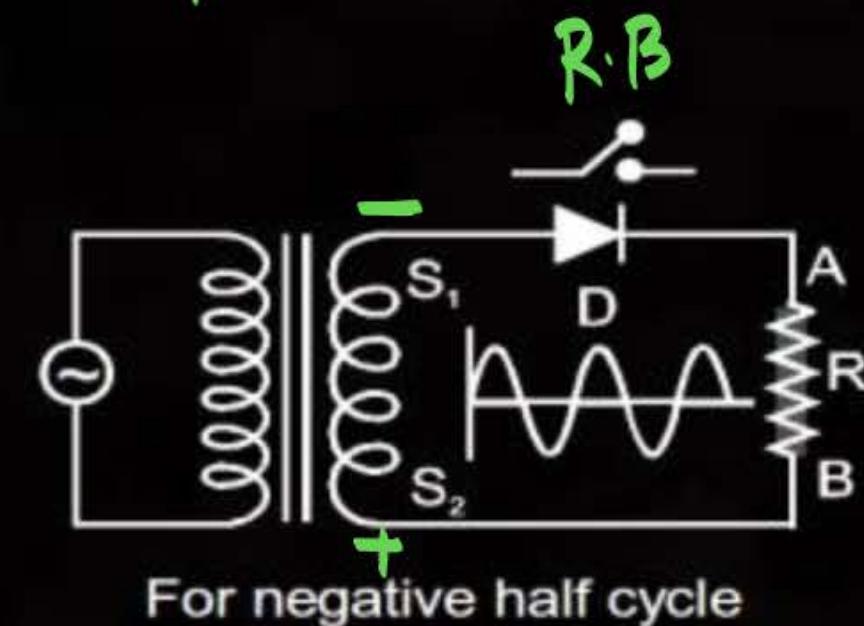
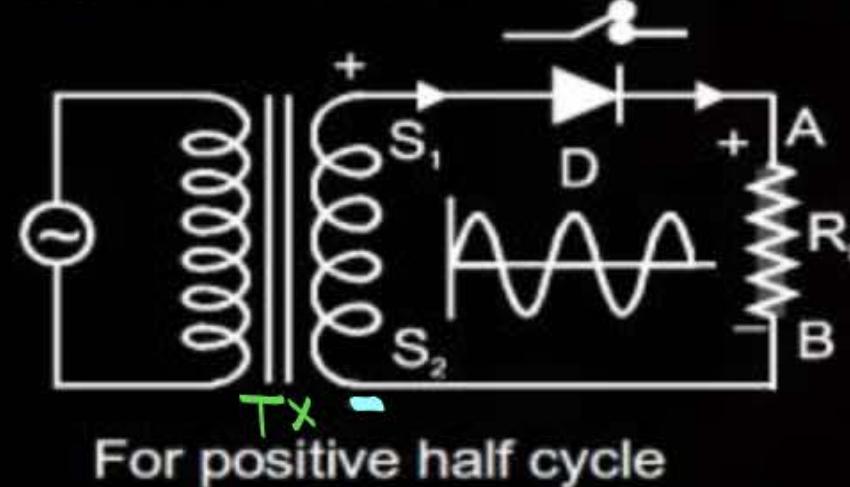


# APPLICATION OF JUNCTION DIODE:



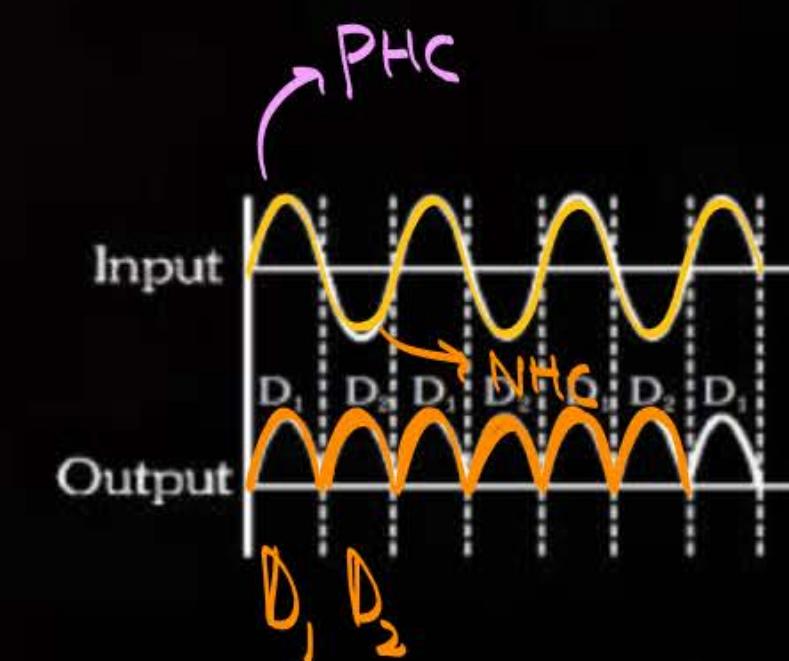
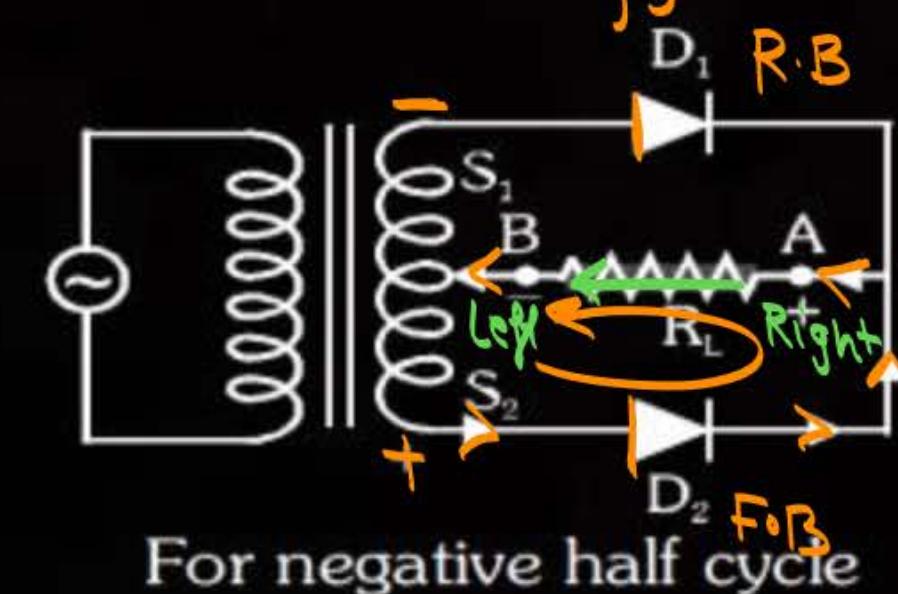
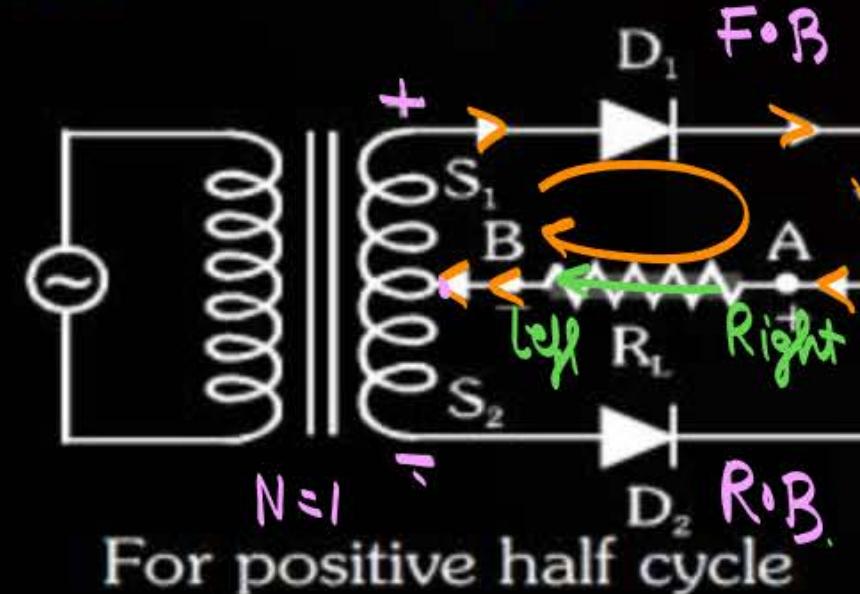
Rectifier  $\rightarrow$  AC  $\rightarrow$  DC output.

## (i) Half wave rectifier



Half wave  
Rectifier.

## (ii) Centre tap rectifier (Full Wave Rectify)



Full Wave  
Rectifier.

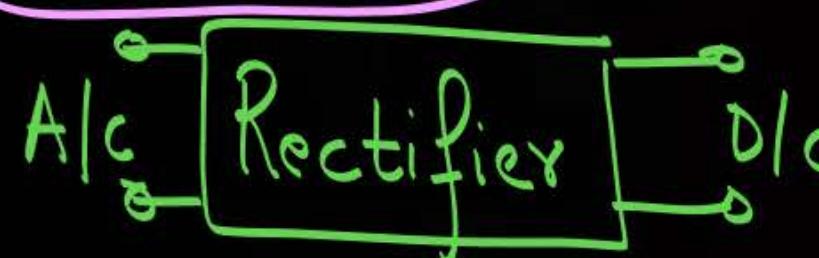
## (i) For half wave rectifier

Input frequency = 50 HzRipple frequency = 50 Hz

## (ii) for full wave rectifier

Input frequency = 50 HzRipple frequency = 100 Hz

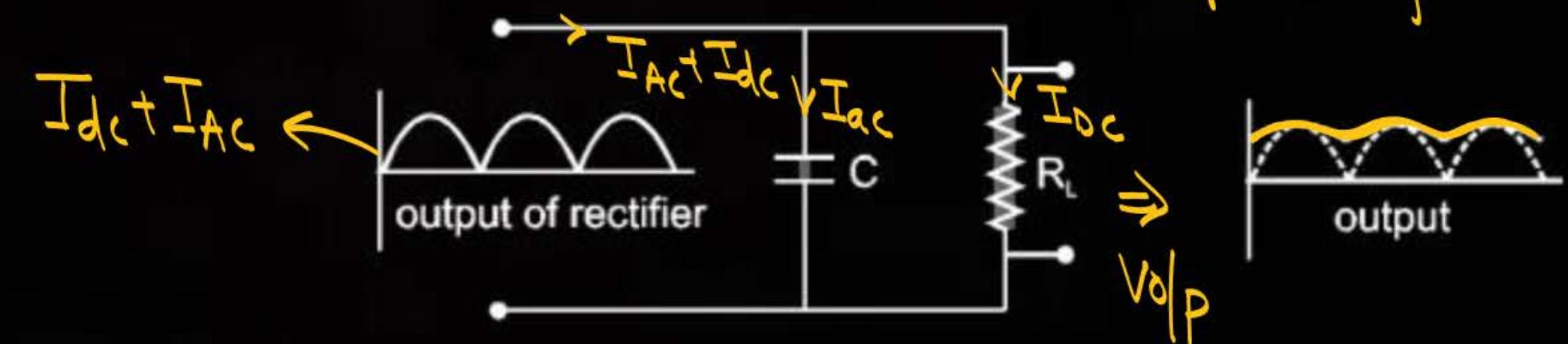
**Filter Circuit** → Capacitor.



Capacitor is connected || $\lambda$   
to Load Resistance.

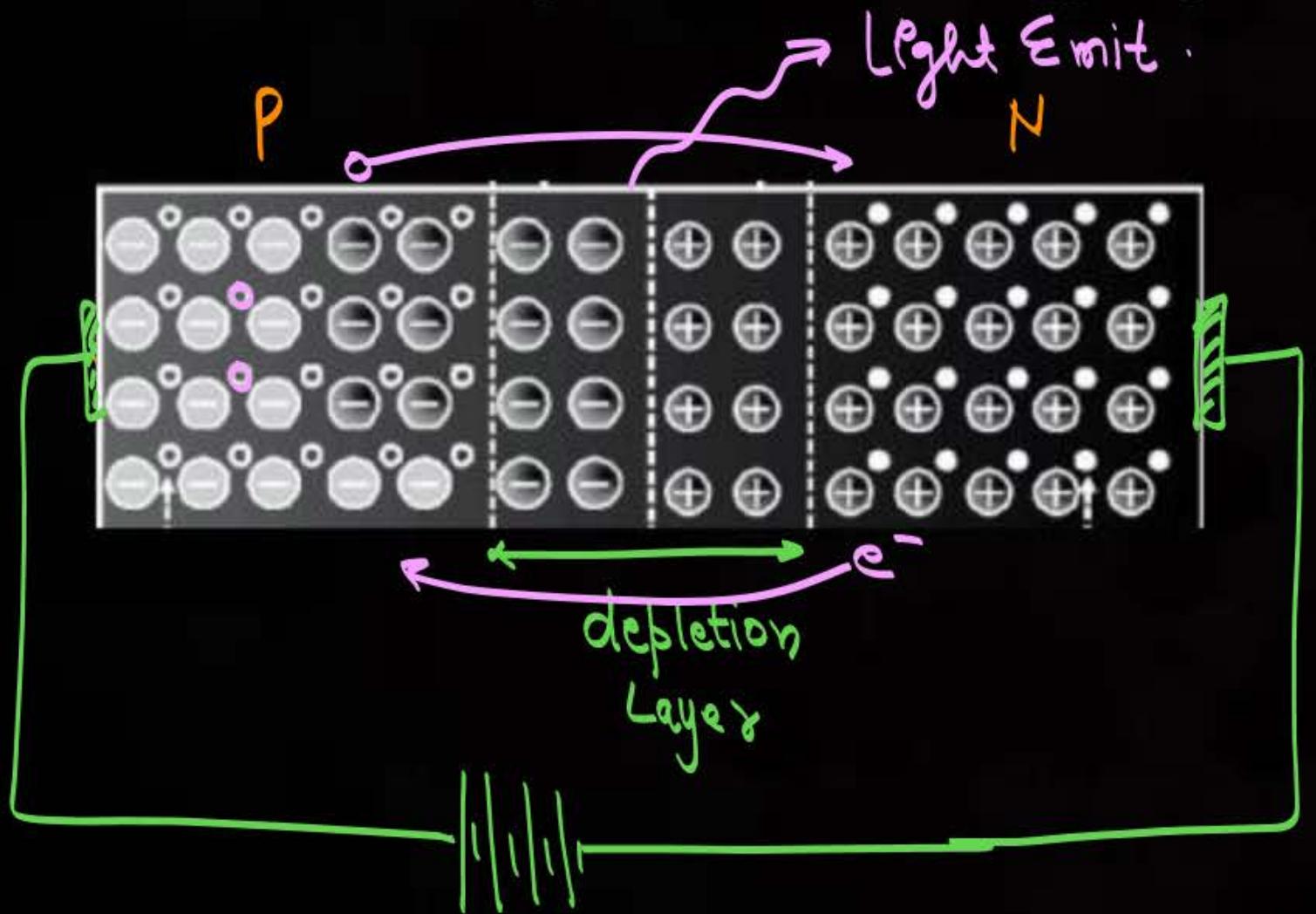
$$X_C = \frac{1}{\omega C} \quad \text{DC} \rightarrow \omega = 0$$

Resistance offered by  $C$   
to DC  $X_C \rightarrow \infty$   
If we AC component for charg.



# Light emitting diode (L.E.D)

LED is forward biased then electrons move from N  $\rightarrow$  P and holes move from P  $\rightarrow$  N. At the junction boundary these are recombined. On recombination, energy is released in the form of photons of energy equal to or slightly less than the band gap.

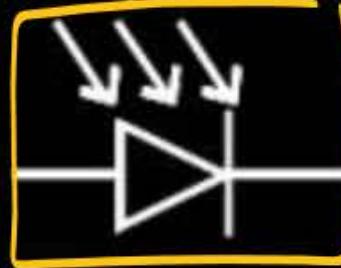


- \* LED (Normal Diode in F.B)
- \*  $e^-$  from N  $\rightarrow$  P & Recombine.
- \* Energy is Released (Visible Spectra)

$$\lambda_{\text{emit}} = \frac{12400}{E_g(\text{eV})} \text{ Å}$$

# Photodiode

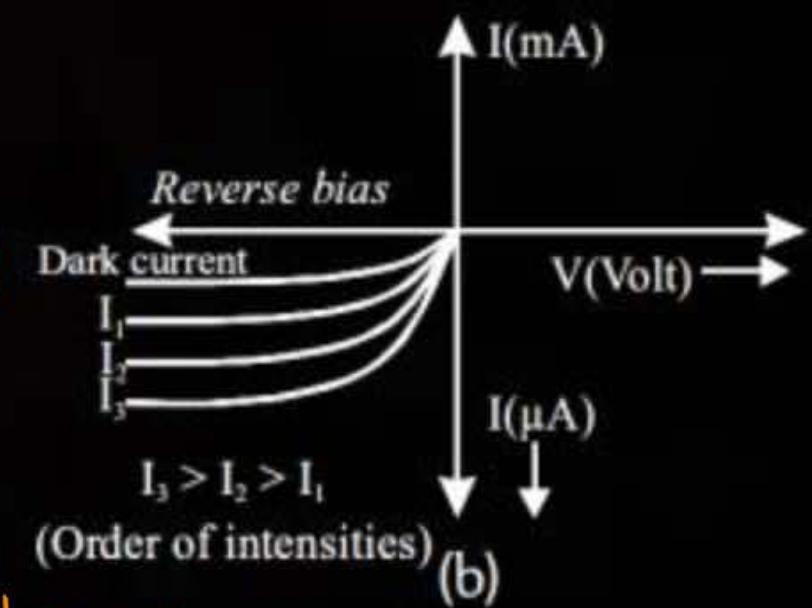
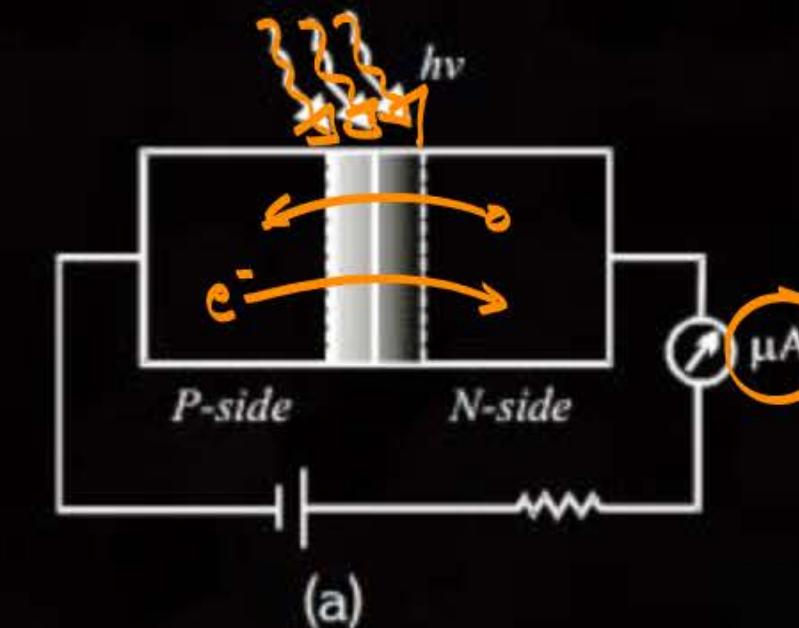
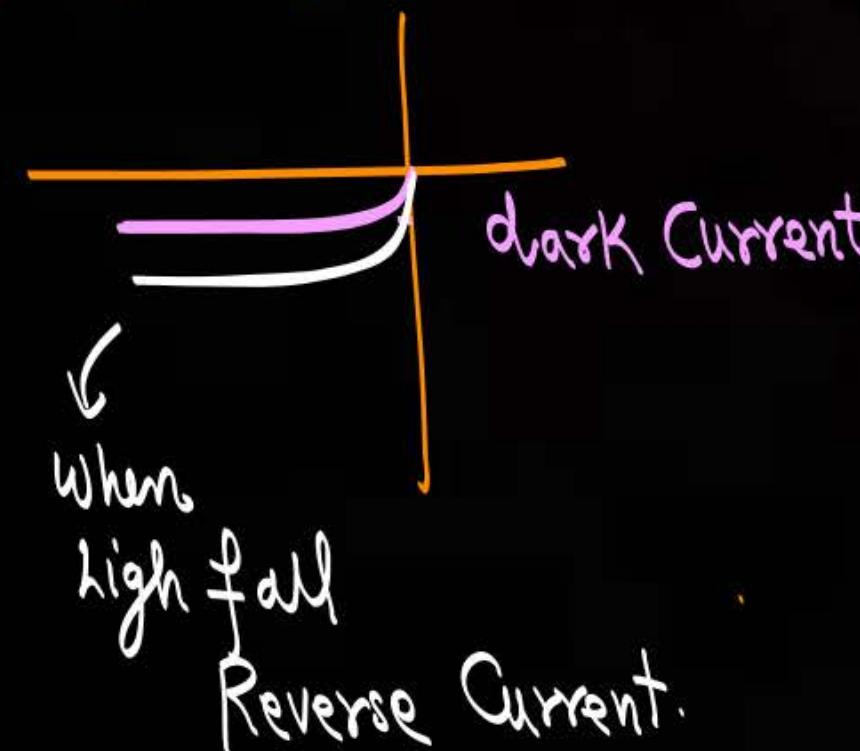
It is a special purpose junction diode used to sense and measure incident

light. its symbol is . It is operated under reverse bias.

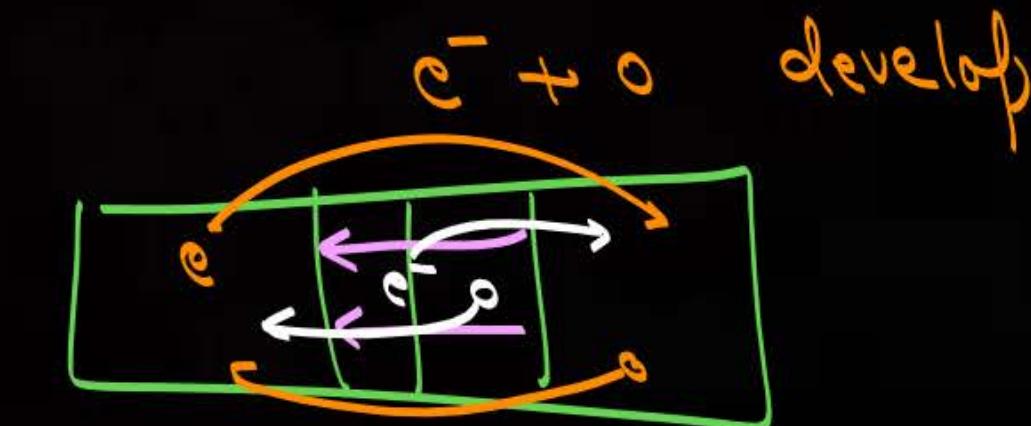
④ diode in R.B.

⑤ Used for detection of light.

⑥ When R.B



⑦ When light falls on depletion layer



# Solar cell

- ④ No biasing
- ④ When light falls on depletion layer

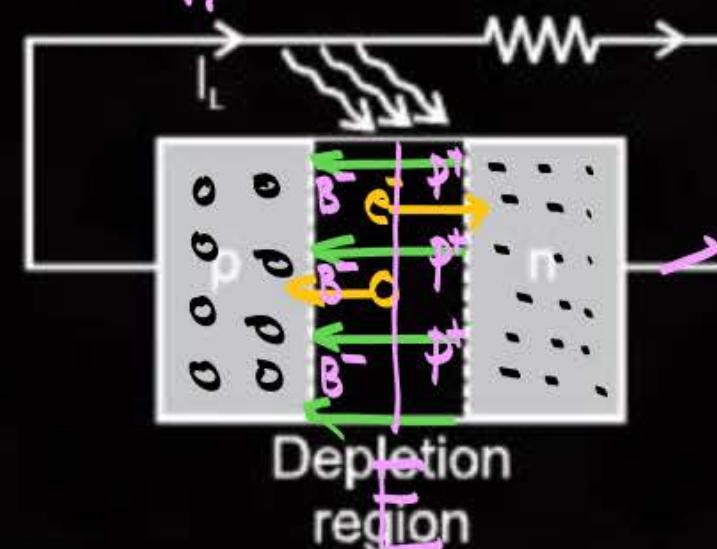
bond  $\rightarrow$  break  $(e^- + o)$   
 move to n move to P.

- ④ with time

$$N \rightarrow n_e \uparrow$$

$$P \rightarrow n_n \uparrow$$

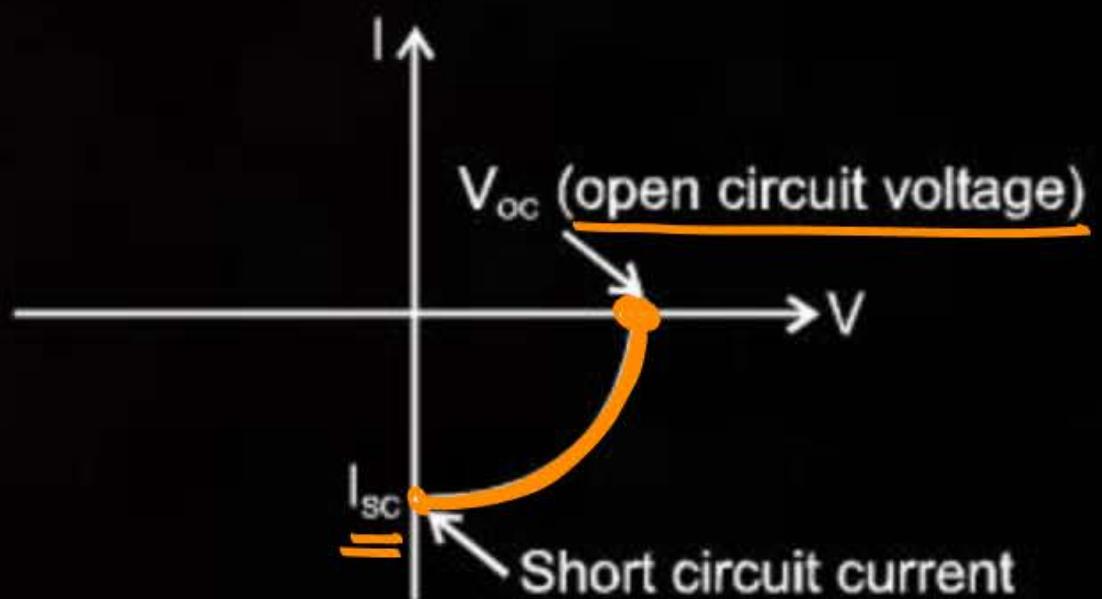
When Short CKT  $I \uparrow$



A typical illuminated p-n junction solar cell

(a)

$$\begin{array}{c} \leftarrow E \\ \leftarrow e \quad \rightarrow \bar{e} \\ \leftarrow \sigma \end{array}$$



I-V characteristics of a solar cell

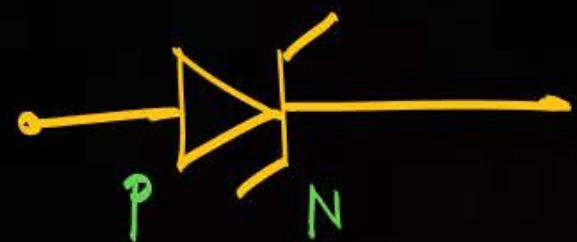
(b)

# ZENER DIODE: (Most Imp)

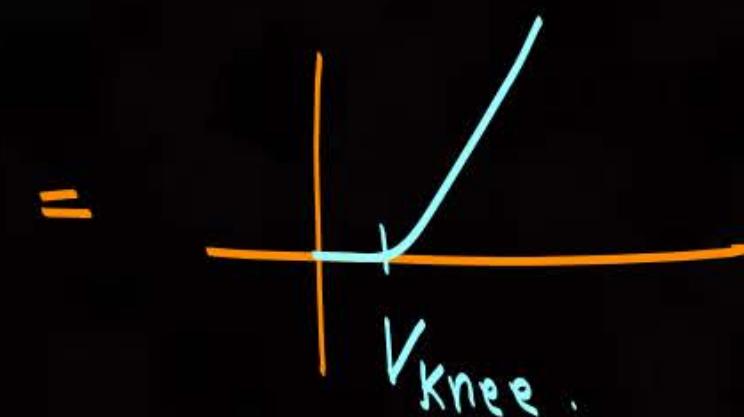
P  
W

\* Zener diode is a Normal diode only.

\* Reb :-



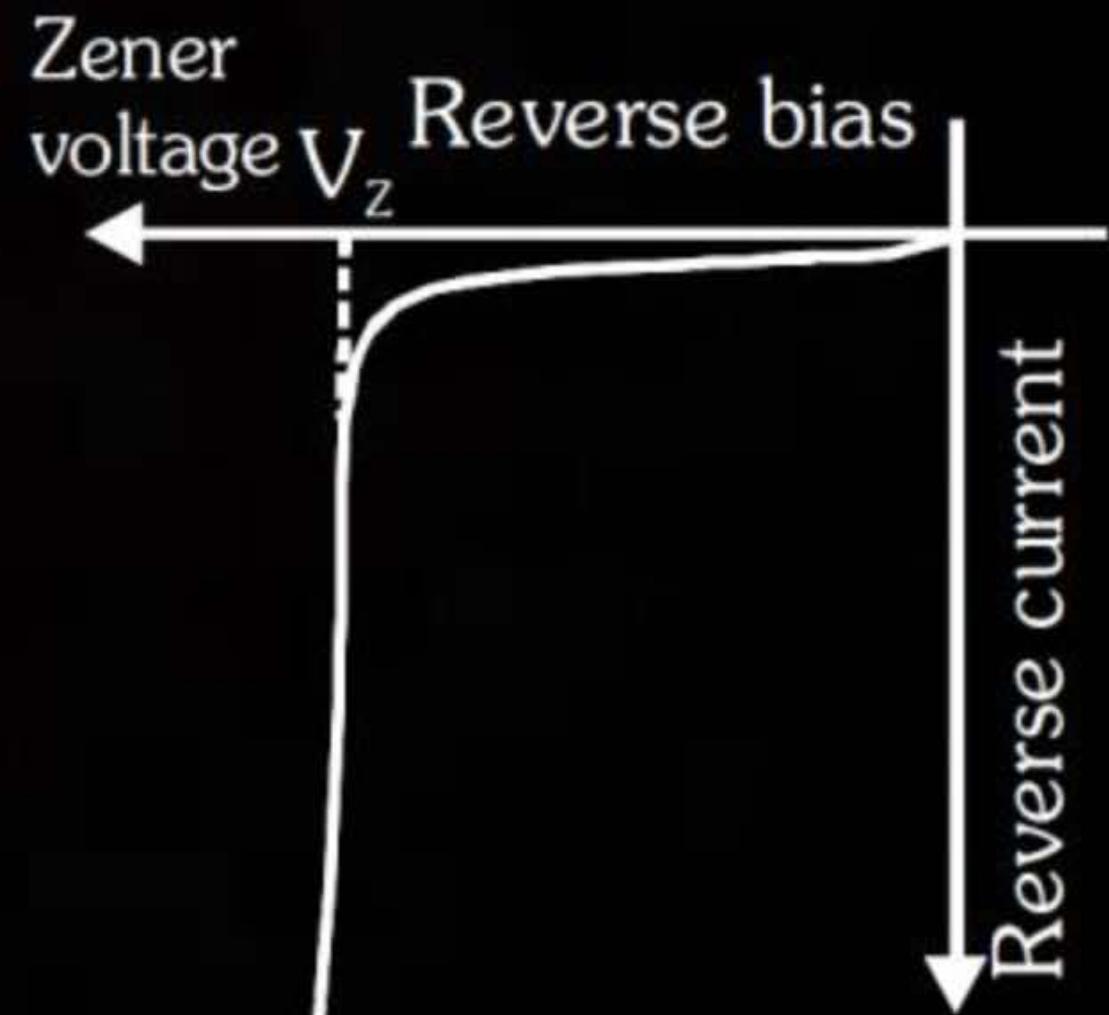
\* It Can be used in F.B



Method of Checking  
F.B., R.B Same.

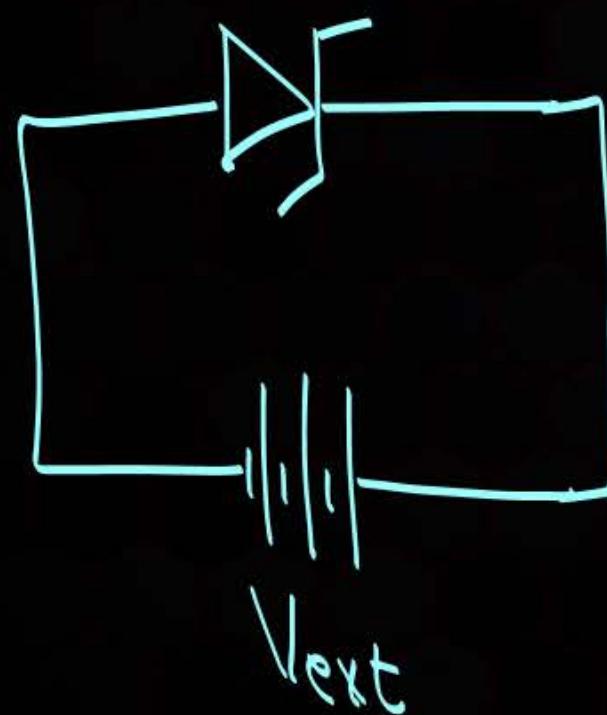
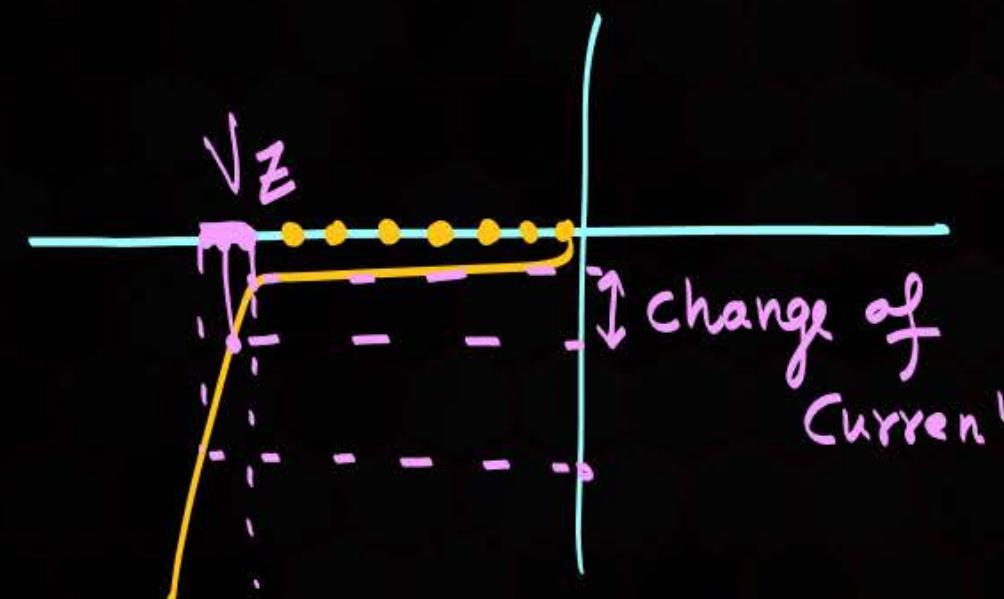
$$V_P - V_N = +ve \text{ F.B.}$$

$$V_P - V_N = -ve \text{ R.B.}$$



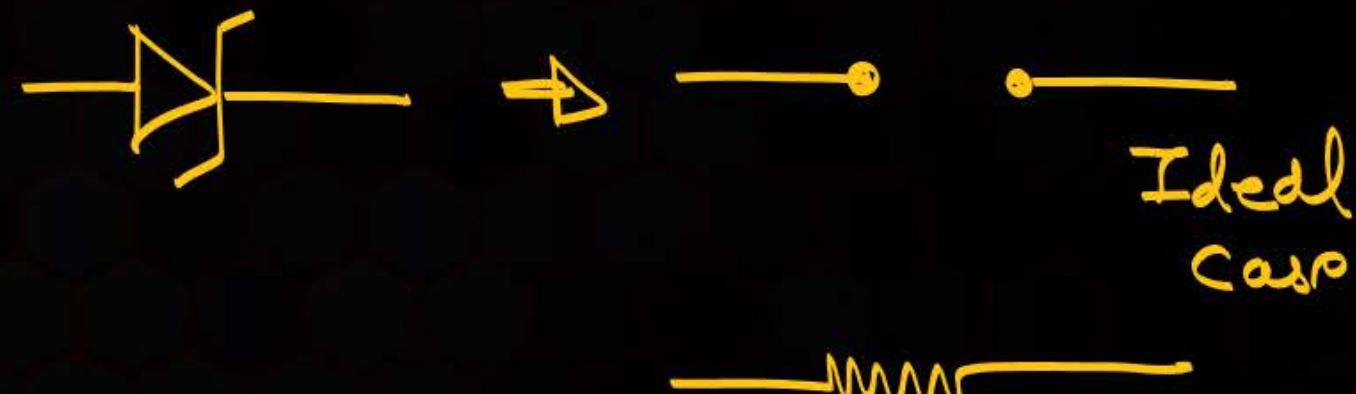
Same as Normal diode.

Q if Zener diode R.O.B



$V_Z$  = Zener breakdown Voltage

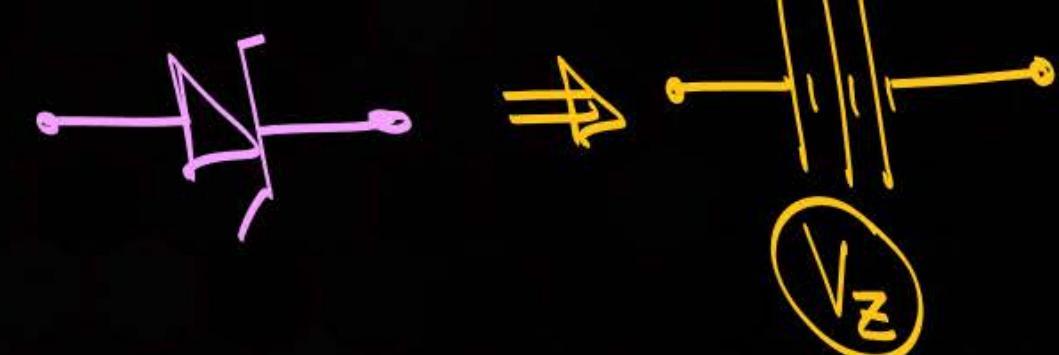
Case 1.  $V_{ext} < V_Z$



Case 2.

Voltage Regulator.  
(in R.O.B)

$V_{ext} > V_Z$



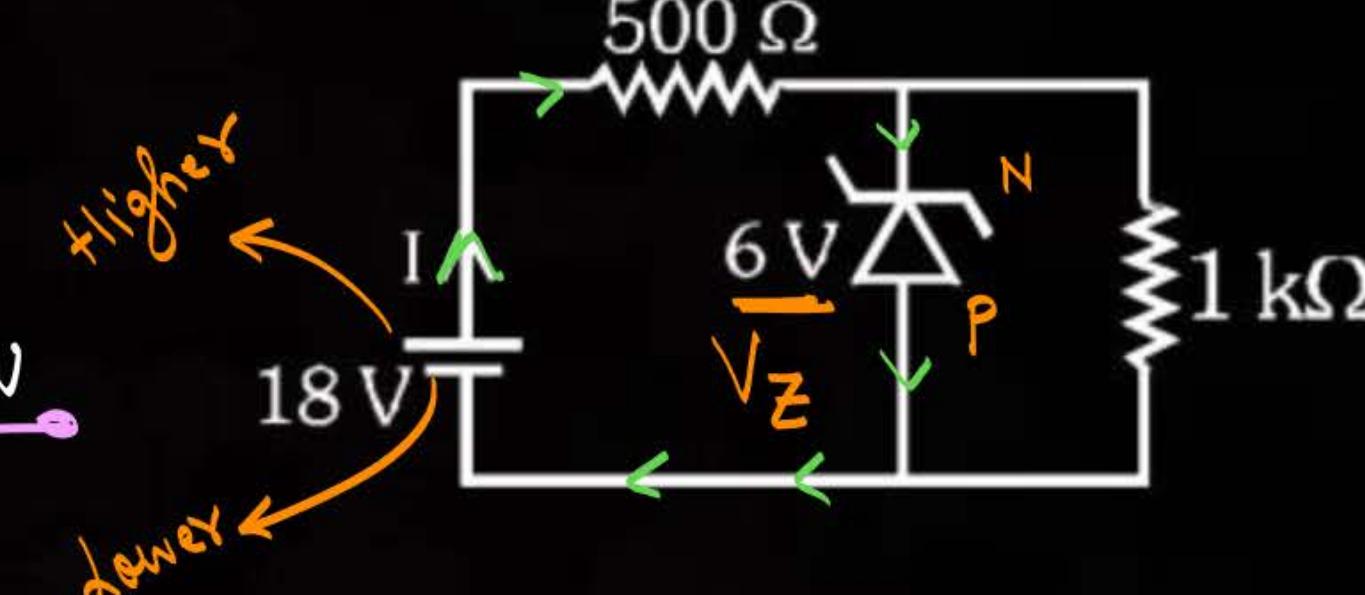
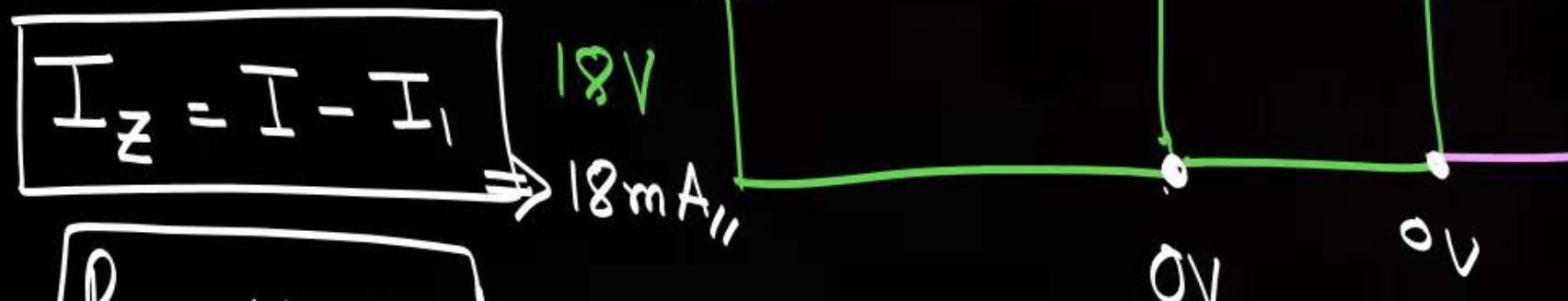
What is the value of current I in given circuits?

\* R.B.

\*  $V_{ext} > V_Z$  (Voltage Reg).

$$I = \frac{18 - 6}{500} = 24 \text{ mA}$$

$$I_1 = \frac{6 - 0}{1000} = 6 \text{ mA}$$



**Q.**

If a semiconductor photodiode can detect a photon with a maximum wavelength of 400 nm, then its band gap energy is :

Planck's constant  $h = 6.63 \times 10^{-34}$  J.s. Speed of light  $c = 3 \times 10^8$  m/s

JEE Main 2020 (Online) 3<sup>rd</sup> September Evening Slot

---

**A**

1.5 eV

**B**

2.0 eV

**C**

3.1 eV

**D**

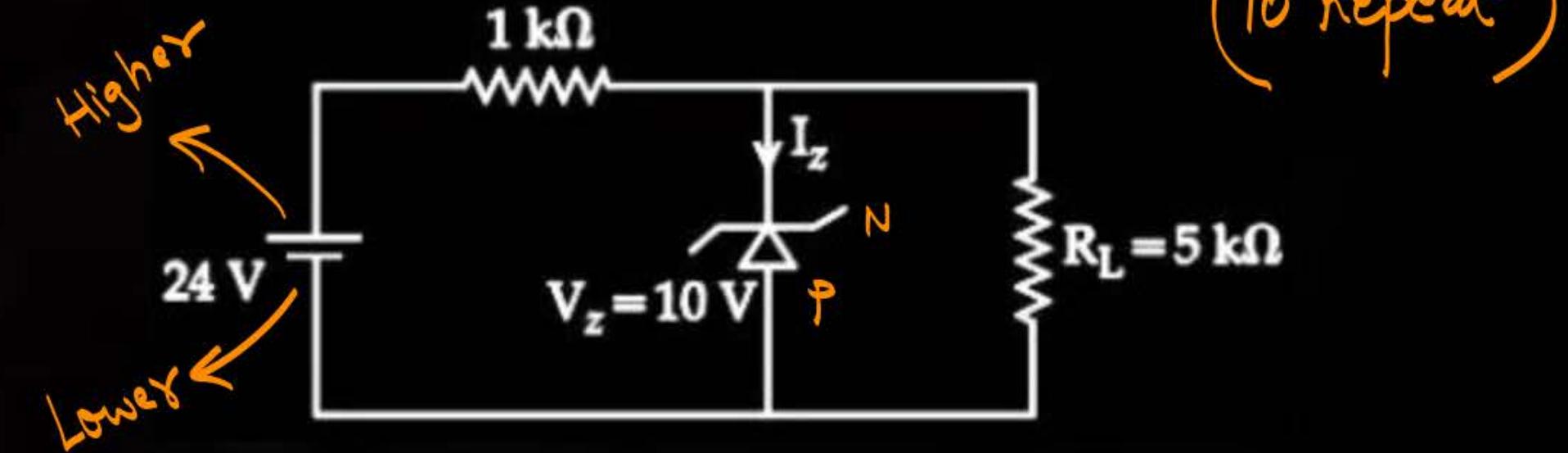
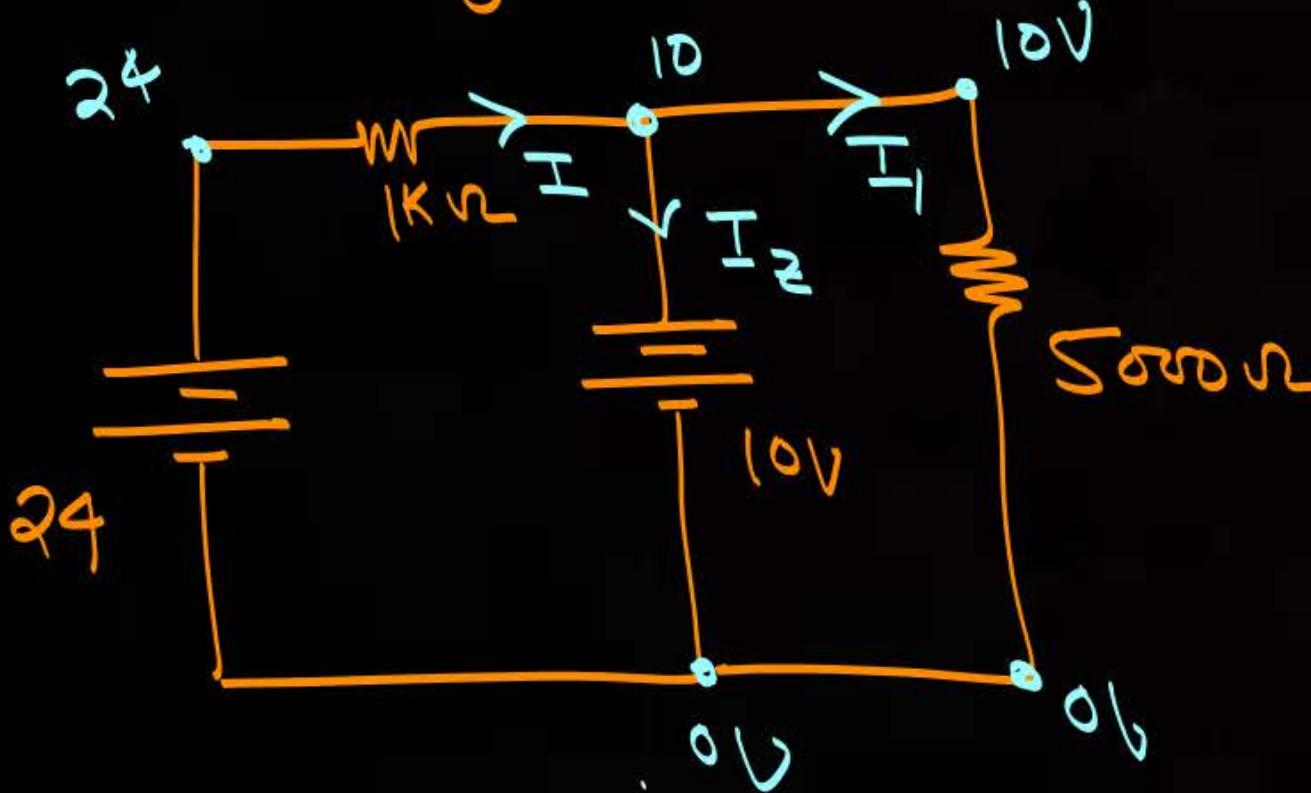
1.1 eV

For the given circuit, the power across Zener diode is ..... 120 mW.

JEE Main 2021 (Online) 26<sup>th</sup> August Evening Shift

- R.O.B.
- $V_{ext} > V_z$

Regulators



$$I = \frac{24 - 10}{1000} = 14 \text{ mA}$$

$$I_1 = \frac{10 - 0}{5000} = 2 \text{ mA}$$

$$I_2 = 12 \text{ mA}$$

$$\begin{aligned} P &= V_z I_2 \\ &= 10 \times 12 \text{ mA} \\ &= 120 \text{ mW} \end{aligned}$$

(10 Repeat)

Q.

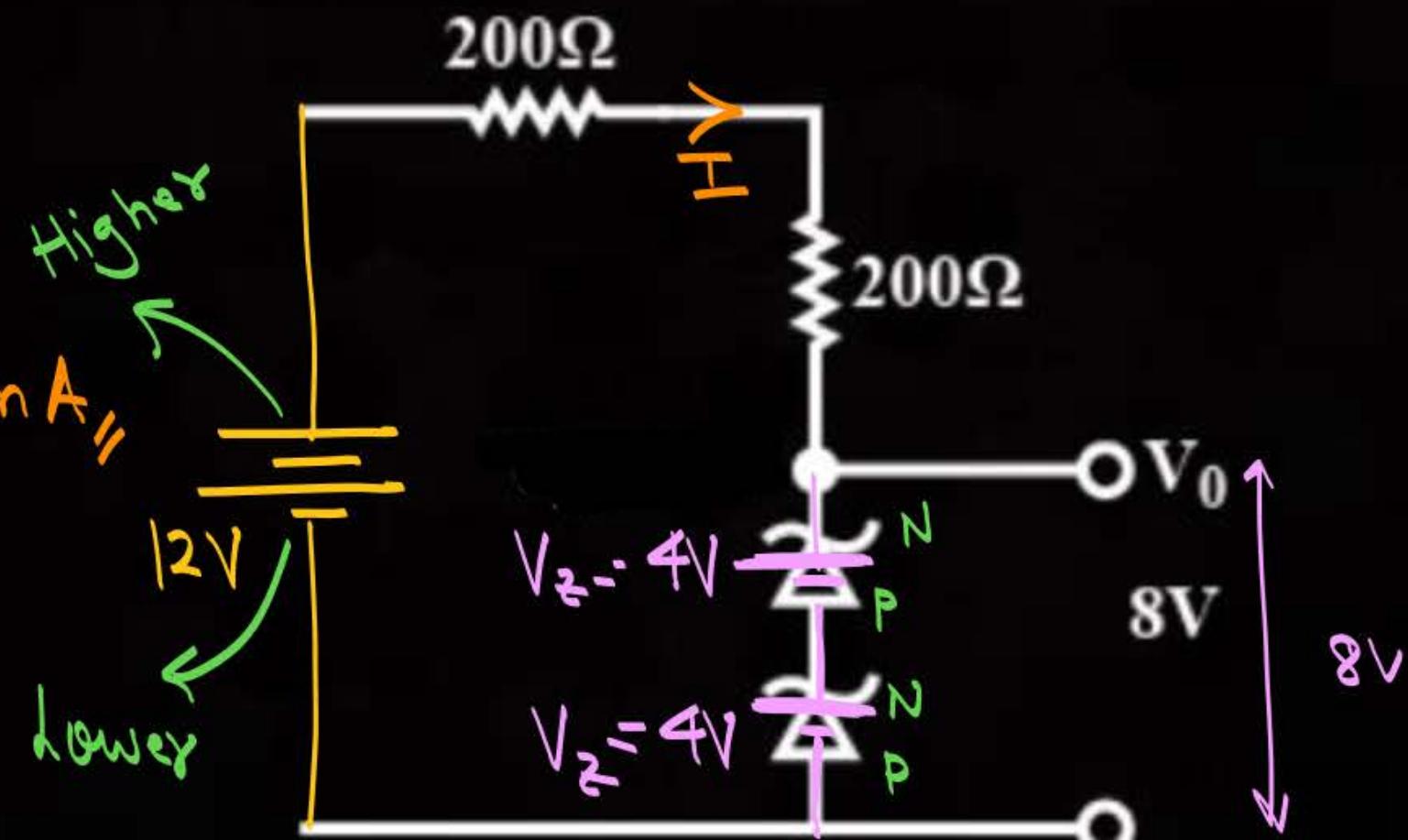
The circuit shown below is working as a 8 V dc regulated voltage source. When 12 V is used as input, the power dissipated (in mW) in each diode is; (considering both zener diodes are identical)  $40$ .  $V_z = 4V$

JEE Main 2020 (Online) 9<sup>th</sup> January Evening Slot

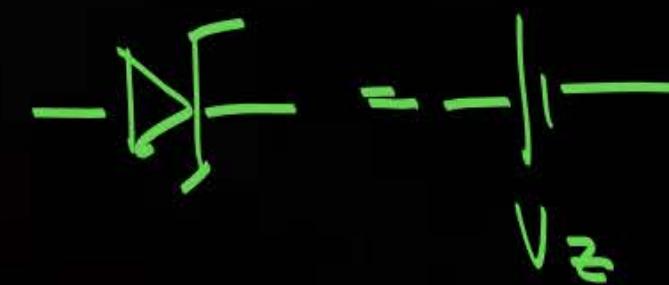
$$I = \frac{12 - 8}{400} = 10mA$$

$$= \frac{4}{400} = 10mA$$

Higher  
Lower



Voltage Regulator



$$\begin{aligned} P &= V_z I_z \\ &= 4 \times 10 \text{ mA} \\ &= 40 \text{ mW} \end{aligned}$$

Q.

With increasing biasing voltage of a photodiode, the photocurrent magnitude :

JEE Main 2020 (Online) 5<sup>th</sup> September Morning Slot

A

Increases initially and after attaining certain value, it decreases

B

Increases linearly

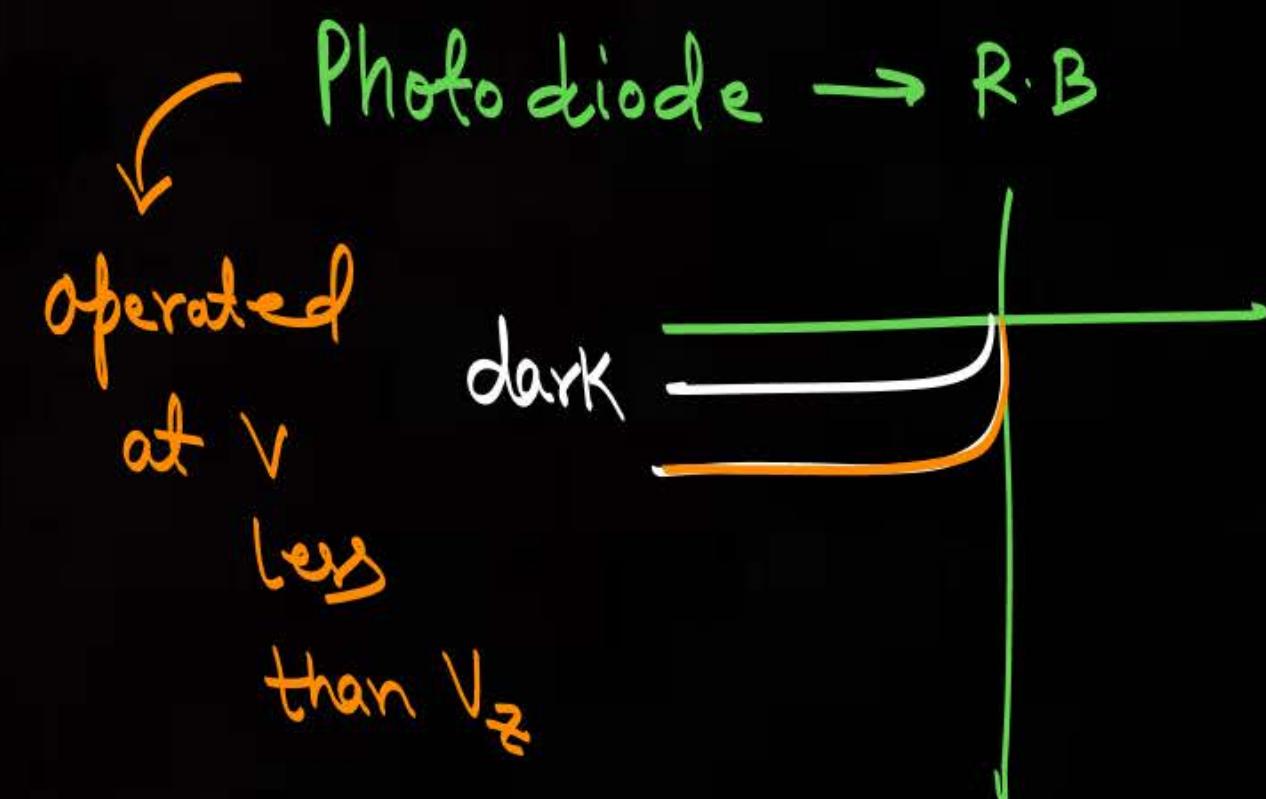
C

Increases initially and saturates finally

*Ans*

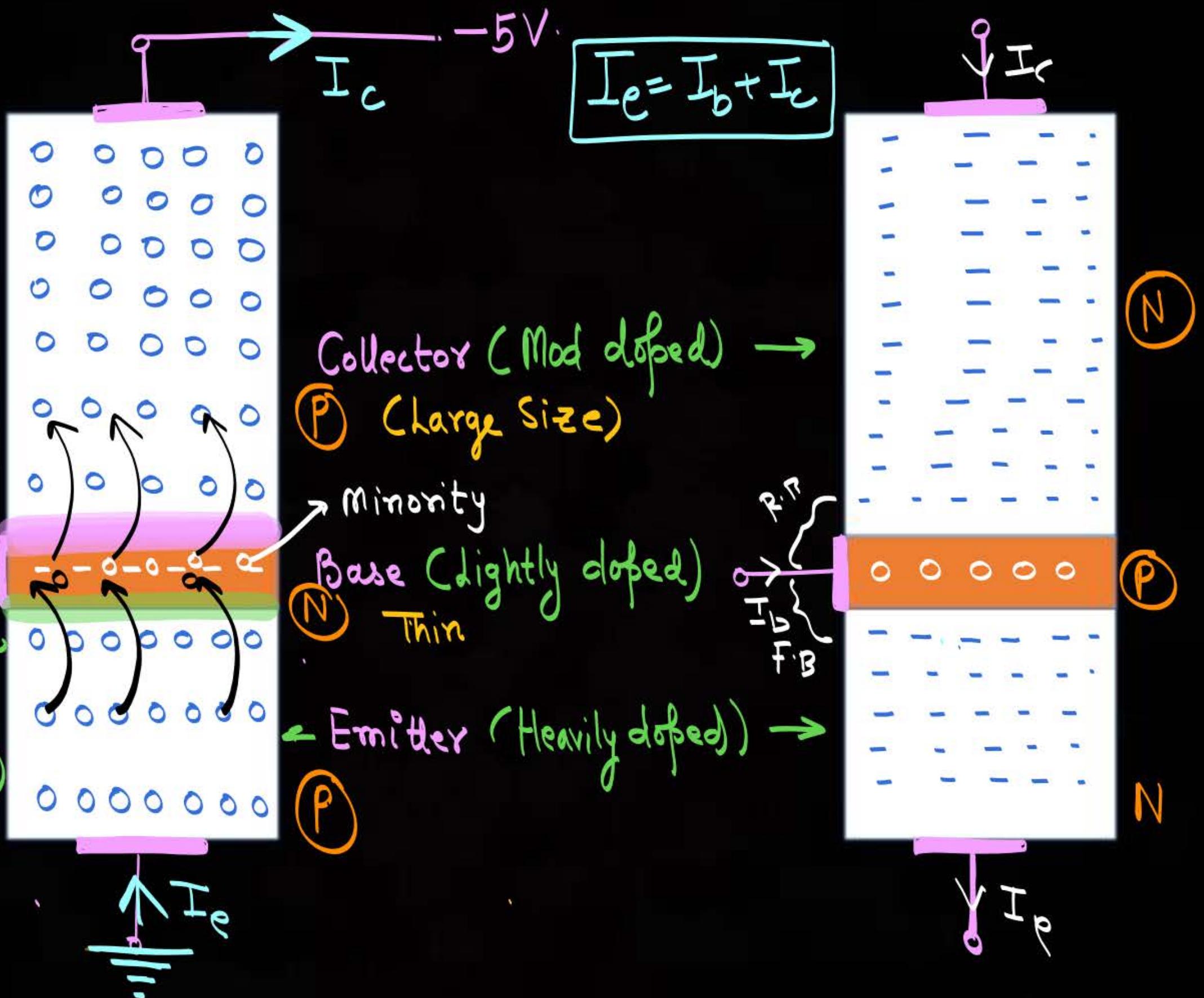
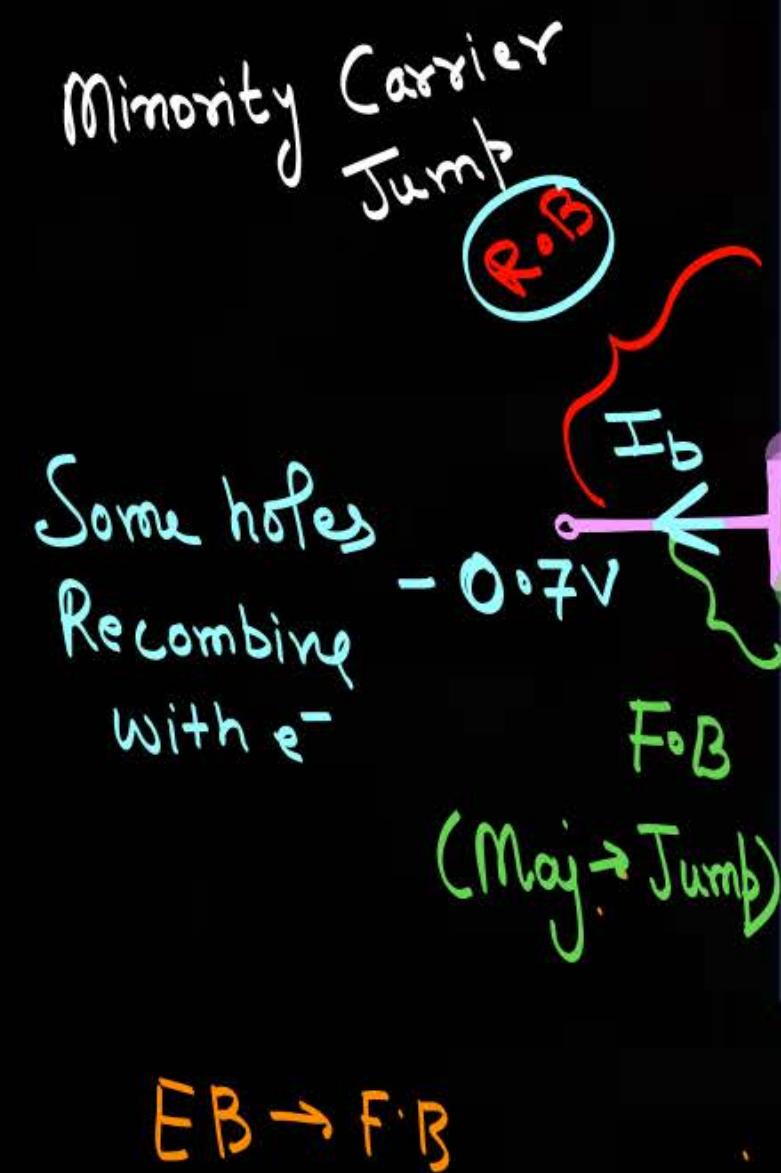
D

Remains constant



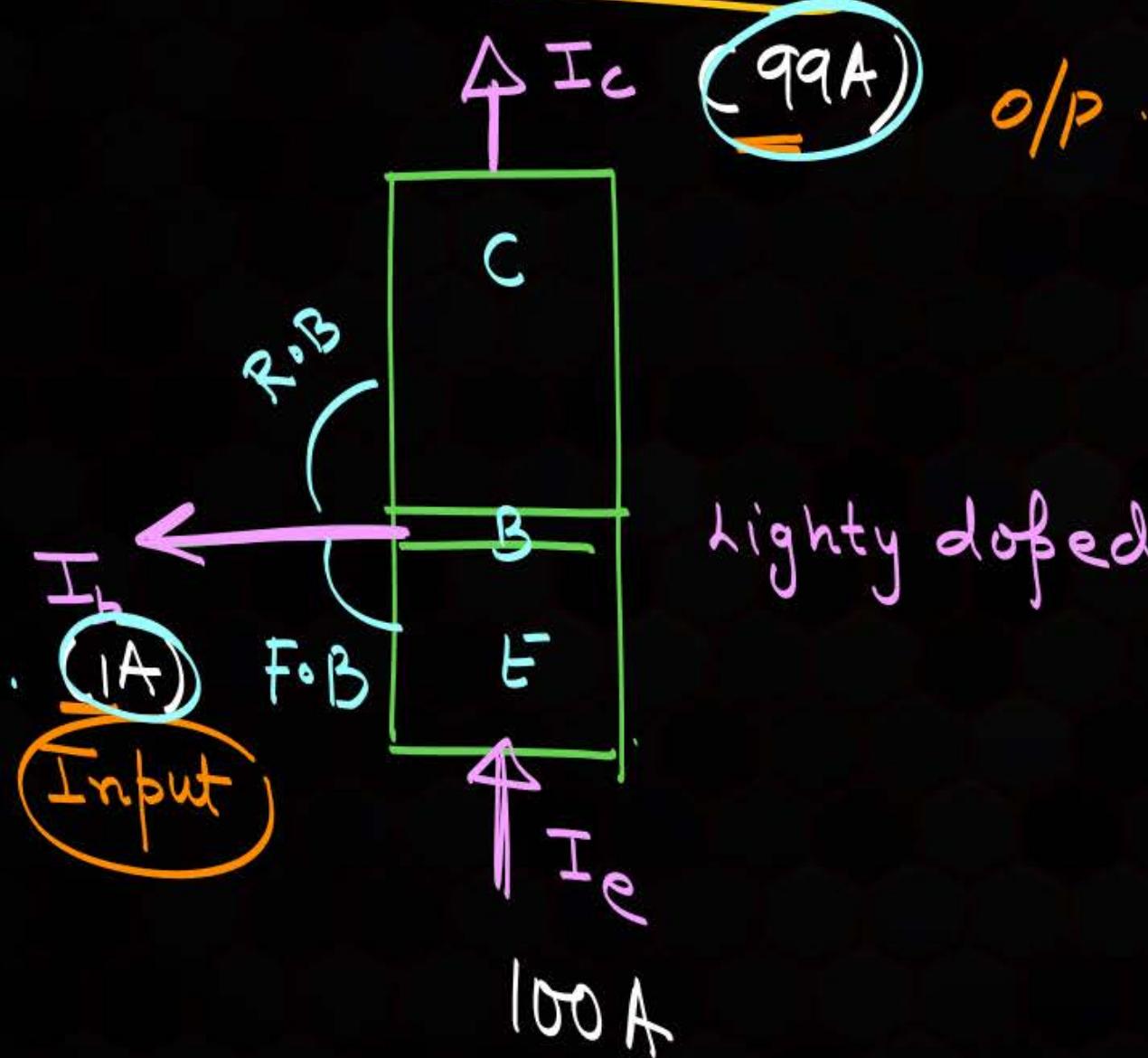
# TRANSISTOR

Two Junction  
Three Terminal diodes.



$$\textcircled{*} \quad I_e = I_b + I_c$$

Always Valid for NPN & PNP

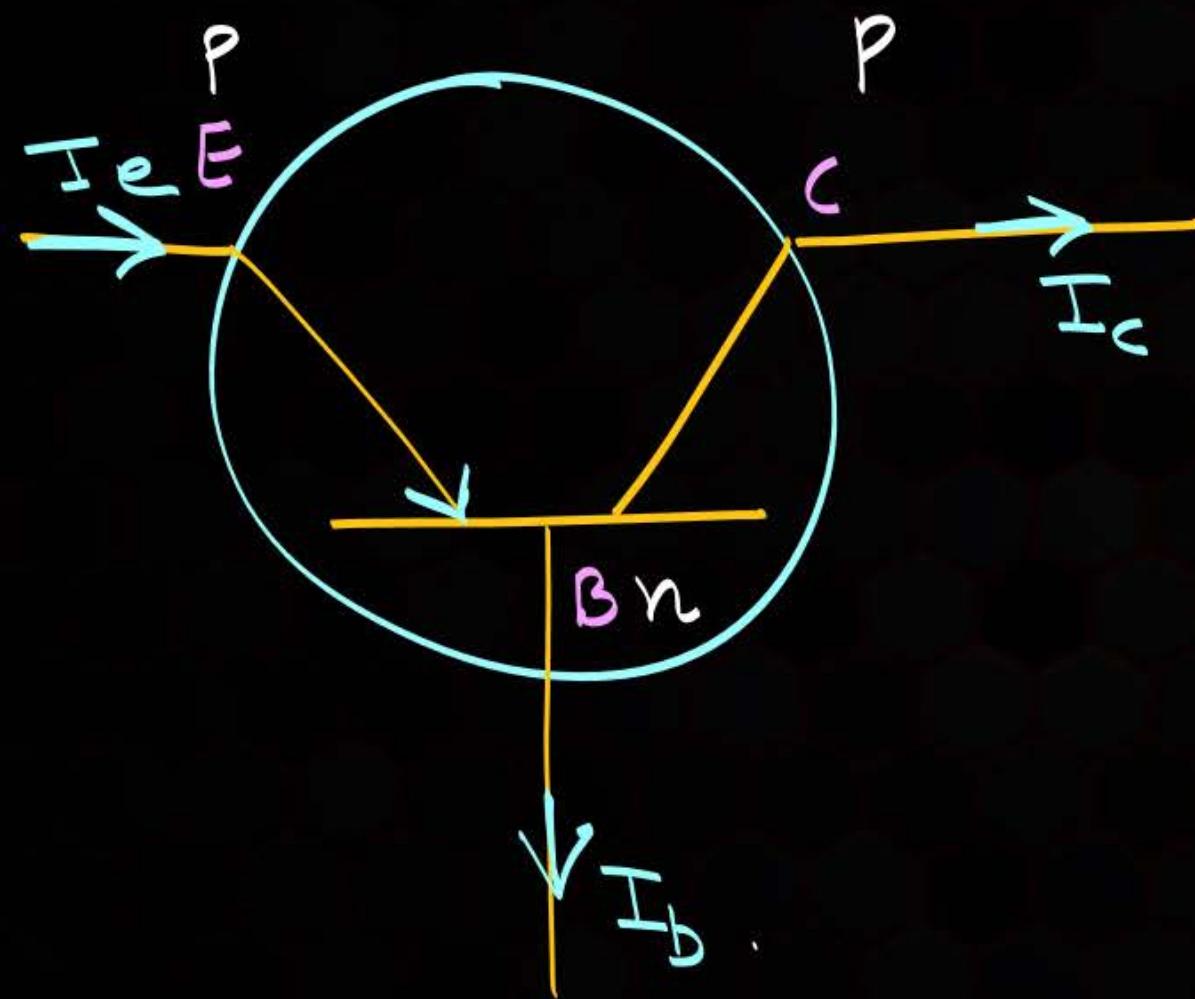


## Transistor

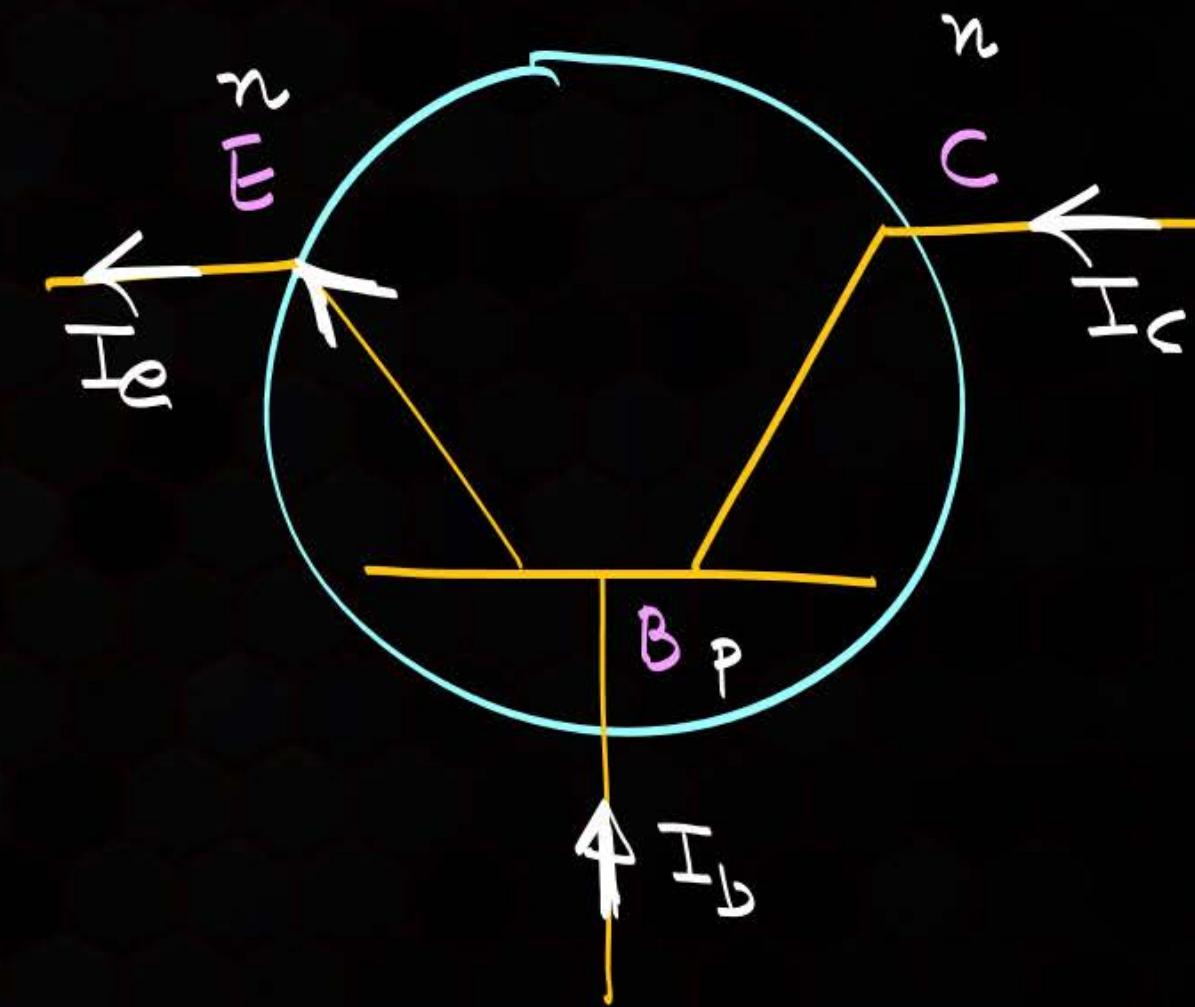
$$I_e = I_b + I_c$$

$$I_b \approx 5\% I_e$$

$$I_c \approx 95\% I_e$$



**PnP**  $P \rightarrow$  Jyada  
 $\rightarrow$  Pravesh

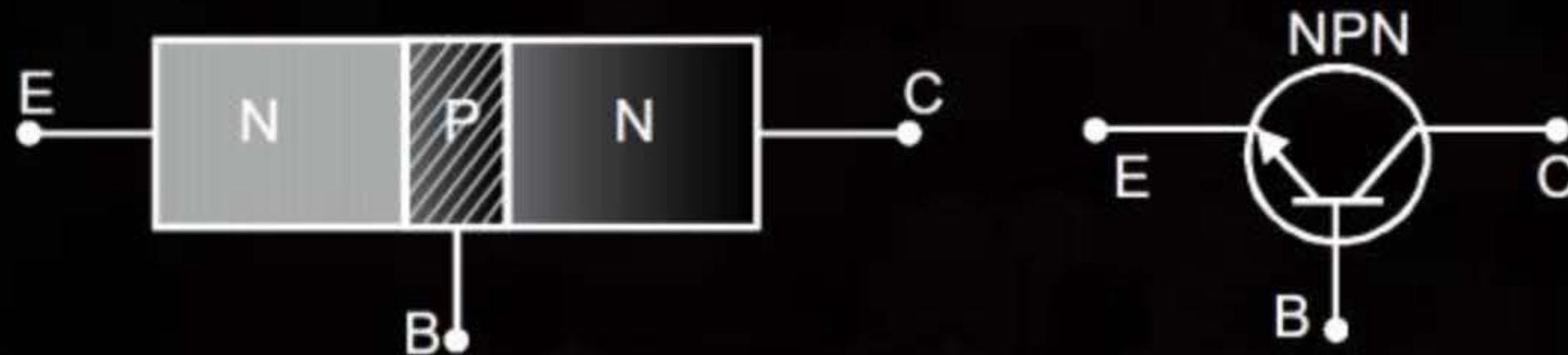


**npn**  $n \rightarrow$  Jada  
- nikau

## Transistors are of two types

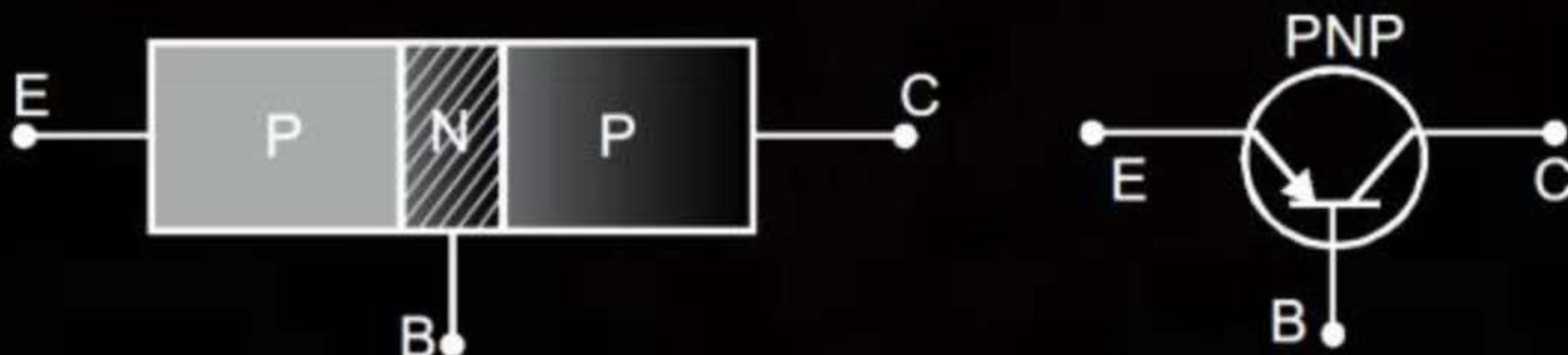
### ❖ N-P-N Transistor

If a thin layer of P-type semiconductor is sandwiched between two thick layers of N-type semiconductor, then it is known as NPN transistor.



### ❖ P-N-P Transistor

If a thin layer of N-type of semiconductor is sandwiched between two thick layer of P-type semiconductor, then it is known as PNP transistor.



Each transistor has three terminals and these are

### (i) Emitter

It is the left most part of the transistor which emits the majority carriers towards base. It is highly doped and medium in size.

### (ii) Base

It is the middle part of transistor which is sandwiched by emitter (E) and collector (C). It is lightly doped and very thin in size.

### (iii) Collector

It is right part of the transistor which collects the majority carriers which is emitted by emitter. It has large size and moderate doping.

- ❖ Transistor have two P-N Junction  $J_{EB}$  and  $J_{CB}$ . On the basis of junction condition transistor work in four regions.

**Emitter-Base**

✓ Forward biased

✓ Reverse biased

Reverse biased

Forward biased

**Collector-Base**

Reverse biased

Forward biased

Reverse biased

Forward biased

**Region of working**

Active

Inverse active

Cut off

Saturation

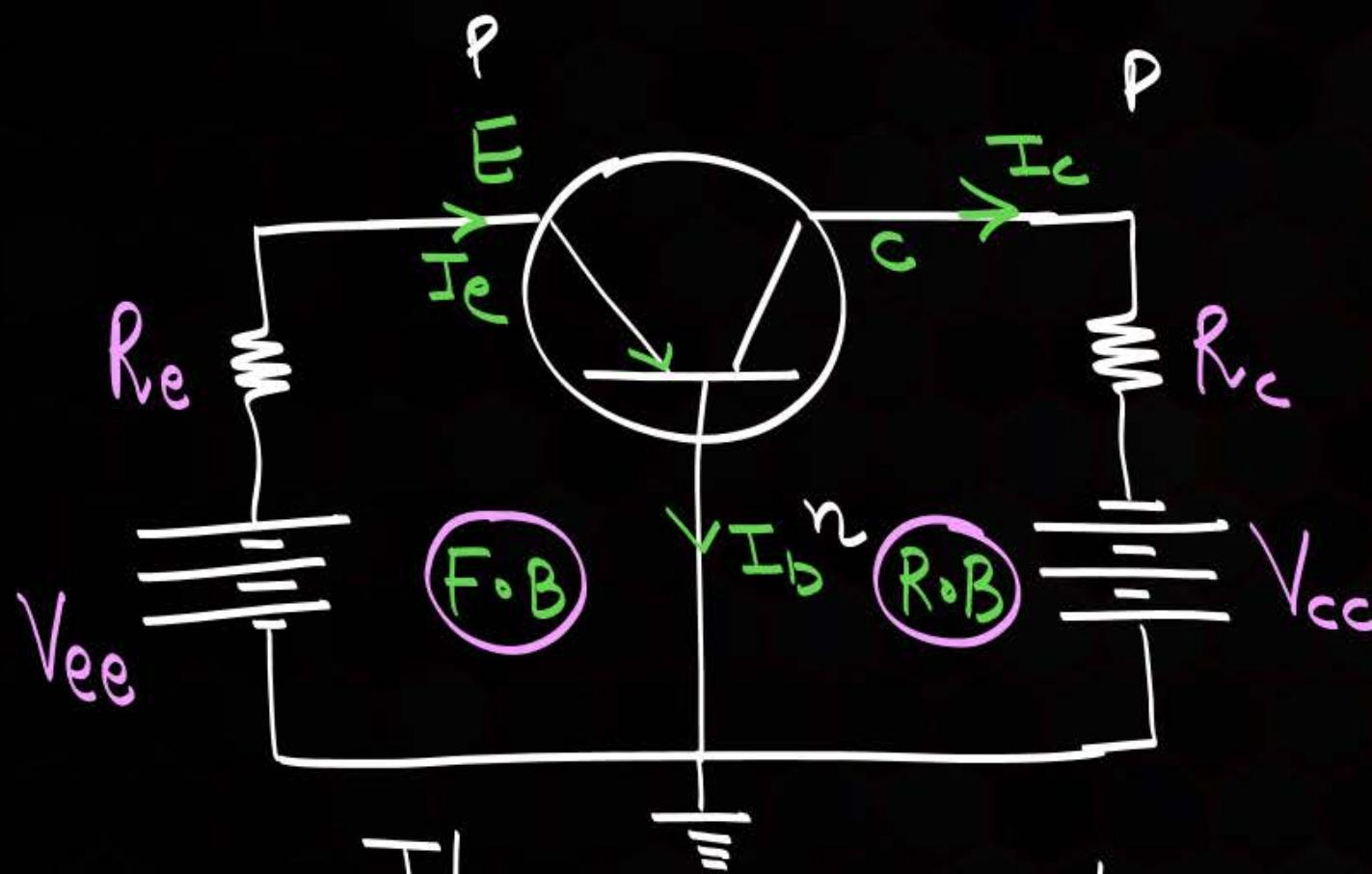
- ❖ The collector region is made physically larger than the emitter. Because collector has to dissipate much greater power.

Input  $\rightarrow F \cdot B$  }      Transistor work  
Output  $\rightarrow R \cdot B$  }

There are two type of CKT

(Prefex)

CB (pnp)

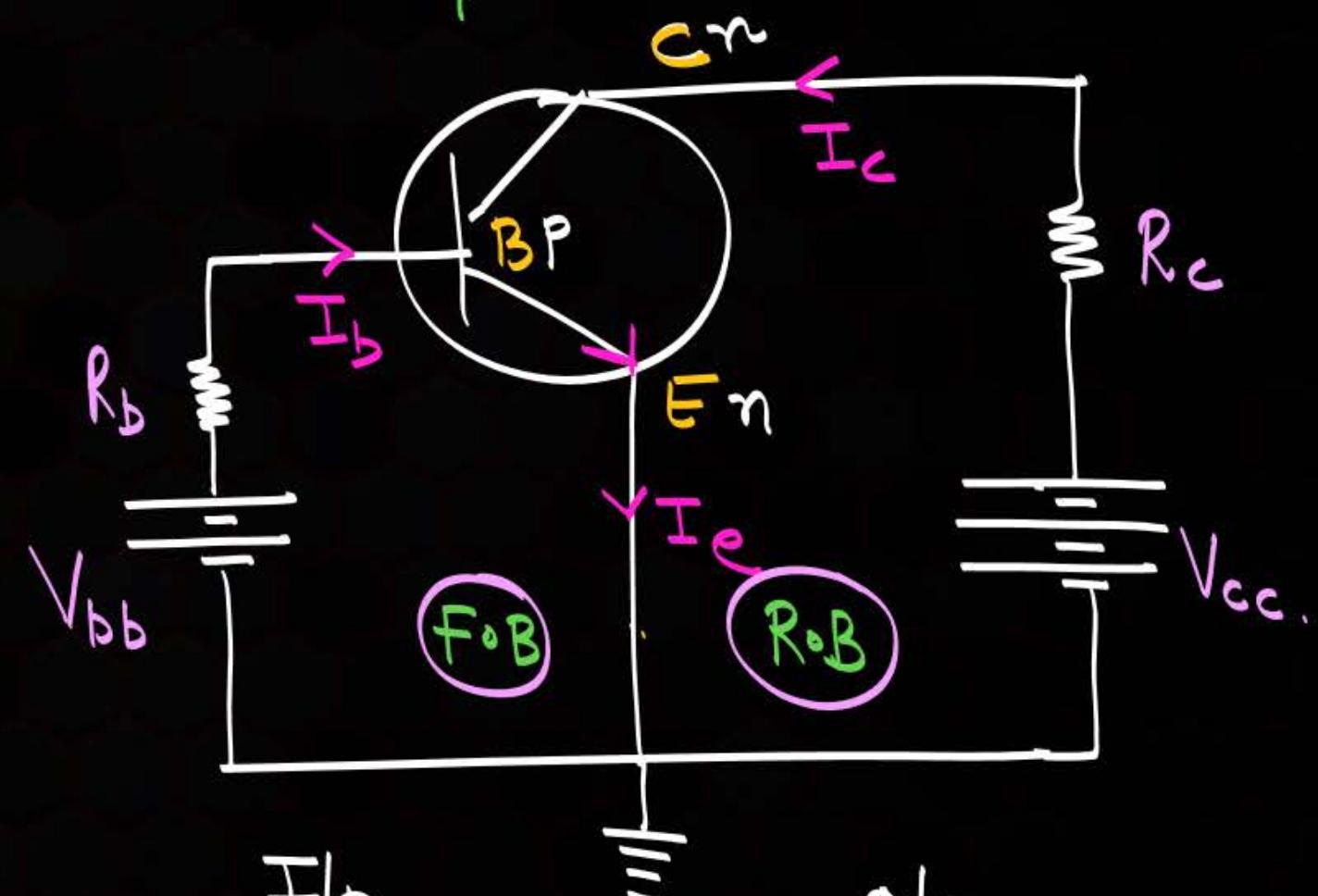


I/P

Emitter

O/P  
Collector

CE (npn)



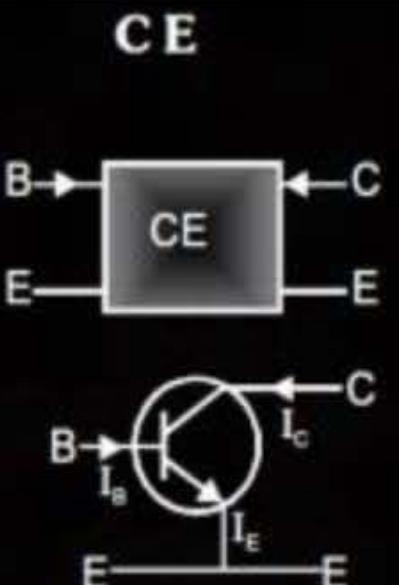
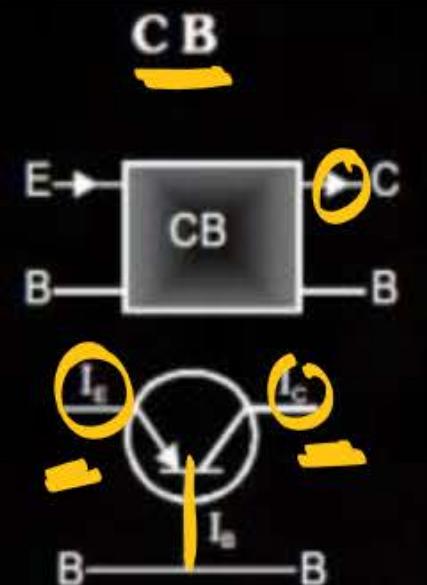
I/P

Input = I<sub>b</sub>

O/P

Collector

Output  
Input



$$P_{\text{gain}} = \frac{P_C}{P_i}$$

**Power Gain**

$$A_p = \frac{P_o}{P_i}$$

$$A_p = \alpha^2 \frac{R_L}{R_i}$$

$$A_p = \frac{P_o}{P_i}$$

$$A_p = \beta^2 \frac{R_L}{R_i}$$

**Phase difference  
(between output  
and input)**

same phase

opposite phase

Current Gain

( $A_i$  or  $\alpha$ )

$$\alpha_{v,i} = \frac{I_c}{I_e}$$

( $A_i$  or  $\beta$ )

$$\beta = \frac{I_c}{I_b}$$

Voltage Gain

$$A_v = \frac{V_o}{V_i} = \frac{I_c R_L}{I_e R_i}$$

$$A_v = \alpha \frac{R_L}{R_i}$$

$$A_v = \frac{V_o}{V_i} = \frac{I_c R_L}{I_b R_i}$$

$$A_v = \beta \frac{R_L}{R_i}$$

$$R_L = \text{load } R \rightarrow R_C$$

$$R_i = \text{Input } R$$

$$\frac{V_C}{I_E} = \frac{I_C R_C}{I_E R_P}$$

Relation between  $\alpha$  &  $B$

$$\begin{array}{c} \Downarrow \\ CB \\ \Downarrow \\ CE \end{array}$$

$$\alpha = \frac{I_c}{I_e} \quad B = \frac{I_c}{I_b}$$

$$\frac{I_e}{I_c} = \frac{I_b}{I_c} + \frac{I_c}{I_c}$$

$$\frac{1}{\alpha} = \frac{1}{B} + 1$$

$$\frac{1}{\alpha} = \frac{1}{B} + 1$$

$$\boxed{\alpha = \frac{B}{B+1}}$$

$$\frac{1-\alpha}{\alpha} = \frac{1}{B}$$

$$\boxed{\frac{\alpha}{1-\alpha} = B}$$

# Transistor as a switch

In o/p KVL

$$V_o = V_{CE} = V_{CC} - I_c R_c$$

Si based Transistor

$$V_i < 0.7V$$

$$V_i > 0.7V$$

$V_i$  High

$$F \cdot B \times I_b = 0 \quad I_c = 0$$

$$I_i \neq F \cdot B \quad I_b \neq 0 \quad I_c \neq 0$$

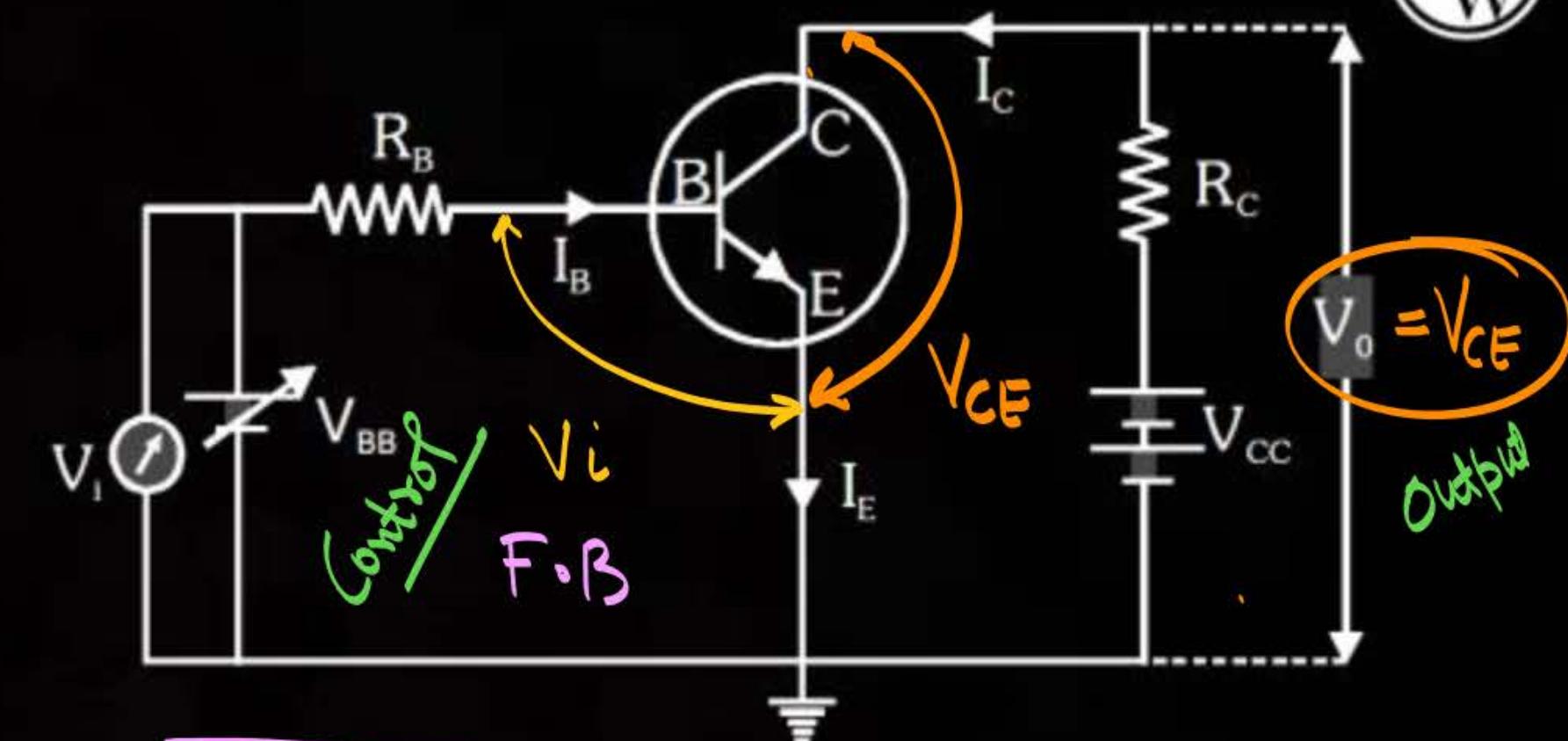
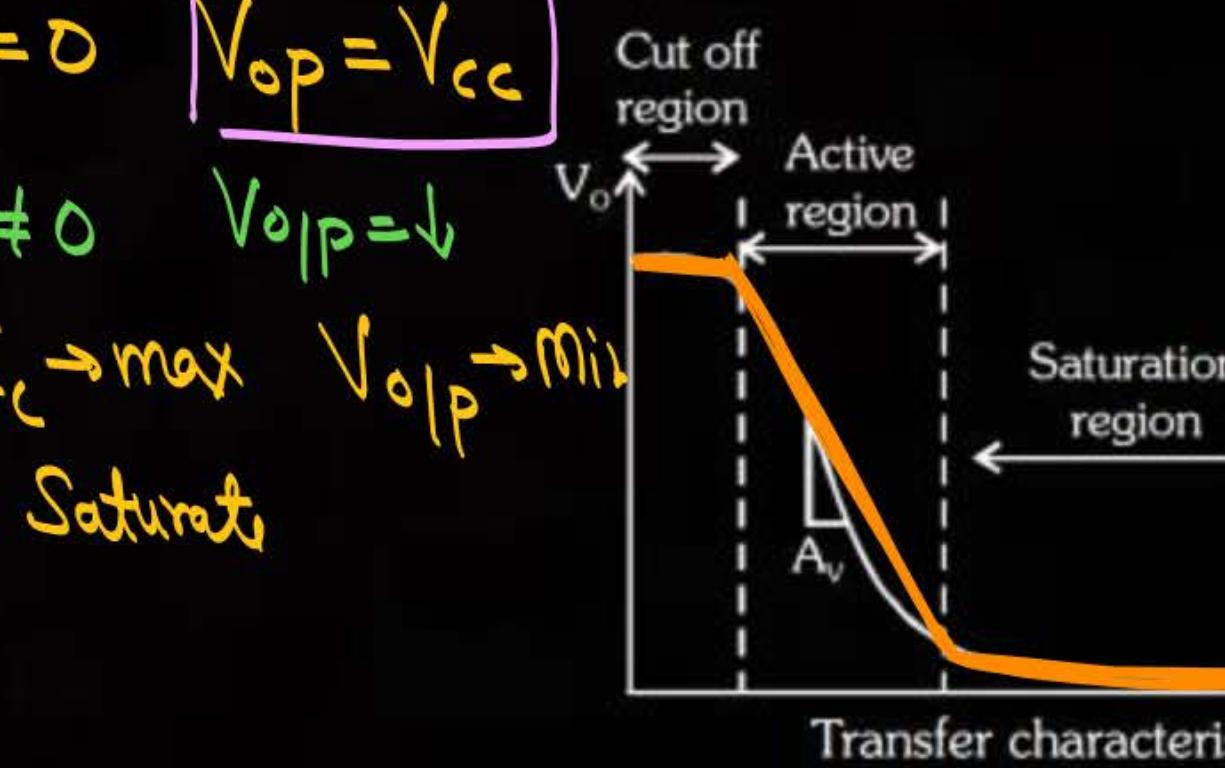
$$I_i \neq F \cdot B \quad I_b \rightarrow \max \quad I_c \rightarrow \min$$

$$V_{OP} = V_{CC}$$

$$V_{O/P} = 0$$

$$V_{O/P} \rightarrow \text{Min}$$

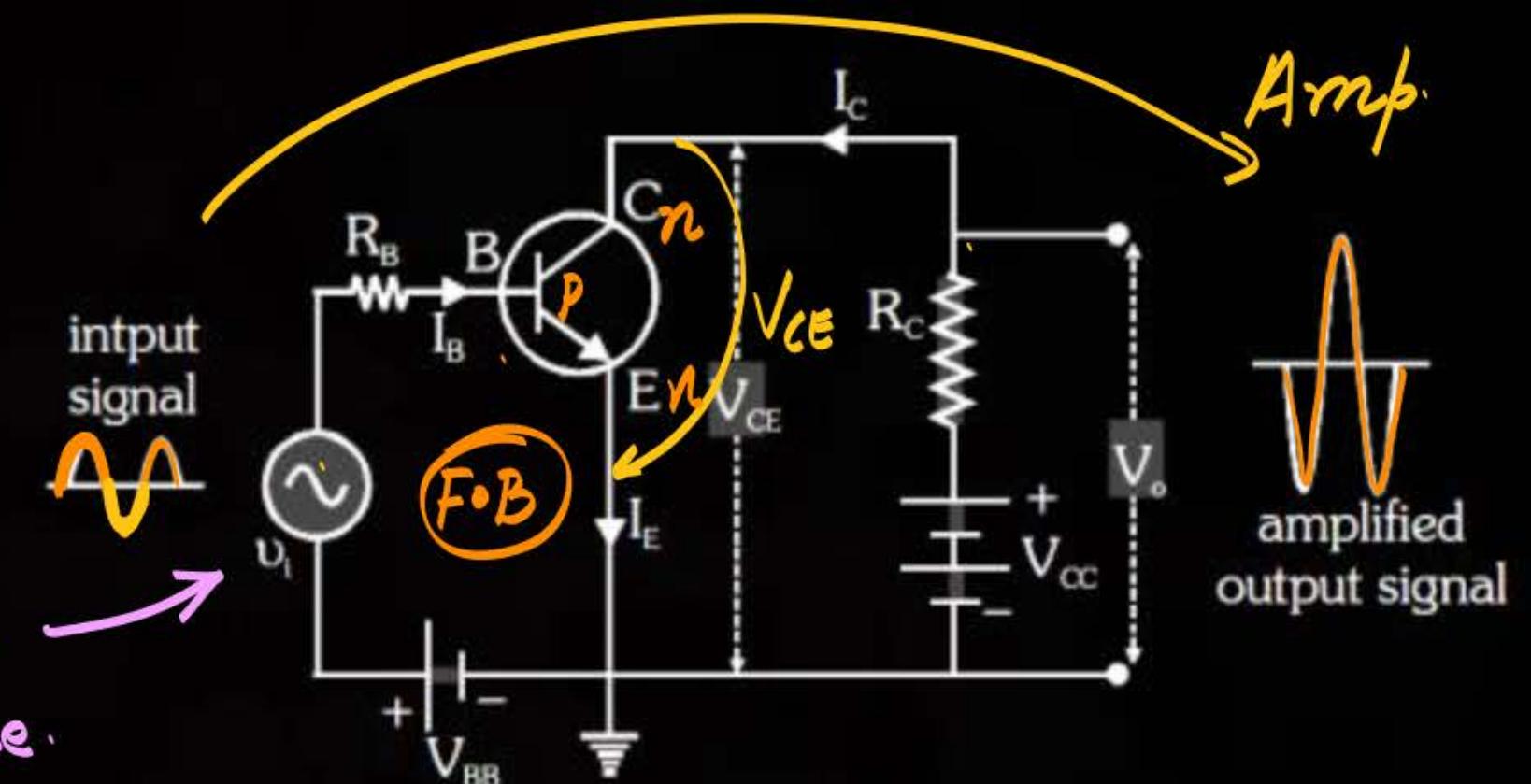
Saturation



# Transistor as an amplifier

Phase diff =  $\pi$  CE

AC Source at Input Side.

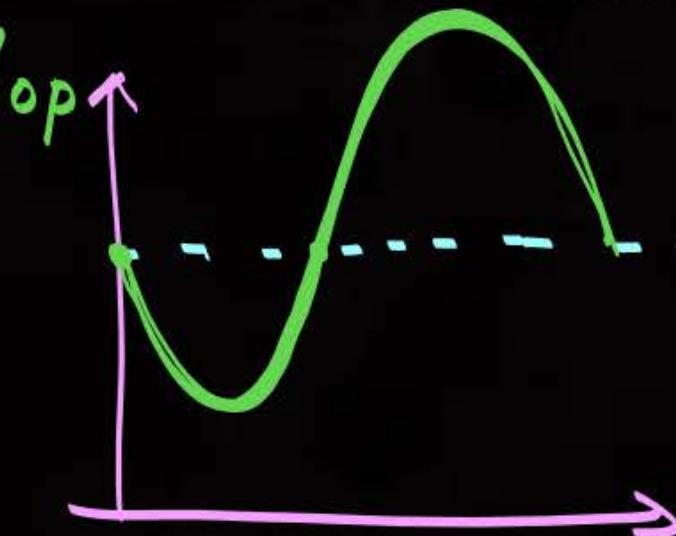


common emitter amplifier NPN transistor

$$V_{o/p} = V_{cc} - I_c R_c = V_{CE}$$

for particular  $I_b$

Now we have applied AC Source.

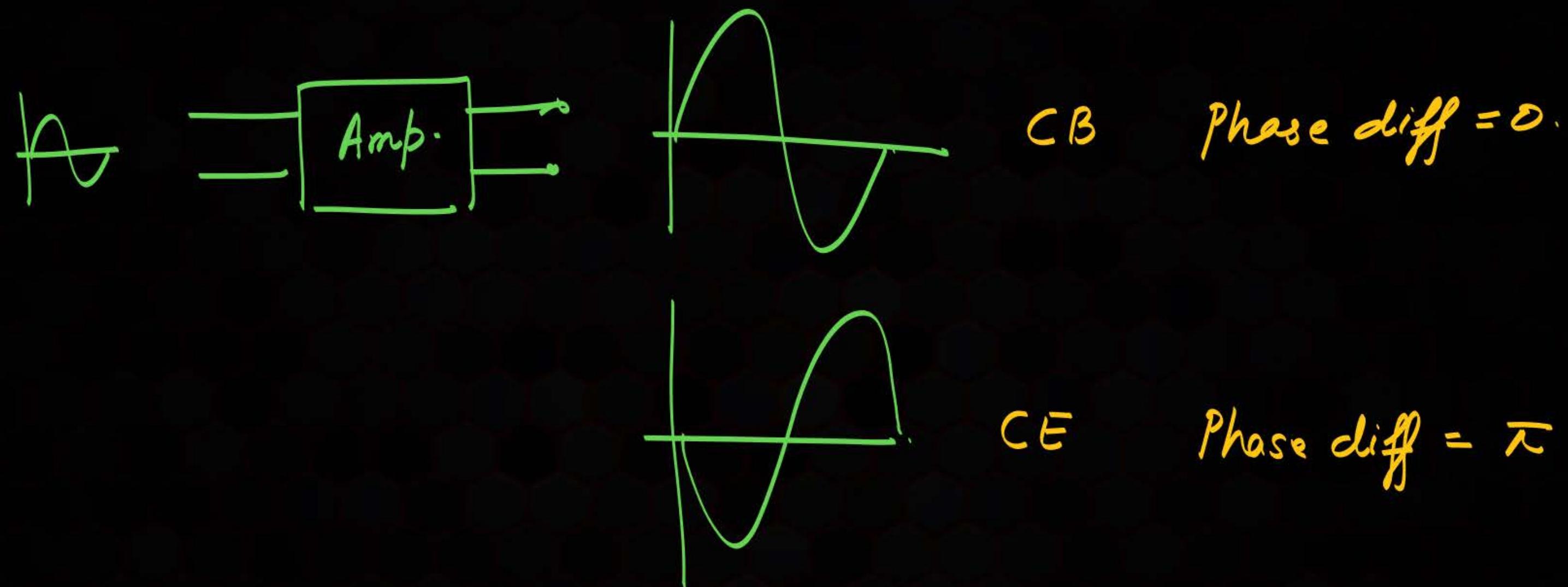


CE

PHC B (+ve) ↑ F·B ↑

$I_b \uparrow$   
 $I_c \uparrow$

NHC  $V_{op} = \downarrow$   
F·B ↓  $I_b \downarrow$   $I_c \downarrow$



Q.

For a transistor in CE mode to be used as an amplifier, it must be operated in :  
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A

Both cut-off and Saturation

B

Saturation region only

C

Cut-off region only

D

The active region only

$$I_o \rightarrow F \cdot B$$

$$O_i \rightarrow R \cdot B$$

Q.

For a transistor  $\alpha$  and  $\beta$  are given as  $\alpha = \frac{I_C}{I_E}$  and  $\beta = \frac{I_C}{I_B}$ . Then the correct relation between  $\alpha$  and  $\beta$  will be :

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(4 times)

**A**  $\alpha = \frac{1 - \beta}{\beta}$

**B**  $\beta = \frac{\alpha}{1 - \alpha}$  *Ans*

**C**  $\alpha\beta = 1$

**D**  $\alpha = \frac{\beta}{1 - \beta}$

*(CB)*  $\alpha = \frac{I_C}{I_E}$

$$\alpha = \frac{\beta}{\beta + 1}$$

*(E)*  $\beta = \frac{I_C}{I_B}$

$$\beta = \frac{\alpha}{1 - \alpha}$$

Q.

If an emitter current is changed by 4 mA, the collector current changes by 3.5 mA. The value of  $\beta$  will be :

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A 0.875

B 0.5

C 3.5

D 7 Ans

$$\Delta I_e = 4 \text{ mA}$$

$$\Delta I_c = 3.5 \text{ mA}$$

$$(CE) = \beta = \frac{\Delta I_c}{\Delta I_b} = \frac{3.5 \text{ mA}}{0.5 \text{ mA}}$$

$$\bar{I}_e = \bar{I}_b + I_c$$

$$\Delta I_e = \Delta I_b + \Delta I_c$$

$$4 = \Delta I_b + 3.5$$

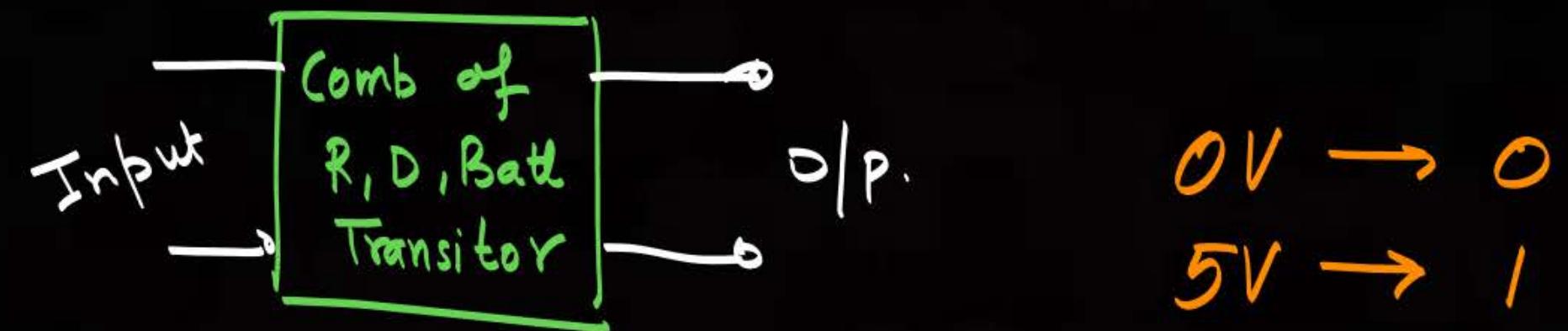
$$0.5 = \Delta I_b$$



## LOGIC GATES



Logical Relation follows.



$$\begin{aligned} 0V &\rightarrow 0 \\ 5V &\rightarrow 1 \end{aligned}$$



## BASIC LOGIC GATES

Basic Gates  $\rightarrow$  OR, AND, NOT

Universal Gates :- NAND, NOR

Special Gates = EXOR, EX-NOR.

**OR**



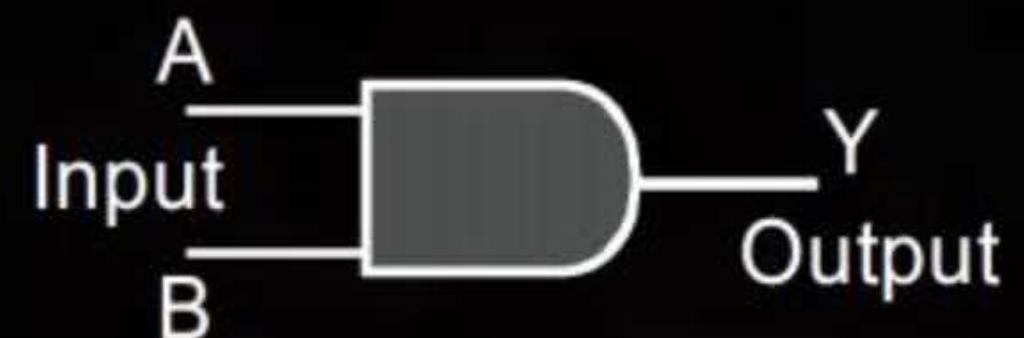
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Truth table

Koi bhi  
Input /  
hua toh  
O/P - 1

$$Y = A + B$$

**AND**



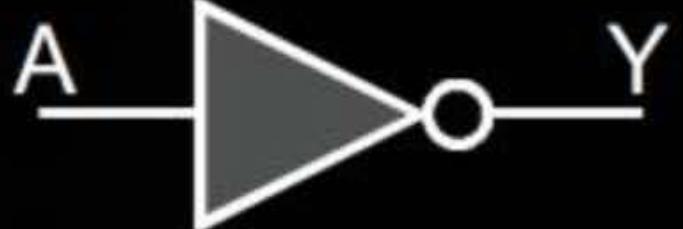
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

Truth table

Jab dono /  
honge tabhi  
O/P - 1 hogta.

$$Y = A \cdot B$$

**NOT**



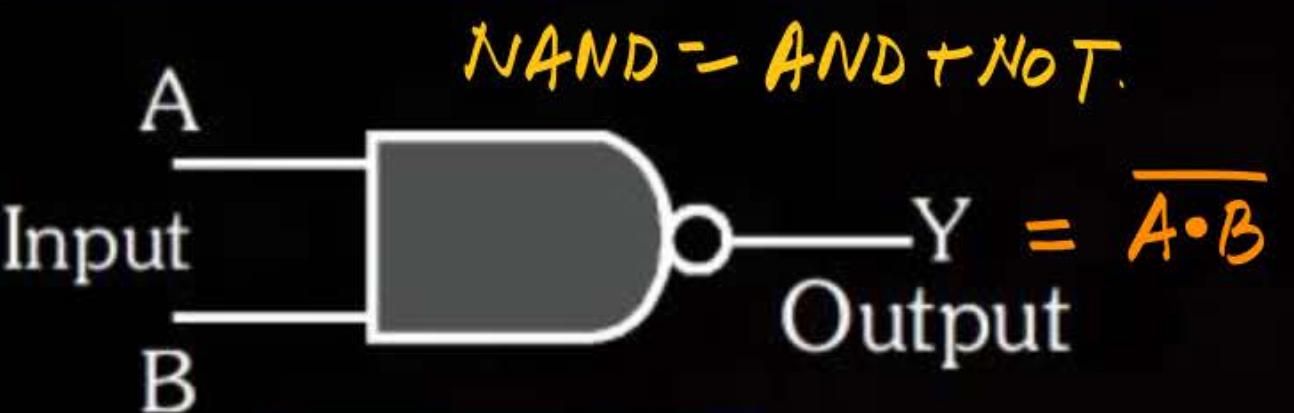
A	Y
0	1
1	0

Truth  
table.

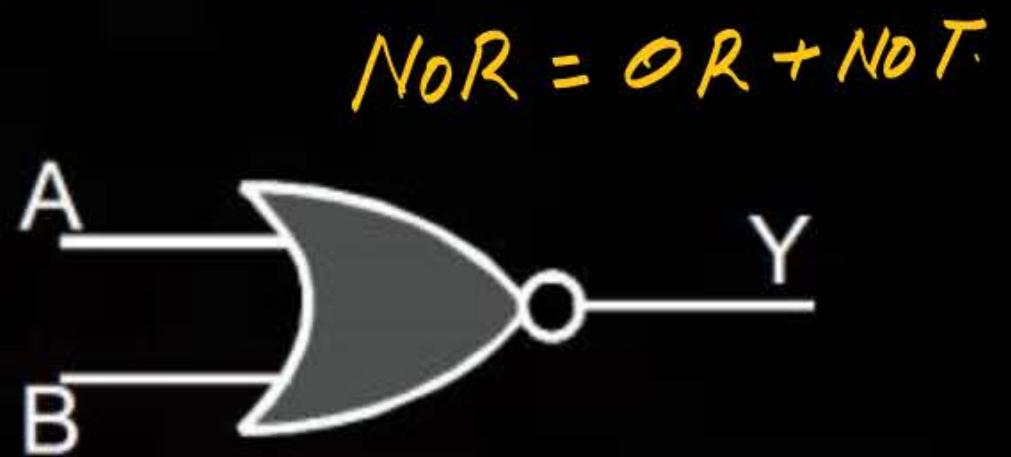
$$Y = \bar{A}$$



## Combination of Gates:



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0



# Laws of Boolean Algebra:

OR	AND	NOT
$A + 0 = A$ ✓ $\boxed{A + 1 = 1}$ $\begin{array}{r} 0+1=1 \\ \downarrow \\ 1+1=1 \end{array}$ $\boxed{A + A = A}$ $\begin{array}{r} 0+0=0 \\ \downarrow \\ 1+1=1 \end{array}$	$A \cdot 0 = 0$ $A \cdot 1 = A$ $\boxed{A \cdot A = A}$	$A + \bar{A} = 1$ $A \cdot \bar{A} = 0$ $\bar{\bar{A}} \cdot A = A$ $\downarrow$ $A \cdot A = A$
		$A = 1 \quad 1 + 0 = 1$ $A = 0 \quad 0 + 1 = 1$ $\bar{A} = A \quad \bar{\bar{A}} = A$

$$(i) A + AB = A [1 + B] = A \cdot 1 = A$$

$$(ii) A \cdot (A + B)$$

$$= A \cdot A + A \cdot B$$

$$A + A \cdot B = A [1 + B] = A.$$

## ❖ De Morgan's theorem :

First theorem :  $\overline{A + B} = \bar{A} \cdot \bar{B}$

Second theorem :  $\overline{A \cdot B} = \bar{A} + \bar{B}$

(+)  $\rightleftharpoons$  •

Break the Line  
Change the Sign

The combination of the gates shown will produce

Q.

A

AND gate  $\times$

B

NAND gate  $\times$

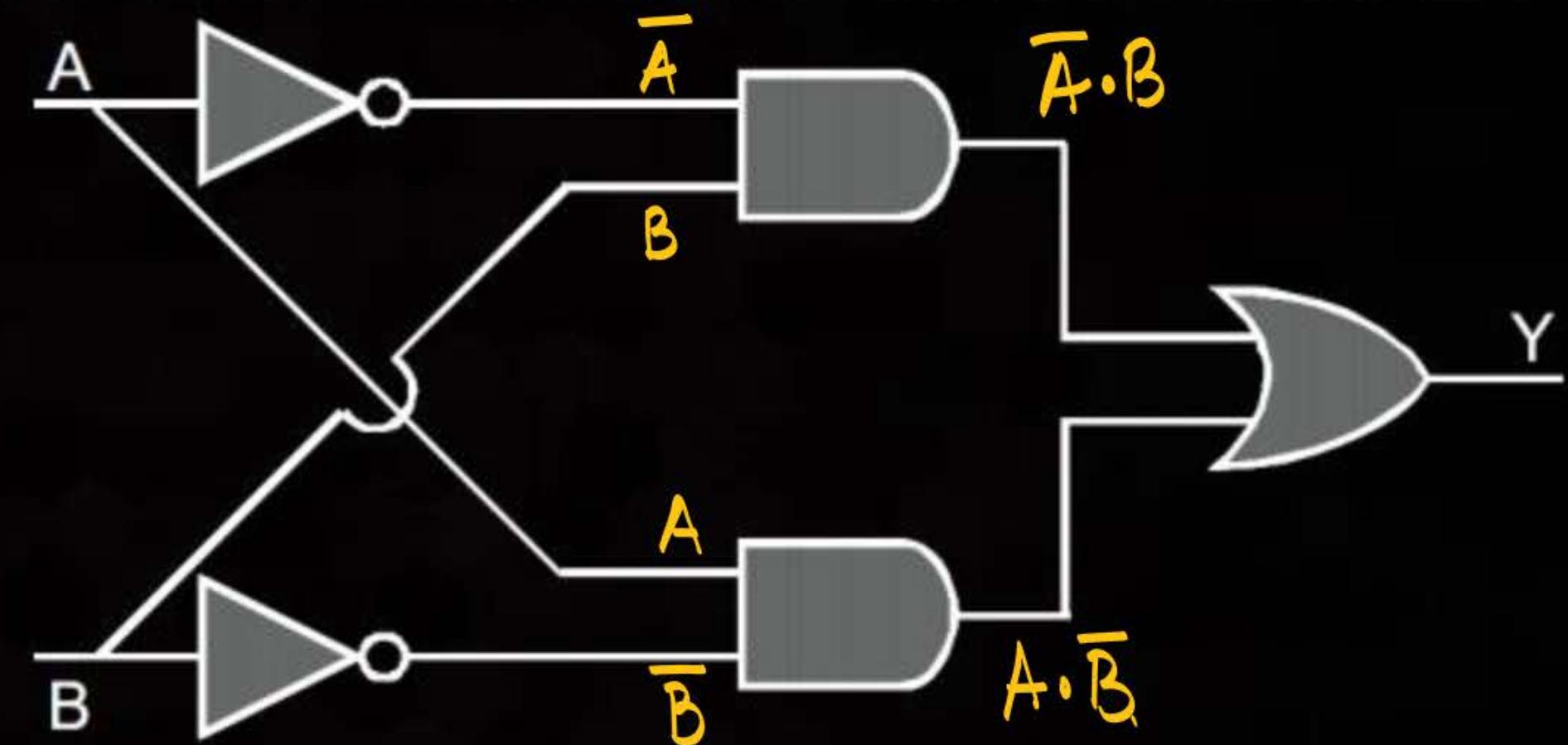
C

NOR gate  $\times$

D

XOR gate  $\cancel{Ans}$

Exclusively OR.



$$Y = \bar{A}B + A\bar{B}$$

X-OR

EX-OR

Exclusively OR



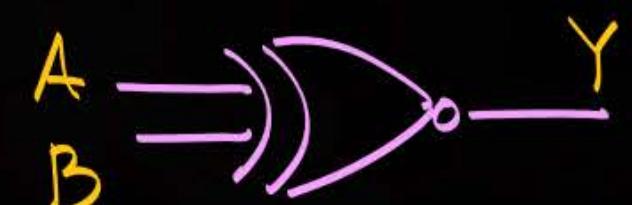
$$Y = \bar{A}B + \bar{B}A$$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

dono mein se koi bhi  
ek 1 hua  
tabhi  
 $O/P = 1$  hogा

$$Y = A \oplus B$$

Ex - NOR



$$Y = A \odot B$$

$$Y = AB + \bar{A}\bar{B}$$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

To get an output 1, the input ABC should be :

Q.

101

Ans

A

100

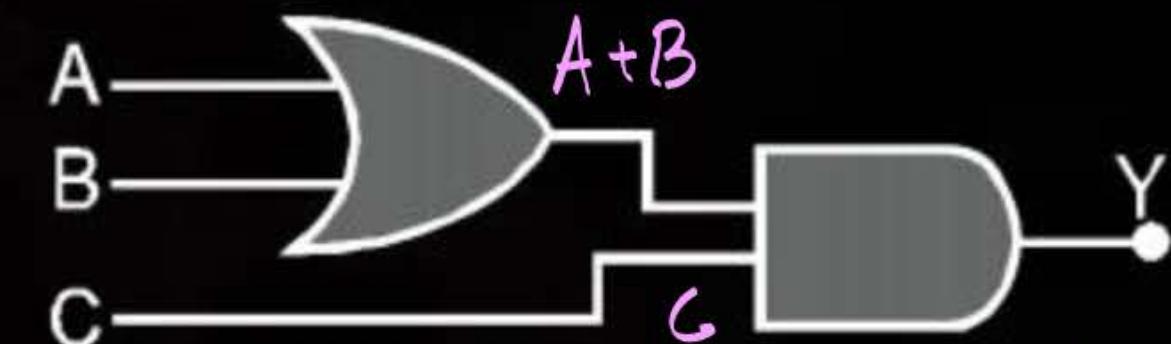
B

110

C

010

D



$$Y = (A + B) \cdot C$$

a)  $Y = (1 + 0) \cdot 1$

$$= 1 \cdot 1$$

$$= 1$$

b)  $(1 + 0) \cdot 0$

$$= 1 \cdot 0$$

$$= 0$$

Q.

Find the truth table for the function Y of A and B represented in the following figure.

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A	B	Y
0	0	0
0	1	1
1	0	0
1	1	0

~~A~~

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	1

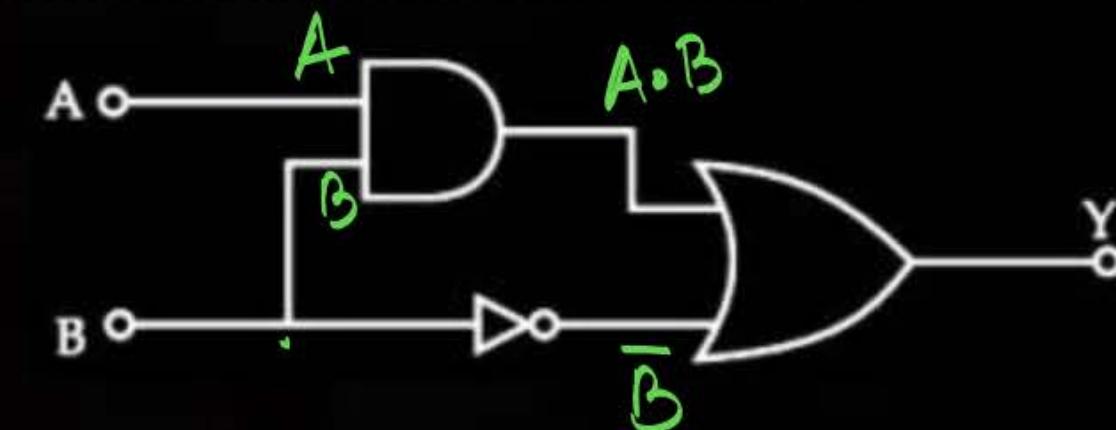
~~B~~

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

~~C~~

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

~~D~~



$$Y = A \cdot B + \bar{B}$$

a)

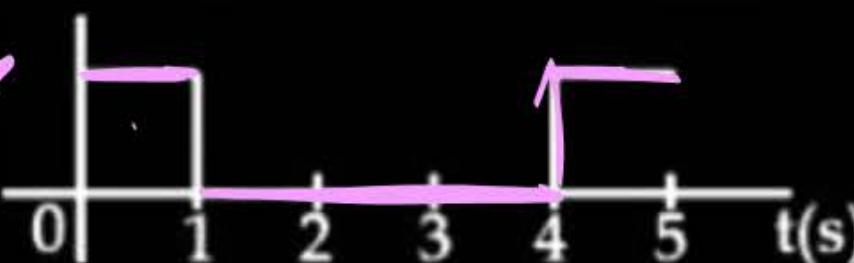
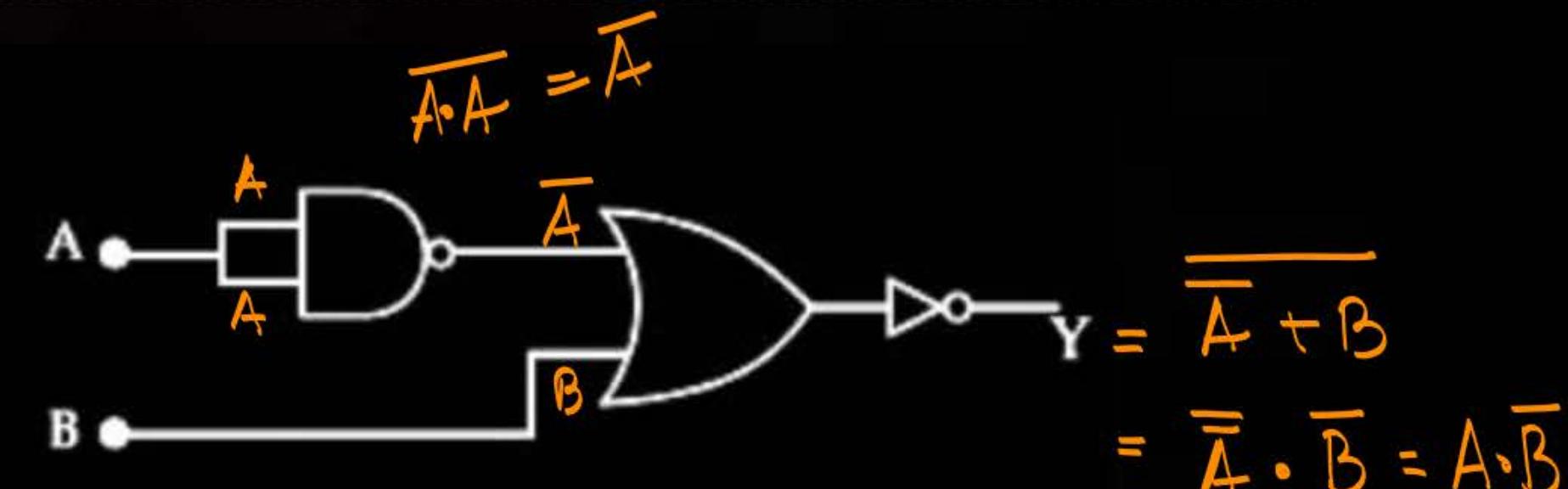
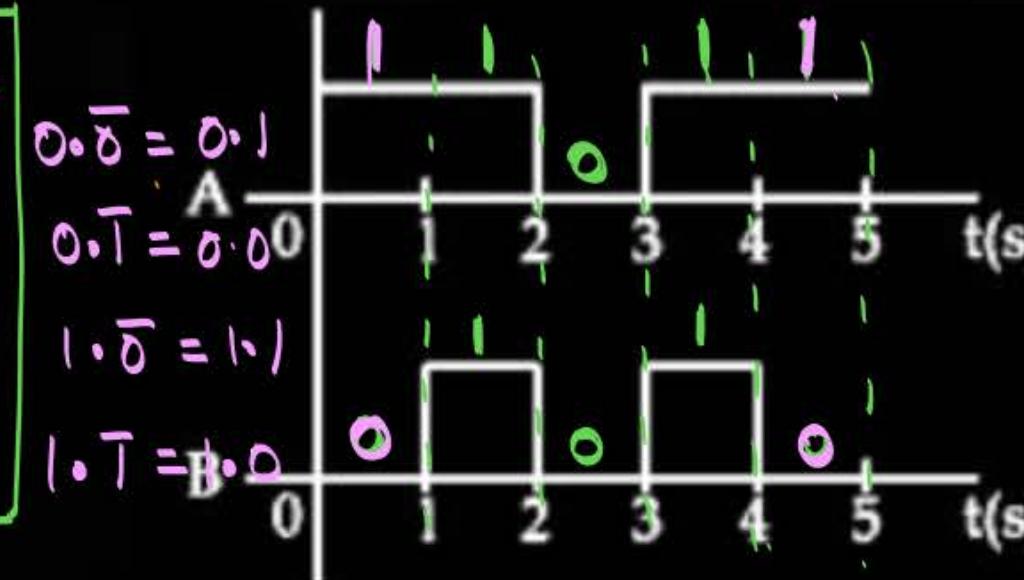
A	B
0	0
0	1
1	0
1	1

$$\begin{aligned} & 0 \cdot 0 + \bar{0} \\ & = 0 + 1 = 1 \end{aligned}$$

Draw the output signal Y in the given combination of gates.

JEE Main 2021 (Online) 26<sup>th</sup> February Evening Shift

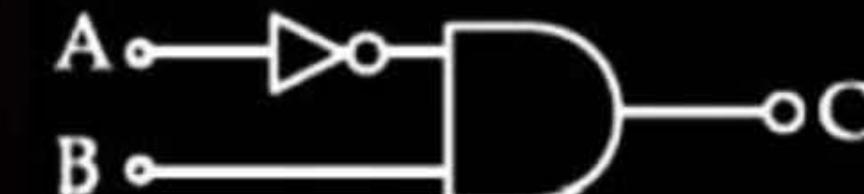
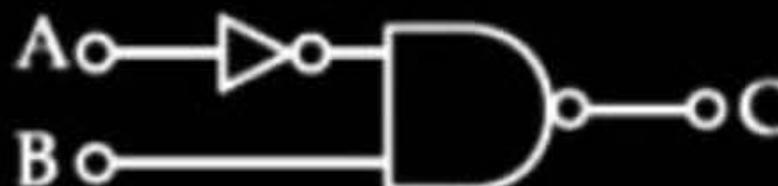
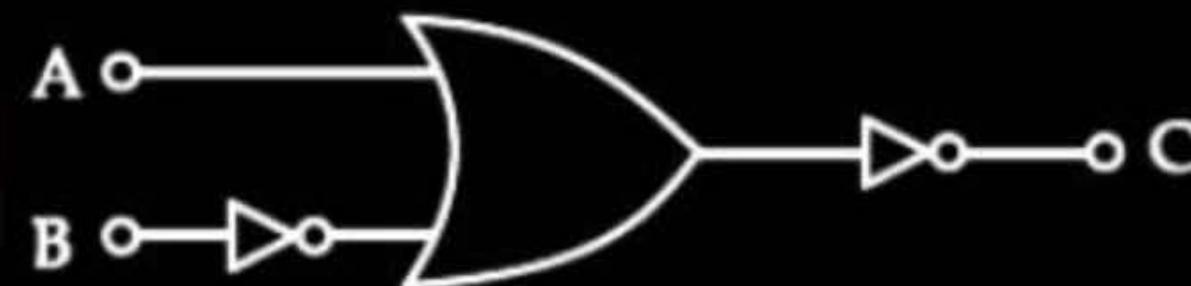
A	B	Y
0	0	0
0	1	0
1	0	1
1	1	0



Q.

The logic circuit shown above is equivalent to :

JEE Main 2021 (Online) 24<sup>th</sup> February Evening Slot

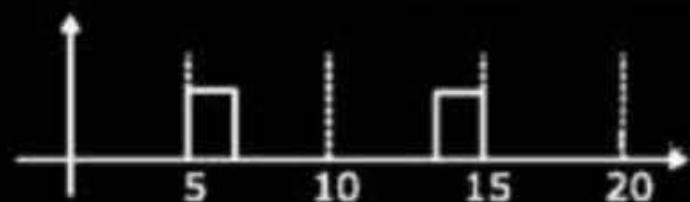


Q.

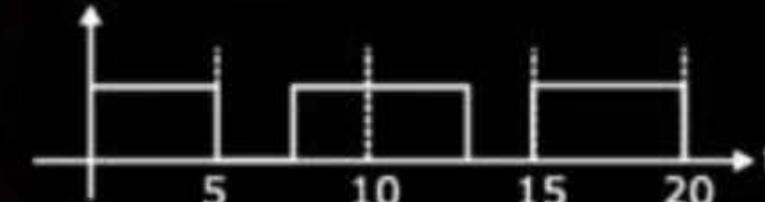
Identify the correct output signal Y in the given combination of gates (as shown) for the given inputs A and B

JEE Main 2020 (Online) 6<sup>th</sup> September Morning Slot

A



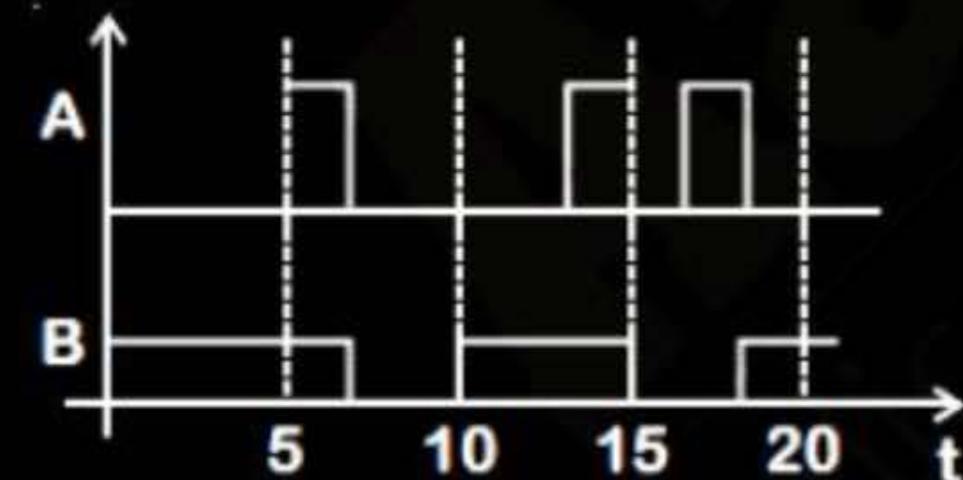
B



C



D



The logic symbols shown here are logically equivalent to

Q.

A

B

C

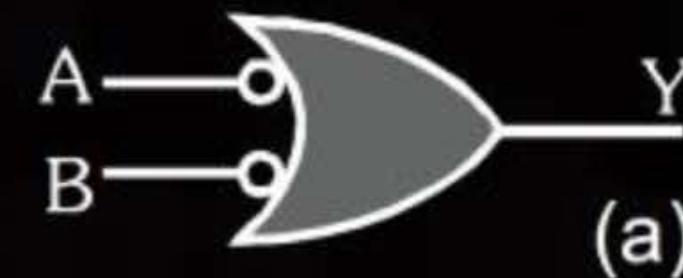
D

- (a) AND and (b) OR gate

- (a) NOR and (b) NAND gate

- (a) OR and (b) AND gate

- (a) NAND and (b) NOR gate



(a)



(b)

Q.

In the given circuit, value of Y is :

JEE Main 2020 (Online) 8<sup>th</sup> January Evening Slot

A

Toggles between 0 and 1

B

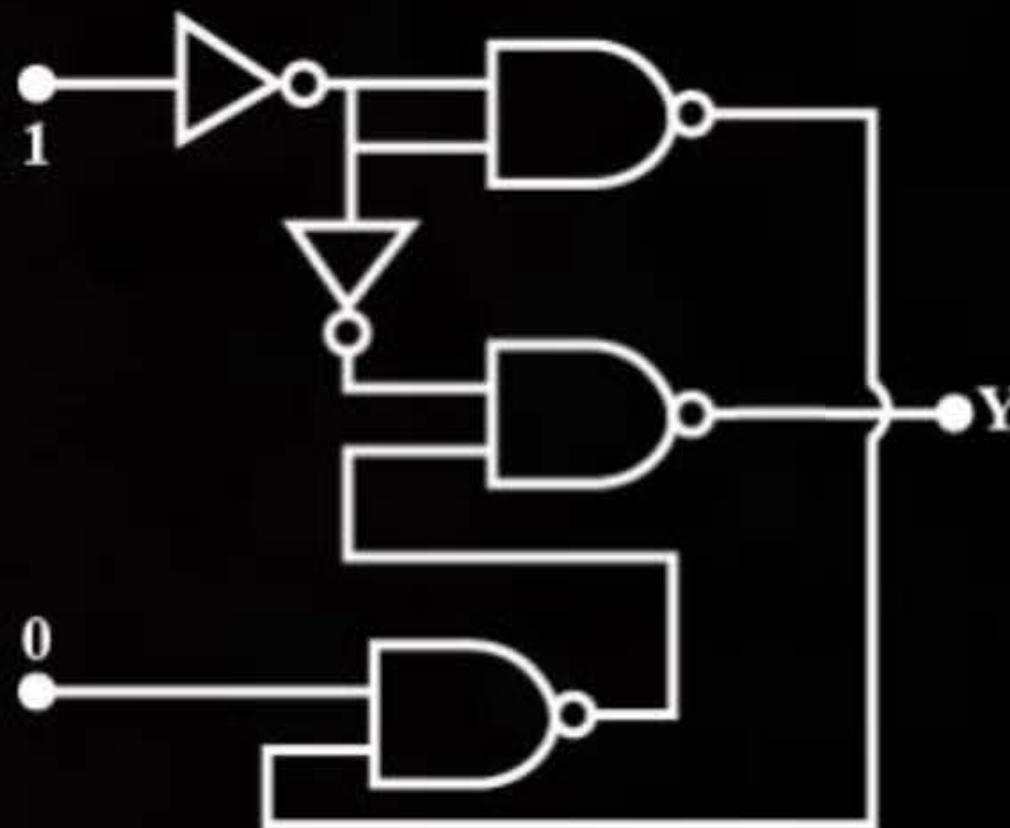
1

C

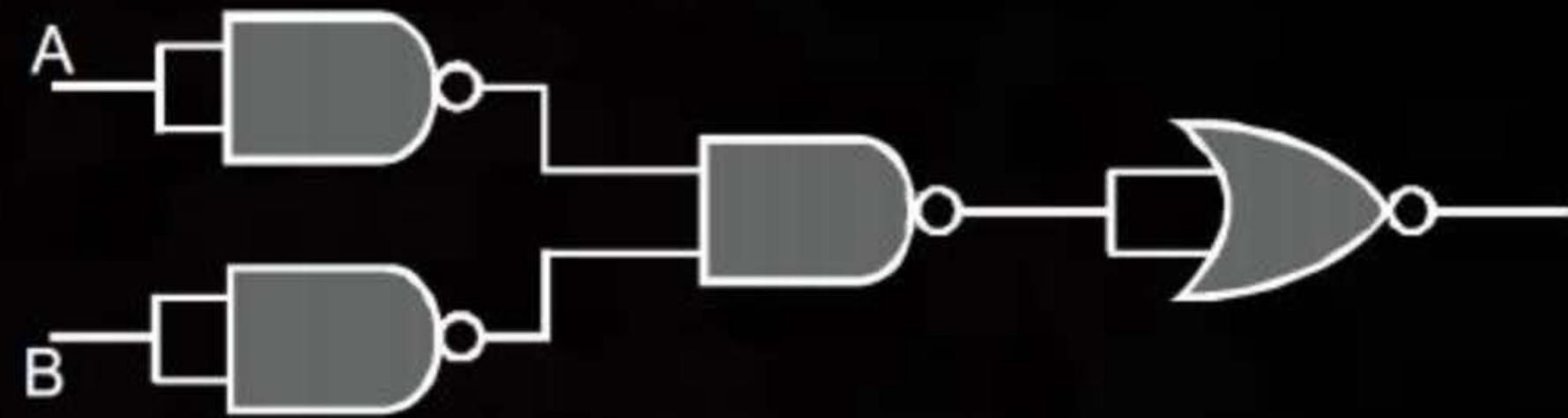
will not execute

D

0



The combination of the gates shown will produce



A OR gate

B AND gate

C NOR gate

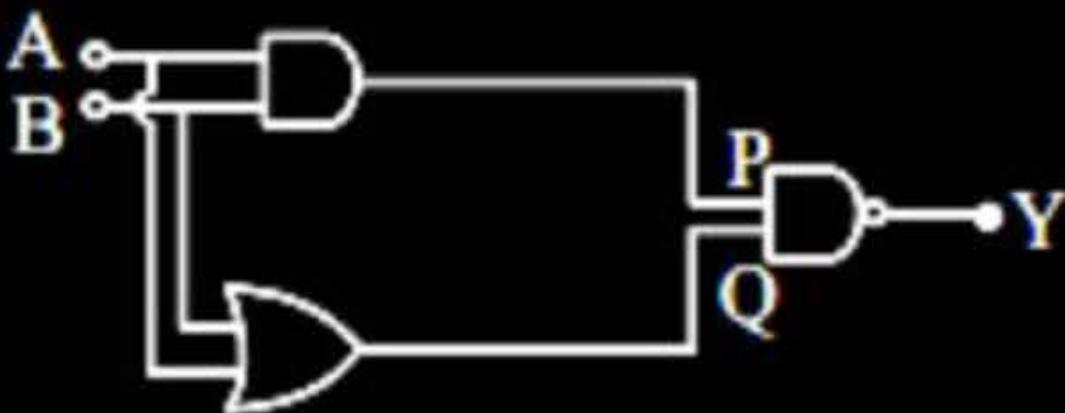
D NAND gate

Q.

In the following logic circuit the sequence of the inputs A, B are (0,0), (0,1), (1,0) and (1,1). The output Y for this sequence will be :

JEE Main 2021 (Online) 31<sup>st</sup> August Morning Shift

- A 1, 0, 1, 0
- B 0, 1, 0, 1
- C 1, 1, 1, 0
- D 0, 0, 1, 1

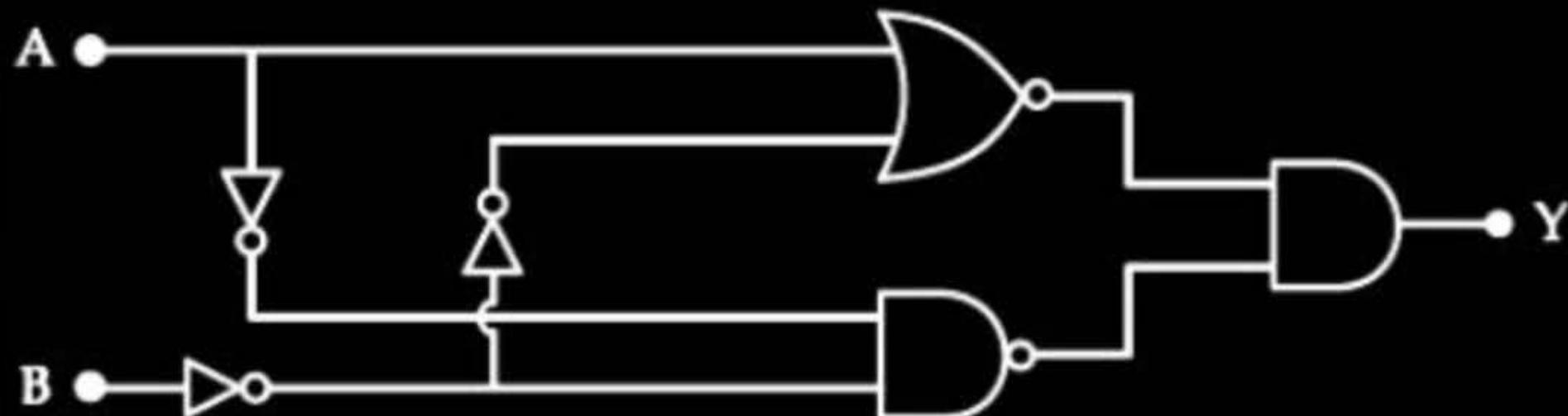


**Q.**

In the logic circuit shown in the figure, if input A and B are 0 to 1 respectively, the output at Y would be 'x'. The value of x is \_\_\_\_\_.

P  
W

JEE Main 2021 (Online) 16<sup>th</sup> March Morning Shift



The truth table for the following logic circuit is :

JEE Main 2021 (Online) 25<sup>th</sup> February Evening Shift

Q.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

A

A	B	Y
0	0	1
0	1	0
1	0	1
1	1	0

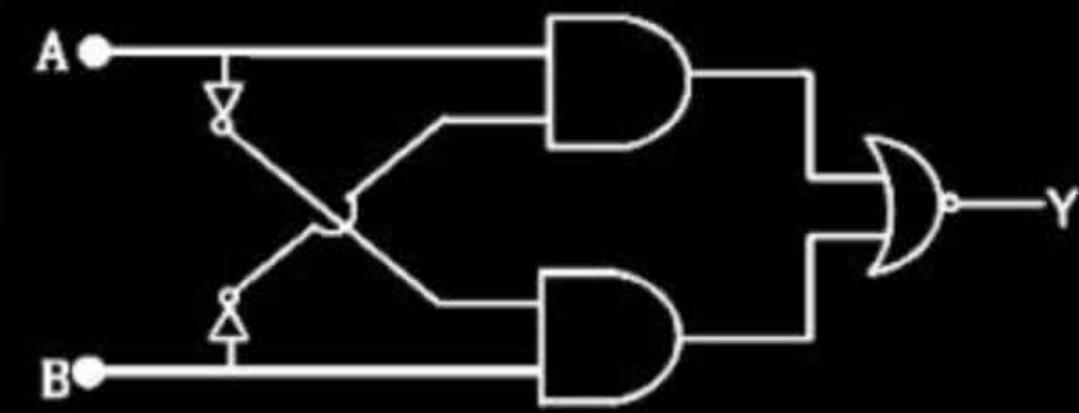
B

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	1

C

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

D



Q.

Identify the operation performed by the circuit given below :

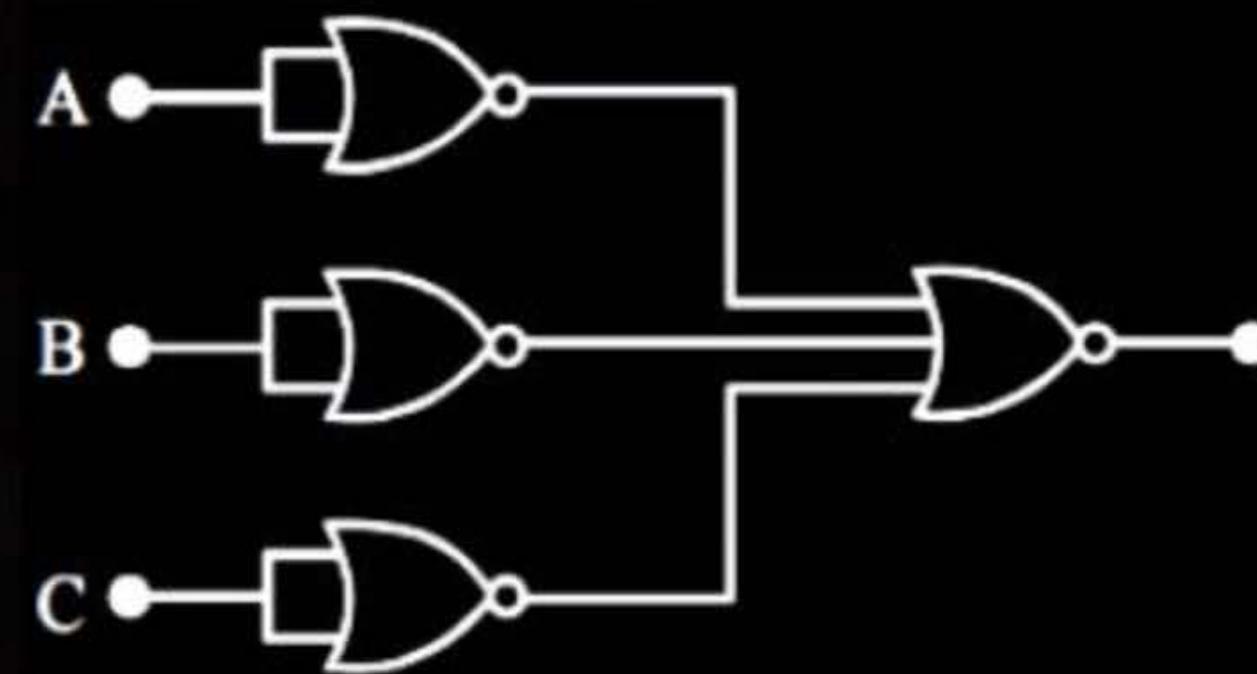
JEE Main 2020 (Online) 4<sup>th</sup> September Evening Slot

A AND

B NAND

C OR

D NOT



Q.

In the following digital circuit, what will be the output at 'Z', when the input (A, B) are (1,0), (0,0), (1,1,), (0,1)

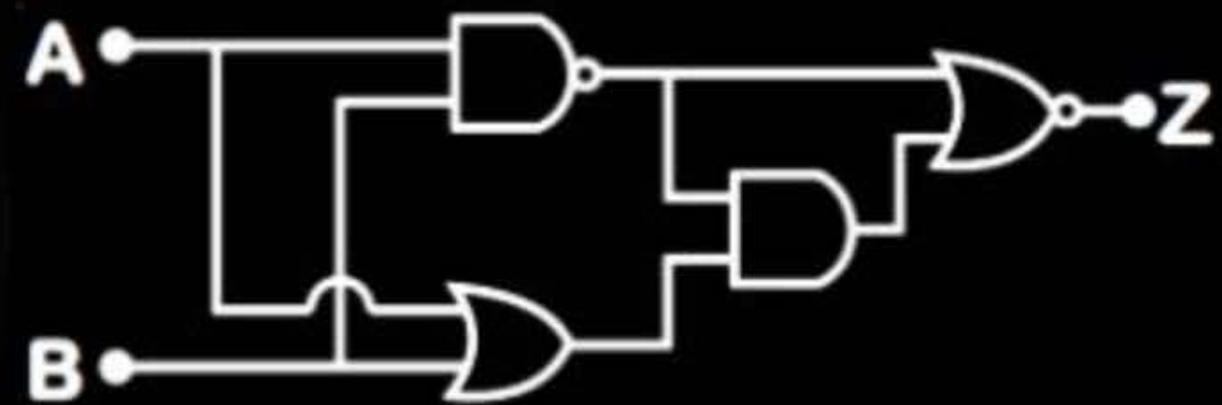
JEE Main 2020 (Online) 2<sup>nd</sup> September Evening Slot

A 1, 1, 0, 1

B 0, 1, 0, 0

C 1, 0, 1, 1

D 0, 0, 1, 0



**Thank You !**