SEMICONDUCTORS

EXTRINSIC SEMICONDUCTORS

- Impure semiconductor
- When pure semiconductor material is mixed with small amounts of certain specific impurities with valency different from that of the parent material, the number of mobile electrons or holes drastically changes. This process is called doping

- $n_e \neq n_h$
- $n_e \times n_h = n_i^2$

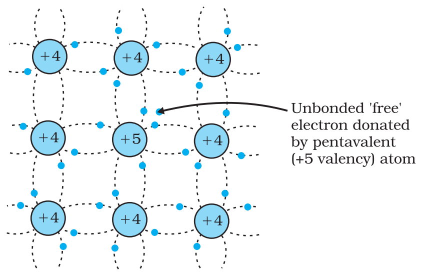
ISC + Impurity → Extrinsic SC

2 TYPES

n Type

Intrinsic semiconductor → Pentavalent Impurity ⇒ N type S C

1) Majority charge carriers - electrons
2) Minority charge carriers - holes
3) n type semiconductor is electrically neutral (not negatively charged)
4) Donor energy level lies just below the conduction band

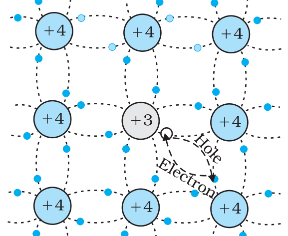


p Type

Intrinsic semiconductor + trivalent Impurity ⇒ P type SC

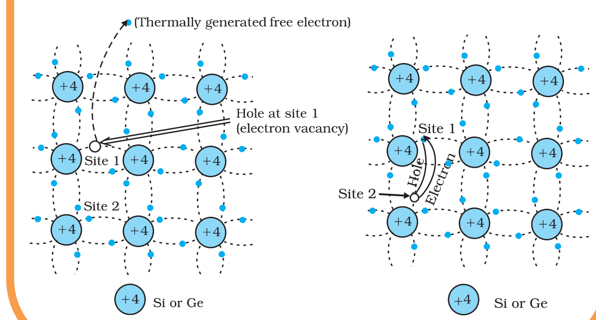
B, Al, Ga, In, Tl

1) Majority charge carriers - holes
2) Minority charge carriers - electrons
3) P type is electrically neutral (not positively charged)
4) Acceptor energy level lies just above the valence band

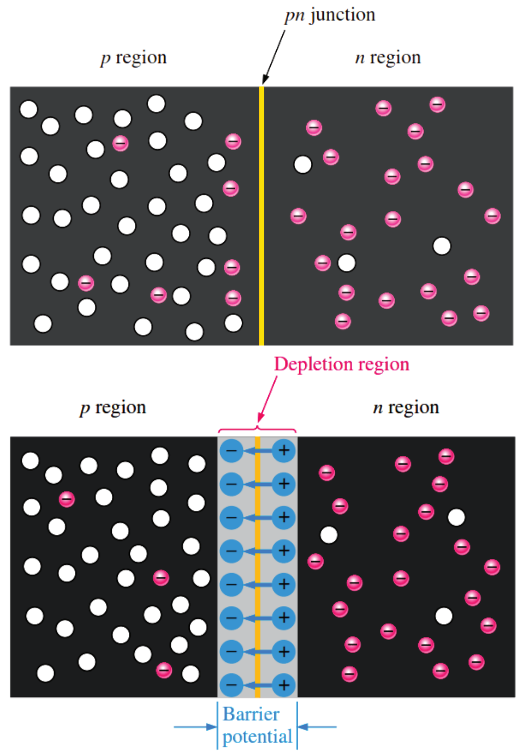


INTRINSIC SEMICONDUCTORS

- Pure semiconductor
- At absolute temperature (0K) conduction band of semiconductor is completely empty and the semiconductor behaves as an insulator.
- As temperature increases, the valence electrons acquire thermal energy to jump into the conduction band (due to breakage of covalent bond)
- when they leave the CB they leave behind the deficiency of electrons in the valence band.
- This deficency of electrons is known as HOLES or cotter
- $n_e = n_h = n_i$



p-n Junction Diode



Depletion layer

Due to diffusion, neutrality of both N and P type semiconductor is disturbed

A layer of negatively charged ions appear near the junction in the p crystals and a layer of positive ions appear near the Junction in n crystals

This layer is called depletion layer

1) The thickness of depletion layer is 1 micron = 10^{-6} m
2) Width of depletion layer $\propto \frac{1}{\text{Doping}}$
3) Depletion is directly proportional to temperature
4) The P N junction diode is equivalent to capacitor in which the depletion layer acts as a dielectric

Barrier potential

The potential difference created across the P N junction due to diffusion of electron and holes is called potential barrier

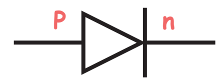
For Ge, V_B = 0.3 V

For Si V_B = 0.7V

Diffusion Current-
Due to flow of majority charge carriers

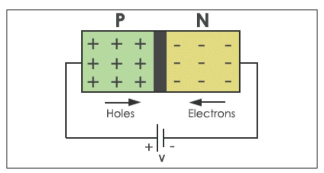
Drift Current -
Due to flow of minority charge carriers

Symbol of p-n Junction Diode

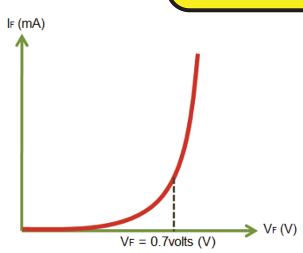


BIASING

Forward biasing



p-side is connected to higher potential and n-side to lower potential.
Forward bias opposes the potential barrier.
In F.B, width of depletion region decreases.
If the applied potential, $V > V_B$, a forward current is set up across the junction.

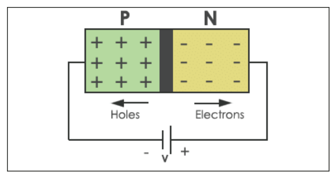


Cut in voltage or knee voltage is the voltage at which current starts to increase rapidly.
It is equal to
V_B For Ge V_B = 0.3V,
Si V_B = 0.7V

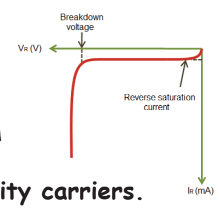
DYNAMIC RESISTANCE

$R_f = \frac{\Delta V}{\Delta I}$

Reverse biasing



p-side is connected to lower potential and n-side to higher potential.
Width of the depletion layer increases.
No current flows through the junction
due to diffusion of majority carriers.
A small current inthe order of μA exists due to drift of minority charge carriers.



BREAKDOWN VOLTAGE

The reverse bias voltage at which breakdown of S.C occurs Eg:- Ge 2.5V , Si 3.5V

Zener Breakdown

- When reverse bias voltage is increased, the electric field at the junction also increases.
- At some stage, electric field becomes so high it can break covalent bond at the junction creating minority charge carriers (e - hole pairs).
- Thus a large no. of charge carriers are generated. This causes a large current flow

Avalanche breakdown

- At high voltage, more minority charge carriers are generated due to breakage of covalent bond by collision of electrons
- Thus more number of charge carriers are generated. A chain reaction is established giving rise to even more collisions, thus creating high current.

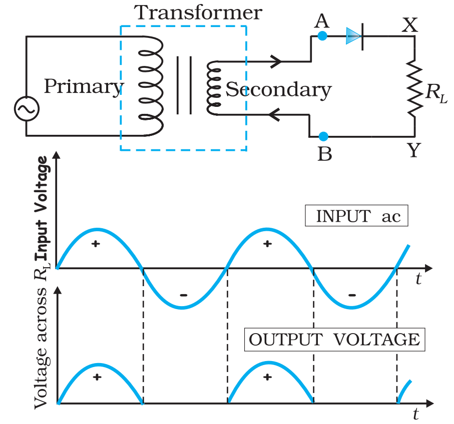
PHYSICS WALLAH

ELECTRONICS

RECTIFICATION

Rectification
- $\frac{1}{2}$ wave rectification-1 Diode
- full wave rectification-2 Diodes

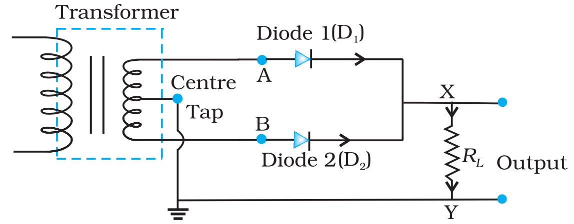
Half wave rectification

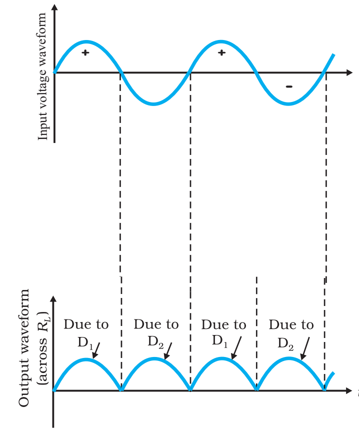


- Rectifies half of the AC wave
- In Positive half cycle, diode is forward biased and output signal is obtained
- In Negative half cycle, diode is reverse biased, output signal is not obtained.

Full wave rectification

It uses a center-tap

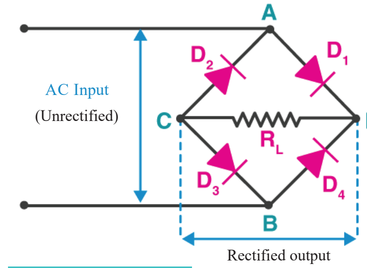




- Positive half cycle diode: D_1- forward bias D_2-Reverse biased
- Negative half cycle, diode: D_1- reverse bias D_2-forward biased

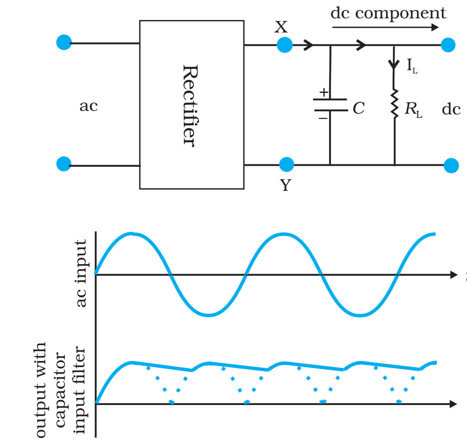
Bridge Rectifier

- 4 Diodes & full wave rectification
- Output is taken from diagonal where both the terminals are same



Filter circuit

- Converts rippled DC into pure DC
- Using parallel capacitor method or by series inductor method

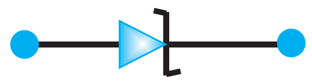


AC $\xrightarrow{\text{Rectifier}}$ Rippled DC $\xrightarrow{\text{Filter}}$ Pure DC

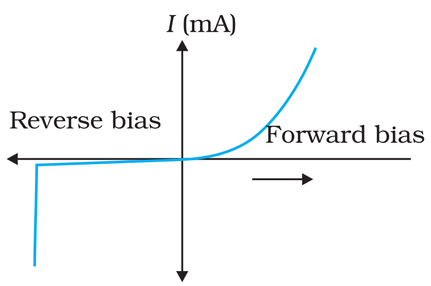
SPECIAL PURPOSE DIODES

Zener diode

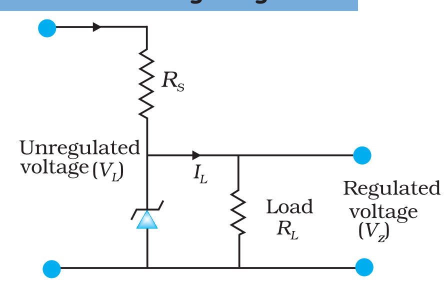
Representation



- Heavily doped p-n junction diode
- Cannot be damaged by high reverse current Always operated in reverse biased condition
- Can operate continuously without being damaged
- Can be used as a voltage regulator (in the region of reverse breakdown voltage)



Zener diode as a voltage regulator

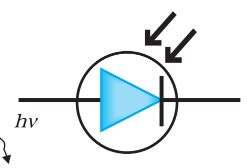


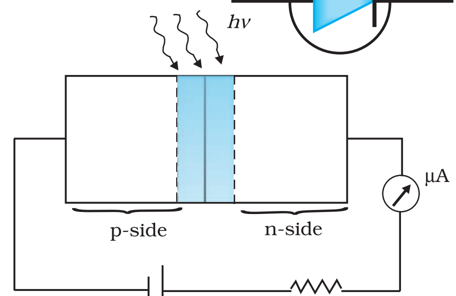
Condition for working, $V > V_z$ V=Applied voltage
V_z=Zener voltage

- Applied voltage will be divided between zener diode and series resistance (R_S)
- Output is obtained from resistance R_L which is connected parallel to zener

Photodiode

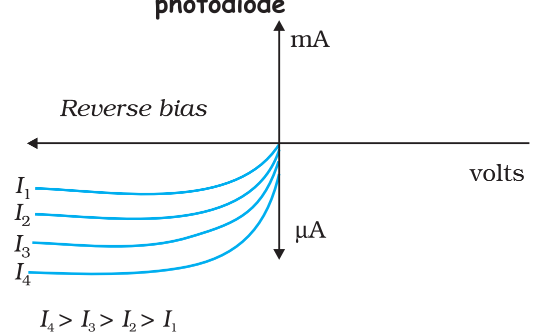
Representation





- Special type of photo detector
- Connected in reverse bias
- p-n junction is fabricated from a photosensitive conductor & provided with transparent window
- $h\nu > E_g$, electron hole pairs are generated due to incident light & photo current can be detected in external circuit

$\lambda(\text{Å}) = \dfrac{12400}{E_g(eV)}$ where λ is maximum value of wavelength which can be detected by photodiode



photocurrent increases with increase in light intensity

Light emitting diode

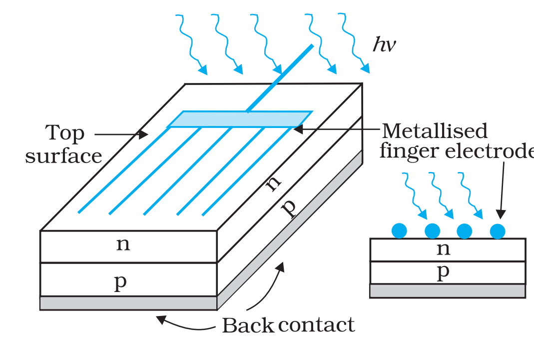
Representation

- Heavily doped; should be connected in forward biased
- Spontaneously converts electrical energy into optical energy
- Recombination of charge carriers at depletion layer results in release of energy in the form of light

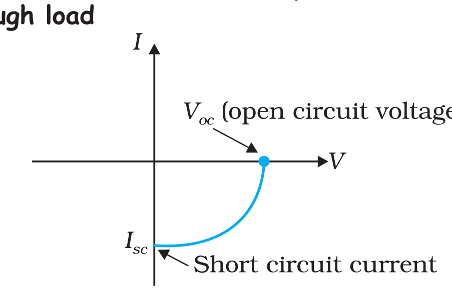
Choices of semi conductor material used in LED:

- λ of visible light ranges from 400-700 nm
- To emit visible light minimum band gap should be 1.8 eV
- Gallium arsenide phosphate (GaAsP) - 1.9 eV (Red light)
- Gallium arsenide -1.5 eV (Infrared)

Solar cell



- Diode is unbiased
- Charge carriers are formed by breaking of covalent bond when light falls on depletion region
- p side becomes positive n side becomes negative giving rise to photo voltage
- When external load is connected, photocurrent I_L flows through load

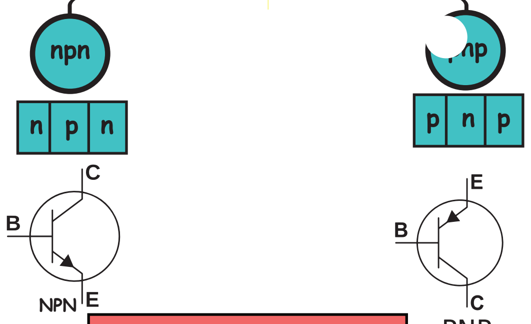


PHYSICS WALLAH

ELECTRONICS

ELECTRONICS

TRANSISTOR



IT HAS THREE PARTS

EMITTERS

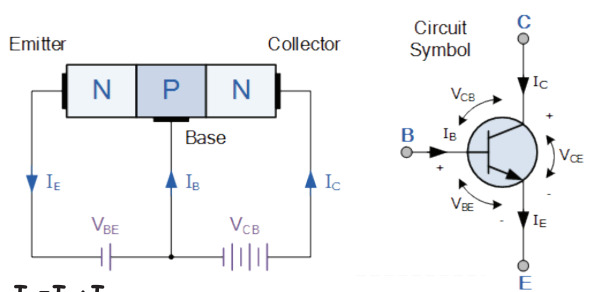
It is a section on one side of the transistor.
It is moderate in size and heavily doped.
It supplies a large number of majority charge carriers for current to flow through a transistor.

BASE

Very thin and lightly doped.

COLLECTOR

It is on the other side of the transistor. Moderately doped and larger in size as compared to the emitter



$I_E = I_B + I_C$

Action of n-p-n Transistor

emitter-base junction - forward biased
base-collector junction - reverse biased

Forward bias of emitter-base circuit repels the electrons of the emitter towards base

Base is very thin and lightly doped, so very few electrons (less than 5%) are neutralised by the holes giving rise to base current I_B

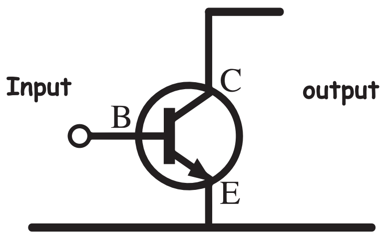
Remaining electrons (greater than 95%) are pulled by the collector which is at higher potential.

The electrons are finally collected by the positive terminal of V_{cc} giving rise to collector current I_c

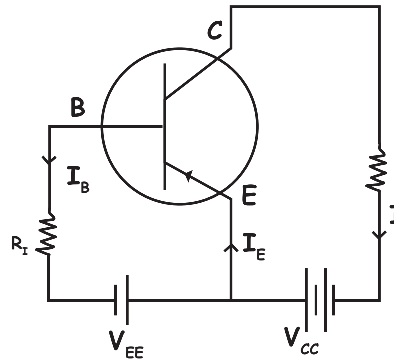
CONFIGURATION OF TRANSISTORS

It is of three types

1 COMMON EMITTER



common emitter

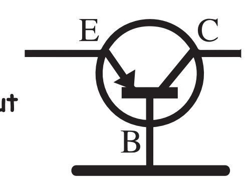


Current gain $\beta = \frac{I_C}{I_B}$

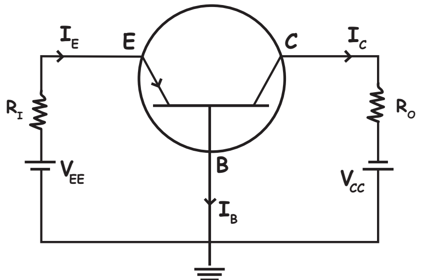
Voltage gain $= \frac{V_O}{V_I} = \frac{I_C R_O}{I_B R_I} = \beta \frac{R_O}{R_I}$

Power gain $= P_g = V_g I_g = \frac{P_{out}}{P_{in}} = \beta \frac{R_O}{R_I} \times \beta = \beta^2 \frac{R_O}{R_I}$

2 COMMON BASE



common base

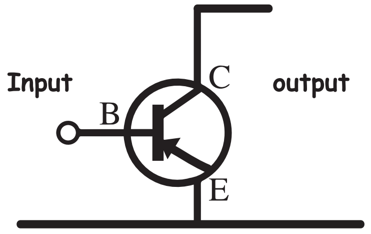


Current gain $\alpha = \frac{I_C}{I_E}$

Voltage gain $= \frac{V_O}{V_I} = \frac{I_C R_O}{I_E R_I} = \alpha \frac{R_O}{R_I}$

Power gain $= P_g = V_g I_g = \alpha^2 \frac{R_O}{R_I}$

3 COMMON COLLECTOR



Common Collector

Current gain $\gamma = \frac{I_B}{I_E}$

RELATIONSHIP BETWEEN α & β

$\alpha = \frac{\beta}{1+\beta}$

$\beta = \frac{\alpha}{1-\alpha}$

TRANSCONDUCTANCE

$T_c = \frac{I_O}{V_I} = \frac{\text{Output current}}{\text{Input voltage}}$

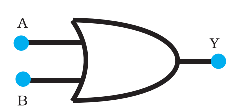
$V_g = \frac{V_O}{V_I} = \frac{I_C \times R_O}{V_I} = T_c \times R_O$

$T_c \propto V_g$

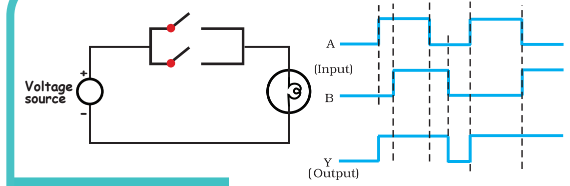
LOGIC GATE

- Principal gates: OR, AND, NOT
- Universal gates: NAND, NOR

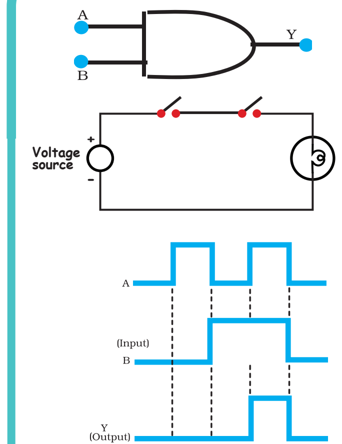
OR GATE



Input		Output
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



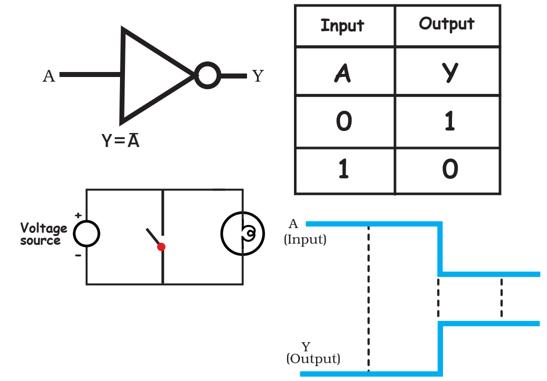
AND GATE



Y=A.B

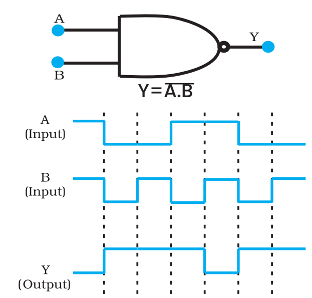
Input		Output
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

NOT GATE



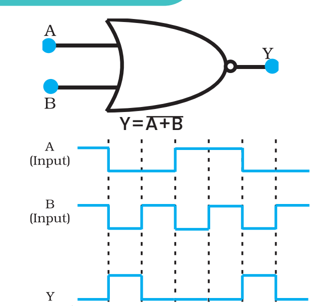
Input	Output
A	Y
0	1
1	0

NAND GATE



Input		Output
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE

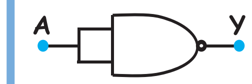


Input		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

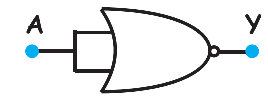
REALISATION OF BASIC GATES USING NAND OR NOR GATE

USING NAND		USING NOR

NOT

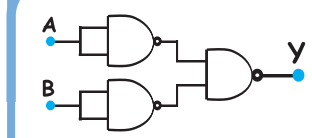


$Y = \overline{A.A} = \bar{A}$

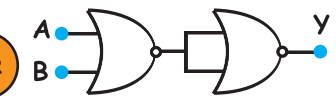


$Y = \overline{A+A} = \bar{A}$

OR

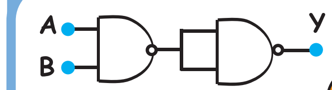


$Y = \overline{\bar{A}.\bar{B}} = A+B$

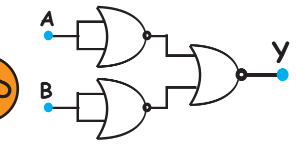


$Y = \overline{\overline{A+B}} = A+B$

AND



$Y = \overline{\overline{A.B}} = A.B$



$Y = \overline{\bar{A}+\bar{B}} = A.B$

BOOLEAN LOGIC

$A+A=A$
$A.A=A$
$A+1=1$
$A.1=A$

$A+0=A$
$A.0=0$
$A.\bar{A}=0$
$A+\bar{A}=1$

$\overline{A+B} = \bar{A}.\bar{B}$
$\overline{A.B} = \bar{A}+\bar{B}$
De-Morgan's law

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