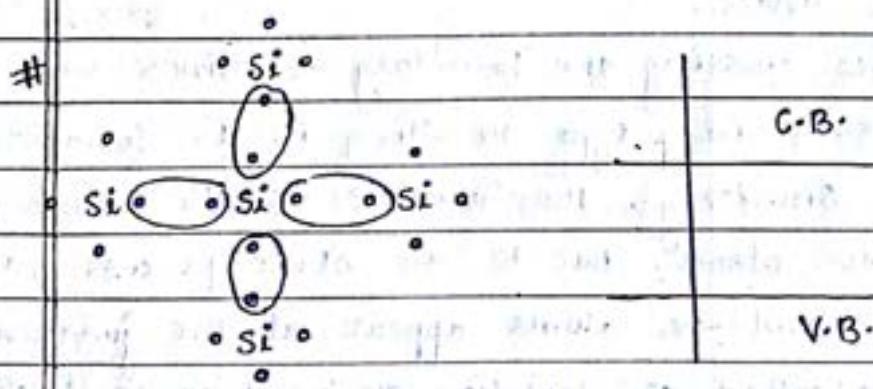
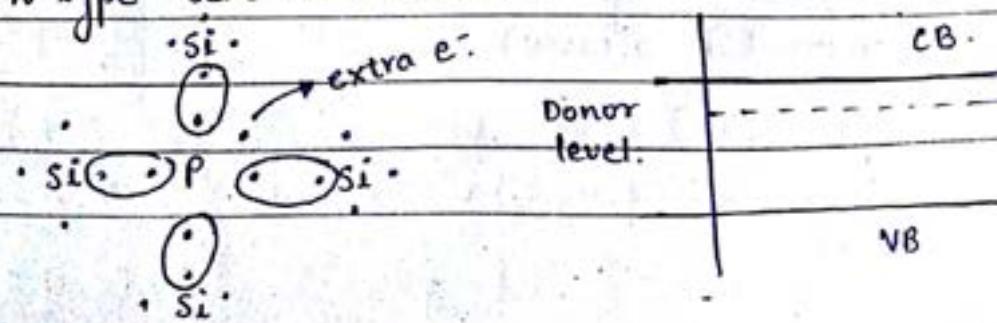


INTRODUCTION

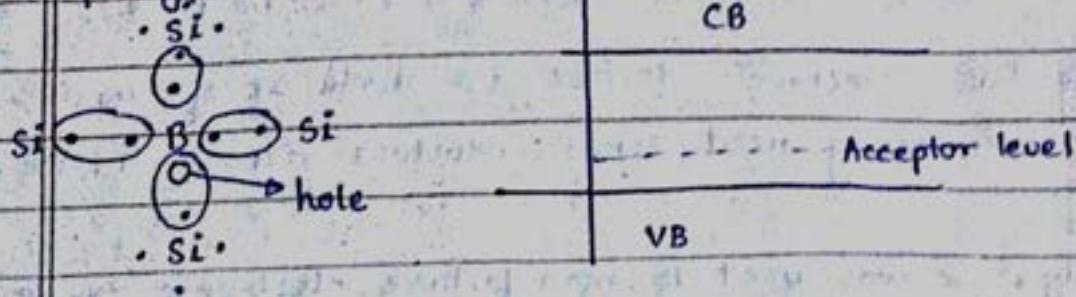
- All the basic electronic devices are made up of semi-conductors.
- The most commonly used semi-conductors are → Si, Ge, GaAs.
- Initially, Ge was used to manufacture electronic components as it was abundantly available but due to high temperature dependency it lead to severe problems.
- Si is nowadays widely used for manufacturing due to its vast availability, less sensitivity to temperature.
- GaAs is another material which is used for making electronic devices and is highly recommended for devices requiring high speed.
- There are two types of semiconductors :-
 - a. intrinsic.
 - b. extrinsic
- Intrinsic semi-conductors are pure semiconductors.
Eg :- Si, Ge.
- Extrinsic semi-conductors are doped with Grp 3 and Grp 5 elements to increase conductivity.
Eg :- n-type and p-type semiconductors.



n-type Semiconductors.

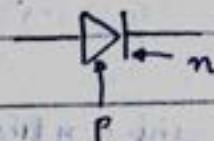
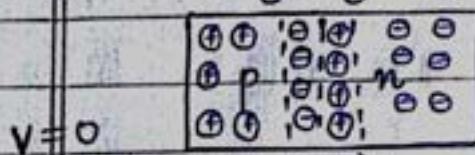


P-type



P-N JUNCTION DIODE

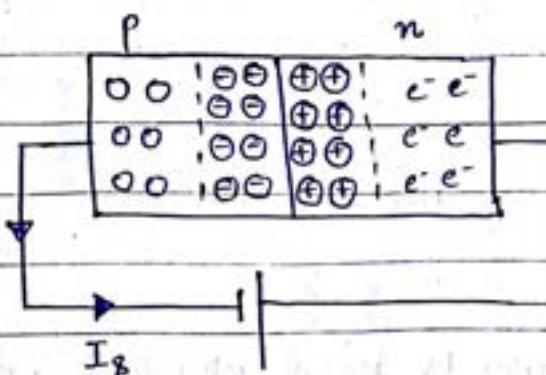
- A p-n junction diode is formed by combining a p-type and a n-type semi-conductor.
- It is a two terminal device.
- Depending on the voltage applied, the diode can either conduct or remain switch off.
- $V_b \oplus$ Built in potential.



- When p and n type are connected movement of charge carriers take place due to which small current flows in the device.
- The electrons after crossing the boundary combines with the hole present in p type resulting in the formation of -ve atom. Similarly, the holes cross the boundary and forms +ve atoms. Due to the above process a region of +ve and -ve atoms appear at the junction. This region is called as depletion region because it is free of mobile charge carriers.

The net current is 0. (zero).

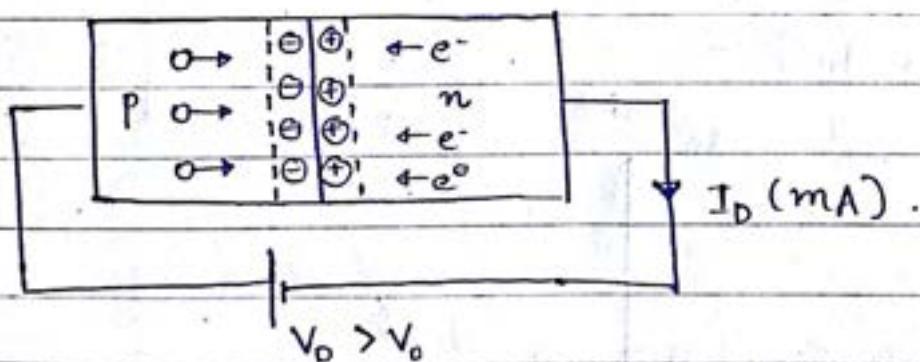
$V < 0$



I_B = Reverse Saturation Current

- In reverse biased condition the width of depletion region increases as the holes and e⁻s are attracted away from the junction.
- A reverse saturation current (I_B) flows in the diode due to minority charge carriers. This current is usually of the order of nanoamperes.

$V > 0$



- When the diode is forward biased, the holes and e⁻s gain sufficient energy and cross the depletion region which finally allows current to flow.

#

SHOCKLEY'S EQUATION

$$I_D = I_S (e^{\frac{V_D}{nV_T}} - 1)$$

✓ V_D = voltage applied across the diode.

✓ I_S = saturation current

✓ n = ideality factor. (depends upon physical property of material).

$n = 1-2$ (n=1 assume).

✓ V_T = Thermal voltage (depends upon temperature).

$$V_T = \frac{kT}{q}$$

→ k = Boltzmann's constant.

→ T = temperature

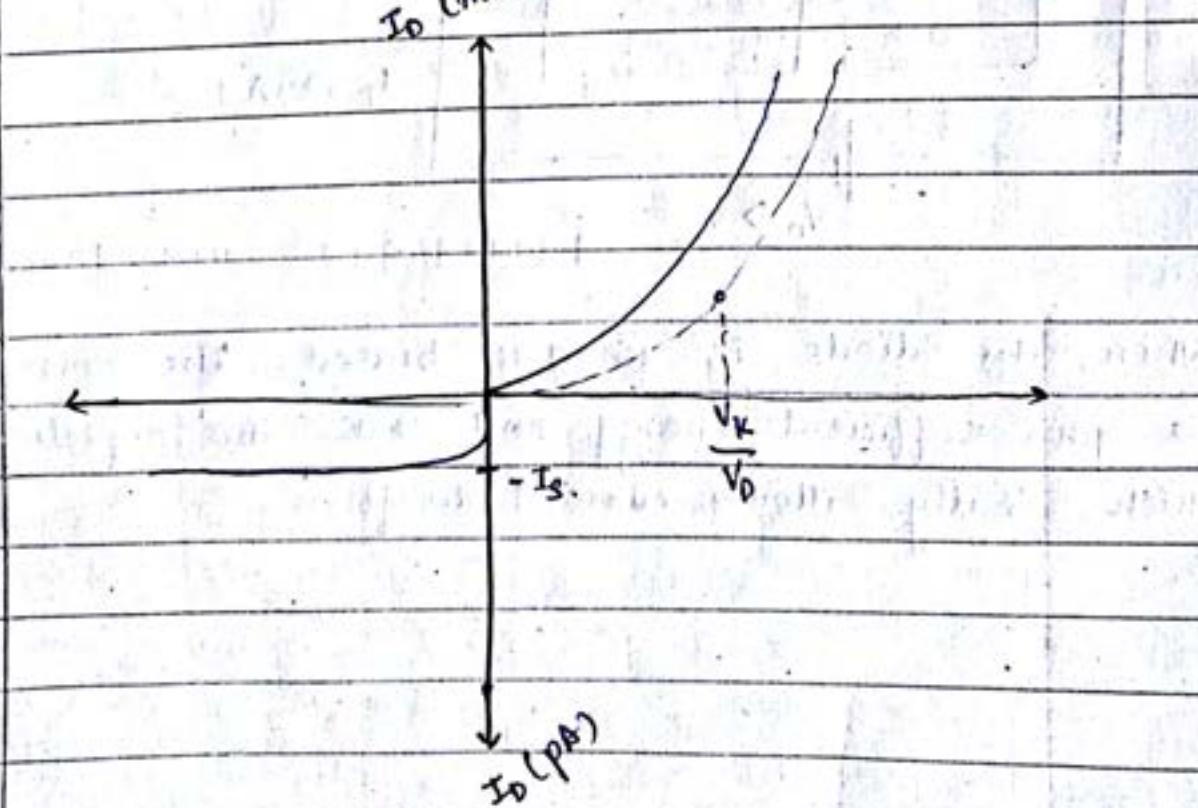
→ q = charge = 1.6×10^{-19} C.

$$V_D = 0, I_D = 0 \quad V_D/V_T n.$$

$$V_D > 0, I_D \approx I_S \cdot e^{V_D/V_T n}$$

$$V_D < 0, I_D \approx -I_S$$

$$I_D (\text{mA})$$

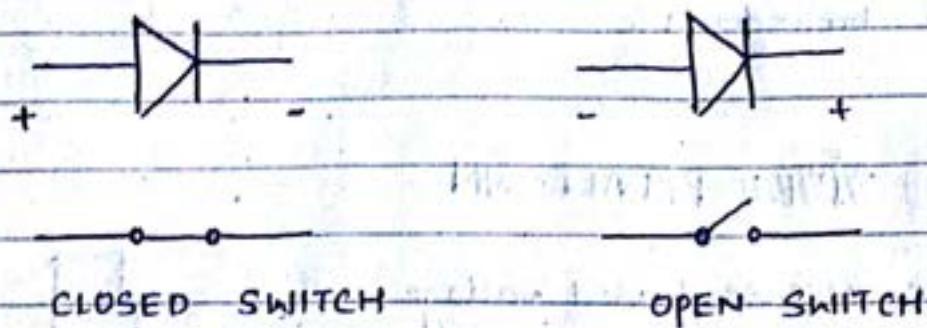


V-I CHARACTERISTICS OF PRACTICAL DIODE

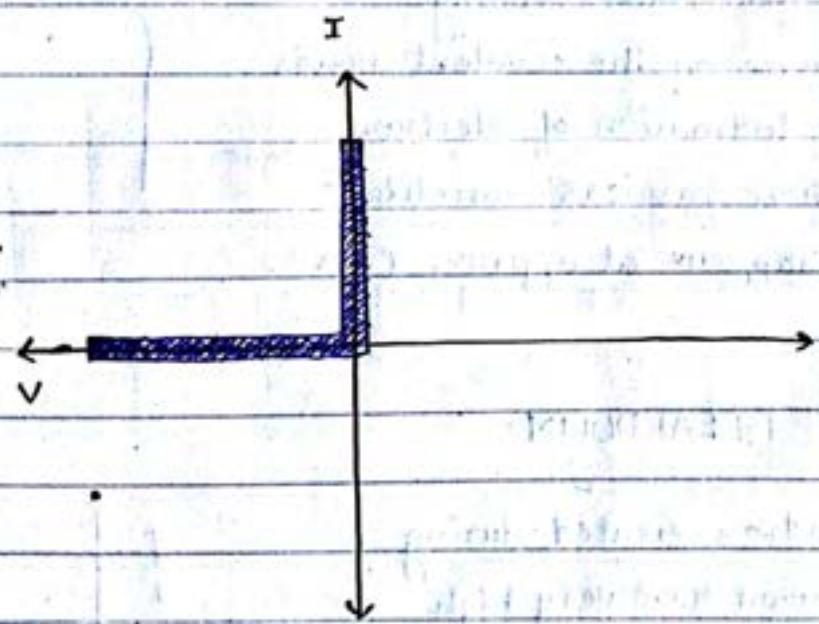
Graph ↪ .

IDEAL DIODE

An Ideal diode behaves as a switch.



V-I CHARACTERISTICS OF IDEAL DIODE



$$R = \frac{V}{I} = \infty$$

In R.B. condition

$$R = \frac{V}{I} = 0$$

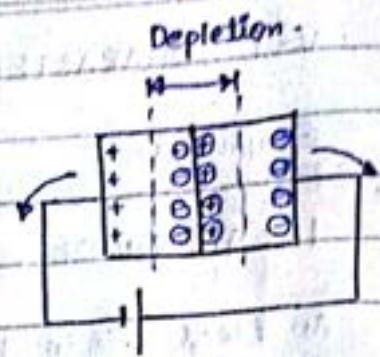
In F.B. condition ideal diode
resistance = 0.

#

BREAKDOWN REGION

Breakdown in a diode happens in reverse biased region. There are two types of breakdown :-

1. Zener breakdown.
2. Avalanche breakdown.

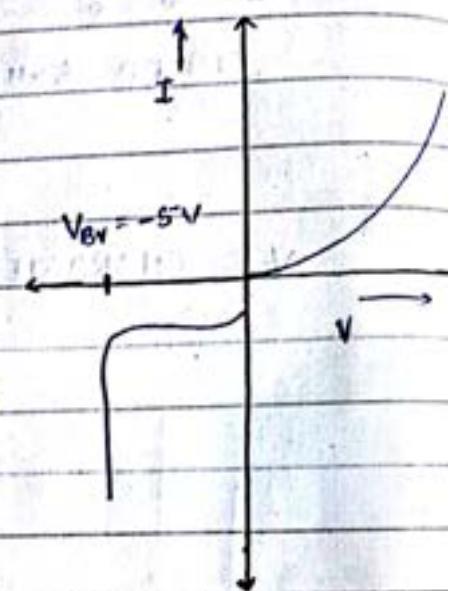


#

ZENER BREAKDOWN

→ When the reverse biased voltage is fed the built in potential also increases resulting in large electric field.

→ This electric field causes strong attraction force on the covalent bonds resulting in formation of electron and holes. These carriers constitute current. It happens at approx. (-5V).



#

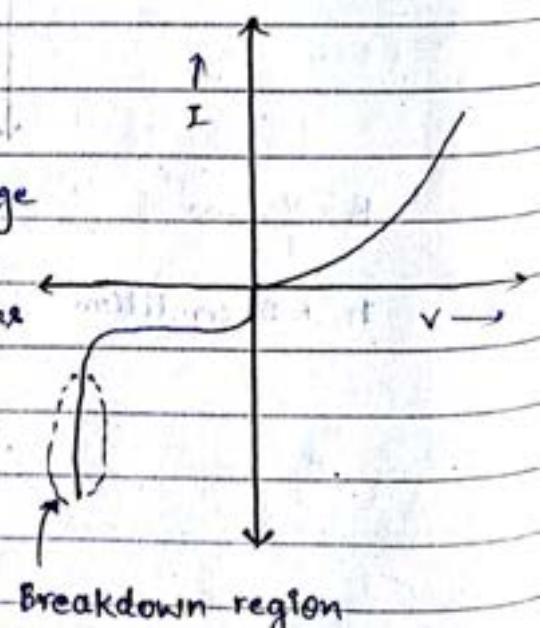
AVALANCHE BREAKDOWN

→ The holes and e⁻s created during zener breakdown have very high speed. As the reverse biased voltage is fed, the speed of charge carrier increases resulting in ionisation of atoms present in p and n type regions.

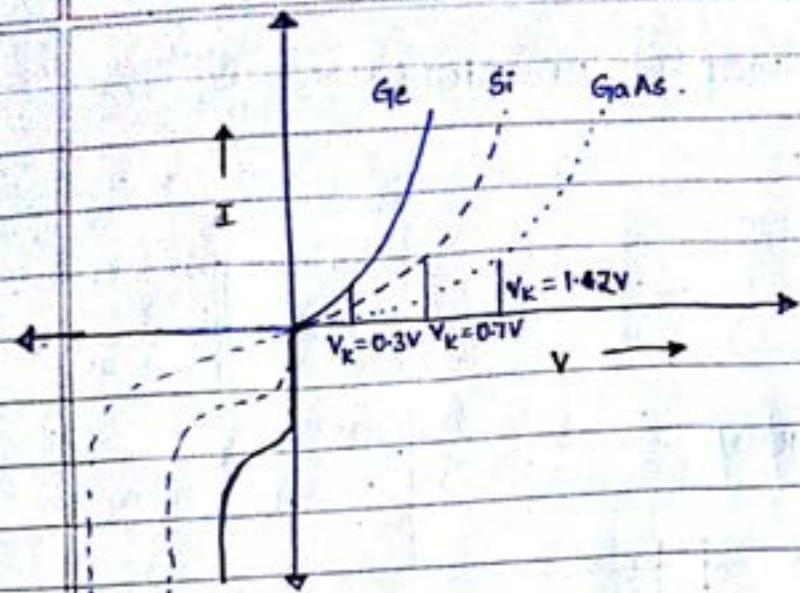
→ These extra charge carriers help in increasing the current.

This is avalanche breakdown.

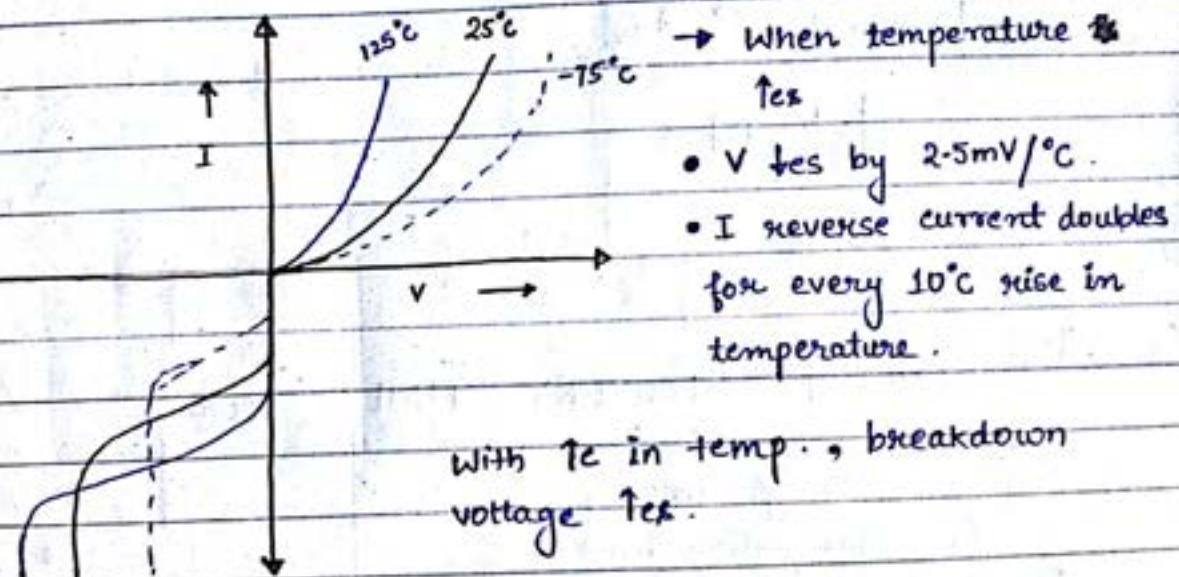
It happens around (-8V).



V_{BR} = Breakdown voltage.

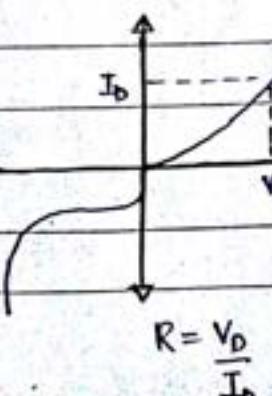


EFFECT OF TEMP. ON V-I CHARACTERISTICS OF DIODE

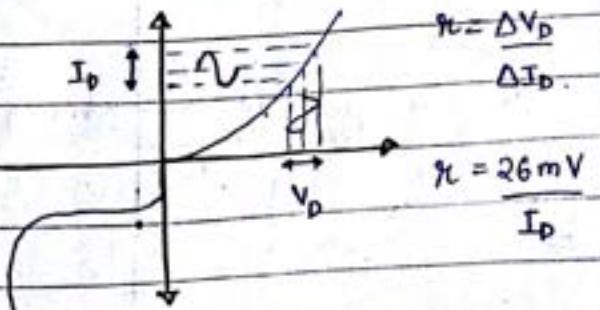


RESISTANCE PRESENT IN A DIODE

(a) D.C. Source.



(b) A.C. Source.

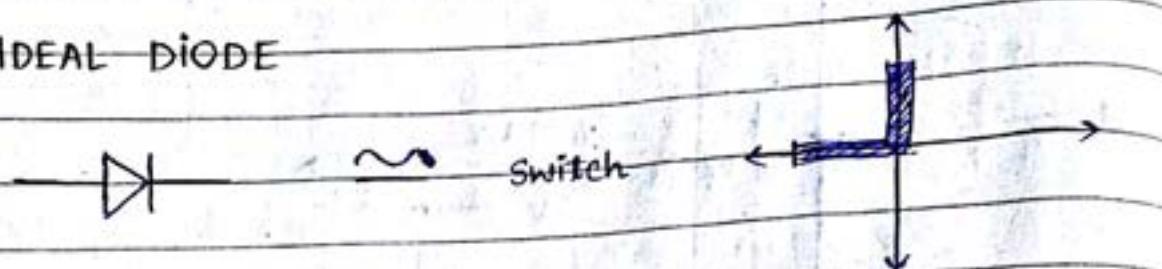


#

EQUIVALENT MODEL OF DIODE

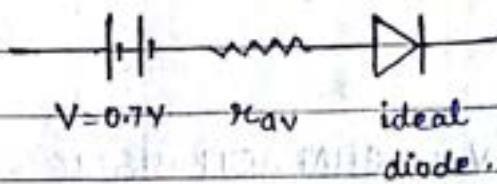
1.

IDEAL DIODE



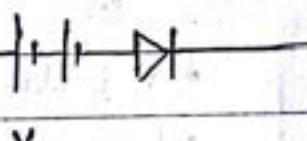
2.

PRACTICAL DIODE



3.

$$R_{\text{network}} \gg r_{av}$$



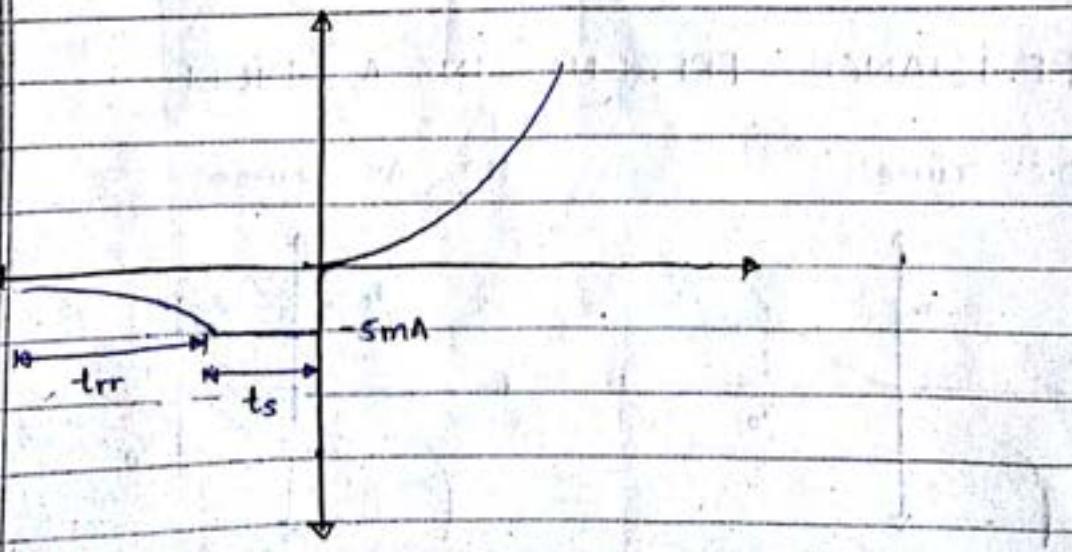
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REVERSE RECOVERY TIME (t_{rrc}).

t_s = storage time

t_t = translation time

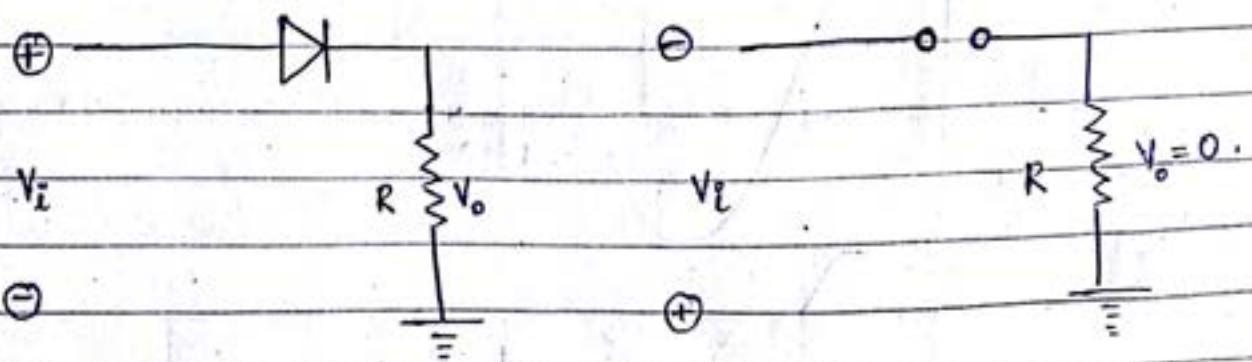
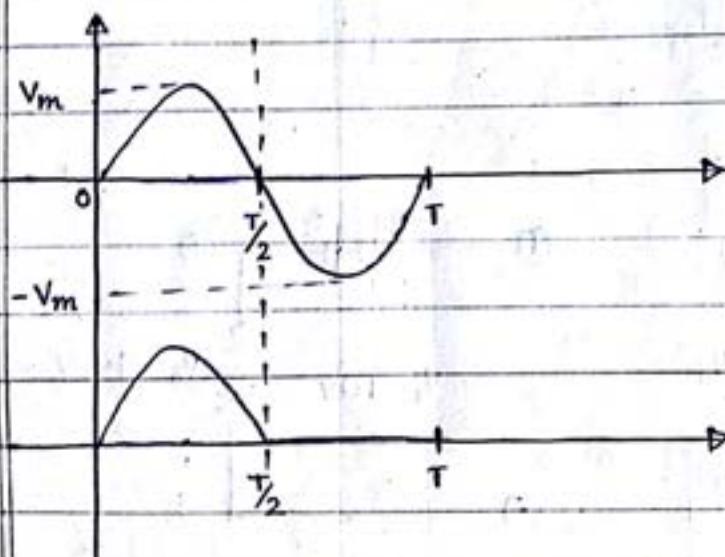
$$t_{rrc} = t_s + t_t$$



- storage time is the time taken by charge carriers to reach their respective regions.
Eg :- e's will try to go to n-region
- transition time is the time taken by the current to reach the reverse saturation current value.
- The reverse recovery time is the summation of storage time and transition time.
- Ideally, t_{rec} should be less.

APPLICATIONS OF DIODE AS A RECTIFIER

1. HALF WAVE RECTIFIER.



During +ve cycle diode behaves as connecting wire

During -ve cycle diode behaves as open switch.

- For time interval $0 \rightarrow T_2$, the diode becomes forward biased and behaves as closed switch. In this condition the output voltage follows the input voltage.
- For time interval $T_2 \rightarrow T$, the diode becomes reverse biased and behaves as open switch. Therefore, no current flows from input to output cycle. ∴, the output voltage is zero.

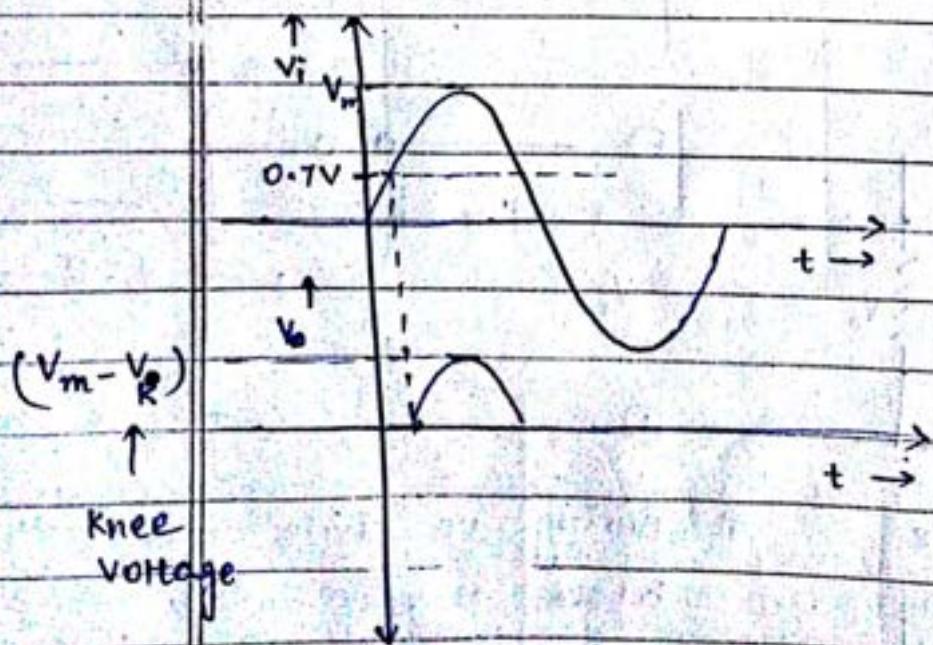
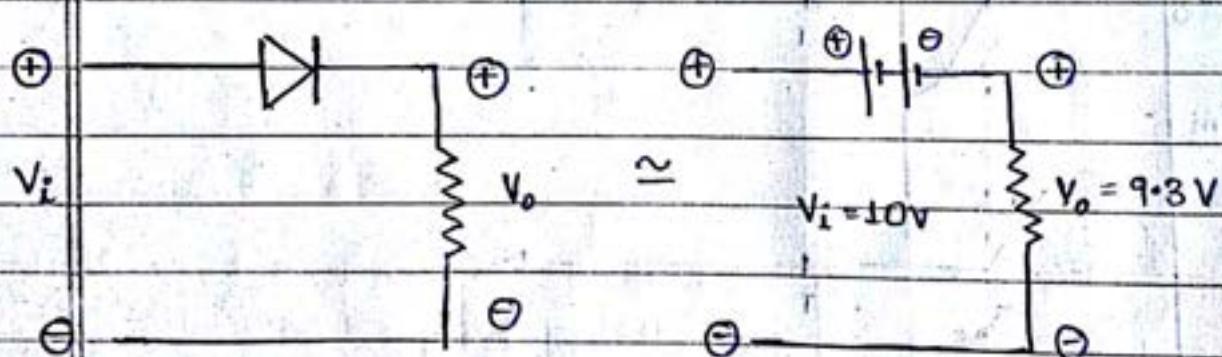
$\rightarrow V_{dc} = 0.318 V_m$

(average value) → max value of input voltage

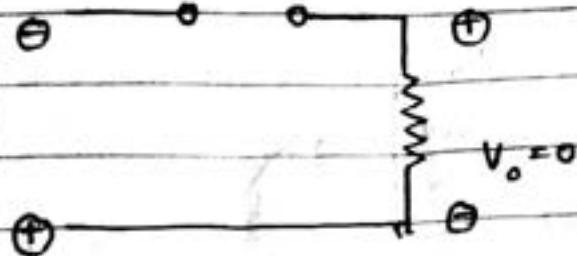
18/08/2017

PRACTICAL DIODE

FORWARD BIASED

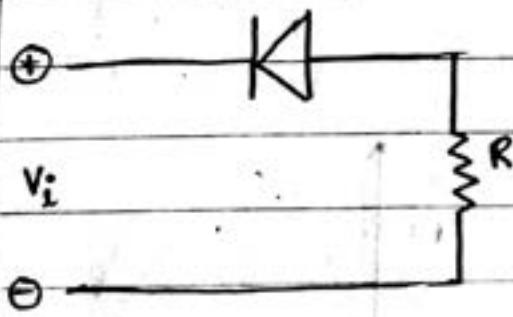


* REVERSE BIASED

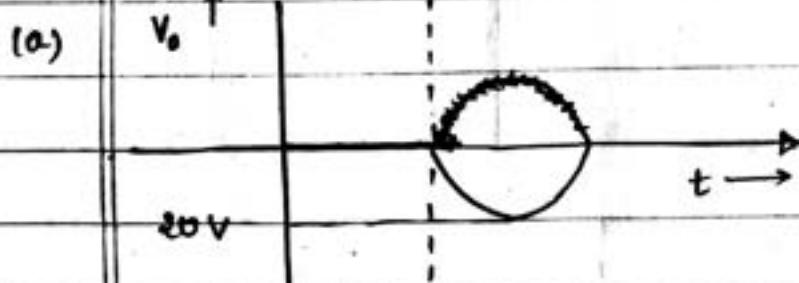
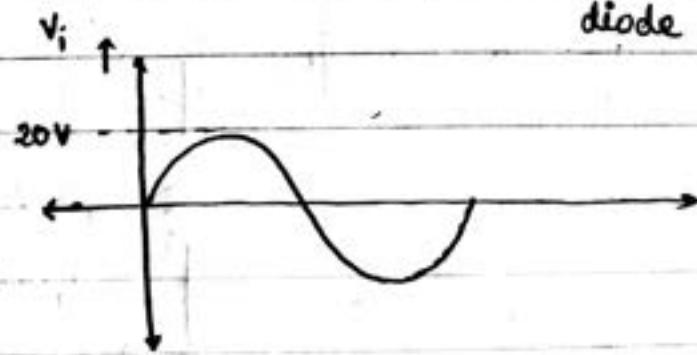


$$V_{dc} = 0.318 (V_m - V_k)$$

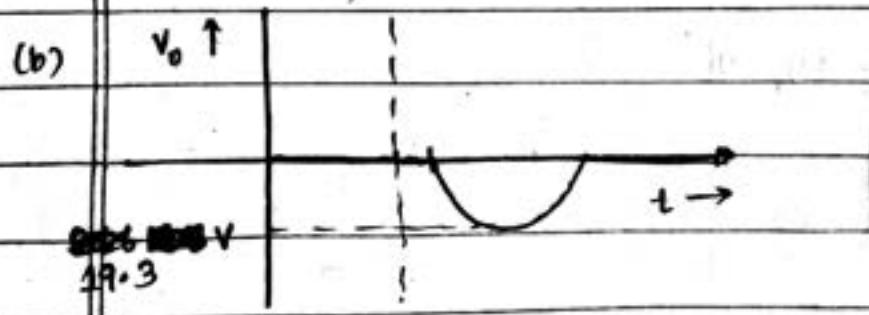
Q Sketch the output waveform and determine the average voltage for the given circuit.



(a) ideal diode (b) practical diode



$$V_{dc} = 0.318 (-20) \\ = -6.36 \text{ V}$$

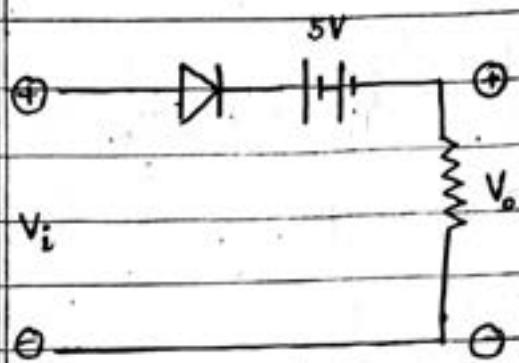


$$V_{dc} = 0.318 (-19.3) \\ =$$

Q

Draw the output voltage waveform for the given circuit for ideal and practical diode.

1.



V_i

20V

5V

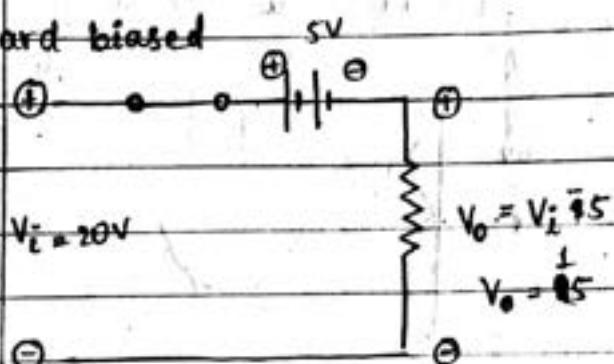
V_o

0

t

i) for ideal.

forward biased



V_o

15

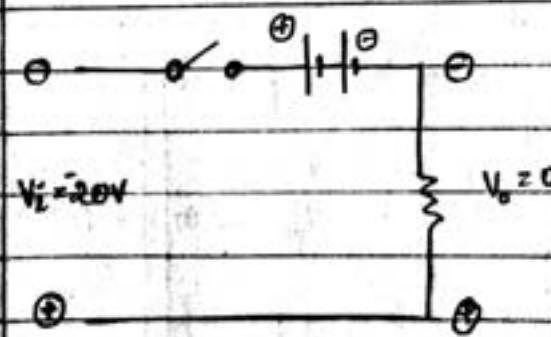
15

$V_o = \frac{1}{2}V_i$

0

t

reverse biased



V_o

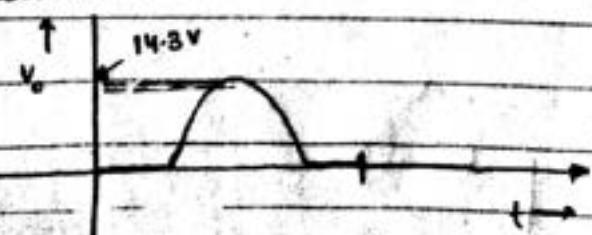
0

0

t

Practical diode

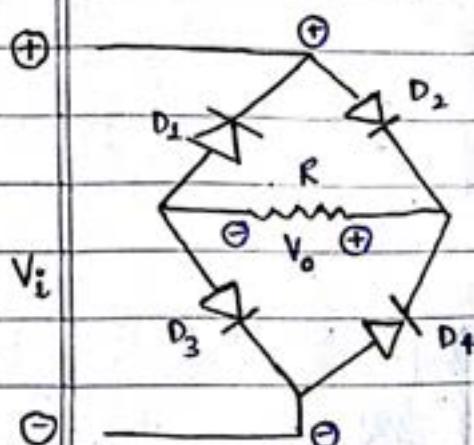
(b)



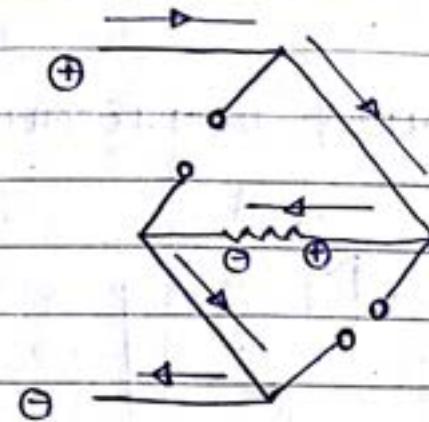
#

FULL WAVE RECTIFIER

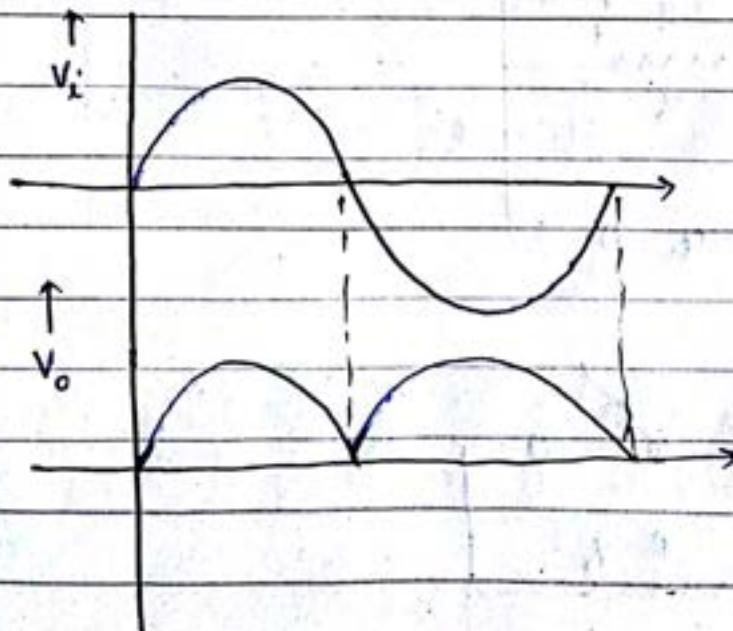
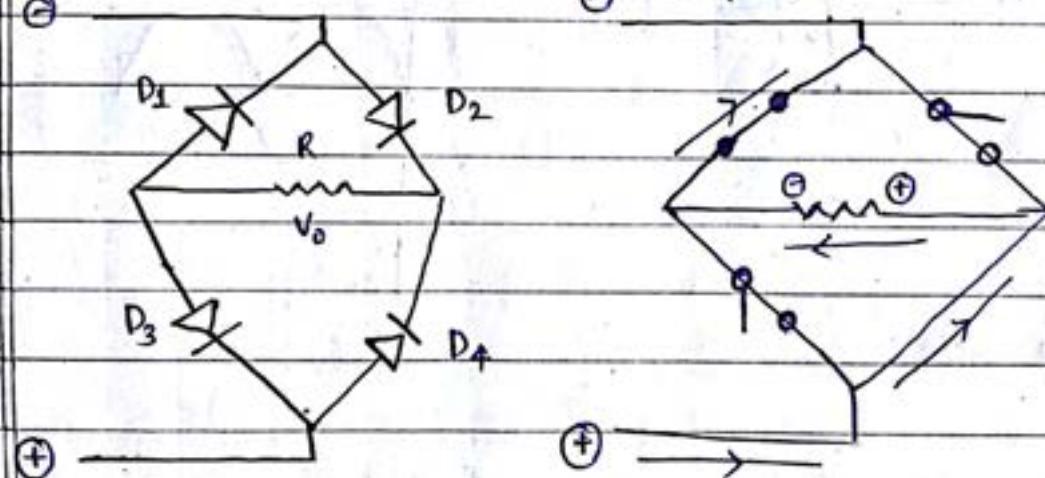
(A)



+ve cycle



(B)



IDEAL DIODES.

$$\rightarrow V_{dc} = 2 \times (V_{dc})$$

(full wave) half wave

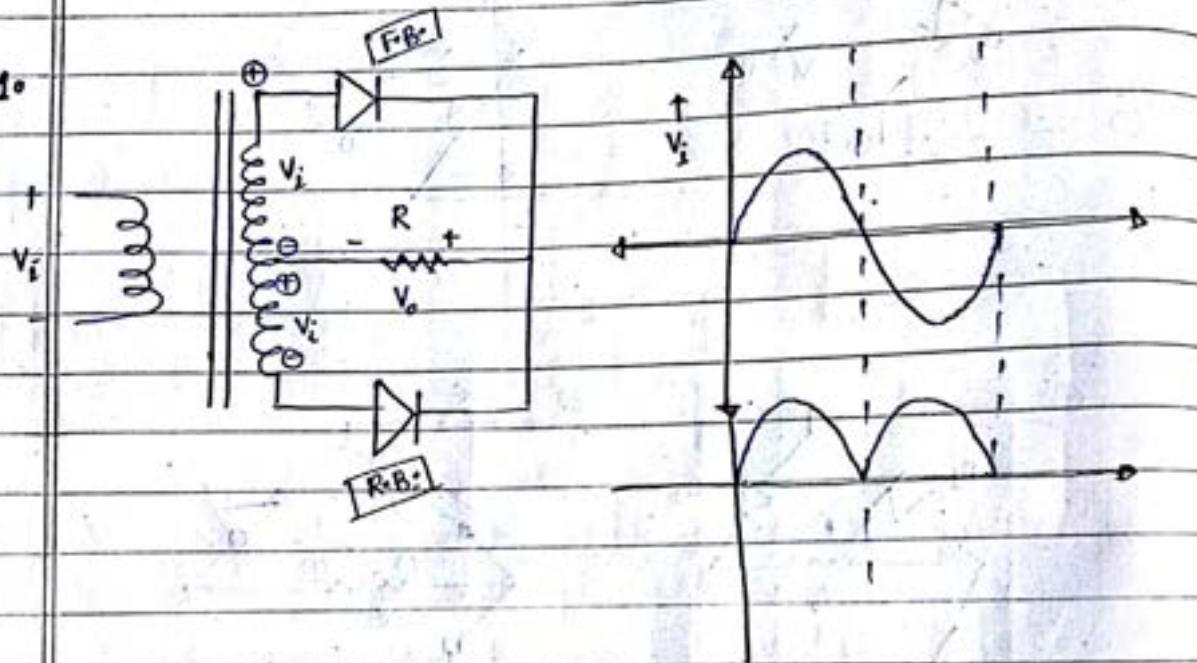
PRACTICAL DIODES

$$V_{dc} = 2 [0.318 (V_m - 2V_k)].$$

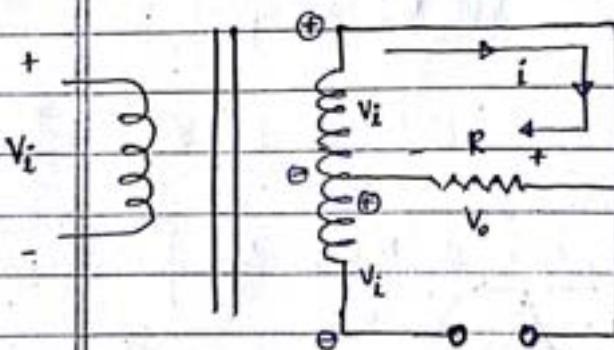
19/8/2017

GENTRE-TAPPED TRANSFORMER.

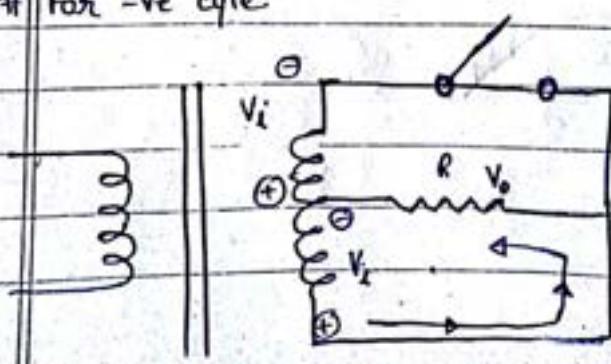
10



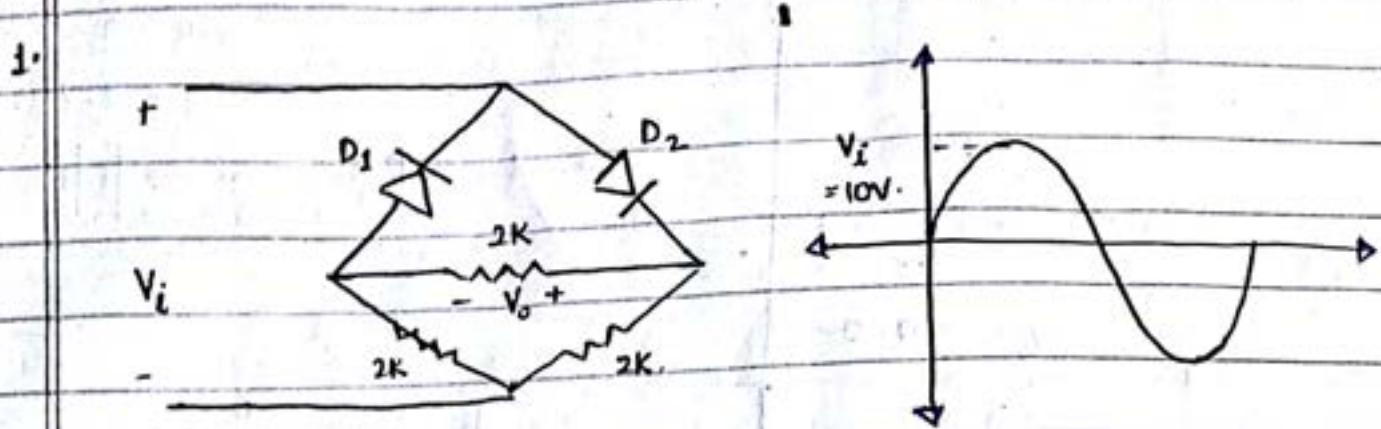
For +ve cycle.



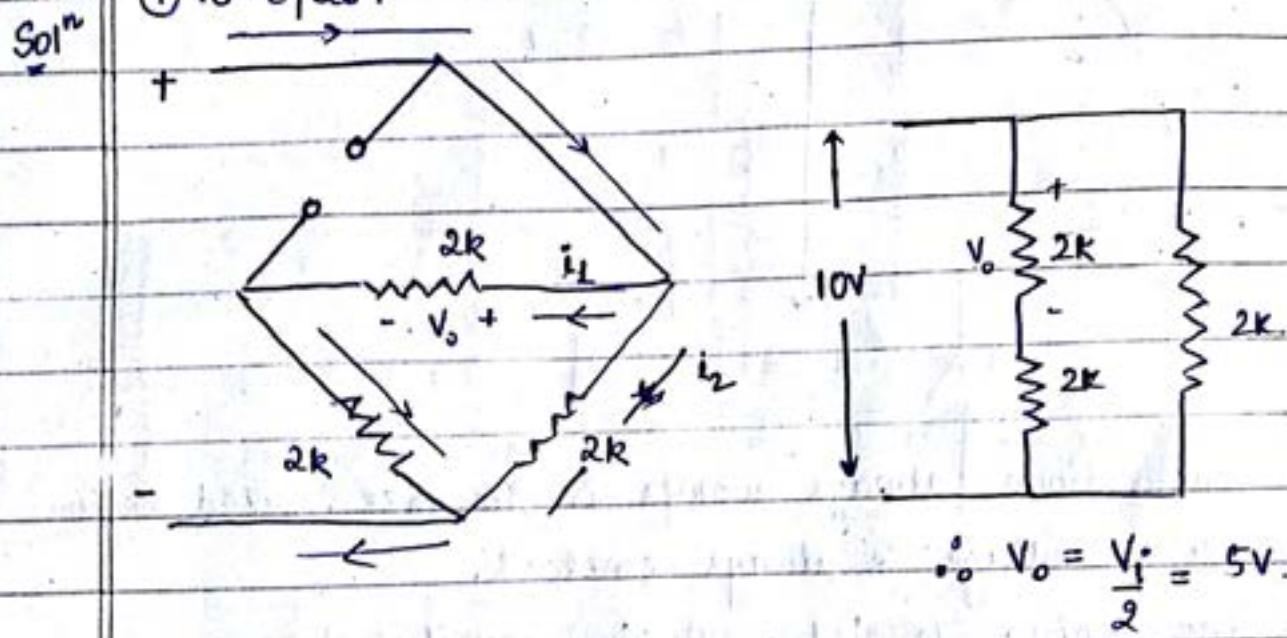
For -ve cycle



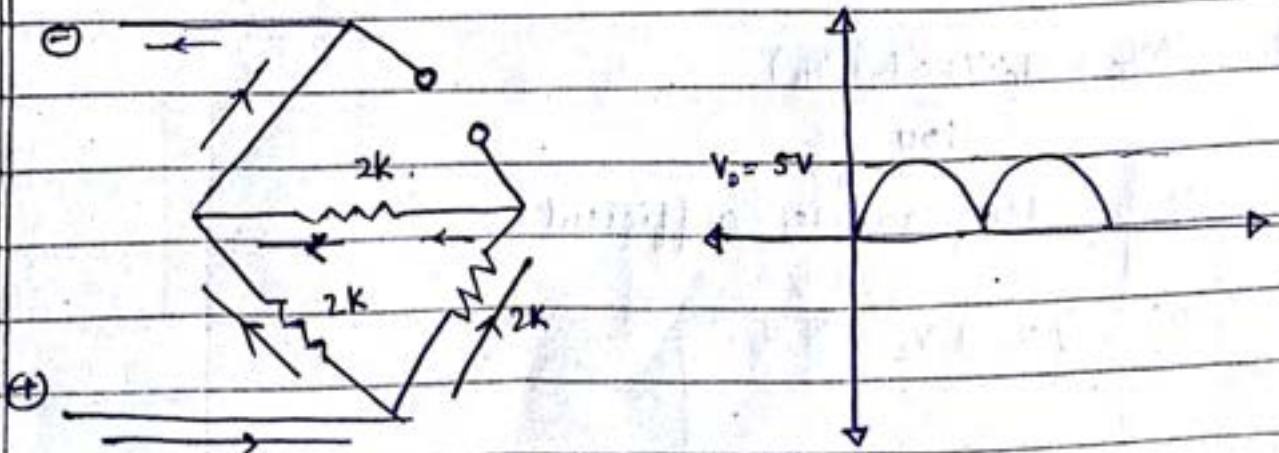
Q. Determine the output waveform and the D.C. level for the given circuit.



+ve cycle.

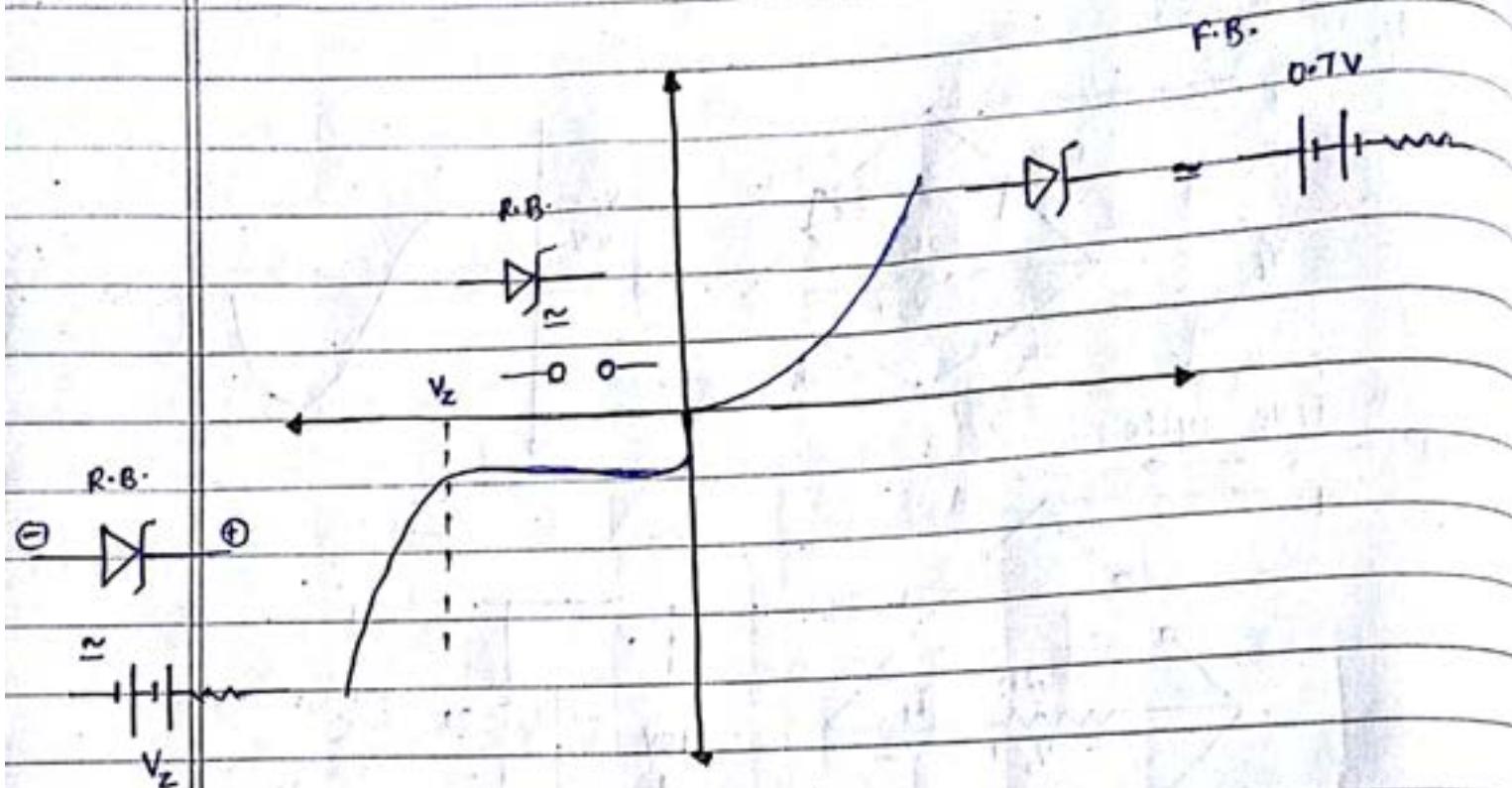
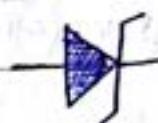


-ve cycle.



#

ZENER DIODES



1. A Zener diode always works in reverse biased region.
2. The zener voltage is always constant.
3. As the doping is \uparrow ed, no. of impurity charge carriers also \uparrow e which in turn reduces Zener voltage.

NOTE : Zener potential is very temperature sensitive as the temp. is \uparrow ed the zener voltage \uparrow es.

$$\Delta V_z = T_c V_z (T_2 - T_1) \\ \text{100}$$

∇T_c = temperature coefficient.

$$V_z' = \Delta V_z + V_z$$

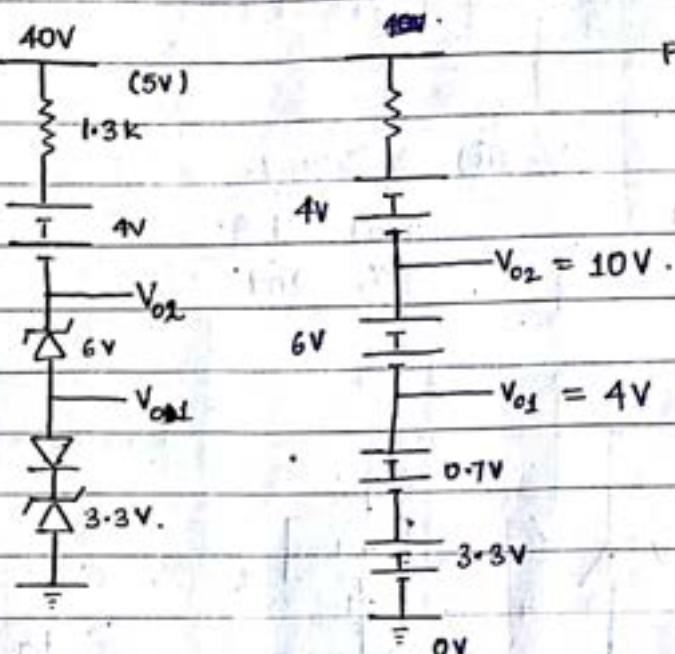
Q Find the new Zener potential if the temperature across a 10V zener diode is \uparrow ed to 100°C .
 $(\nabla T_c = 0.072\text{V}^\circ\text{C}^{-1})$

$$\Delta V_x = \frac{T_C V_x (V_2 - V_1)}{100}$$

$$V_x' = 10.0054 \text{ V}$$

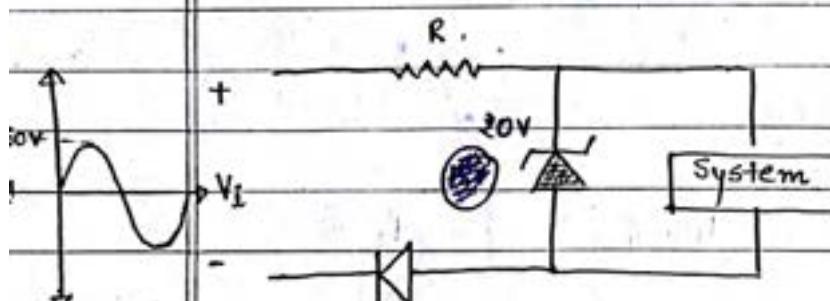
$$\Rightarrow \Delta V_x = \frac{(0.072 \times 10^{-2})(10)(75)}{100} = 0.0054$$

Q



Find V_{o1} and V_{o2}

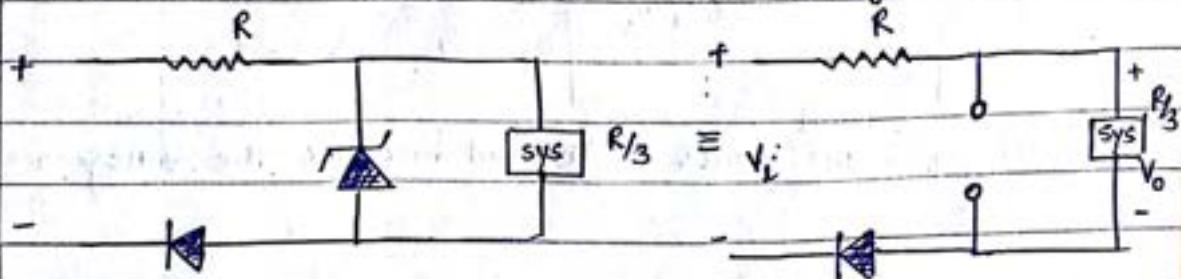
Q Determine the output voltage waveform for given circuit.



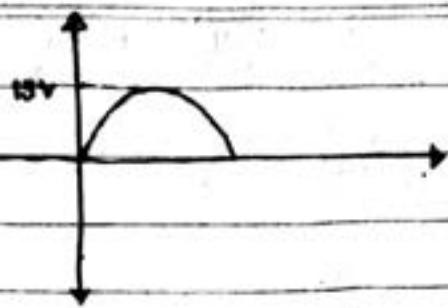
(i) Assume system resistance as $R/3$.

→ O.C. the zener diode and measure voltage across the diode

Soln (a) For +ve cycle



$$V_o = \frac{R/3 \times V_i}{R + R/3} = 15 \text{ V}$$



→ As this potential is less than the breakdown potential of zener diode, in this configuration zener diode will always be open circuit.

(b) +ve cycle.

$$(i) \quad V_i < 20.7$$

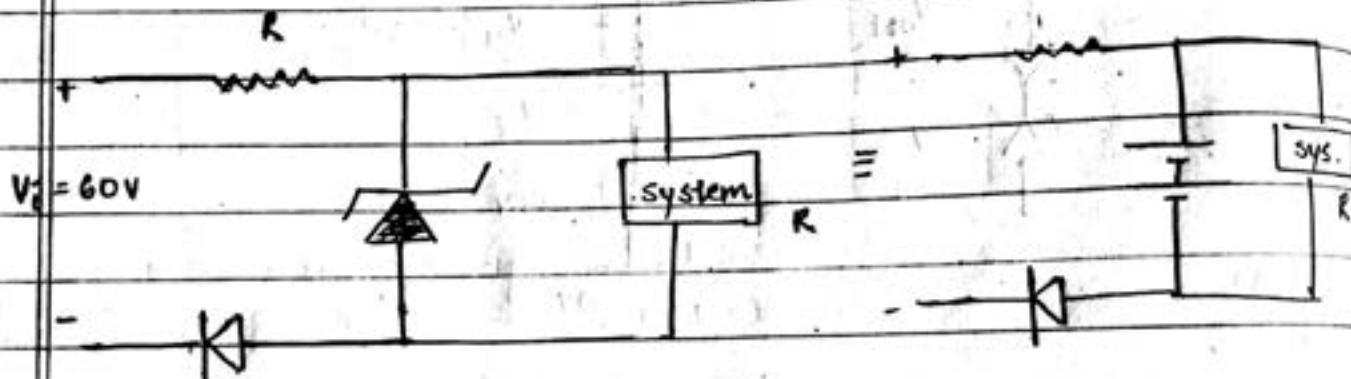
$$\text{Diode} = R \cdot B$$

$$V_o = 0$$

$$(ii) \quad V_i > 20.7$$

$$\text{Diode} = F \cdot B$$

$$V_o = 20V$$



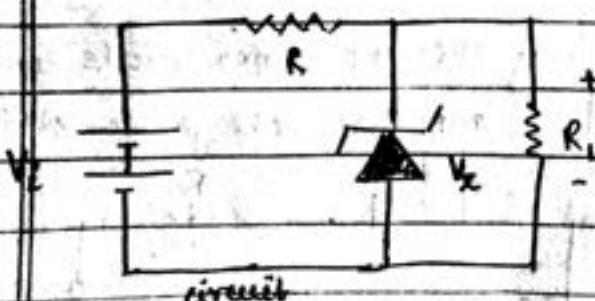
$$V_o = \frac{R}{R+R} (60V)$$

$$V_o = 30V$$

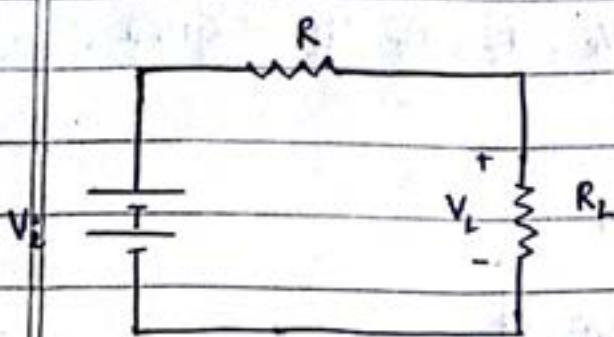


1 Fixed V_i , fixed R_1

I_L , V_L , I_R , I_Z , P_Z .



i) open the zener diode and measure the voltage across it



$$V_L = \frac{R_L V_i}{R_L + R}$$

CASE 1 :- $V_i < V_z$

Zener diode will be open circuit.

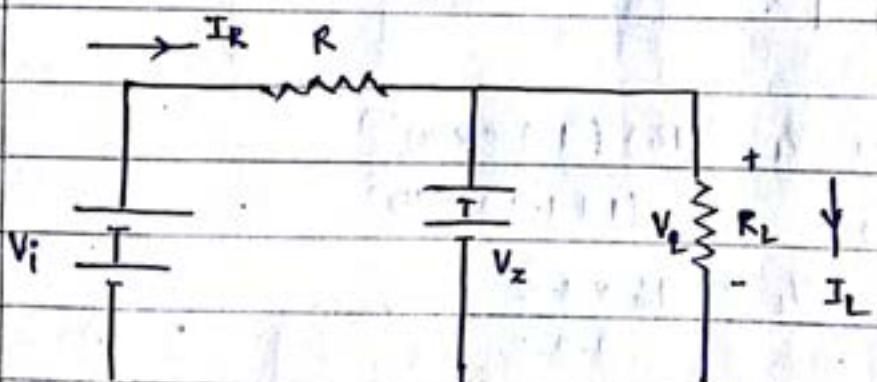
$$I_L = \frac{V_L}{R_L}, \quad P_z = 0$$

$$V_R = I_L R = V_i - V_L$$

$$I_R = I_L$$

$$I_z = 0$$

CASE 2 :- $V_L > V_z$



Zener diode will behave
as a battery of V_z

(a) $V_L = V_z$

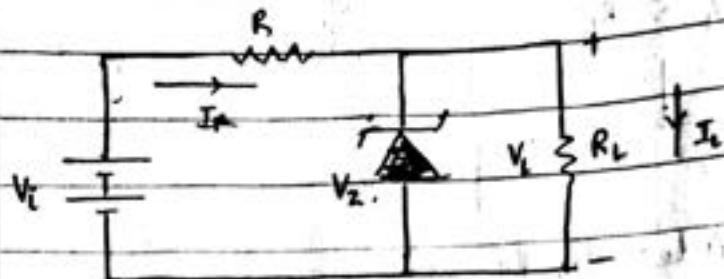
$$I_R = \frac{V_R}{R} = \frac{V_i - V_z}{R}, \quad P_z = V_z I_z$$

$$I_L = \frac{V_L}{R_L} = \frac{V_z}{R_L}$$

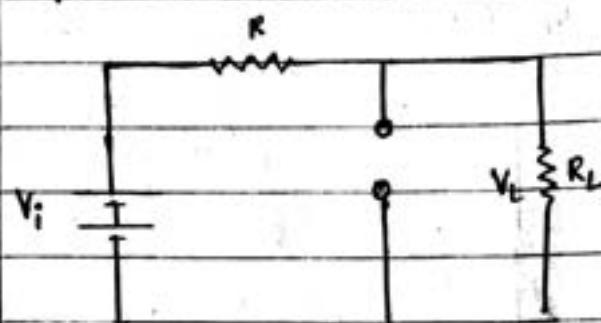
$$P_z = (I_R - I_L)^2 R$$

$$V_R = V_i - V_z$$

Q Determine the values of V_L , V_R , I_Z , P_Z . If $R = 1\text{ k}\Omega$,
 $V_Z = 10\text{ V}$, $R_L = 1.2\text{ k}\Omega$, $V_i = 16\text{ V}$.



Solⁿ (i) open the zener diode.



$$V_L = \frac{V_i R_L}{R + R_L} \Rightarrow V_L = \frac{(16)(1.2 \times 10^3)}{(1 + 1.2) \times 10^3}$$

$$V_L = \frac{16 \times 1.2}{2.2}$$

$$V_L = 8 \times 10 = 8.72\text{ V}$$

$$V_R = V_i - V_L = 16 - 8.72 \\ = 7.28\text{ V}$$

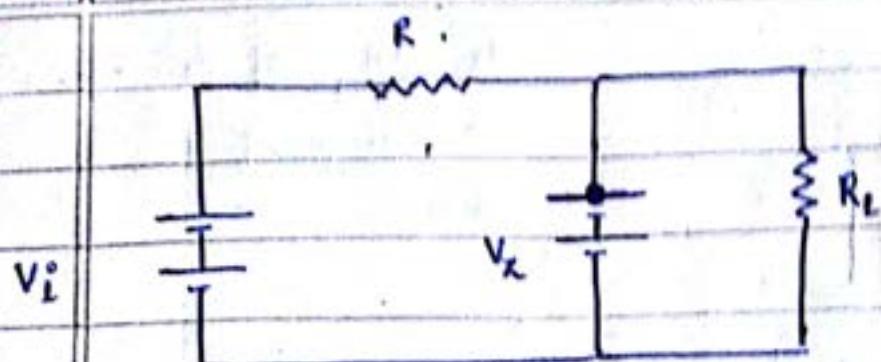
$$I_Z = 0$$

$$P_Z = 0$$

(b) $R_L = 3\text{ k}\Omega$, $R = 1\text{ k}\Omega$, $V_Z = 10\text{ V}$, $V_i = 16\text{ V}$

$$V_L = (16) \left(\frac{3}{3+1} \right) = 12\text{ V}$$

$V_L > V_Z$ zener behaves as battery



$$V_L = 10V$$

$$V_R = V_L - V_Z$$

$$= 10 - 6$$

$$V_R = 4V$$

$$I_Z = I_R - I_L$$

$$I_Z = \frac{6}{10^3} - \frac{10}{3 \times 10^3}$$

$$I_Z = 10^{-3} \left(6 - \frac{10}{3} \right)$$

$$P_Z = V_Z I_Z$$

$$= (10) (2.67 \times 10^{-3})$$

$$P_Z = 2.67 \times 10^{-2}$$

$$I_K = 10^{-3} (6 - 3.33)$$

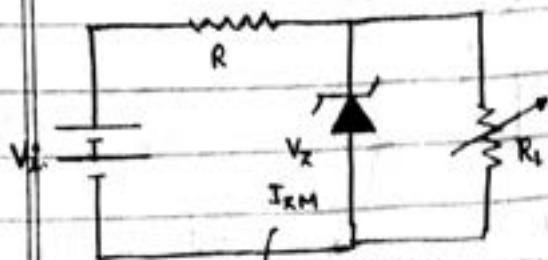
$$I_K = 2.67 \times 10^{-3}$$

* FIXED V_i , VARIABLE R_L .

→ Range of R_L

→ Range of I_L

→ V_R



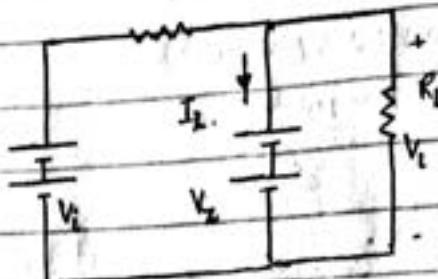
↳ maximum zener current.

(i) $R_{L\min}$ is the resistance at which zener diode is on.

$$\frac{I_R}{R} = \frac{I_L}{R_L}$$

$$V_Z = V_L = \frac{V_i R_L}{R + R_L}$$

$$R_{L\min} = \frac{V_Z R}{V_i - V_Z}$$



$$\rightarrow I_{L(\max)} = \frac{V_L}{R_{L(\min)}}$$

$$\rightarrow V_R = V_L - V_Z$$

$$I_L = I_R - I_{Z\max}$$

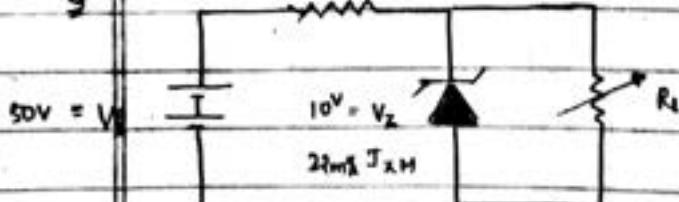
$$I_R = \frac{V_R}{R}$$

$$I_{L\min} = I_R - I_{Z(\max)}$$

$$R_{L\max} = \frac{V_L}{I_L} = \frac{V_Z}{I_{L(\min)}}$$

Q

$$R = 1 \text{ k}\Omega$$



$R_L \rightarrow I_L$

$$\text{Soln} \quad V_L = \frac{V_i R_{L(\min)}}{R_L + R_{\text{min}}} = V_Z$$

$$R_{\text{min}} = 100 \Omega$$

$$\Rightarrow 50 R_{L(\min)} = 10 R_{L(\min)} + 10000$$

$$\Rightarrow \frac{50 (R_{L(\min)})}{R_{L(\min)} + 1000} = 10$$

$$40 R_{L(\min)} = 10000$$

$$R_{L(\min)} = 250 \Omega$$

$$I_L = \frac{V_L}{R_L} = 10' \xrightarrow{\text{min.}} I_L(\max) = 0.04 A$$

$$I_L(\max) = 40 \text{ mA}$$

$$I_R = I_{ZM} + I_L$$

$$I_L(\min) = I_R - I_{ZM}$$

$$I_R = \left(\frac{R_L}{R+R_L} \right) \frac{V_i}{R_L} = \frac{50}{1250} = \frac{1}{25} \Rightarrow 40 \text{ mA} - 32 \text{ mA} \\ = 8 \text{ mA}$$

$$I_L(\min) =$$

$$V_R = V_i - V_Z$$

$$R_L(\max) = \frac{10}{8} = 1.25 \text{ k}\Omega$$

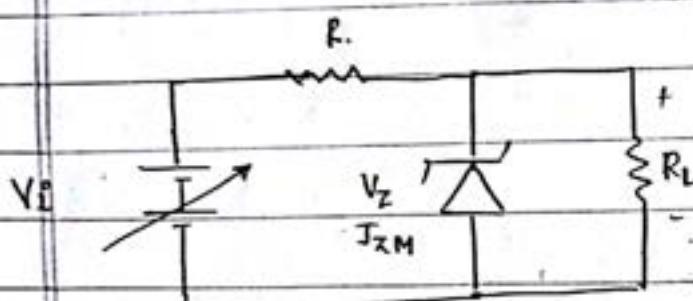
$$V_R = 50 - 10$$

$$V_R = 40 \text{ V}$$

$\rightarrow R_L$ (range) :- 250Ω to 1250Ω .

$\rightarrow I_{ZM}$ (range) = 8 mA to 40 mA

VARIABLE V_i ; FIXED R_L



$$\rightarrow V_L = \frac{V_i R_L}{R_L + R}$$

$$\rightarrow I_L = \frac{V_L}{R_L} = \frac{V_Z}{R_L}$$

Assuming zener diode is on.

$$\rightarrow I_R = I_{ZM} + I_L$$

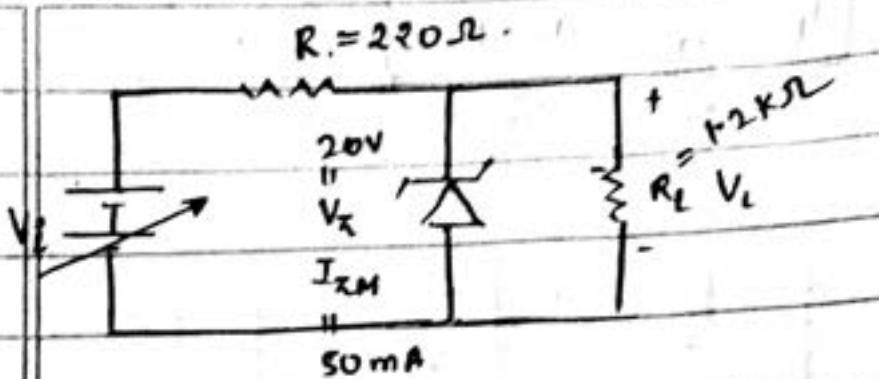
$$V_L = V_Z$$

$$V_R = I_R (R)$$

$$V_Z = \frac{V_i R_L}{R_L + R}$$

$$V_i(\max) = V_R + V_Z$$

$$V_i(\min) = \frac{V_Z (R+R_L)}{R_L}$$



$$V_L = \frac{V_i R_L}{R_L + R}$$

$$V_{i(\min)} = (20) (1200 + 220)$$

1200

$$= 23.66 \text{ V}$$

$$V_{i(\max)} = V_R + V_L$$

$$= 20 + I_R (R)$$

$$= 20 + 220 (I_{XM} + I_L)$$

$$= 20 + 220 \left(50 \times 10^{-3} + \frac{20}{1200} \right)$$

$$= 20 + 220 (50 \times 10^{-3} + 16.66 \times 10^{-3})$$

$$= 20 + 220 (66.66) \times 10^{-3}$$

$$= 20 + 14.66$$

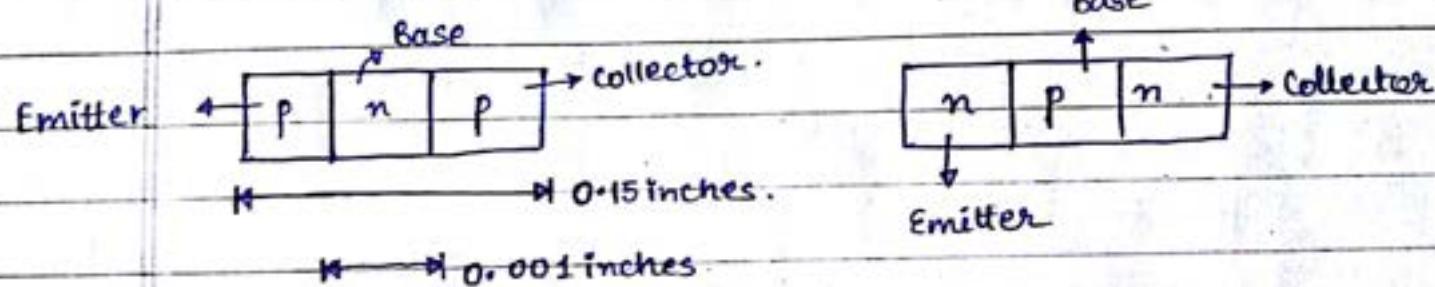
$$V_{i(\max)} = 34.66 \text{ V}$$

BIPOLAR JUNCTION TRANSISTORS

1. A BJT was developed by three scientists :- William Shockley, Bardeen and Brattain. in 1947 at Bell laboratories.
2. Bipolar means both electrons and holes constitute current
3. In a B.J.T. two p-n junctions are present. ∴ the term junction comes in B.J.T.
4. Transistor is derived from two words transfer resistor as it has the resistance from low to high value.

#

CONSTRUCTION OF B.J.T.



- Collector > Emitter > Base (Area)
- Emitter > Collector > Base (Doping level)

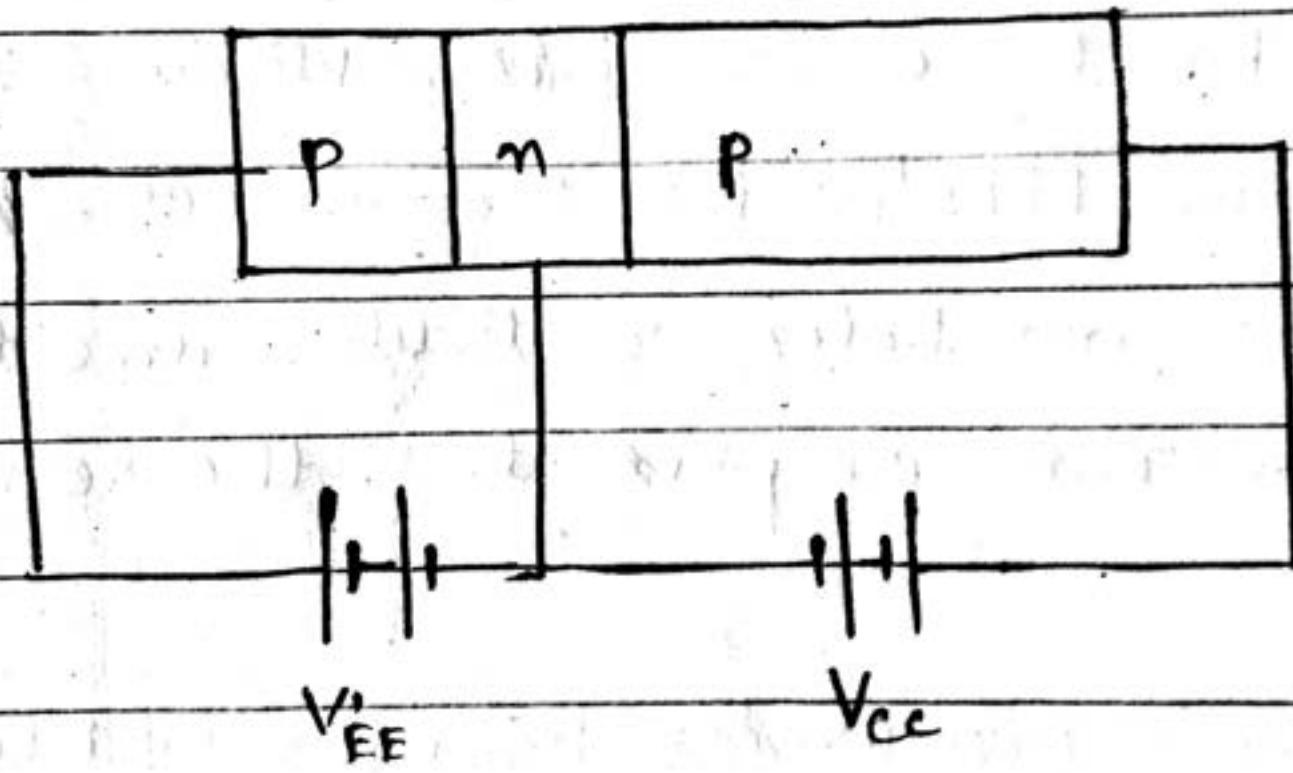
• WORKING

E-B	C-B	operation	F B	I B	C
FB	FB	Saturation region (1)	P	I n	P
FB	RB	Active (Amplifier)			
RB	FB	Cut-off (0)			
RB	RB	Reverse saturation region			

E-B. B-C junction junction

CASE 1. $E-B \rightarrow FB$.

$B-C \rightarrow FB$

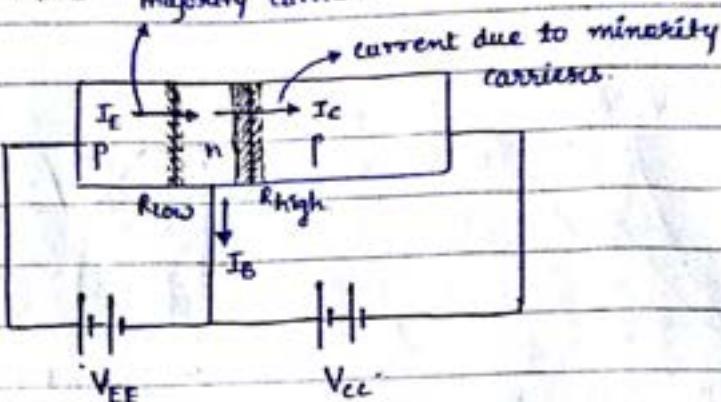


* For biasing Emitter should be forward biased.
Collector " " reverse " .

KUMAR
Date: 26/10/2017
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$E-B \rightarrow F-B$

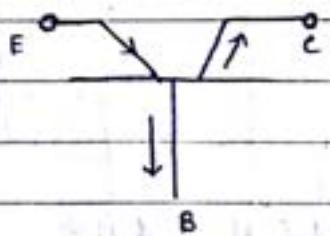
$C-B \rightarrow R-B$ current due to majority carriers



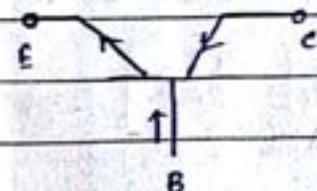
$$I_E = I_C + I_B$$

1. Transistor operates when the emitter-base junction is forward biased and collector-base junction is reverse biased.
2. In the emitter-base region, holes are the majority carriers and they flow from emitter to base.
3. In collector-base junction, holes are the minority carriers in the base region and flow under the influence of reverse biasing.
4. The emitter current is very high, the collector current is approximately equal to emitter current.

F



pnp (pointing in)



npn (not pointing in)

→ $I_C = I_C(\text{Majority}) + I_C(\text{Minority})$

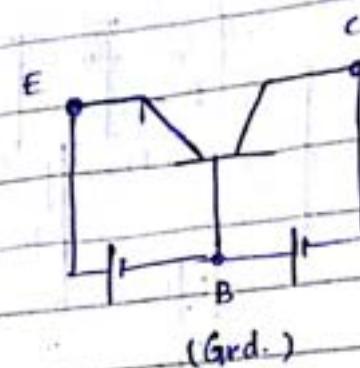
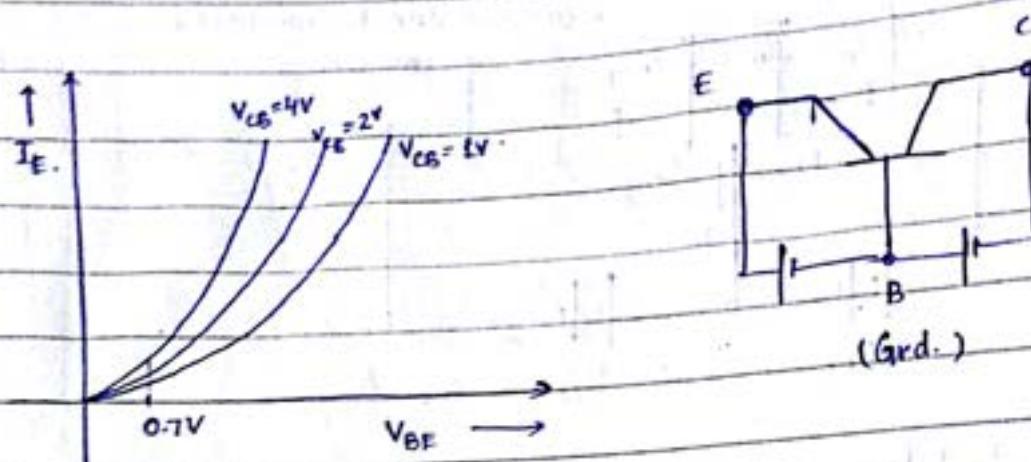
→ There are 3 configurations in a BJT.

a. common-base configuration.

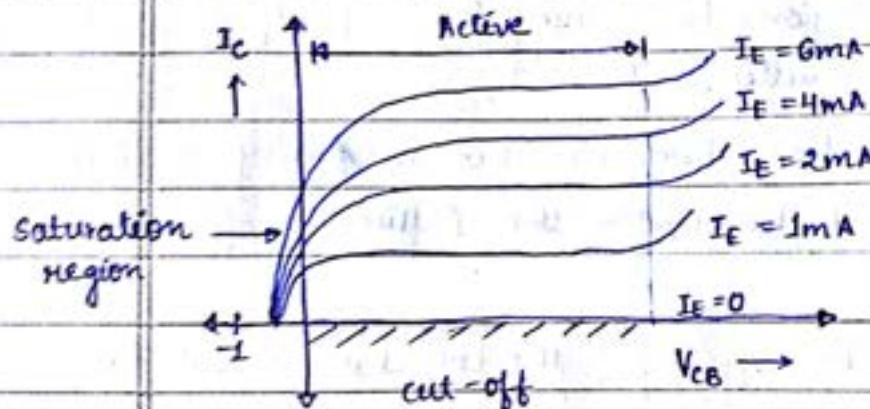
b. common-emitter "

c. common-collector "

1. COMMON BASE CONFIGURATION



- The input characteristics of B-J-T. is similar to diode characteristics in forward biased region.
- The characteristics depends on output voltage V_{CB} .



- As seen in the Graph collector current is approximately equal to emitter current.

#

ALPHA (α)

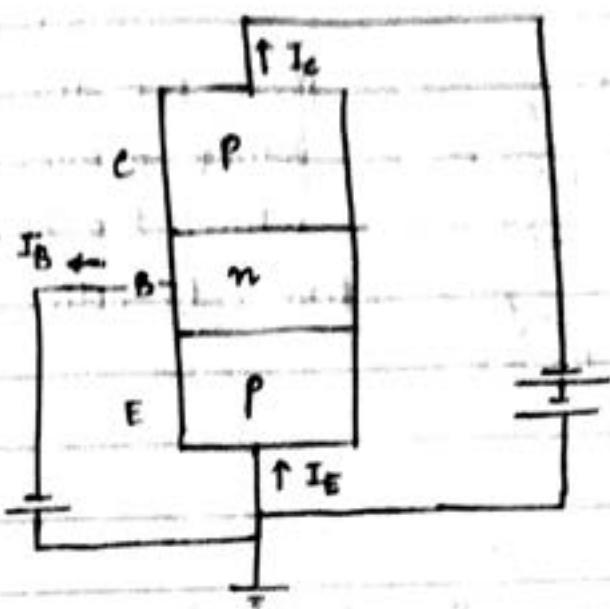
Alpha is called as common-base amplification factor.

$$\alpha = \frac{I_C}{I_E} \leq 1. \quad (\text{D.C. biasing})$$

$$\alpha = \frac{\Delta I_C}{\Delta I_E} \quad (\text{A.C. biasing})$$

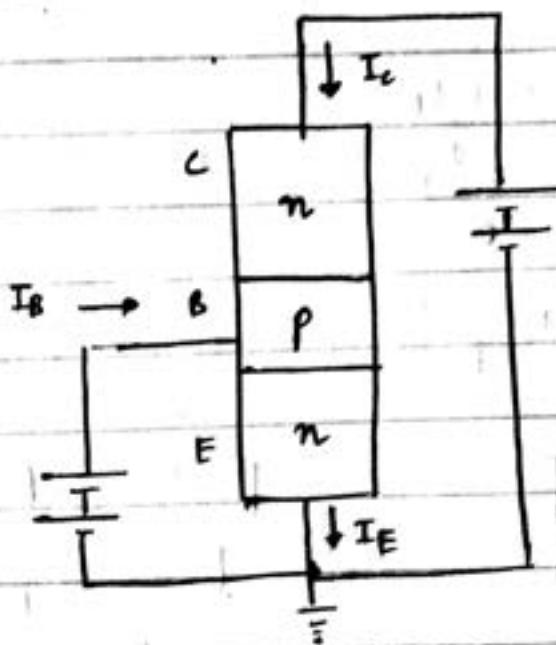
II COMMON - Emitter CONFIGURATION

1.



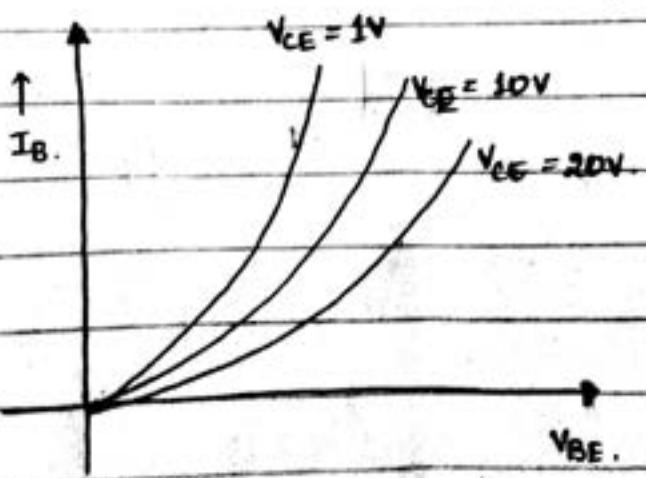
pnp.

2.

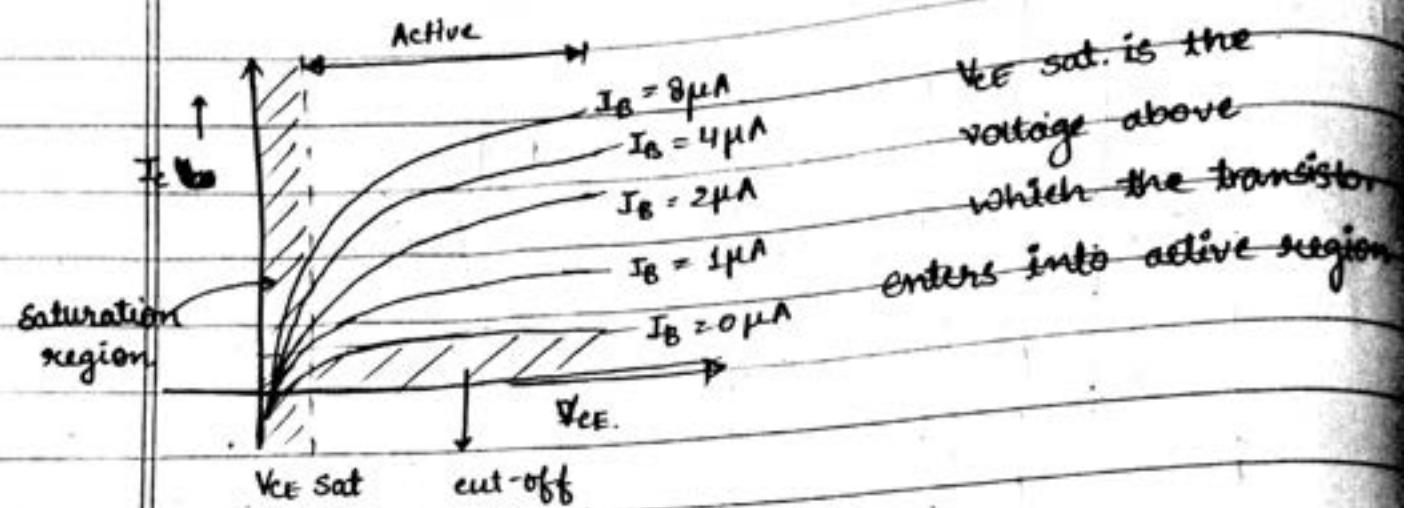


npn.

INPUT CHARACTERISTICS.



OUTPUT CHARACTERISTICS



β. (common emitter amplification factor.).

$$\beta = \frac{I_C}{I_B} \gg 1$$

$$I_E = I_C + I_B$$

$$\alpha = \frac{I_C}{I_E} \Rightarrow \frac{I_E}{I_C} = \frac{I_B}{I_C} + 1$$

$$\Rightarrow \frac{1}{\alpha} = \frac{1}{\beta} + 1$$

$$\alpha = \frac{\beta}{\beta + 1}$$

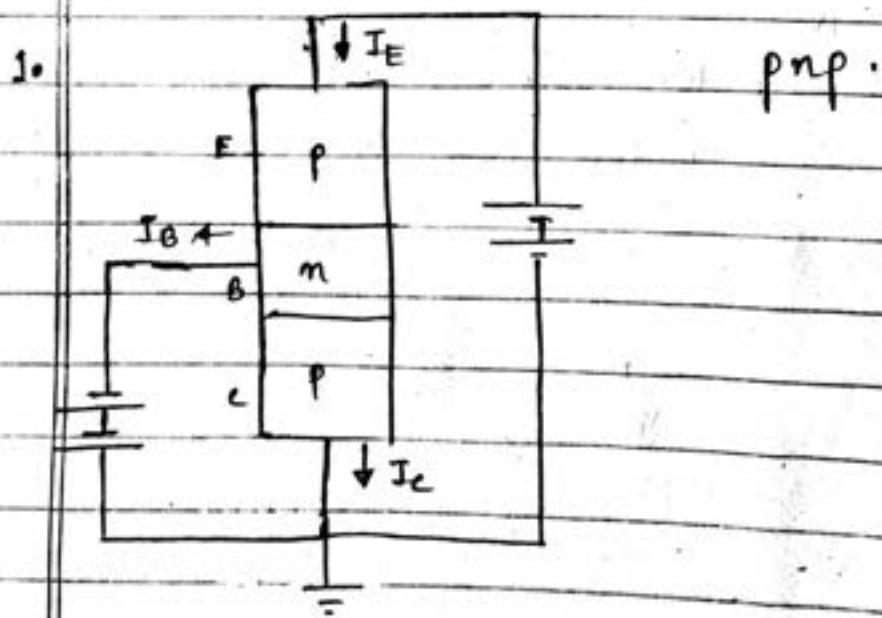
$$\Rightarrow \beta\alpha + \alpha = -\beta$$

$$\beta = -\frac{\alpha}{\alpha - 1}$$

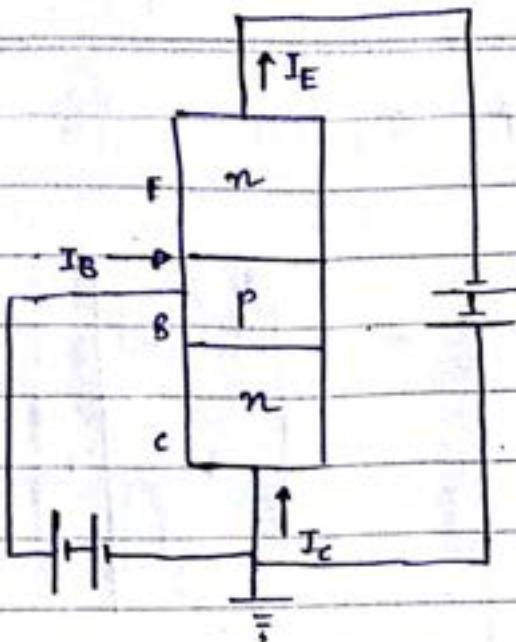
$$\beta = \frac{\alpha}{1 - \alpha}$$

#

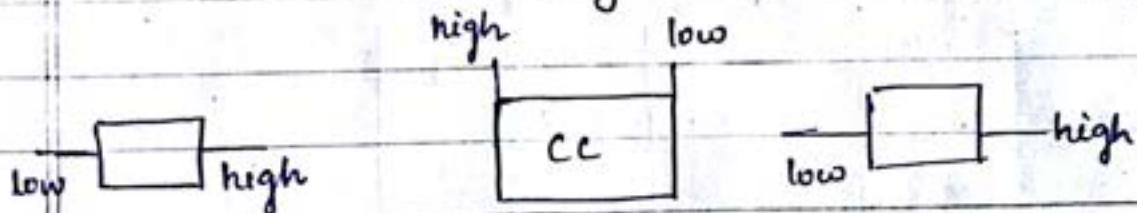
COMMON COLLECTOR CONFIGURATION.



2.



- The input and output characteristics of common collector are same as common emitter configuration.
- In CB and CE configurations, the input resistance is low and the output resistance is high.
Yes in CC just reverse happens.
This is the reason why CC is used for impedance matching.



γ (common-emitter collector amplification factor)

$$\gamma = \frac{I_E}{I_B}$$

$$I_E = I_B + I_C$$

$$\Rightarrow \frac{I_E}{I_B} = 1 + \frac{I_C}{I_B}$$

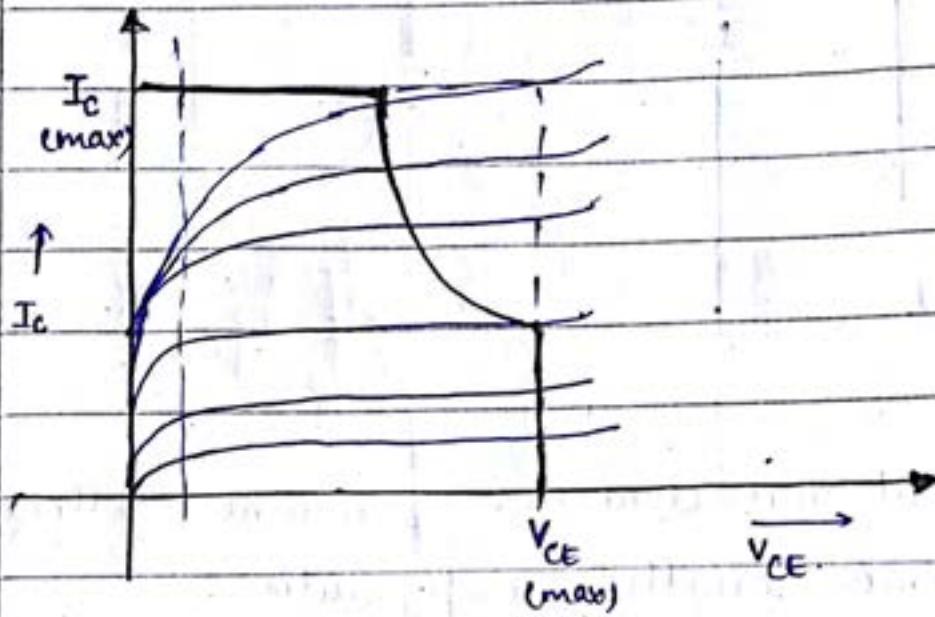
$$\gamma = \beta + 1$$

$$\gamma = \left(\frac{\alpha}{1-\alpha} \right) + 1$$

$$\gamma = \frac{\alpha + 1 - \alpha}{1 - \alpha}$$

$$\boxed{\gamma = \frac{1}{1-\alpha}}$$

LIMITS OF OPERATION

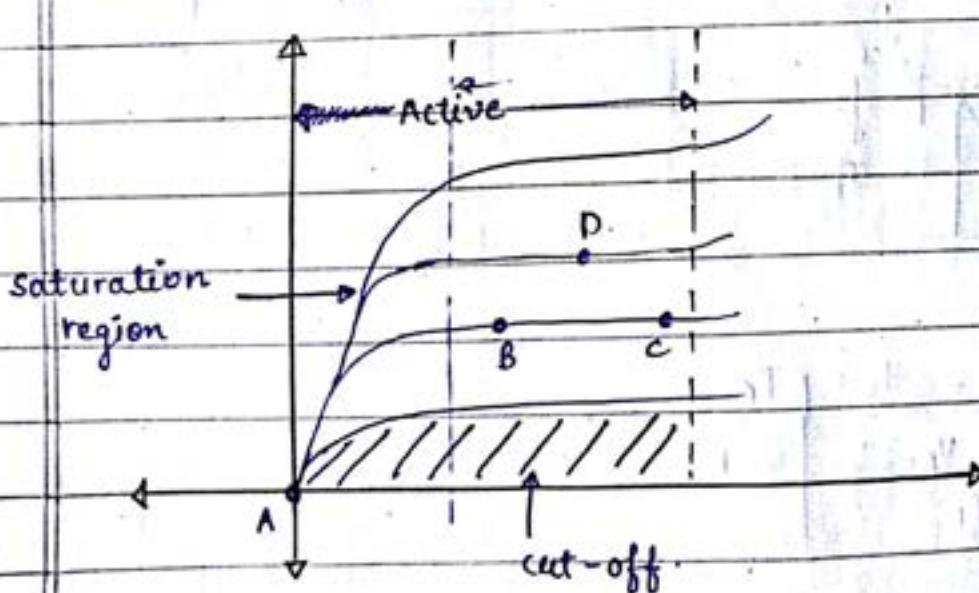


$$V_{CE(\max)} = \frac{P_{C\max}}{I_{C(\max)}}$$

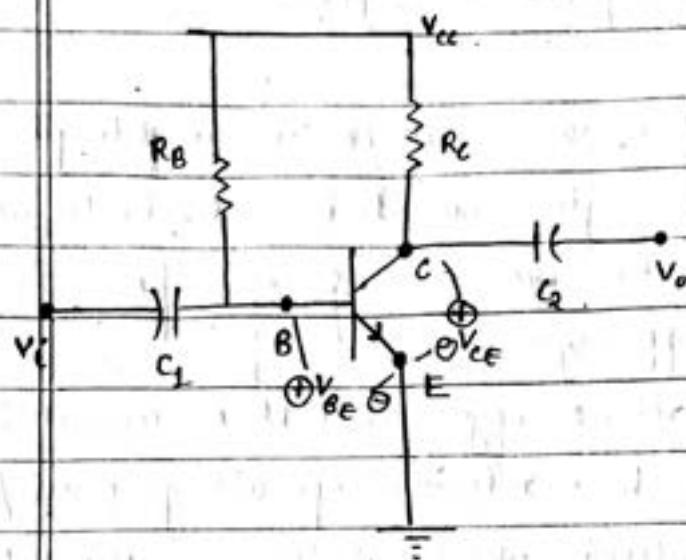
→ Limit of operation defines the boundary within which the transistor can operate freely.

D.C. BIASING.

- operating point or quiescent point or Q-point.
- Point A lies in the cut-off region. ∴ it is unsuitable pt.
- Point B lies in the active region but it is not stable as slight variation can cause the transistor to enter into either saturation or cut-off region.
- Point C also lies in the active region but it is unsuitable because it is very close to maximum operating point/limit.
- Point D is the best operating pt. as it lies in the active region and is also stable.
- $V_{BE} = 0.7V$
- $I_E = I_C + I_B$.
- $I_E = (1+\beta) I_B$.
- $I_C = \beta I_B$



FIXED BIAS CONFIGURATION

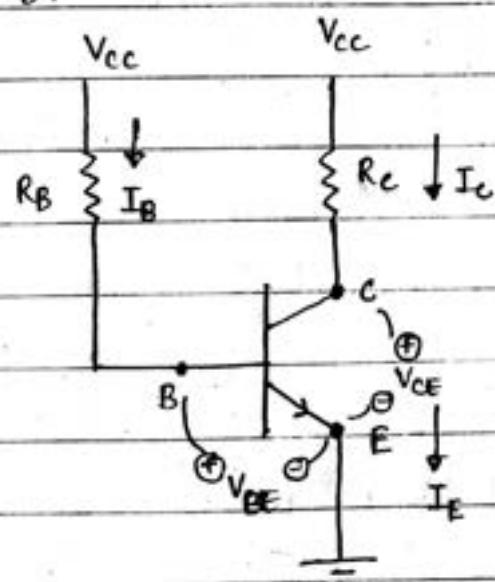


In DC, $f = 0$

$$X_C = \frac{1}{2\pi f C} = \infty$$

\therefore capacitor acts as open circuit.

(a) I_B .



Applying KCL rule.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

(b) I_c

We know that, $I_c = \beta I_B$.

$$\Rightarrow I_c = \beta \left(\frac{V_{CC} - V_{BE}}{R_B} \right)$$

(c) V_{CE}

$$V_{CC} - I_c R_c - V_{CE} = 0$$

$$\Rightarrow V_{CE} = V_{CC} - I_c R_c$$

(d) V_c

$$V_{CE} = V_c - V_E$$

as E is grounded $\therefore V_E = 0$.

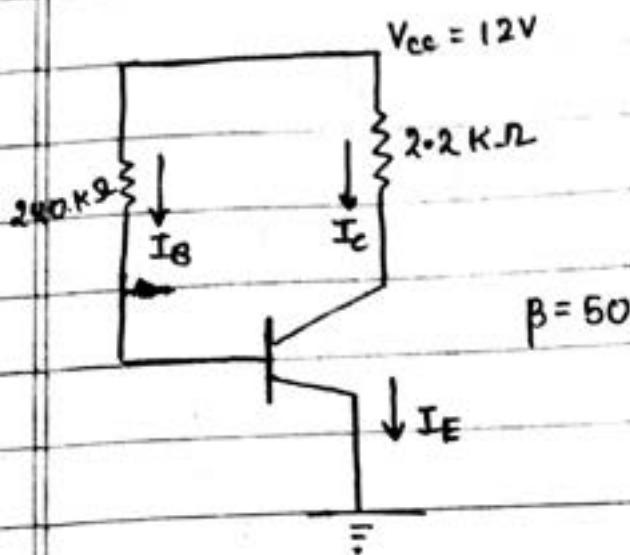
$$V_{CE} = V_c$$

②

$$V_B = V_{BE} + V_E$$

$$V_{BE} = V_B - V_E$$

Q



Determine I_{BO}, I_{CO}, V_{CEO}, V_C,

$$V_B > V_{BE}$$

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$\Rightarrow I_C = \beta I_B$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B}$$

$$\Rightarrow I_C = 50 (0.04708 \times 10^{-3})$$

$$I_B = \frac{12 - 0.7}{240 \times 10^3}$$

$$I_C = 2.354 \times 10^{-3} \text{ Amp}$$

$$I_B = 0.04708 \times 10^{-3} \text{ Amp}$$

$$\Rightarrow V_{CE} - I_C R_C = V_{CE}$$

$$\Rightarrow V_{CE} = 12 - (2.354) (2.2 \times 10^3) (10^{-3})$$

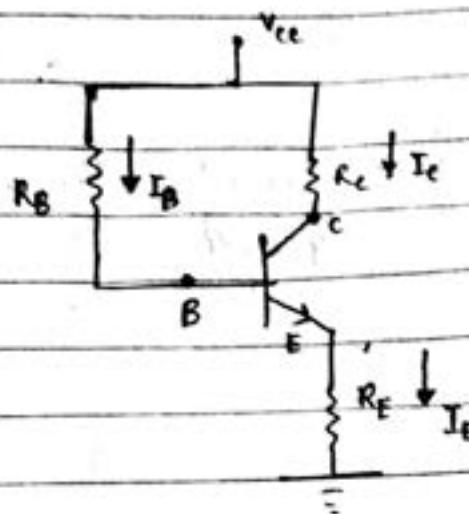
$$\Rightarrow V_{CE} = 12 - 5.1788$$

$$\Rightarrow V_{CE} = 6.821 \text{ Volts}$$

$$V_{BC} = V_B - V_C$$

$$= 0.7 - 6.821 = -6.121 \text{ Volts}$$

(Q.) Emitter Bias Configuration



$$\rightarrow V_{cc} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$I_B = \frac{V_{cc} - V_{BE} - I_E R_E}{R_B} \quad \text{if } I_E = (1 + \beta) I_B$$

$$R_B I_B = V_{cc} - V_{BE} - R_E (1 + \beta) I_B$$

$$\Rightarrow I_B = \frac{V_{cc} - V_{BE}}{R_B + R_E (1 + \beta)}$$

$$\rightarrow I_C = \beta I_B$$

$$\rightarrow V_{cc} - I_C R_E = V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CE} = V_{cc} - I_C R_E - I_E R_E$$

$$\Rightarrow I_E = I_B + I_C$$

assume, $I_C \approx I_E$

$$V_{CE} = V_{cc} - I_C (R_E + R_E)$$

$$\rightarrow V_E = I_E R_E$$

$$\rightarrow V_B = V_{BE} + V_E$$

$$\rightarrow V_C = V_{CC} - I_C R_C \\ = V_{CC} + V_E$$

Q The value of R_B is $430 \text{ k}\Omega$

$$R_E = 2 \text{ k}\Omega, R_C = 1 \text{ k}\Omega, V_{CC} = 20 \text{ Volts}, \beta = 50$$

$$\text{Ans } V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$$

$$20 - 0.7 - (430)(10^{-3})(I_B) - (10^3)[1+50](I_B) = 0$$

$$\Rightarrow I_B (430 \times 10^{-3} + 51 \times 10^3) = 19.3$$

$$\Rightarrow I_B = 0.04012 \times 10^{-3} \text{ Amp}$$

$$I_C = \beta I_B$$

$$\Rightarrow I_C = 2.006 \times 10^{-3} \text{ Amp}$$

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

$$\Rightarrow V_{CE} = 20 - (2.006 \times 10^{-3})(2 \times 10^3) - (51)(0.04012 \times 10^{-3})(10^3) = 0$$

$$\Rightarrow V_{CE} = 20 - 4.012 - 2.04612$$

$$V_{CE} = 13.94 \text{ Volts}$$

$$V_E = I_E R_E = (50+1)(0.04012 \times 10^{-3})(10^3)$$

$$= 2.04 \text{ Volts}$$

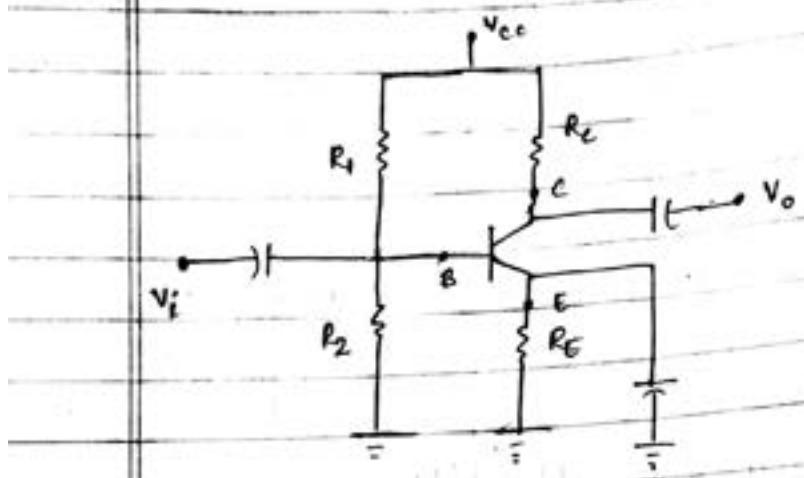
$$V_C = V_{CE} + V_E$$

$$= 13.94 + 2.04$$

$$= 16.04$$

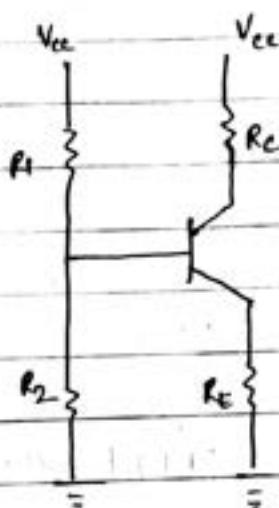
$$V_B = 2.74 \text{ Volts}$$

3- VOLTAGE DIVIDER CONFIGURATION

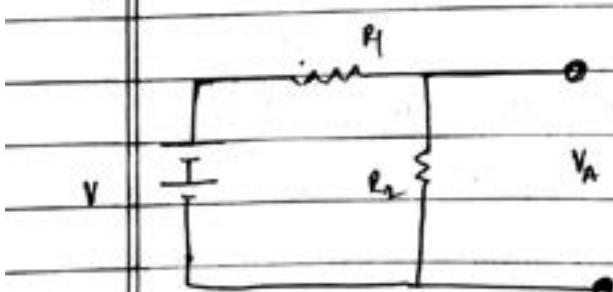


(i) Remove all capacitors.

(ii)



~~#~~ EXACT ANALYSIS

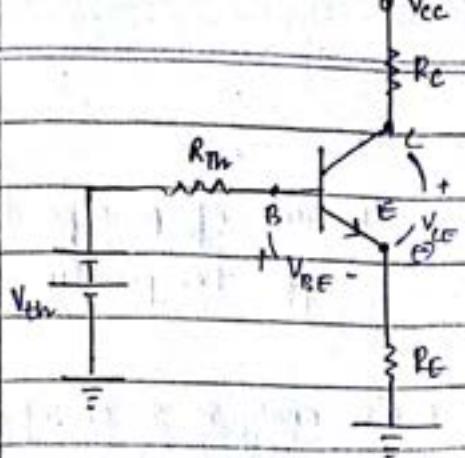


Thevenin's
theorem

$$V_{th} = \frac{R_2}{R_1 + R_2} V_i$$

$$R_{th} = R_1 \parallel R_2$$

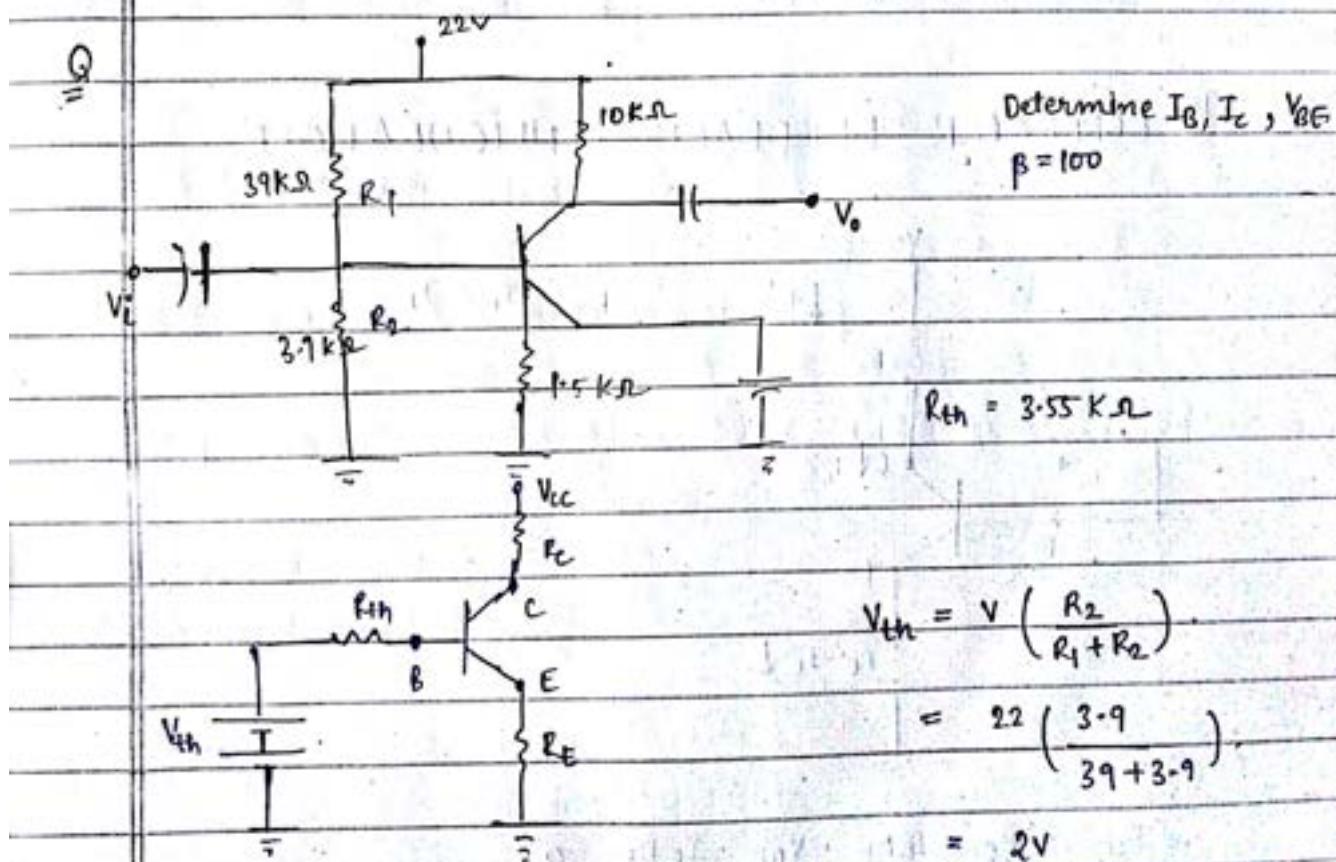
$$\frac{1}{R_{th}} = \frac{1}{R_1} + \frac{1}{R_2}$$



$$\rightarrow V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$I_E = (1 + \beta) I_B$$

$$I_B = \frac{V_{th} - V_{BE}}{R_{th} + (1 + \beta) R_E}$$



$$V_{th} - I_B R_{th} - V_{BE} - I_E R_E = 0$$

$$I_C = 0.838 \text{ mA}$$

$$I_B = \frac{2 - 0.7}{(3.55 \times 10^3) + (101) 1.5 \times 10^3}$$

$$I_B = 8.3 \mu\text{A}$$

$$V_{cc} - I_C R_C = 22 - \frac{(10 + 1.5) \times 10^3}{10^3} \times 0.838 \times 10^{-3}$$

$$= 19.363 \text{ mV}$$

APPROXIMATE ANALYSIS.

Condition :- $\beta R_E > 10 R_2$
 Assume $I_B \approx 0$

→ value of β depends upon temperature.

$$(i) V_E = V_{BE} - V_{BE}$$

→ This analysis is independent of β and is therefore advantageous to use this method.

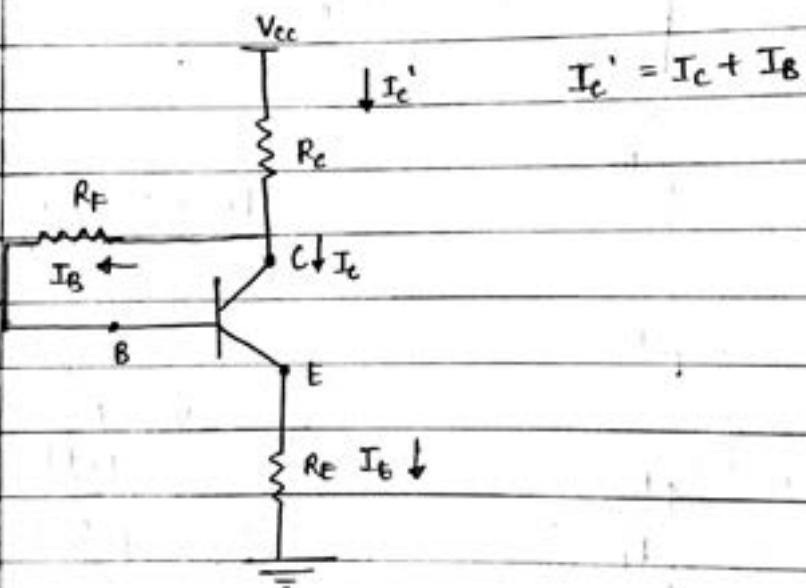
$$(ii) V_B = \frac{R_2 V_{CC}}{R_1 + R_2}$$

$$(iii) I_E = \frac{V_E}{R_E}$$

$$(iv) I_C = I_E \text{ at } I_B \approx 0$$

$$(v) V_{CE} = V_{CC} - I_C (R_E + R_F)$$

4. COLLECTOR FEEDBACK CONFIGURATION



$$\Rightarrow V_{CC} - I_c' R_C - I_B R_F - V_{BE} - I_E R_E = 0$$

$$\Rightarrow V_{CC} - \beta I_B R_C - I_B R_F - V_{BE} - \beta I_B R_E = 0 \quad \text{Assume } I_c' \approx I_c \approx \beta I_B \\ \Rightarrow I_B (\beta R_C + R_F + \beta R_E) = V_{CC} - V_{BE}$$

$$\Rightarrow I_B = \frac{V_{CC} - V_{BE}}{\beta (R_C + R_E) + R_F}$$

$$(ii) I_C = \beta I_B$$

$$(iii) V_{CE} =$$

$$V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$$

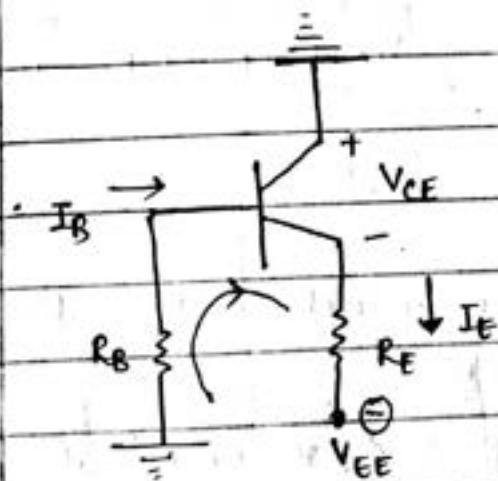
$$\therefore V_{CE} = V_{CC} - I_C R_C - I_E R_E$$

$$V_{CE} = V_{CC} - (R_C + R_E) I_B \beta$$

5. Emitter Follower Configuration

↓
COMMON COLLECTOR.

→ whenever we give supply
from emitter then we
give -ve supply for F.B.



$$-I_B R_B - V_{BE} - I_E R_E + V_{EE} = 0$$

$$I_E = (1 + \beta) I_B$$

$$\therefore V_{EE} = -I_B R_B - V_{BE} - (1 + \beta) I_B R_E = 0$$

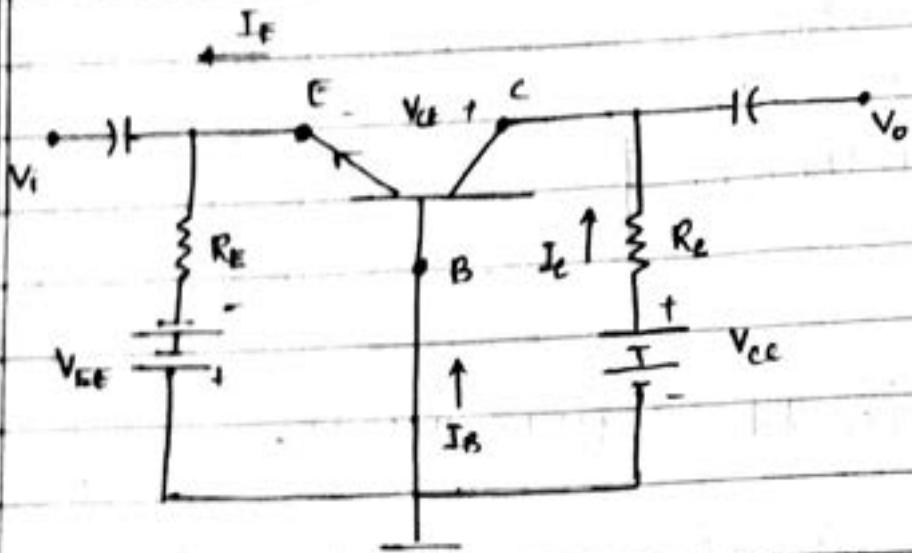
$$\therefore I_B = \frac{V_{EE} - V_{BE}}{R_B + R_E (1 + \beta)}$$

$$\rightarrow V_{CE} =$$

$$-V_{CE} - I_E R_E + V_{EE} = 0$$

$$V_{CE} = V_{EE} - I_E R_E$$

6. COMMON BASE CONFIGURATION.



$$\Rightarrow -V_{BE} - I_E R_E + V_{EE} = 0 \quad \Rightarrow V_{CE} - I_C R_L - V_{CE} - I_E R_E + V_{EE} = 0$$

$$\boxed{I_F = \frac{V_{EE} - V_{BE}}{R_E}}$$

$$\boxed{V_{CE} = V_{CC} + V_{EE} - I_C R_L - I_E R_E}$$

Q Why is D.C. biasing necessary?

Ans 1. Biasing is done to stabilize the circuit so that the transistor operates in active region.

2. There are some parameters like β and reverse sat current which are highly dependent on temp.

The role of biasing is to make the circuit less dependent on temp.

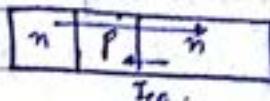
BIAS STABILIZATION

→ I_c depends upon temperature.

→ $I_c \rightarrow I_{co}$ (\uparrow with $\uparrow T$)

β (\uparrow with $\uparrow T$)

V_{BE} (\downarrow with $\uparrow T$)



$$I_c = \beta I_B + (\beta + 1) I_{co}$$

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$$\rightarrow S(\beta) = \frac{\Delta I_c}{\Delta \beta} \quad \rightarrow S(V_{BE}) = \frac{\Delta I_c}{\Delta V_{BE}} \quad \rightarrow S(I_{co}) = \frac{\Delta I_c}{\Delta I_{co}}$$

→ if ΔI_c is higher than the circuit is not stable.

→ if ΔI_c is lower than the circuit is stable.

→ Total effect on I_c .

$$\Delta I_c = S(\beta) \Delta \beta + S(V_{BE}) \Delta V_{BE} + S(I_{co}) \Delta I_{co}$$

$S(I_{co})$

1. Fixed bias. $S(I_{co}) \approx \beta$

2. Emitter bias. $S(I_{co}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E}$

3. Voltage divider bias. $S(I_{co}) = \frac{\beta(1 + R_{th}/R_E)}{\beta + R_{th}/R_E}$

4. feedback Bias ($R_E = 0$) $S(I_{co}) = \frac{\beta(1 + R_B/R_E)}{\beta + R_B/R_E}$

fixed bias.

$$I_B = \frac{V_{cc} - V_{BE}}{R_B}$$

$I_B \approx \text{constt}$

$$\uparrow I_c = \beta I_B + (1 + \beta) I_{co} \uparrow$$

emitter bias.

$$\downarrow I_B = \frac{V_{cc} - V_{BE} - V_E}{R_B}$$

$$V_E = I_E R_E \approx I_c R_E$$

$V_E \uparrow$

FIXED BIAS

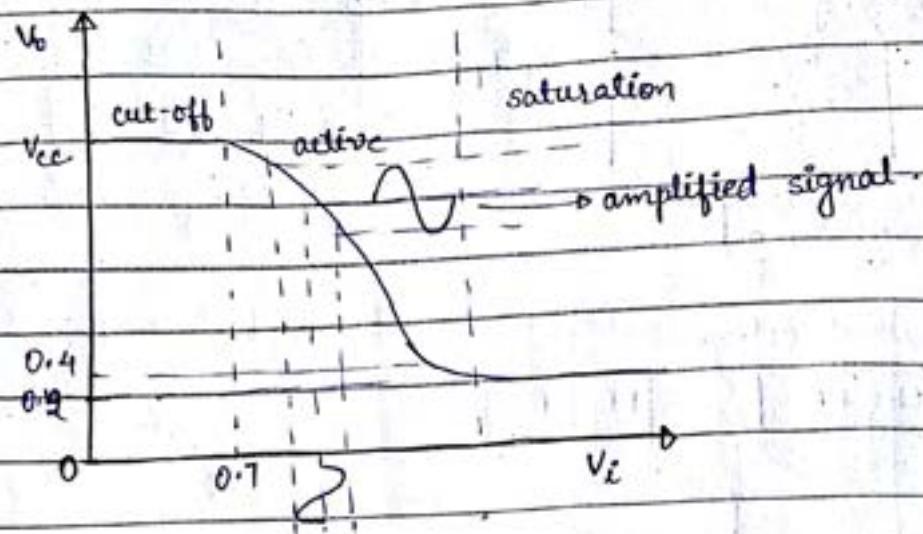
- As the temperature T_{es} , I_{eo} \propto $e^{-\frac{V_T}{kT}}$ which $\propto e^{-\frac{V_T}{kT}} \propto I_c$.
- In this configuration, the value of I_B is constant $\therefore I_c$ tends to $\propto e^{-\frac{V_T}{kT}}$ with V_T in temp. \therefore the circuit is unstable.

Emitter Bias.

- In this configuration at temperature T_{es} , $I_c \propto e^{-\frac{V_T}{kT}}$: The value of I_B is calculated using $I_B = \frac{V_{ce} - V_{BE} - V_E}{R_B}$, $V_{BE} = I_E R_E \approx I_c R_E$
- V_E in I_c causes V_E to $\propto e^{-\frac{V_T}{kT}}$ as a result I_B $\propto e^{-\frac{V_T}{kT}}$, this \propto I_B causes I_c to $\propto e^{-\frac{V_T}{kT}}$ and \therefore makes it stable

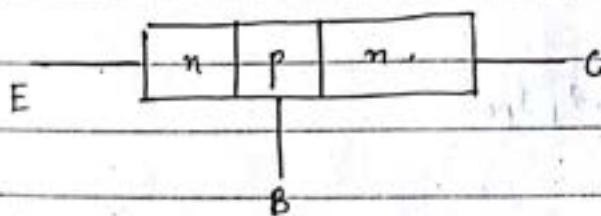
$$S(V_{BE}) \cdot S(\beta)$$

BJT TRANSFER CHARACTERISTICS

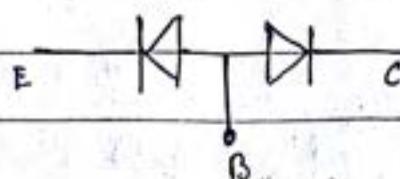


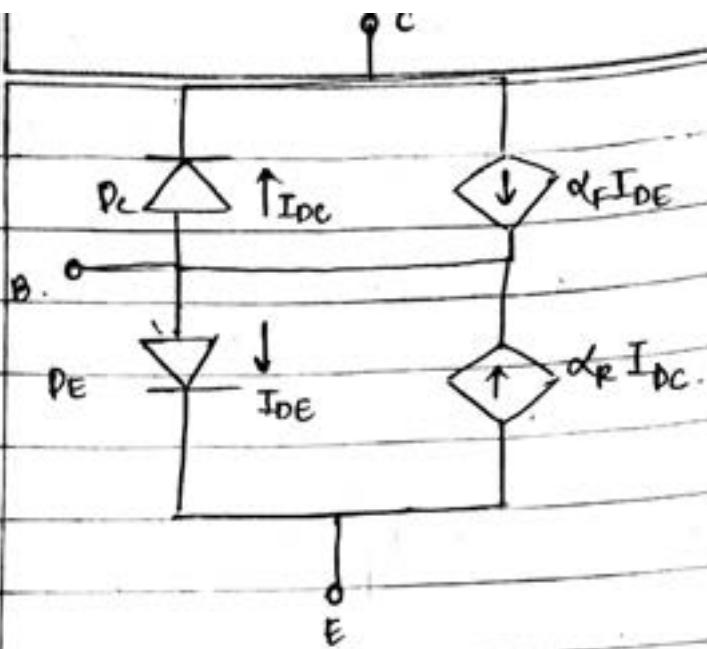
1. When the value of V_i is less than 0.7 V, transistor is in cutoff region. $V_o = V_{ce}$.
2. As V_i increases, transistor enters into active region and the value of V_o less. $V_o = V_{ce} - I_c R_c$.
3. As the value of V_{ce}/V_o goes beyond 0.4 V, transistor enters into saturation region.
4. The saturation voltage (V_{sat} / V_{cesat}) is approximately equal to 0.2 V.

EBER'S MOLL MODEL :-



→ This model helps in understanding the BJT using diodes and current sources.

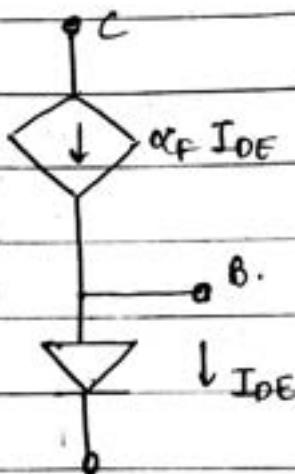




Case 1. Forward active.

$$CB = RB$$

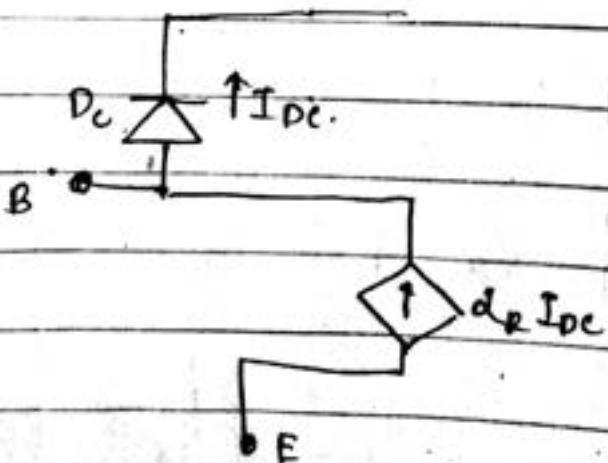
$$EB = FB$$



α_F = forward current gain

Case 2. Reverse Active.

$$CB = FB, EB = RB$$



FIELD EFFECT TRANSISTOR.

FET

1. It is a unipolar device.
2. It is voltage controlled device.
3. $I_D \propto f(V_{GS})$
↓
output current.
4. It can be of two types:-
 - (a) n-channel
 - (b) p-channel.
5. It has high input impedance.
6. It is less temperature dependent.
7. Very small in size.
8. It is a symmetrical device.

BJT

1. It is bipolar device.
2. It is current controlled device.

$$I_C, V_{CE} \propto f(I_B)$$

(a) npn.

(b) pnp.

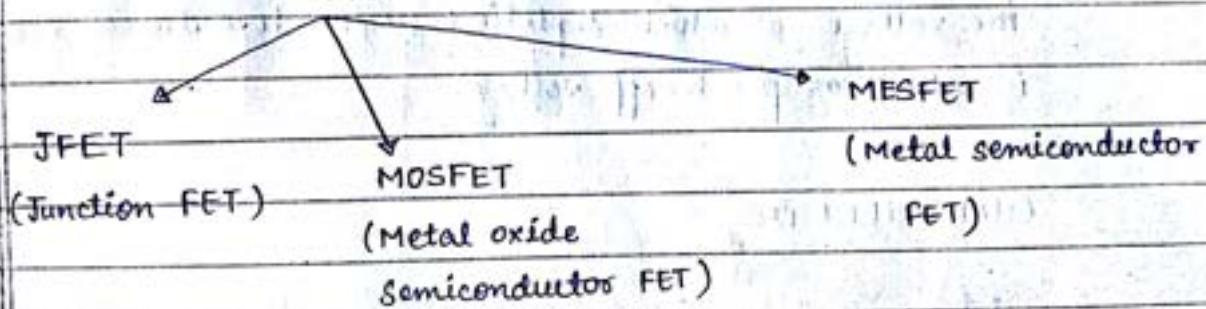
5. It has low input impedance

6. It is more temperature dependent.

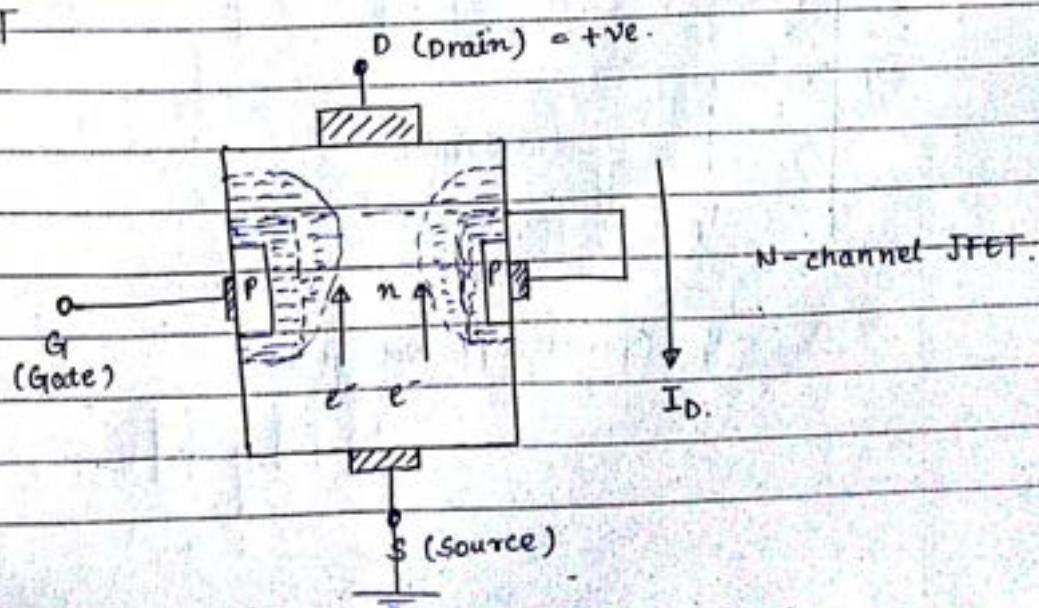
7. It has larger size as compared to FET.

8. It is asymmetric device.

FET

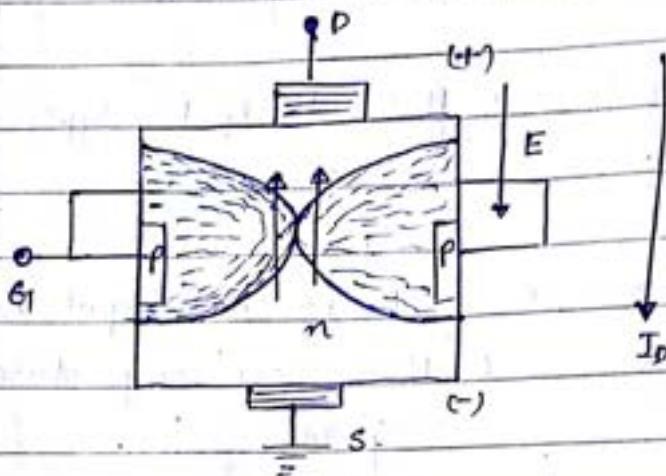


JFET



CASE 1. $V_{GS} = 0$ $V_{DS} \geq 0$

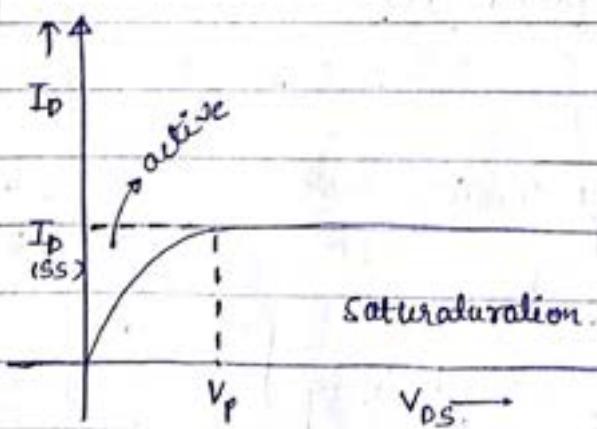
When a +ve potential is applied at Drain (D) terminal, the junction DG becomes more reverse biased as a result the depletion width $\propto V_{DS}$. The GS terminal is not biased \therefore , the depletion region remains the same.



As the drain voltage is further fed the depletion region tends to combine together, thereby blocking the path of e⁻.

The voltage at which depletion region boundaries meet is called as pinch off voltage.

CHARACTERISTIC



$$V_{DS} = V_p \text{ (pinch off voltage)}$$

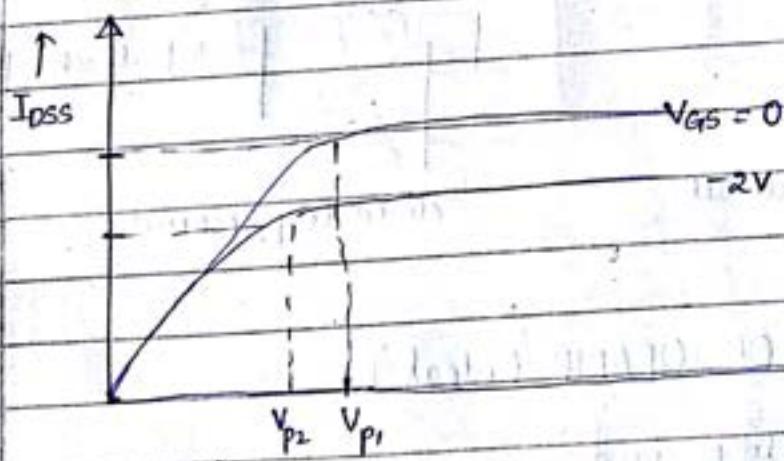
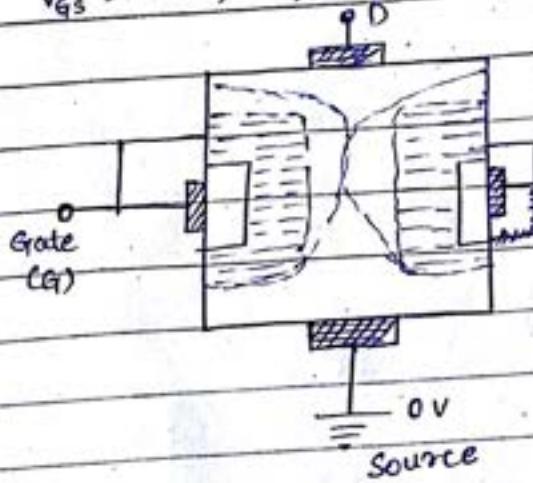
→ As V_{DS} is fed beyond V_p , a strong electric field develops between drain and source terminal which causes the electrons to flow. This region is known as saturation region and current has maximum value.

CASE 2 :- $V_{GS} < 0$

$$V_{GS} < 0 ; V_{DS} = 0$$

$$V_{GS} = -2V ; V_{DS} = 0V$$

$$V_{GS} = -2V ; V_{DS} = 2V$$

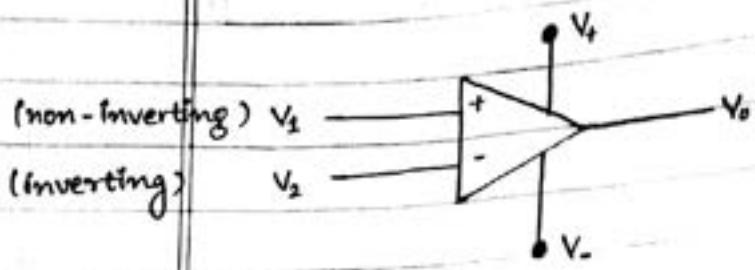


→ $I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_p} \right)^2$ → input voltage (Gate to source).
 ↓ max value of current
 ↓ pinch off voltage

$$V_p = \infty$$

$$\frac{\left(1 - \frac{V_{GS}}{V_p} \right)^2}{V_p}$$

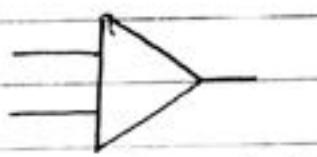
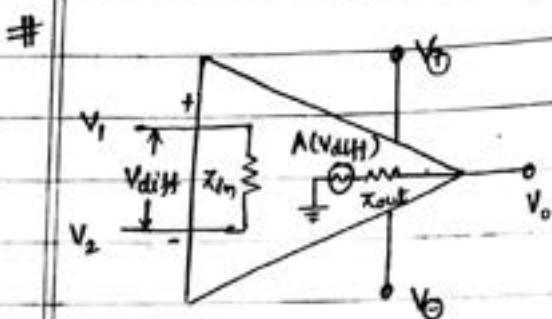
OP-AMP (operational Amplifier).



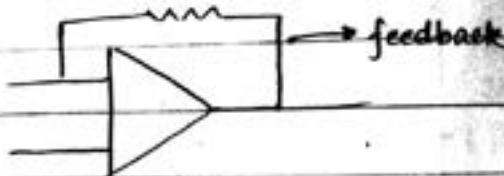
$$V_{out} = A_{vid} (V_1 - V_2)$$

Amplifier Gain

differential input



open loop circuit



closed loop circuit

• PROPERTIES OF OPAMP (ideal).

1. Infinite open loop gain.
2. Infinite input impedance. ($Z_{in} = \infty$)
3. zero output impedance ($Z_{out} = 0$)
4. zero noise contribution.
5. zero output offset voltage and current.
6. infinite bandwidth.
7. Differential Inputs stick together
8. zero common mode gain.

Common mode means both the inputs are same.

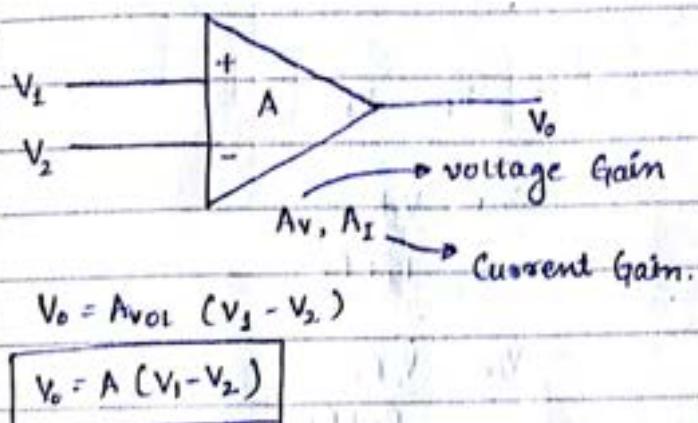
9. Infinite common mode rejection ratio. (CMRR)

$$CMRR = \frac{V_1 + V_2}{V_1 - V_2} = \infty$$

10. Infinite slew rate. (change of output voltage with change in time)

$$\frac{\Delta V}{\Delta t}$$

OPEN LOOP OpAmp :-



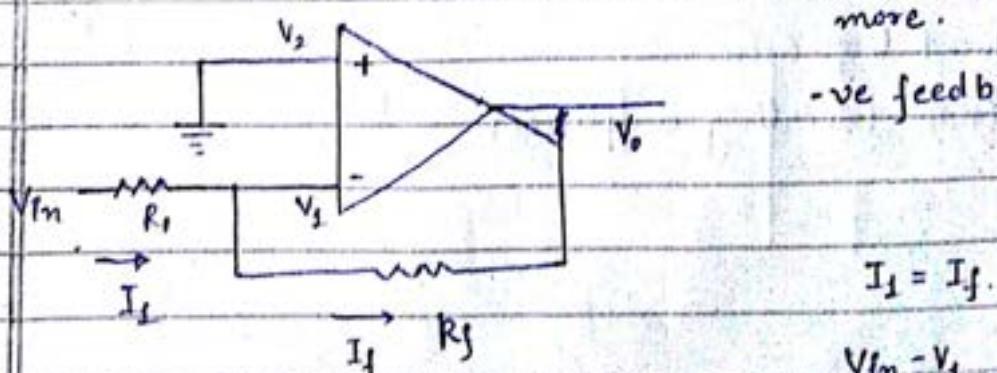
CLOSED LOOP OpAmp :-

1. Inverting Amplifier.

→ In -ve feedback, Gain is less.

→ In +ve feedback, Gain is more.

-ve feedback.



$$V_2 = 0$$

$$V_f = V_2$$

$$\therefore V_f = V_2 = 0 \quad (\text{virtual ground concept})$$

$$\frac{V_{In} - V_1}{R_1} = \frac{V_1 - V_o}{R_f}$$

$$V_1 = 0$$

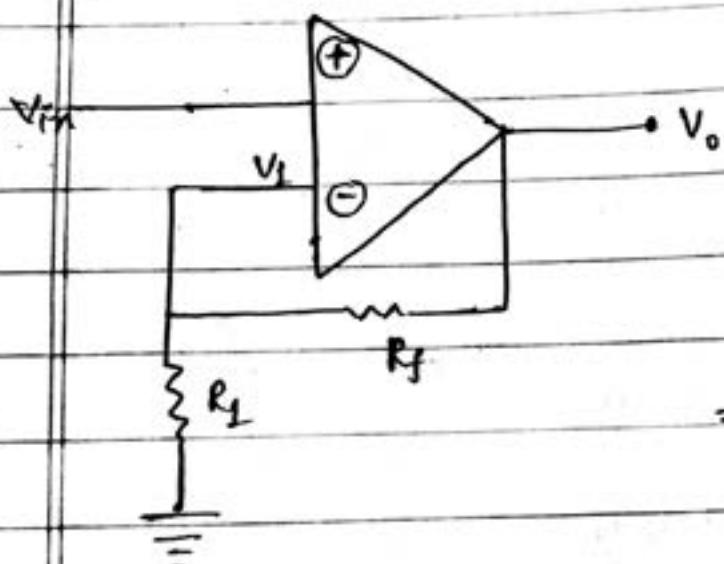
$$\frac{V_{In}}{R_1} = -\frac{V_o}{R_f}$$

$$\frac{V_o}{V_{in}} = -\frac{R_f}{R_i}$$

$$A_{CL} = -\frac{R_f}{R_i}$$

closed loop
Gain (inverting amplifier)

2. Non-Inverting Amplifier.



$$\Rightarrow V_{in} = V_1$$

$$\Rightarrow V_1 = \frac{V_o R_1}{R_1 + R_f}$$

$$\Rightarrow V_{in} = \frac{V_o R_1}{R_1 + R_f}$$

$$\Rightarrow \frac{V_o}{V_{in}} = \frac{1 + R_f}{R_1}$$

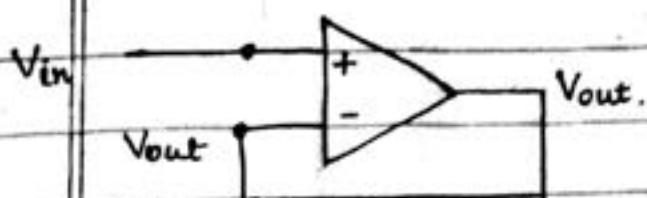
$$\Rightarrow A_{CL} = 1 + \frac{R_f}{R_1}$$

closed loop Gain

(non-inverting amplifier)

* APPLICATIONS OF OPAMP

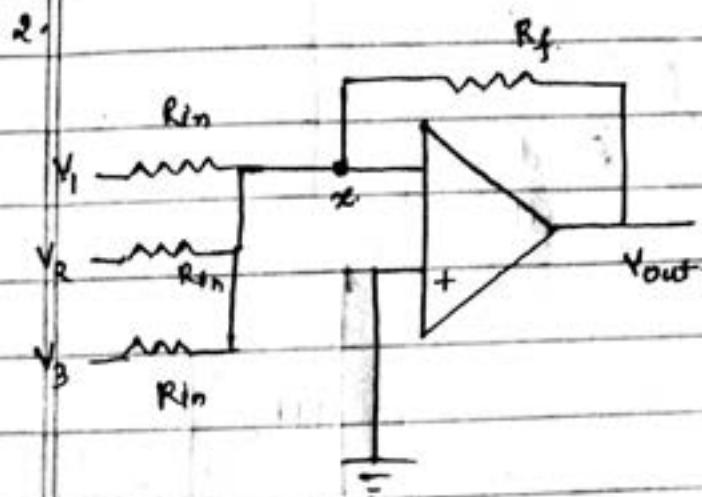
1. VOLTAGE FOLLOWER.



$$V_{out} = V_{in}$$

$$V_{out} = \left(1 + \frac{R_f}{R_i}\right) V_{in}$$

$$V_{out} = V_{in} \quad (\text{as } R_f = 0)$$



SUMMER / SUMMING AMPLIFIER.

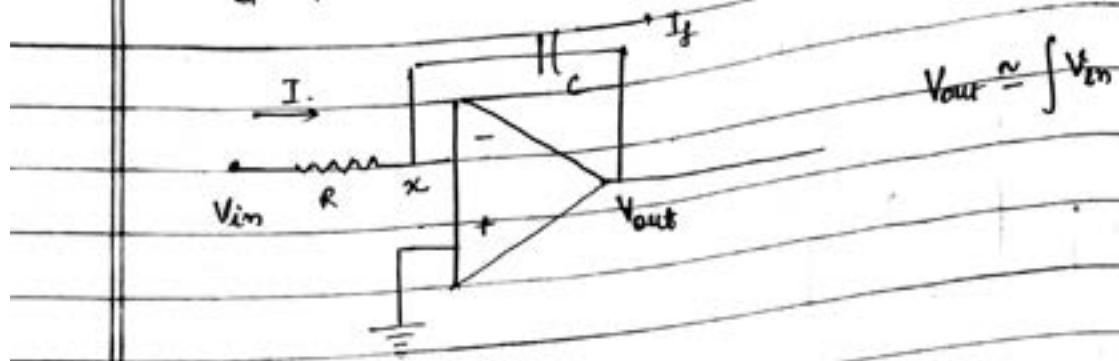
By virtual Ground concept. $x=0$. whole current will flow through R_f

$$I_1 + I_2 + I_3 = I_f$$

$$\frac{V_1}{R_{in}} + \frac{V_2}{R_{in}} + \frac{V_3}{R_{in}} = -\frac{V_{out}}{R_f}$$

$$V_{out} = -\frac{R_f}{R_{in}} (V_1 + V_2 + V_3)$$

3. INTEGRATOR / LOW PASS FILTER.



$$I = I_f$$

$$\frac{V_{in} - 0}{R} = -\frac{V_{out}}{X_c} \quad X_c = \frac{1}{\omega C}$$

$$\Rightarrow V_{out} = -\frac{X_c}{R} V_{in}$$

$$S = \frac{d}{dt}$$

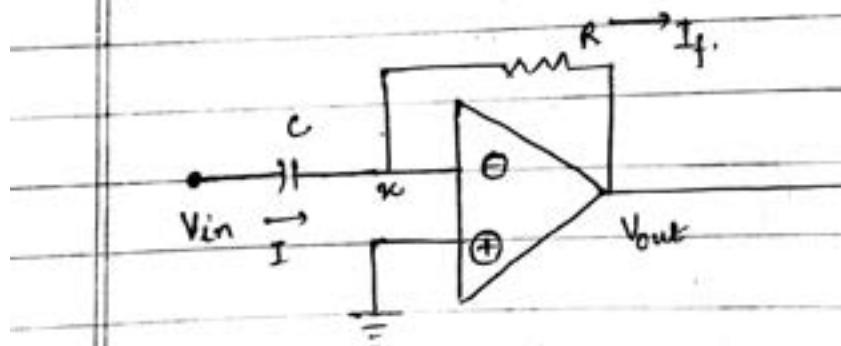
$$\Rightarrow V_{out} = -\frac{1}{SCR} V_{in}$$

$$\Rightarrow V_{out} = -\frac{1}{RC} \int V_{in} dt$$

LPF

f

4. DIFFERENTIATOR / HIGH PASS FILTER.

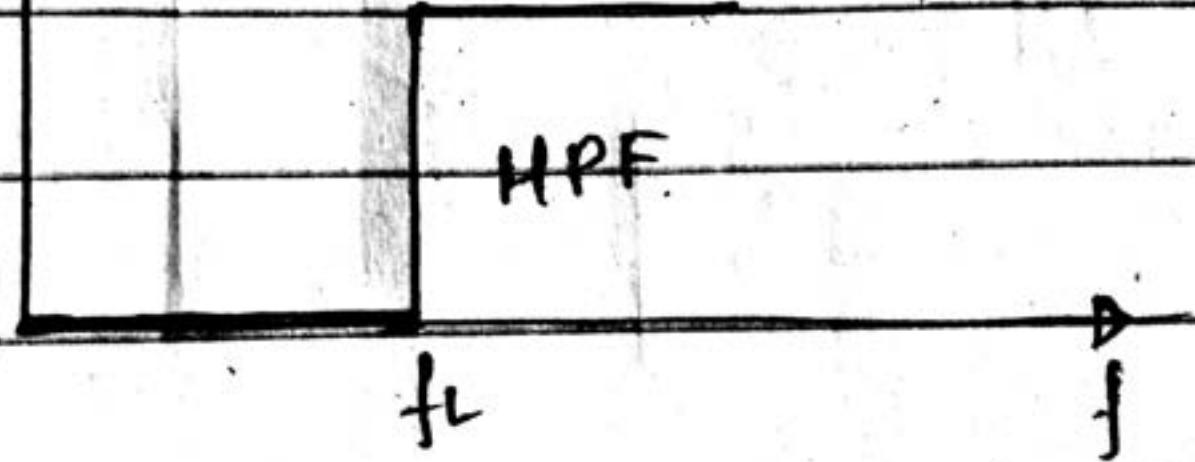


$$I = I_f$$

$$\frac{V_{in} - 0}{X_c} = -\frac{V_{out}}{R}$$

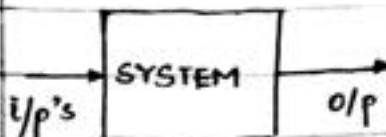
$$V_{out} = -\frac{R}{X_c} V_{in} \quad \Rightarrow V_{out} = -\frac{R(SC)}{X_c} V_{in}$$

$$V_{out} = -RC \frac{d(V_{in})}{dt}$$

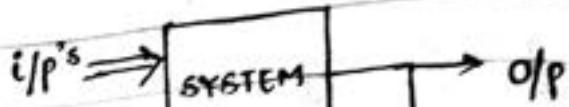


FLIP-FLOPS.

Combinational

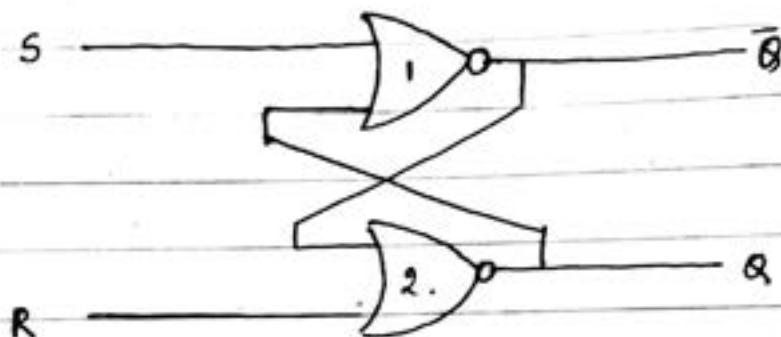


Sequential.



LATCH

(A) SR (NOR) LATCH



NOR. (truth table)

S	R	Q
0	0	1
0	1	0
1	0	0
1	1	0

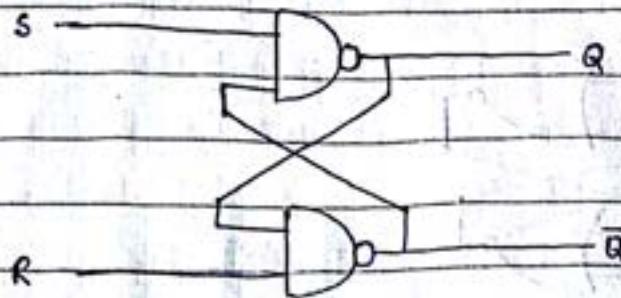
SR latch. (truth table)

S	R	Q
0	1	0
0	0	0
1	0	1
0	0	1

1 1 indeterminate.

S	R	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	X invalid.

(B) SR (NAND) LATCH



NAND (truth table)

A	B	$\bar{A} \cdot B$	S	R	$Y(Q)$	(SR NAND latch truth table)
0	0	1			1	
0	1	1			0	
1	0	1			0	
1	1	0			0	Xinvalid.

S R $Q(t+1)$

0 0 Xinvalid

0 1 1

1 0 0

1 1 $Q(t)$

Differences b/w flip-flops and latch.

FLIP-FLOP

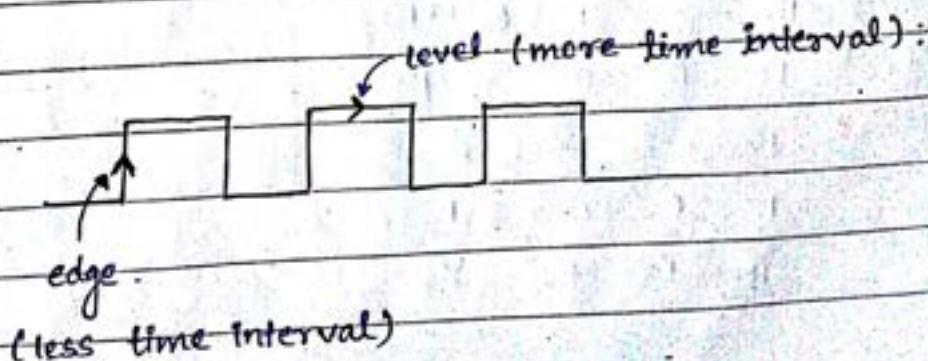
- These circuits have clock in them.

- Flip-flops are edge triggered

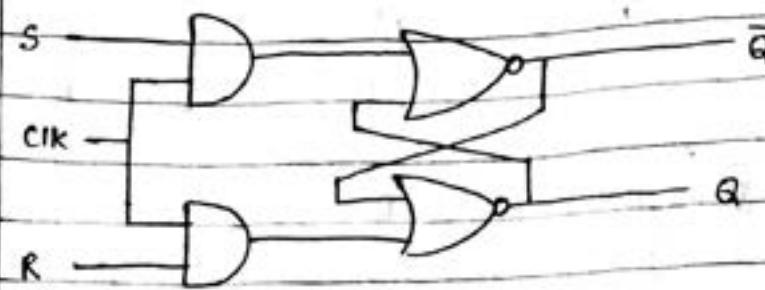
LATCH

- These circuits do not have clock in them.

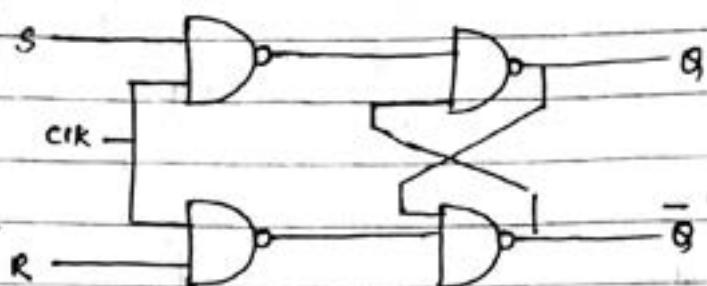
- Latch are level triggered.



(A) S-R FLIP-FLOPS USING NOR LATCH.



(B) S-R FLIP-FLOPS USING NAND LATCH.



(A) SR flip flop (NOR latch) ^{using}

(B) SR flip flop (NAND LATCH) ^{using}

CLK	S	R	Q	CLK	S	R	Q
1	0	1	0	1	0	1	0
1	0	0	0	1	1	1	0
1	1	0	1	1	1	0	1
1	0	0	1	1	0	1	1
1	1	1	X invalid.	1	0	0	X invalid

CLK	S	R	Q(t+1)
1	0	0	Q(t)
1	0	1	0
1	1	0	1
1	1	1	X

$Q(t)$	S	R	$Q(t+1)$
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	X
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	X

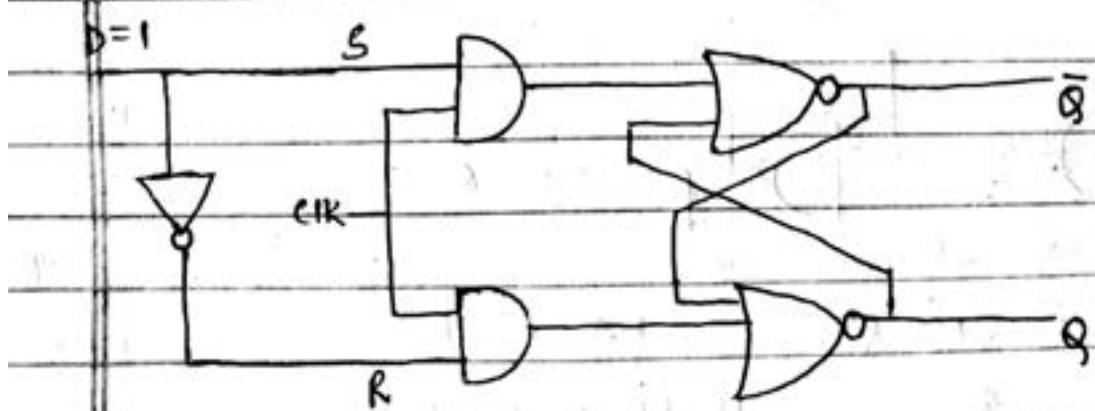
→ CHARACTERISTIC EQ :-

$$Q(t+1) = \begin{matrix} \cancel{S}R & \bar{S}\bar{R} & S\bar{R} & SR & \bar{S}\bar{R} \\ Q & 00 & 01 & 11 & 10 \end{matrix}$$

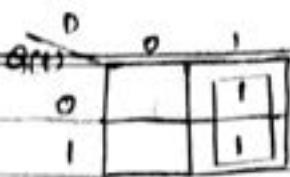
\bar{Q}	0	0	1	X	1	0
Q	1	1	0	X	0	1

$S + \cancel{R} \rightarrow Q\bar{R}$

D-FLIP FLOP (Delay / Data)



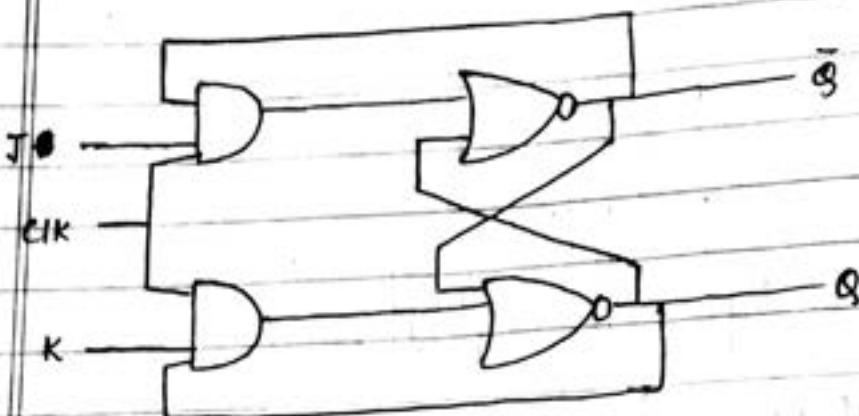
D	Q	$Q(t)$	D	$Q(t+1)$
0	0	0	0	0
1	1	0	1	1
		1	0	0



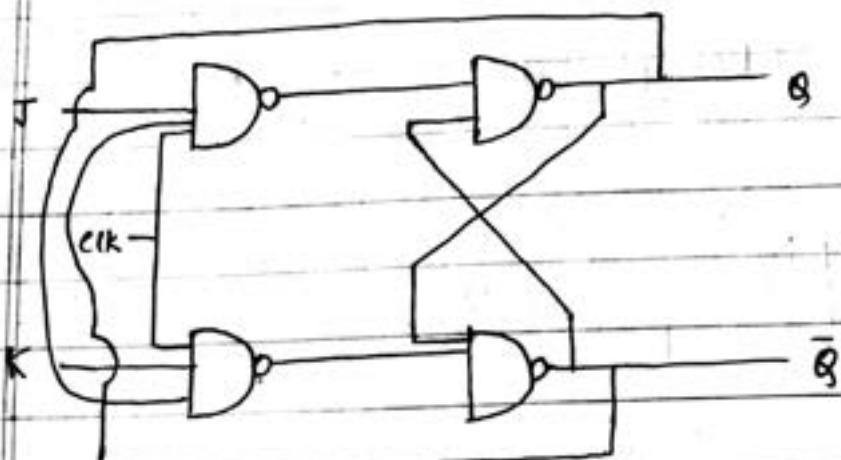
$$Q(J+K) = D$$

J.K. FLIP-FLOPS (JACK KILBY)

①



②



CLK J K Q.

JK FF (using NOR)

1 0 0 L 0

1 0 0 0

Race Around condition.

1 1 0 ,

→ An ~~advantage~~ advantage of JK FF
is that it uses all four
combinations.

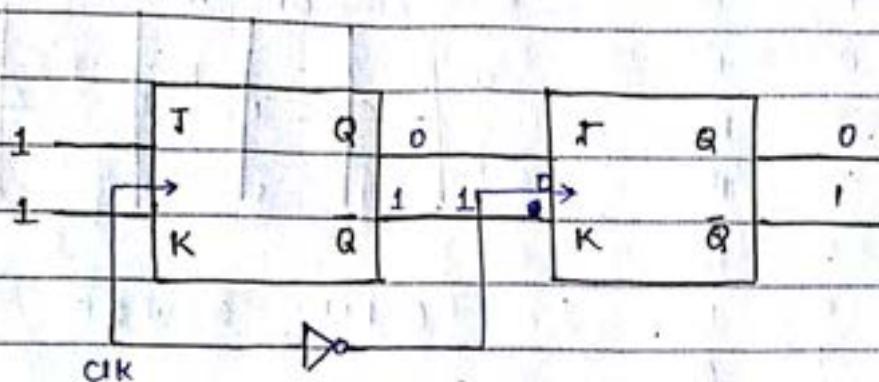
1 0 D ,

→ Disadvantage of JK FF is
race-around condition.

1 1 1 Toggle.

→ If the clock is one for a long duration and the value of T and K is one, then the output changes continuously.

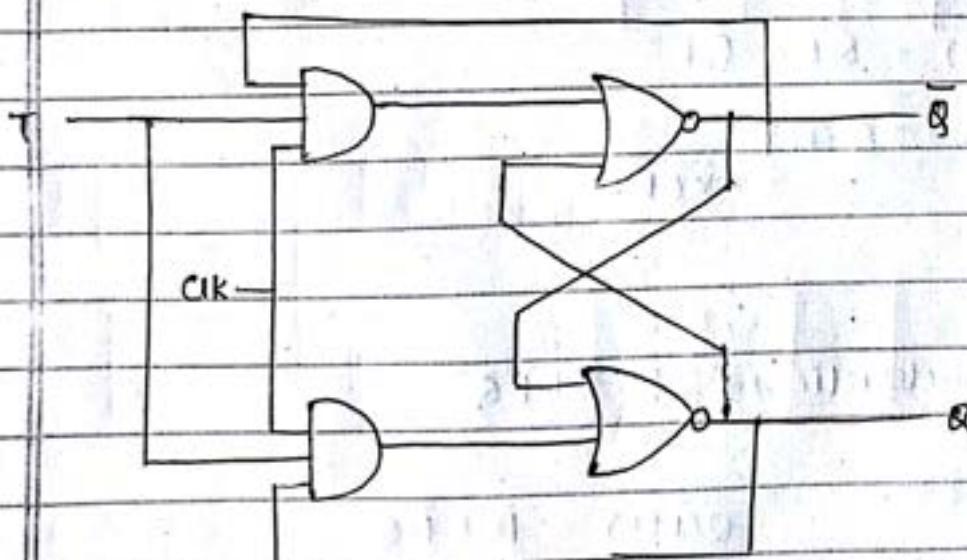
Master Slave FF



one way to remove race around condition is master slave flip-flop.

#

T- FLIP FLOP (Toggle flip-flop.)



$Q \ T \ Q(t+1)$

0 0 0

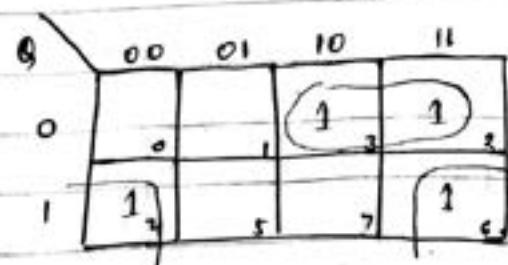
0 1 1

1 0 1

1 1 0

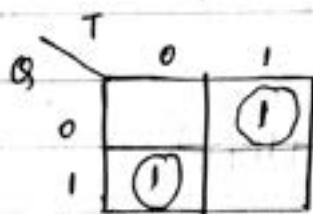
Characteristic eqⁿ. of JK FF

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



$$Q(t+1) = \bar{Q}J + QK$$

Characteristic eqⁿ of T-FF



$$Q(t+1) = Q\bar{T} + \bar{Q}T$$

$$= Q \oplus T$$

XOR.

SR (characteristic eqⁿ) :- $S + \bar{R}Q$

→ for D-FF $Q(t+1) = D + \bar{D}Q$

$$S = D \quad = D + DQ$$

$$R = \bar{D} \quad = D(1+Q) = D.$$

→ For JK-FF

$$S = J\bar{Q} \quad Q(t+1) = J\bar{Q} + \bar{K}\bar{Q}Q$$

$$R = KQ \quad = J\bar{Q} + (\bar{K} + \bar{Q})Q$$

$$\Rightarrow J\bar{Q} + \bar{K}Q + Q\bar{Q} \Rightarrow$$

$$J\bar{Q} + \bar{K}Q$$

→ For T-FF

$$S = T\bar{Q}$$

$$R = TQ$$

$$Q(t+1) = T\bar{Q} + \bar{T}\bar{Q}(Q)$$

$$= T\bar{Q} + (\bar{T} + \bar{Q})Q$$

$$= T\bar{Q} + \bar{T}Q + Q$$

$$\therefore Q(t+1) = T\bar{Q} + \bar{T}Q.$$

• EXCITATION TABLE

Q	Q(t+1)	S	R	T	K	D	T
0	0	0	x	0	x	0	0
0	1	1	0	1	x	1	1
1	0	0	1	x	1	0	1
1	1	x	0	x	0	1	0

Q S R Q(t+1)

0 0 0 0

0 0 1 0

0 1 0 1

0 1 1 x

1 0 0 1

1 0 1 0

1 1 0 1

1 1 1 x

CONVERSION OF FF's.

b Convert SRFF to JKFF.

J	K	Q(t)	Q(t+1)	S	R
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	X	0
1	1	0	1	1	0
1	1	1	0	0	1

for S

J	KQ	00	01	10	10
0			X		
1		X			1

~~TQ~~ JQ

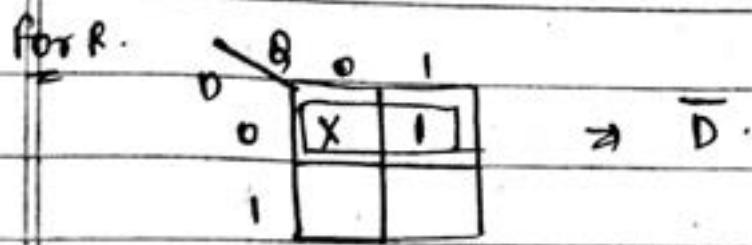
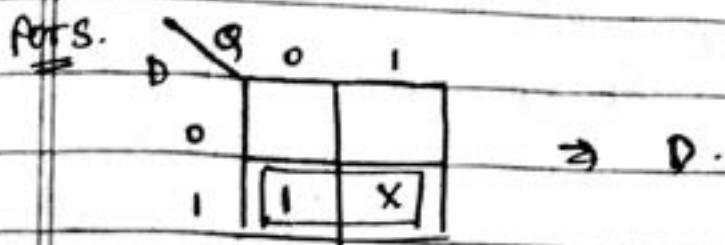
for R

J	KQ	00	01	11	10
0	X				
1				1	X

KQ.

c Convert SRFF to DFF.

D	Q	Q(t+1)	S	R.
0	0	0	0	x
0	1	0	0	1
1	0	1	1	0
1	1	1	x	0



3. JKFF to SRFF

S	R	Q	Q(t+1)	J	K
0	0	0	0	0	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	0	x	1
1	0	0	1	1	x
1	0	1	1	x	0
1	1	0	x	-	-
1	1	1	x	-	-

4

JK FF to D-FF

D	Q	Q(t+1)	J	K
0	0	0	0	x
0	1	0	1	x
1	0	1	x	#1
1	1	1	x	0

$\rightarrow (m)$

minterm $\rightarrow \bar{A}\bar{B}C + \bar{A}BC + ABC$ (SOP)

maxterm $\rightarrow (A+\bar{B}+C)(A+B+C)(\bar{A}+B+C)$ (P)



(M)

		CD	00	01	11	10
		AB	00	01	11	10
AB	CD	00	0	1	3	2
		01	4	5	7	6
11		12	13	15	14	
10		8	9	11	10	

$$f(A, B, C) = \sum(1, 5, 6, 7) + D(3, 4).$$

$$\Rightarrow A+C.$$