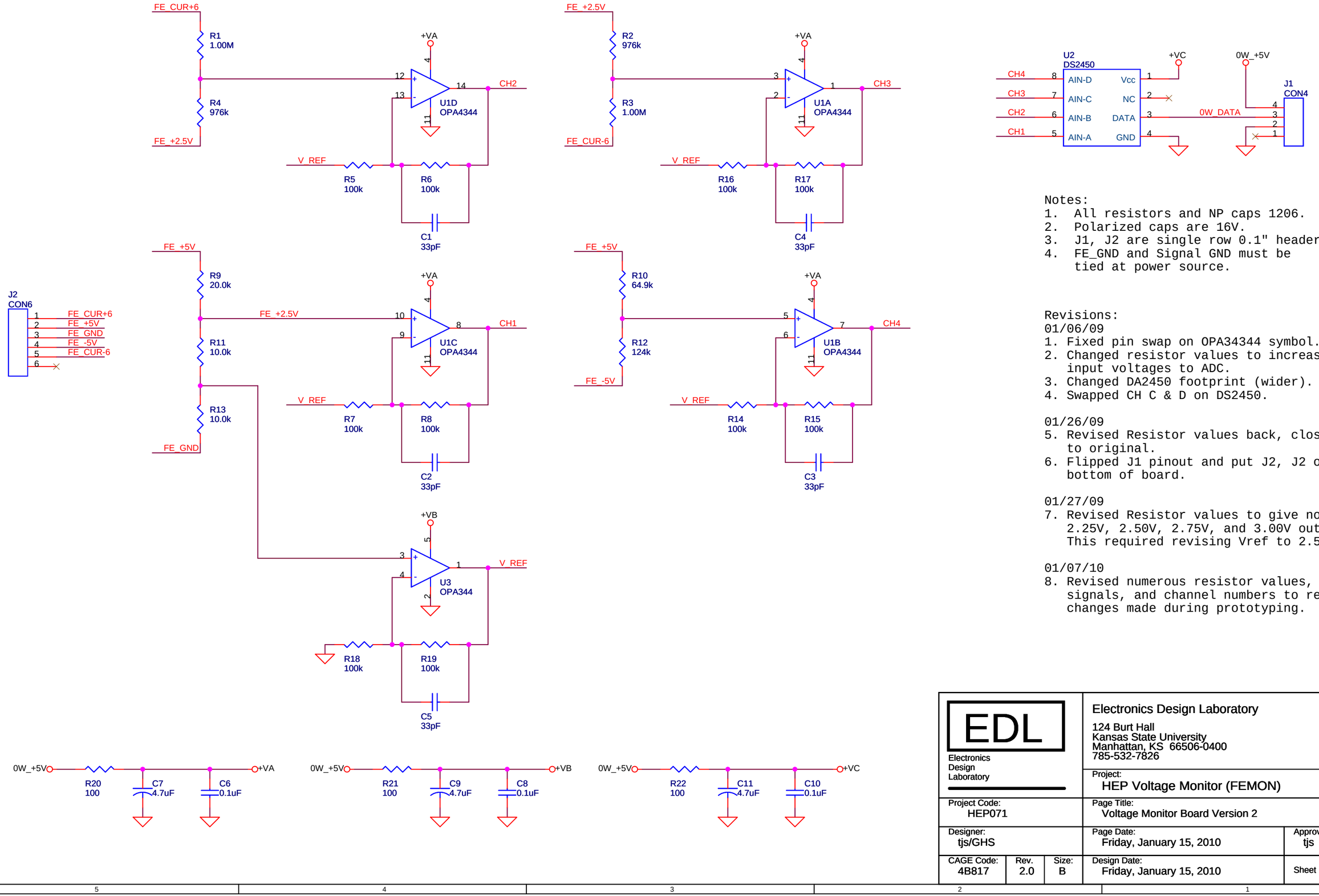

Notes:
1. All resistors and NP caps 1206.
2. Polarized caps are 16V.
3. J1, J2 are single row 0.1" headers.
4. FE_GND and Signal GND must be tied at power source.

Revisions:

01/06/09
1. Fixed pin swap on OPA34344 symbol.
2. Changed resistor values to increase input voltages to ADC.
3. Changed DA2450 footprint (wider).
4. Swapped CH C & D on DS2450.

01/26/09
5. Revised Resistor values back, closer to original.
6. Flipped J1 pinout and put J2, J2 on bottom of board.

01/27/09
7. Revised Resistor values to give nominal 2.25V, 2.50V, 2.75V, and 3.00V outputs. This required revising Vref to 2.50V.

01/07/10
8. Revised numerous resistor values, input signals, and channel numbers to reflect changes made during prototyping.

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Project: HEP Voltage Monitor (FEMON)				
Project Code: HEP071			Page Title: Voltage Monitor Board Version 2	
Designer: tjs/GHS			Page Date: Friday, January 15, 2010	Approval: tjs
CAGE Code: 4B817	Rev. 2.0	Size: B	Design Date: Friday, January 15, 2010	Sheet 1 of 1