

Final Project Report

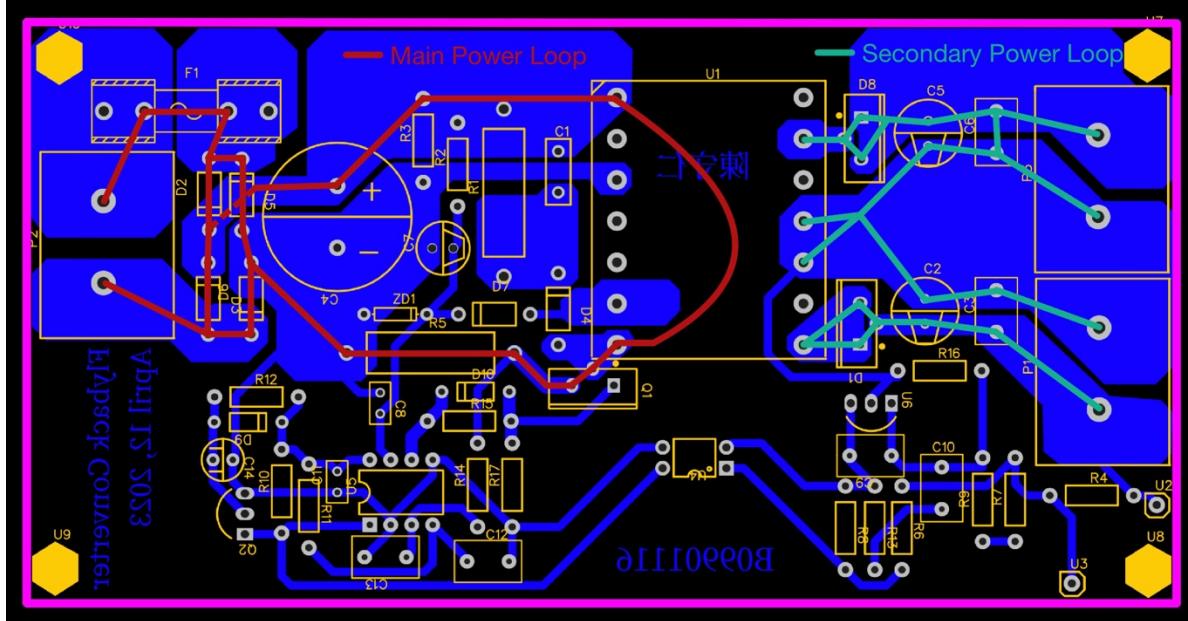
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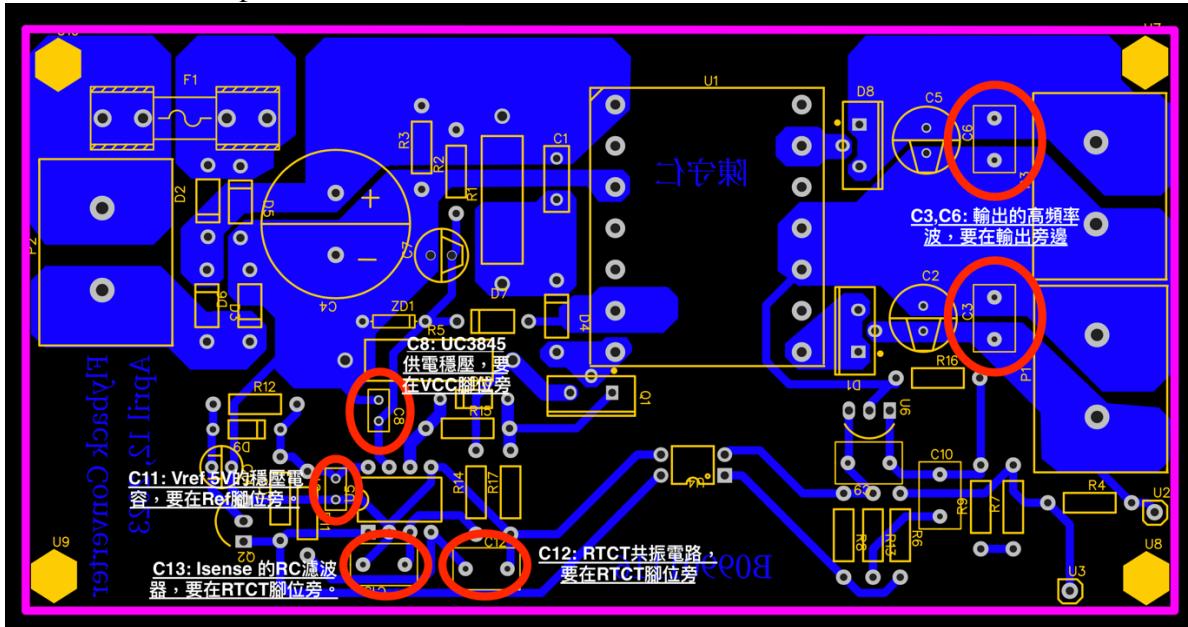
時段：C 時段

Layout Analysis:

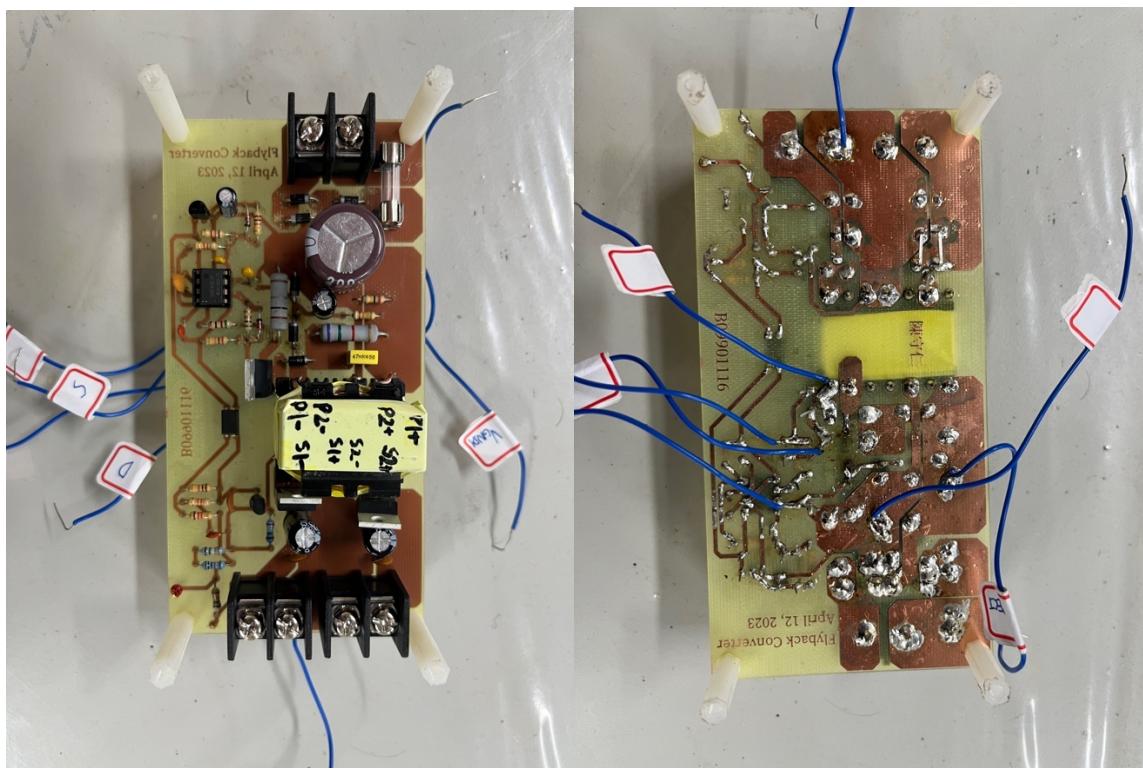
A. Main Power Stage Analysis



B. Filter and Capacitor



C. Picture and Size



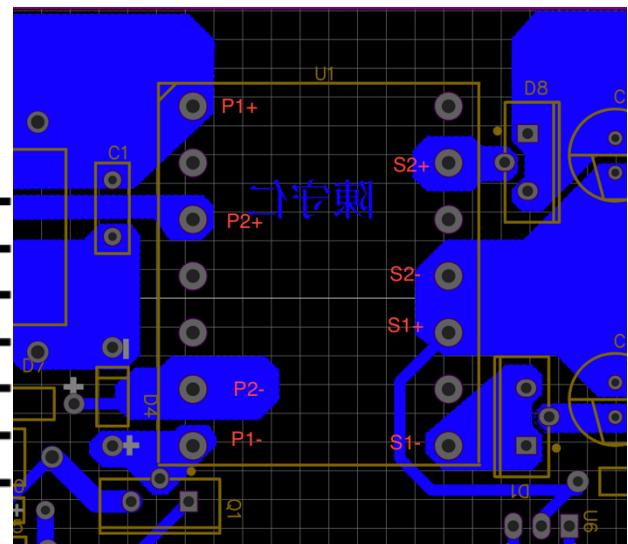
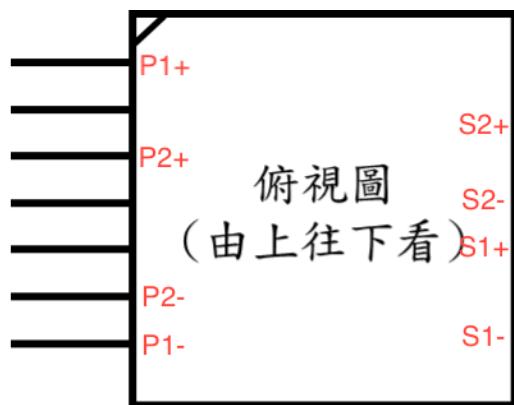
Front

Back

Size: Length - 14 cm Width – 7.1 cm

Transformer:

A.



Original L_m from P1	Air-gapped L_m from P1	Air-gapped L_m from P2	Air-gapped L_m from S1	Air-gapped L_m from S2
2.465mH	533.3uH	32.86uH	32.90uH	31.19uH

$$L_p = (N_p/N_s)^2 L_s, \text{匝數平方比 } (N_p/N_s)^2 = (24/6)^2 = 16$$

P1-P2 = 533/32.86 = 16.22	P1-S1 = 533.3/32.90 = 16.21	P1-S1 = 533.3/31.19 = 17.10
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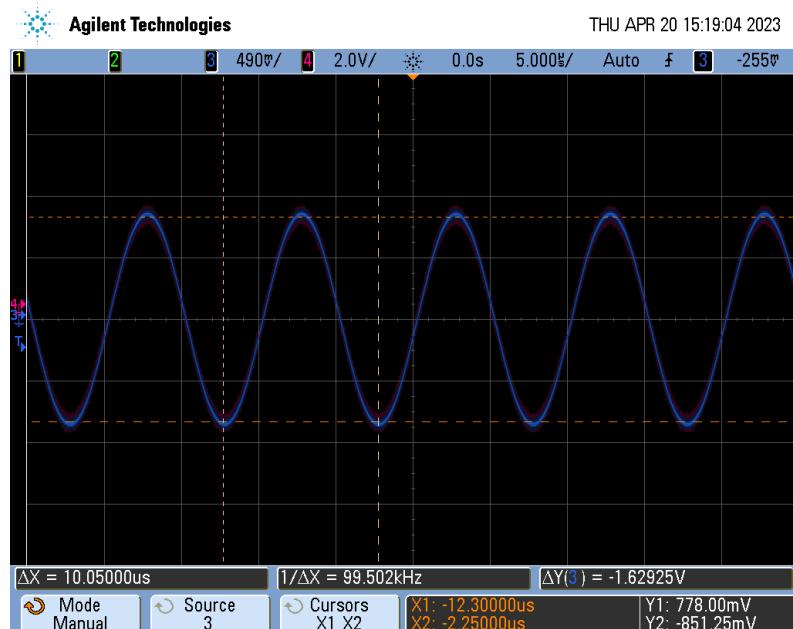
檢查氣隙後電感值是否正比於匝數平方比 Check the air-gapped L_m values are proportional to the N^2 .

	S1 short	S2 short	P2 short
Leakage Inductance (Measured from P1)	26.66uH	11.92uH	35.3uH
Ratio(divided by air-gapped L_m from P1)	4.9%	2.24%	6.62%

B.

(1) S1 to P1

a. 概略法



Ratio = $2/0.49 = 4.08$, matches the turn ratio of 4

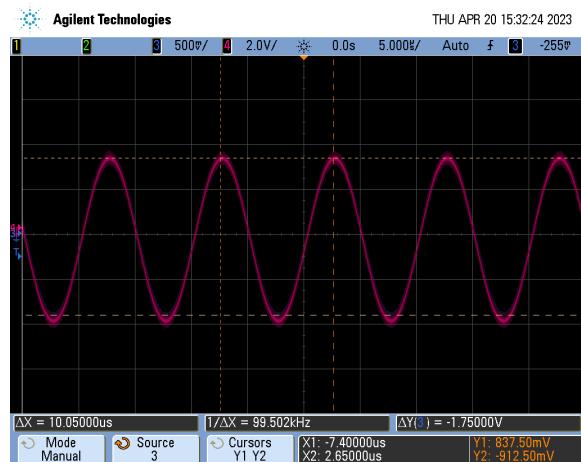
b. 精確法



Ratio = $7.065/1.65 = 4.28$, approximately matches the turn ratio of 4

(2) S2 to P1

a. 概略法



Ratio = $2/0.5 = 4$, matches the turn ratio of 4

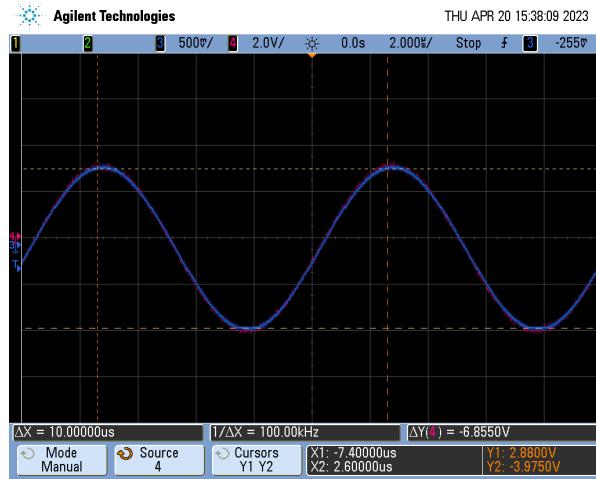
b. 精確法



Ratio = $7.185/1.75 = 4.106$, approximately matches the turn ratio of 4

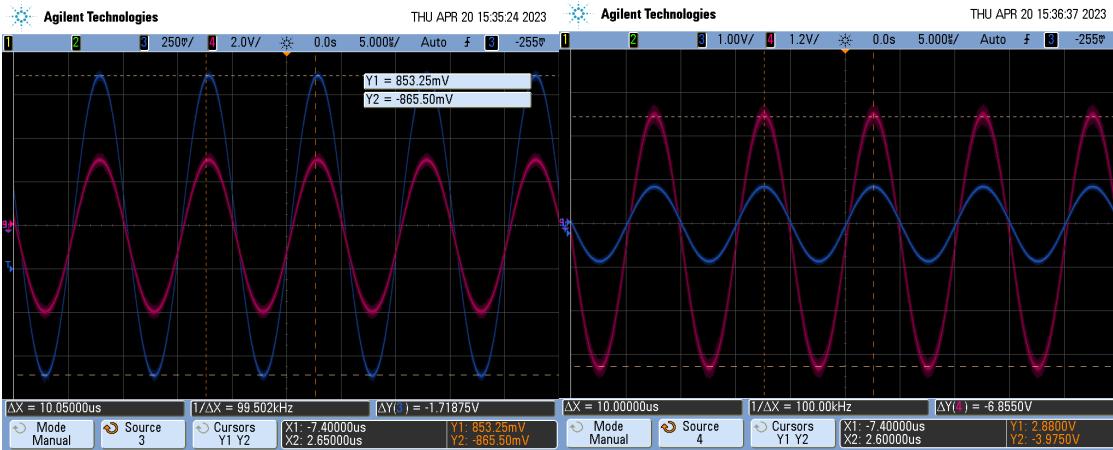
(3) P2 to P1

a. 概略法



Ratio = $2/0.5 = 4$, matches the turn ratio of 4

b. 精確法



Ratio = $6.855/1.71875 = 3.988$, approximately matches the turn ratio of 4

DC Open-Loop Testing

CH1 : V_{GS}

- Purpose: Switch driving signal
- Measure : Duty

CH2 : V_{DS}

- Purpose: Switching condition, ensuring voltage does not exceed component limit
- Measure : Maximum
- Simulated V_{DS} voltage when the switch is closed: $V_{IN} + N * V_O$

CH3 : V_O

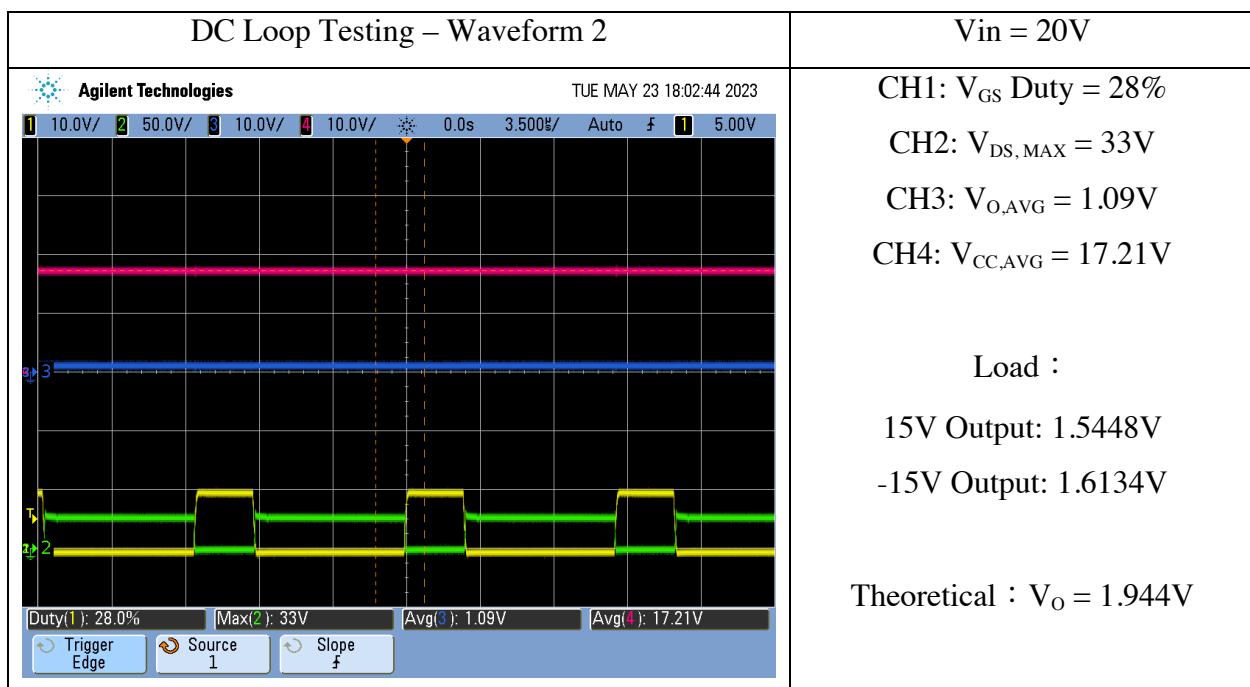
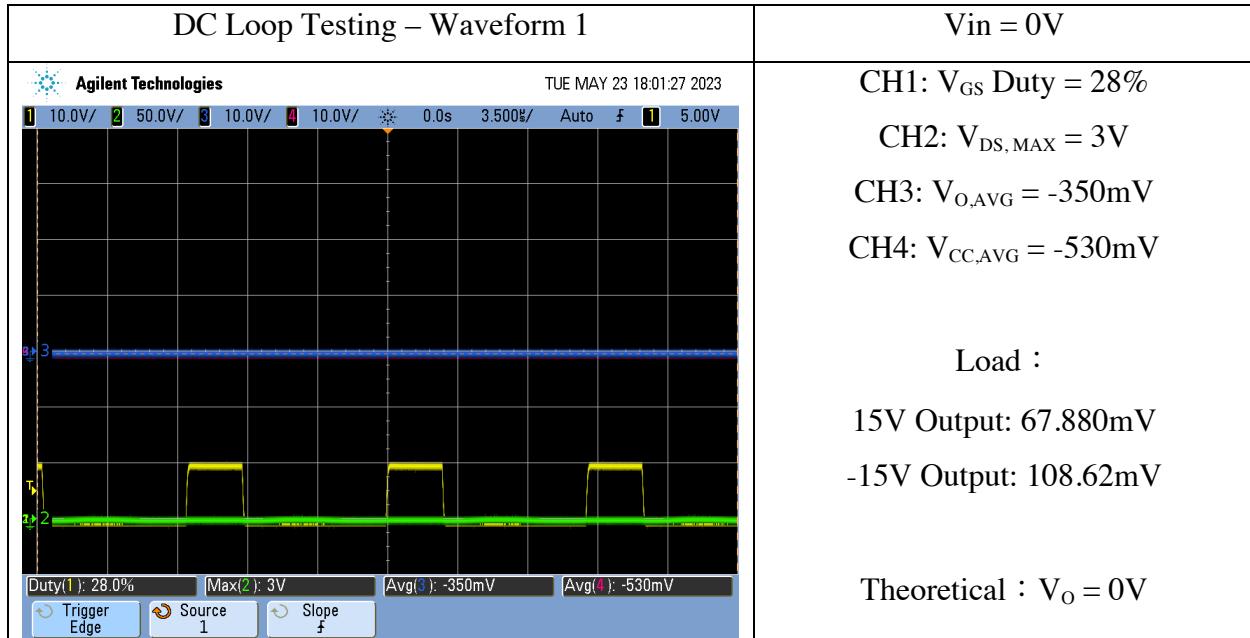
- Purpose: Output voltage, verifying if the circuit output matches the theoretical value.
- Measure : Average

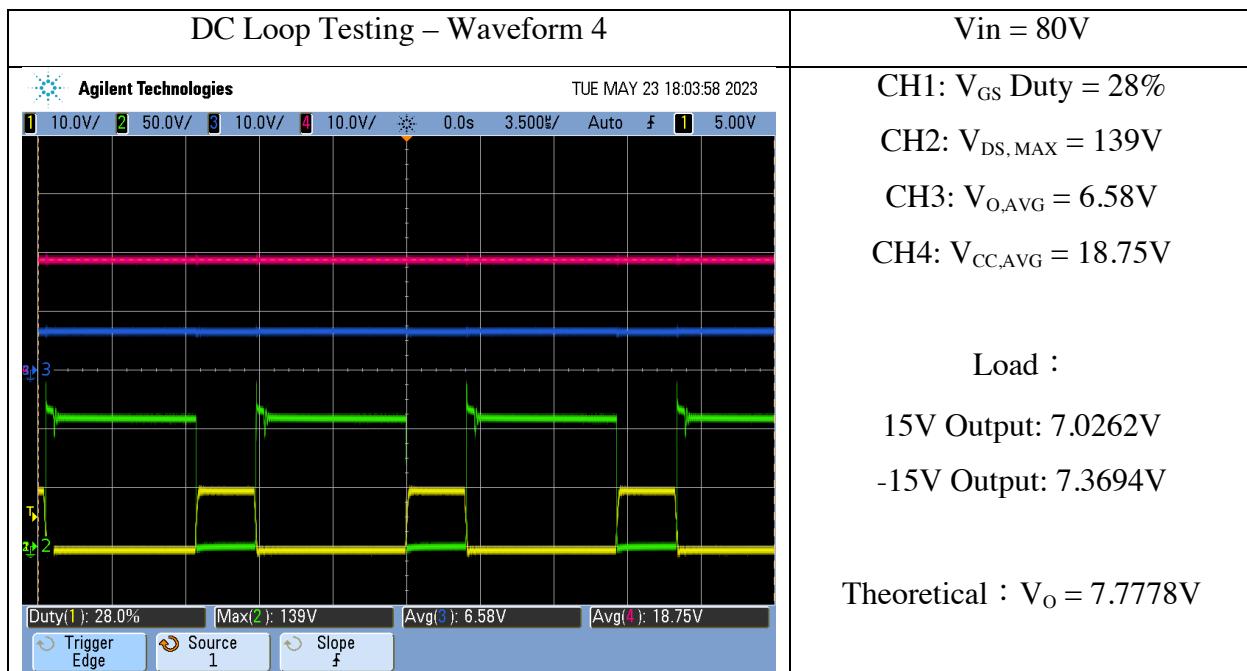
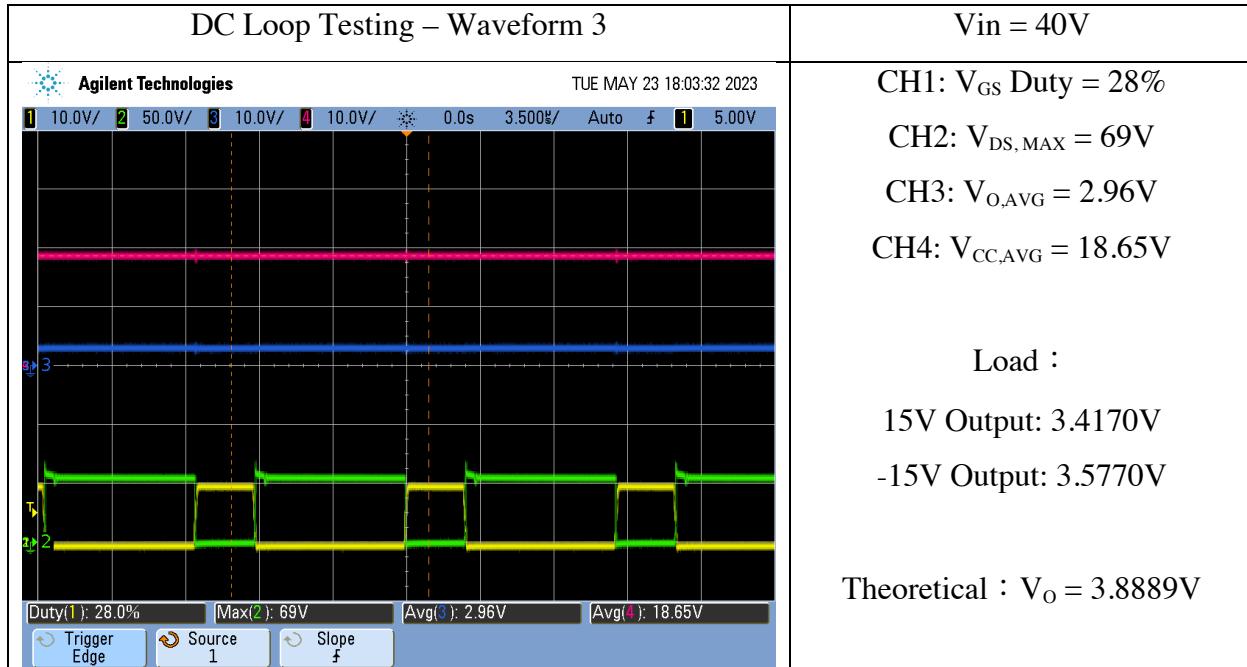
CH4 : V_{CC}

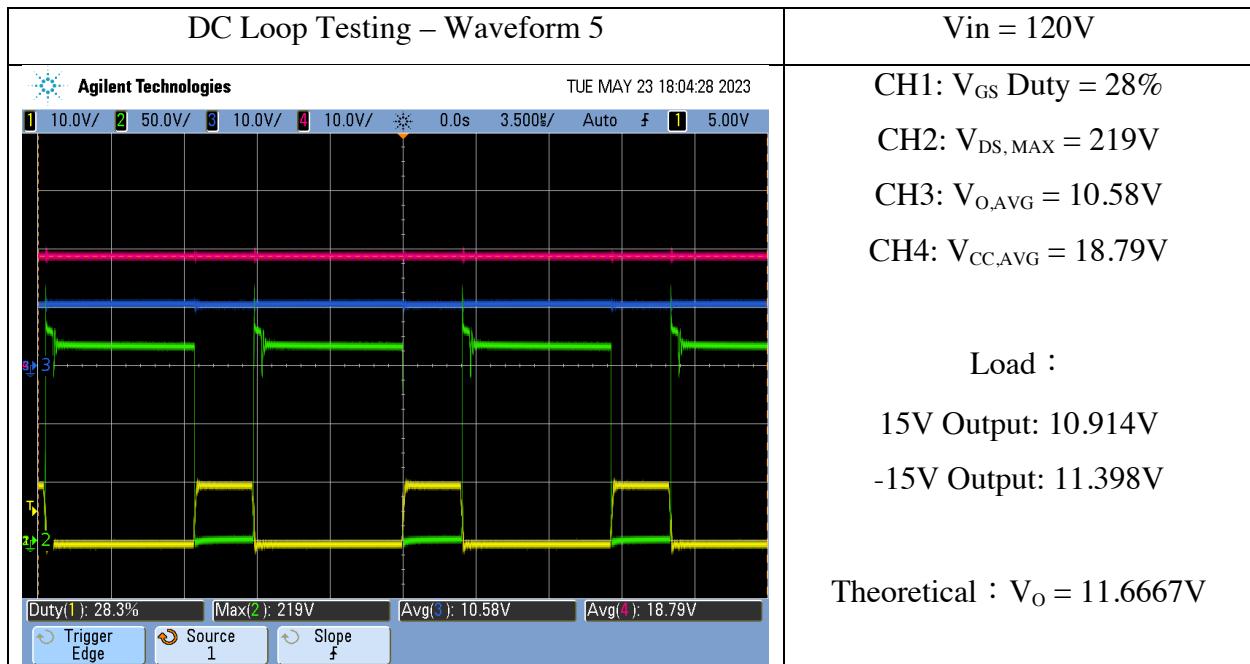
- Purpose: Auxiliary output voltage, confirming normal power supply for the auxiliary output.
- Measure : Average

$$\text{Theoretical } V_O = \frac{D}{1-D} \frac{N_S}{N_P} V_{in}$$

CR mode: 7.5 Ω







Waveform Analysis(Waveform 5: Vin = 120V):

CH1(V_{GS}) : It is a periodic square waveform, we can clearly see Miller Plateau when V_{DS} charge and discharge. This is caused by the driving current into the C_{GD} to keep V_{GS} constant.

CH2(V_{DS}) : It is a periodic square waveform, at rising there are a short oscillation between leakage inductor and C_{DS}.

CH3(V_O) : It is the output voltage at a constant line, where there are a bit of oscillation when there is a Miller Plateau.

CH4(V_{CC}) : It is a constant line, where there are a bit of oscillation when there is a Miller Plateau.

Numerical Analysis:

$$1. \text{ Theoretical } V_O = \frac{D}{1-D} \frac{N_S}{N_P} V_{in} = 11.667 \text{ V}$$

$$\text{Experimental Avg}(V_O) = 10.58 \text{ V}$$

$$\text{Error} = \frac{|\text{Theoretical} - \text{Experimental}|}{\text{Theoretical}} \times 100 = 9.3\%$$

The error might be caused by loss from components, such as IRF740, IN4007. Also, there might be an error due to the N because the winding of wire might be loosen up after several weeks.

2. When switch is on, $V_{DS} = 0$. When switch is off, the maximum $V_{DS,\max} = 219V$.

$$\text{Theoretical } V_{DS} = V_{in} + nV_{out} = 120 + 4(10.58) = 162.32V.$$

From the figure from Waveform 5, the final converging V_{DS} is at around 170.93V, which fits the theoretical V_{DS} .

$$\text{Error} = (170.93 - 162.32)/162.32 = 5.304\%$$

$$V_{DS,\max} = V_{in} + V_{Snubber} =$$

$$V_{Snubber} = V_{DS,\max} - V_{in} = 219 - 120 = 99 V$$

The snubber will clamp the Vds voltage when the switching Vds voltage is too high.

Closed-loop Test (External Power Supply)

CH1 : V_{GS}

- Measure : Duty

CH2 : V_{DS}

- Measure : Maximum

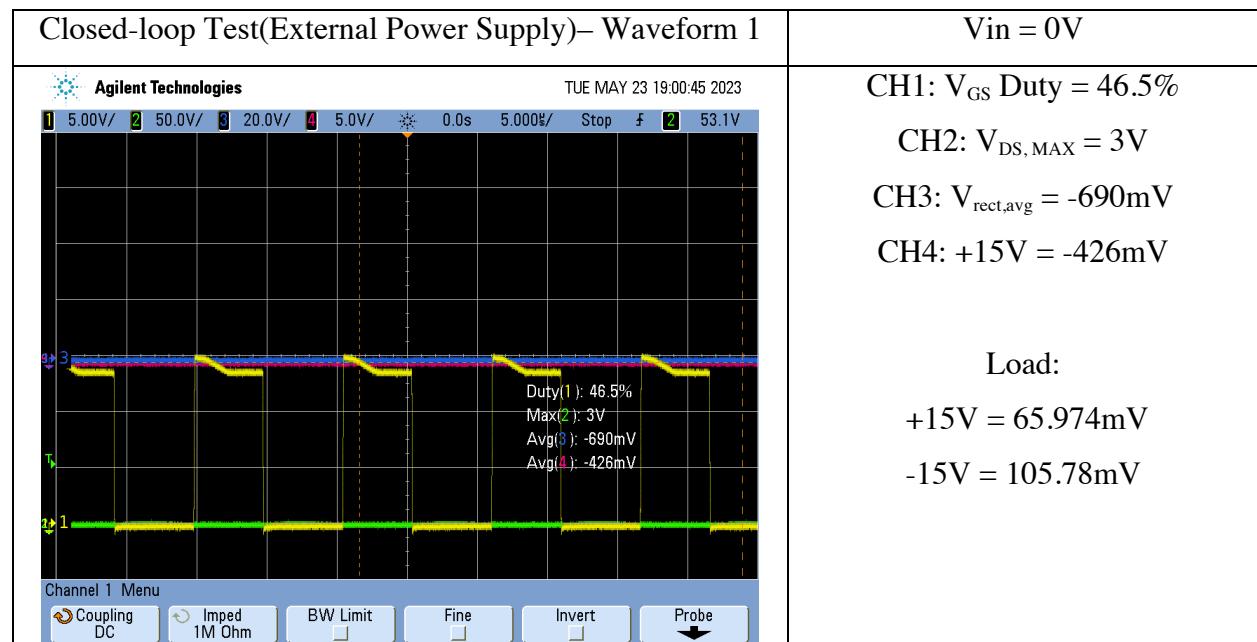
CH3 : $V_{in}(V_{rect})$

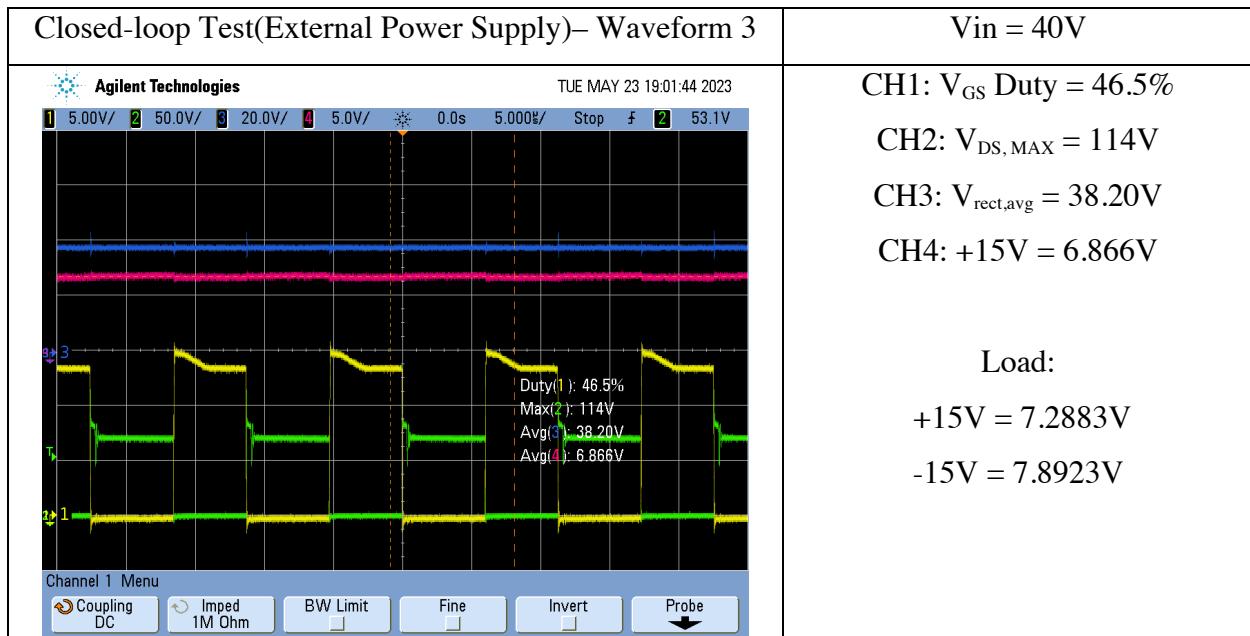
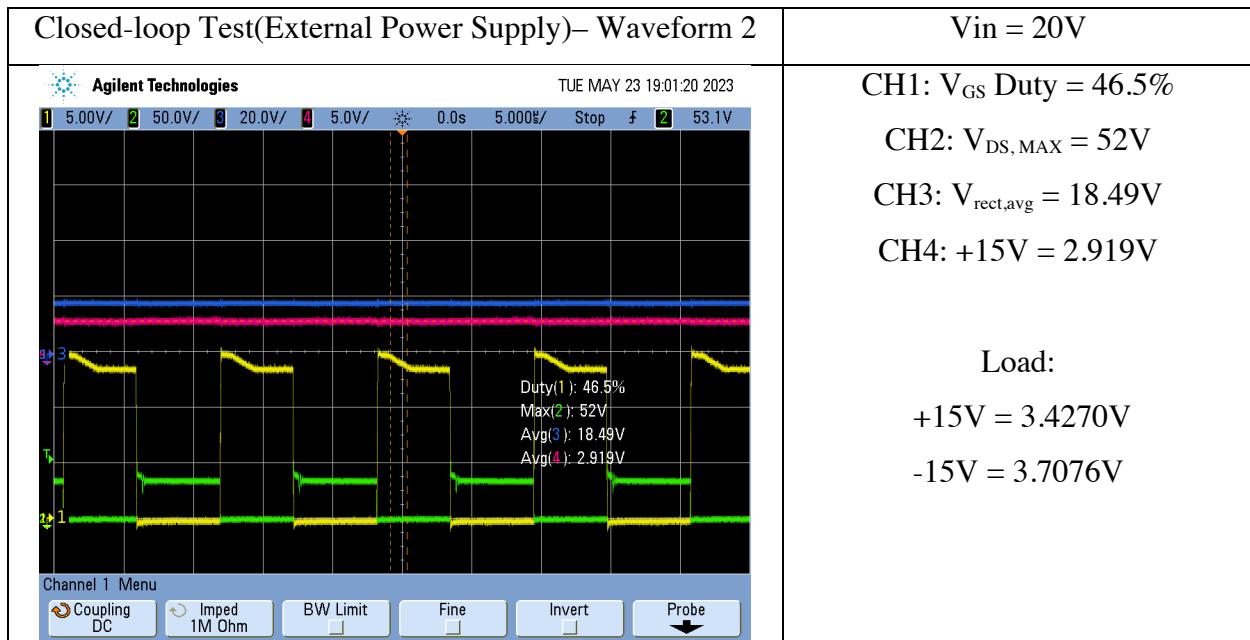
- Measure : Average

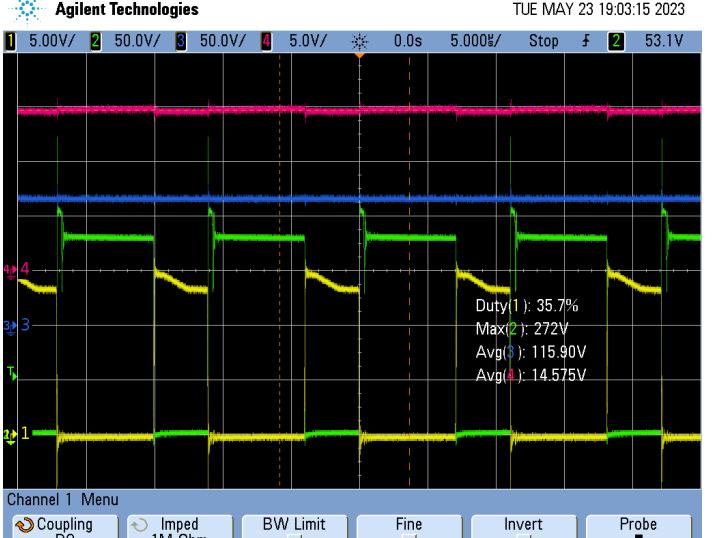
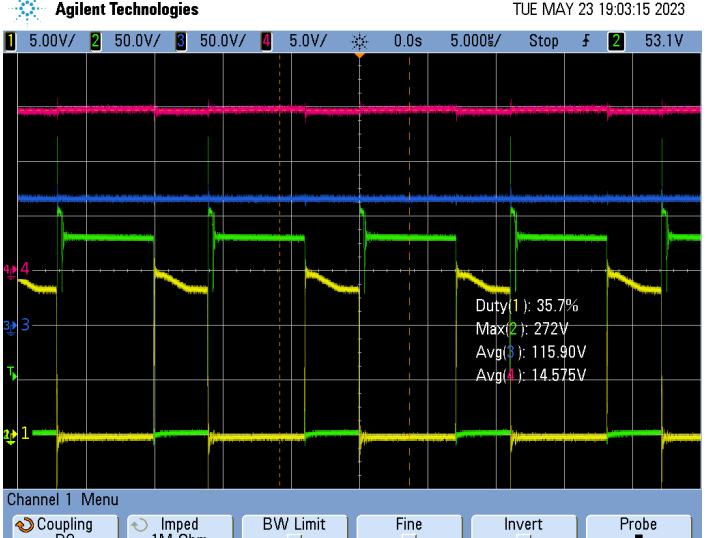
CH4 : +15V

- Measure : Average

CR mode: 7.5Ω





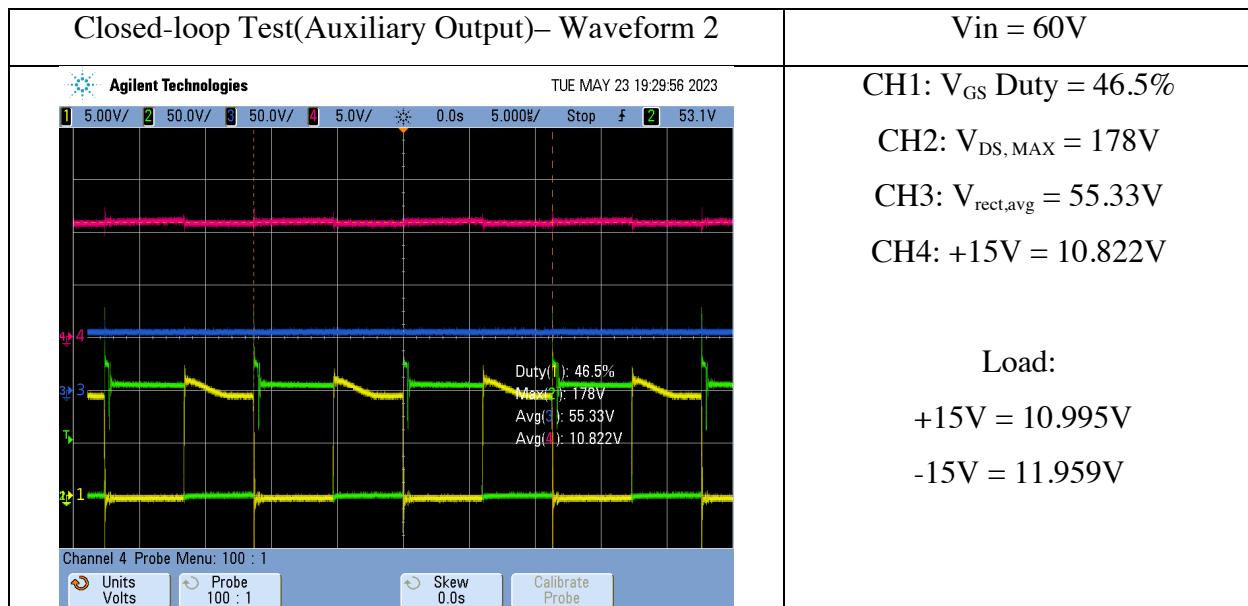
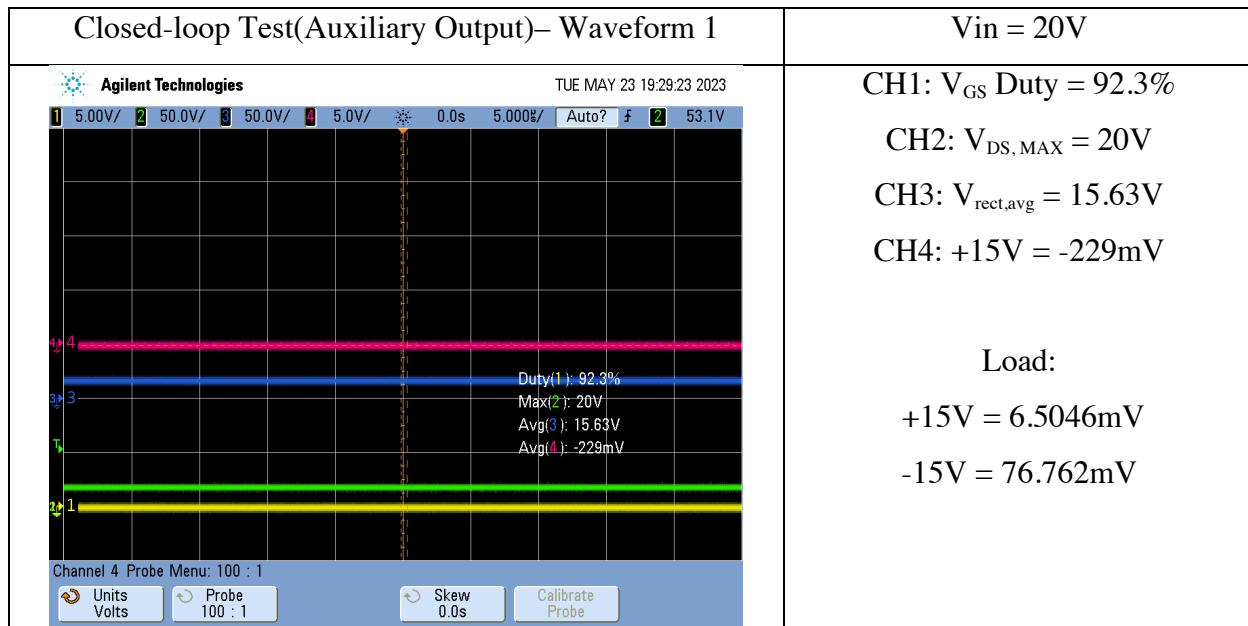
<p>Closed-loop Test(External Power Supply)– Waveform 4</p> 	<p>Vin = 80V</p> <p>CH1: V_{GS} Duty = 46.4%</p> <p>CH2: $V_{DS, MAX} = 259V$</p> <p>CH3: $V_{rect,avg} = 77.61V$</p> <p>CH4: +15V = 14.564V</p> <p>Load:</p> <p>+15V = 14.915V</p> <p>-15V = 16.131V</p>
<p>Closed-loop Test(External Power Supply)– Waveform 5</p> 	<p>Vin = 120V</p> <p>CH1: V_{GS} Duty = 35.7%</p> <p>CH2: $V_{DS, MAX} = 272V$</p> <p>CH3: $V_{rect,avg} = 115.90V$</p> <p>CH4: +15V = 14.575V</p> <p>Load:</p> <p>+15V = 14.947V</p> <p>-15V = 15.923V</p>

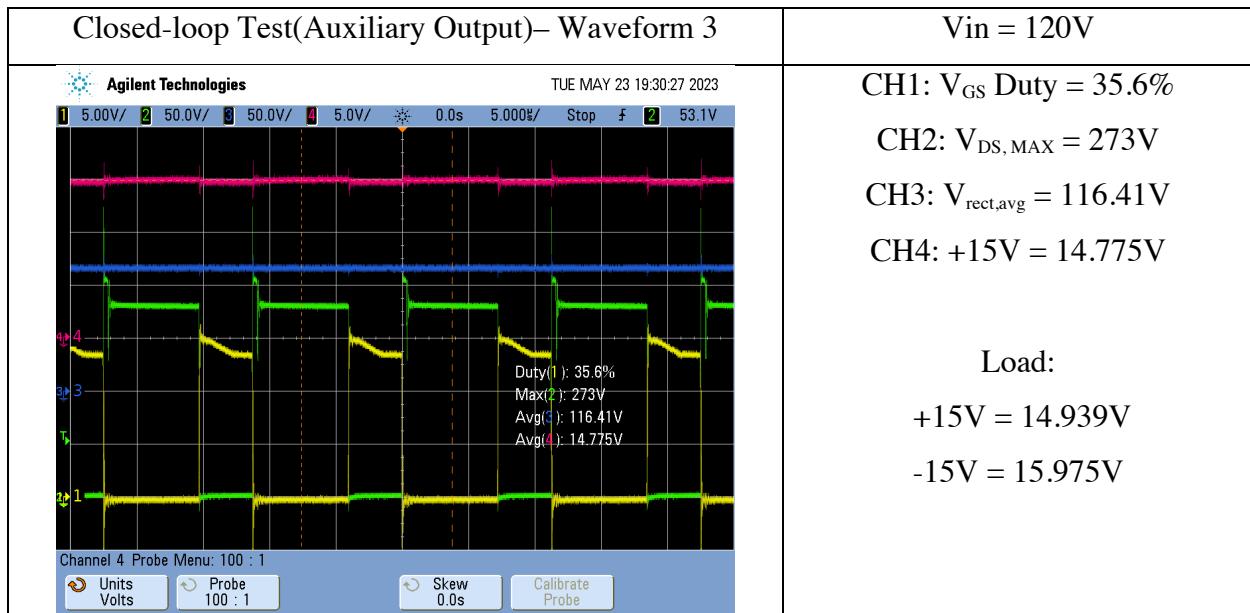
State why or how the converter pass the test.

The control stage can regulate the output voltage, excluding start-up and soft start circuits. The waveform 5 shows that the output voltage is regulated around 15V when input voltage is 120V. The V_{DS} is normal as it hovers around $V_{DS} = V_{in} + nV_{out} = 120 + 4(14.575) = 178.3V$ which matches as shown in the graph.

Note: Duty changes in Vin = 120V due to subharmonic noise because of the bad control stage.

Closed-loop Test (Auxiliary Output)

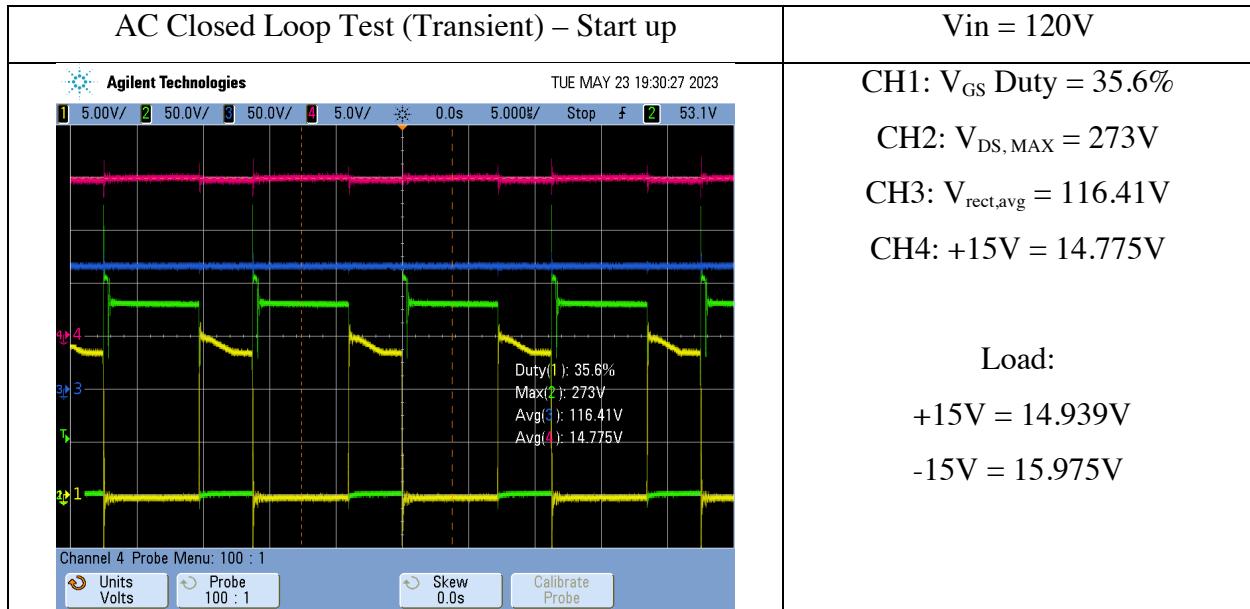




State why or how the converter pass the test.

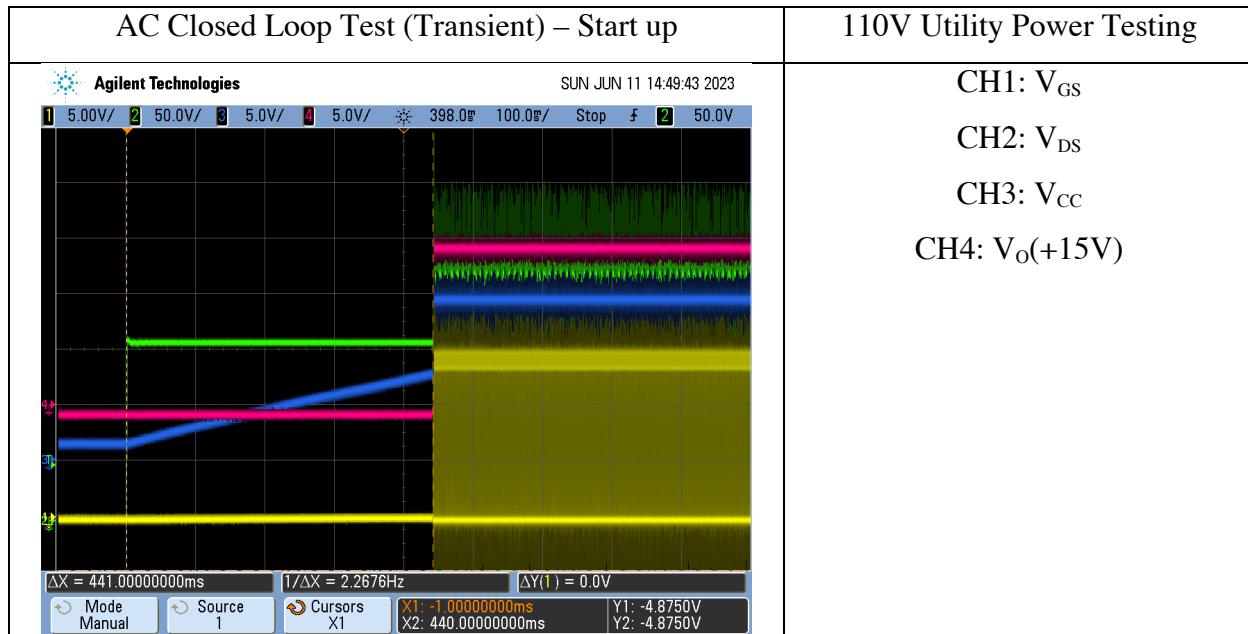
The control stage can regulate the output voltage, including start-up and soft start circuits. The waveform 3 shows that the output voltage is regulated around 15V when input voltage is 120V, which means it is normal. The V_{DS} is normal as it hovers around $V_{DS} = V_{in} + nV_{out} = 120 + 4(14.575) = 178.3V$ which matches as shown in the graph.

AC Closed Loop Test (Steady State)



The 120Hz rectified input seems as DC because the switching frequency 100kHz is far larger than the 120Hz. After input utility power 60Hz 110V_{RMS}, after rectified and regulate into DC, there are still a little wave. Due to feedback control, although input voltage will oscillate, output voltage could still be regulated to a constant.

Transient Start Up



Waveform Description:

From the waveform, we can see that from startup voltage to UVLO voltage, the time it took to startup is around 441ms. The blue which represents Vcc where input rectified voltage charges up the capacitor to increase Vcc voltage until UVLO voltage, which will cause the UC3845 to power on.

Numerical Analysis:

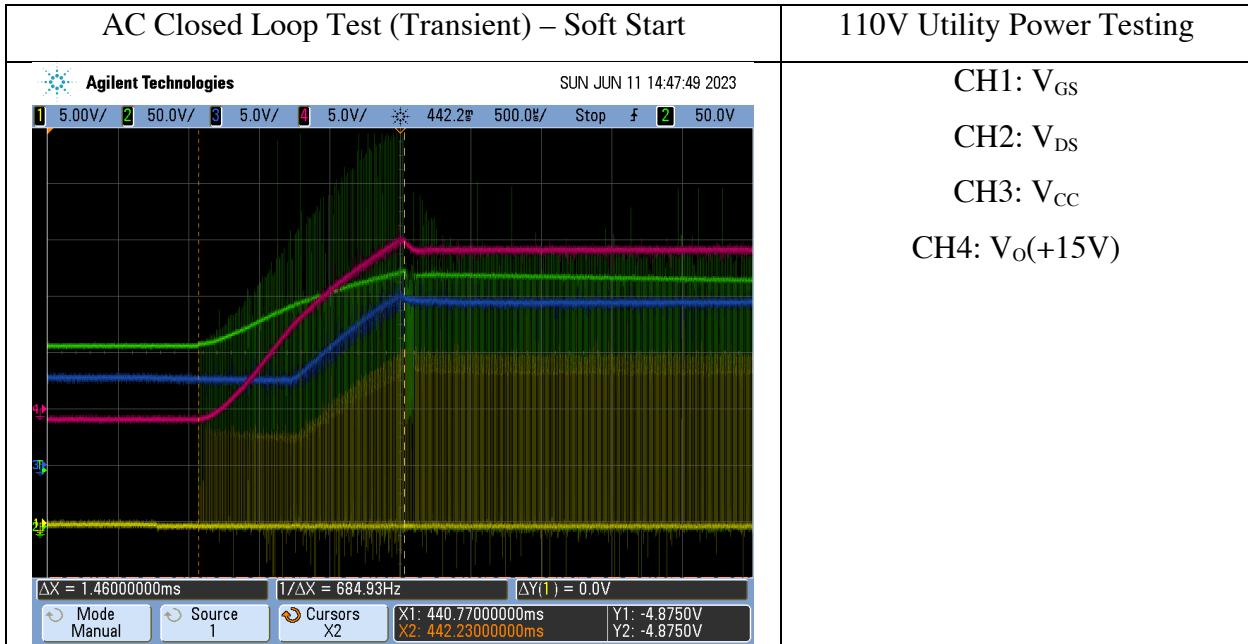
$$V_{rect} = 153 \text{ V}, R = 91\text{k}, C = 100\mu\text{F}, \text{ and } V_{CC,initial} = 1.1\text{V}, V_{CC,UVLO} = 7.9\text{V}$$

$$V_{CC,UVLO} = V_{rect} - (V_{rect} - V_{CC,initial})e^{-t/RC} \rightarrow 7.9 = 153 - (153 - 1.1)e^{-t/(91k * 100\mu\text{F})}$$

$$t = 0.4168\text{ms} = 416.8\text{ms}, \text{ Measured start up is 441ms, error = 5.8\%}.$$

Error might be due to when I measured multiple times, I didn't allow enough time for capacitor to discharge, so when calculating, the initial Vcc might have small measurement error. Also, my cursor is not exactly from the starting to the end, so the measurement should be a little smaller.

Transient Soft Start



Waveform Description:

- When IC turns on, the output voltage gradually increase to 15V.
- When duty of V_{GS} starts getting larger, the V_{CC} voltage rises from UVLO voltage to 15V, then we can see a gap in the middle(yellow/CH1/VGS). The soft start is not enough, the inductor current is still overcharged, which causes the output voltage away from 15V, so in order to control the output voltage back to 15V, there is a period with 0 duty.
- The time it took for V_{CC} to rise to 15V was 1.46ms.

Numerical Analysis:

V_{base} get from 0 to 5V

$$V_C = V_I - (V_I - V_0)e^{-t/RC}$$

$$V_I = 5 \text{ V}, V_0 = 0\text{V}, R = 91\text{k}, C = 100\mu\text{F},$$

$$\text{Approximately } V_C = 4.583\text{V}$$

$$t = 0.005465 = 5.465\text{ms}, \text{Measured soft start is } 1.46\text{ms, error} = 73.3\%.$$

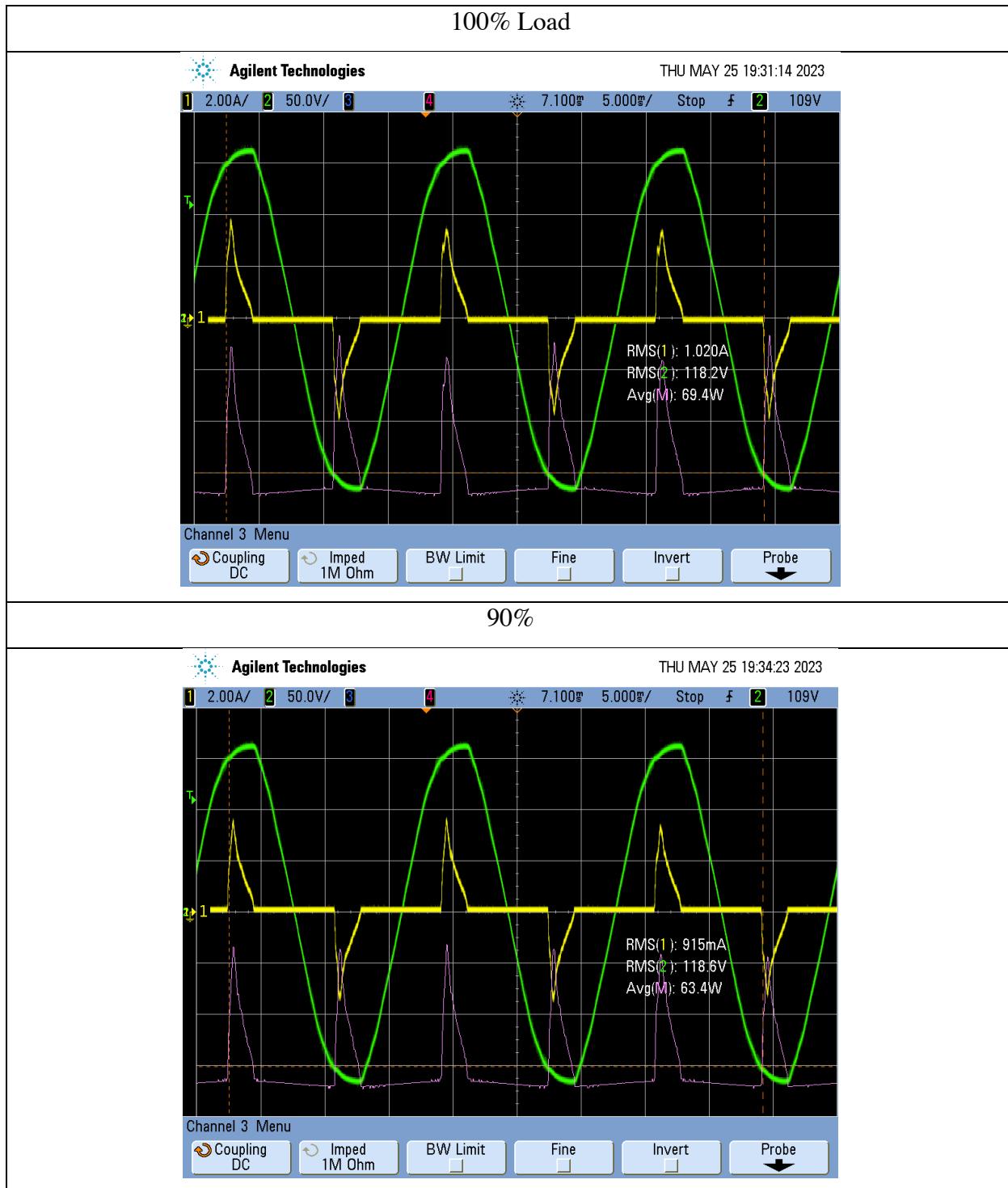
Error might be due to the fact that I measured the soft start by without using the time from the V_{base}, but the time of the rise in V_{CC}. In the calculations, I use V_{base} approximation, so that is why there's a really big error. Due to USB loss, my original waveform is gone, and I forgot to get V_{comp} on my second time. Next time, I should measure V_{base} or V_{comp} for a more accurate measurement.

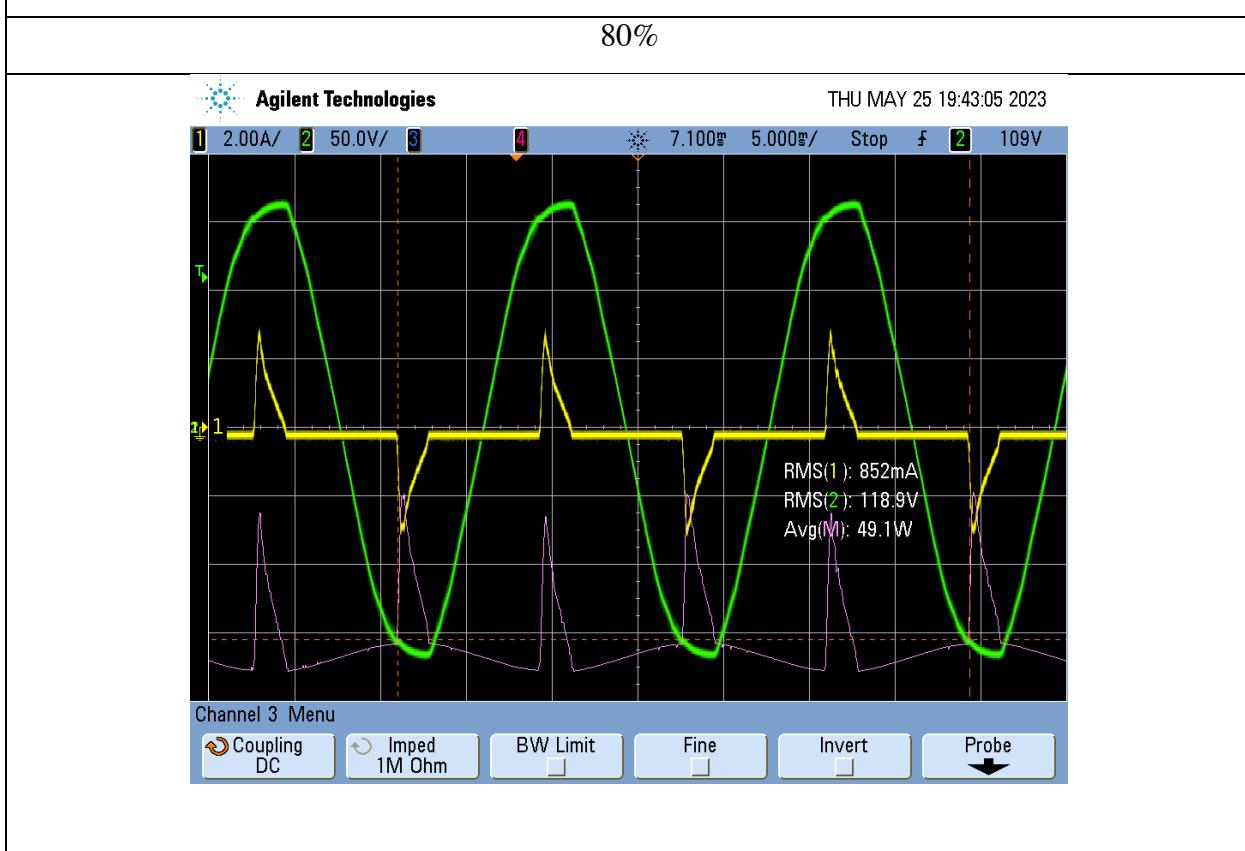
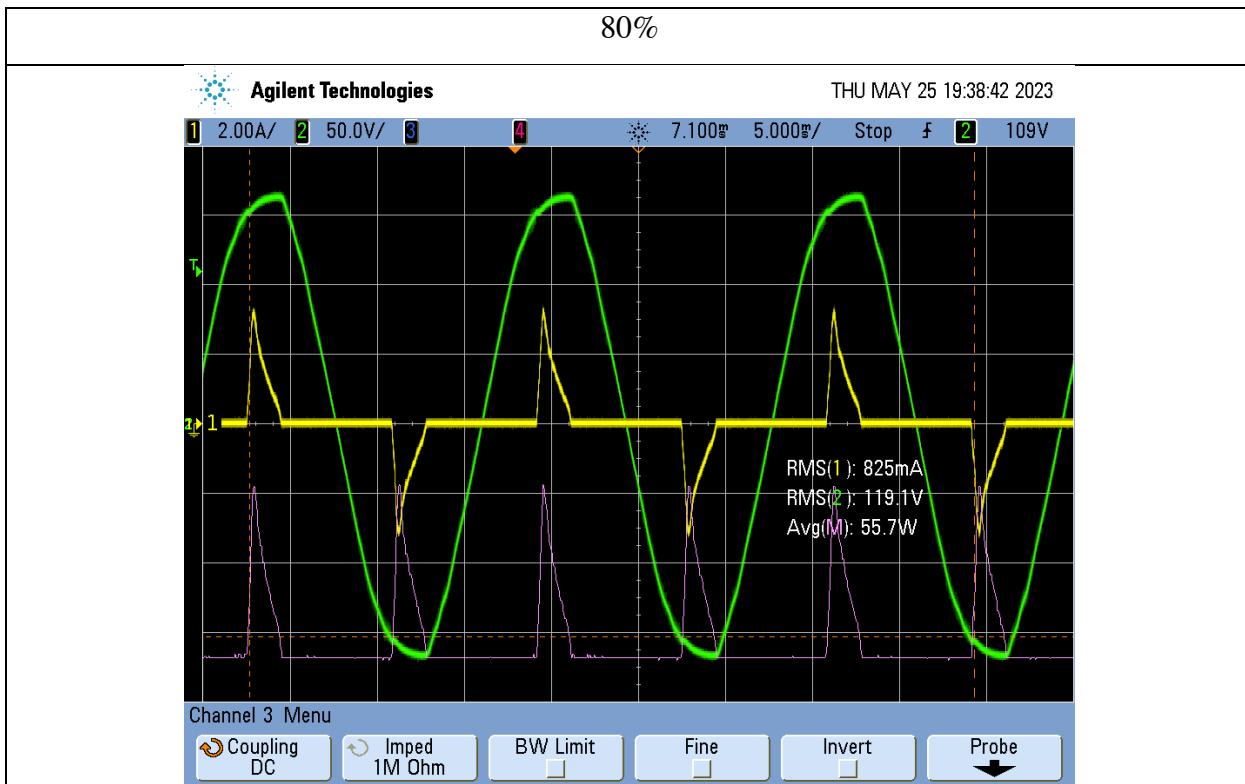
Efficiency

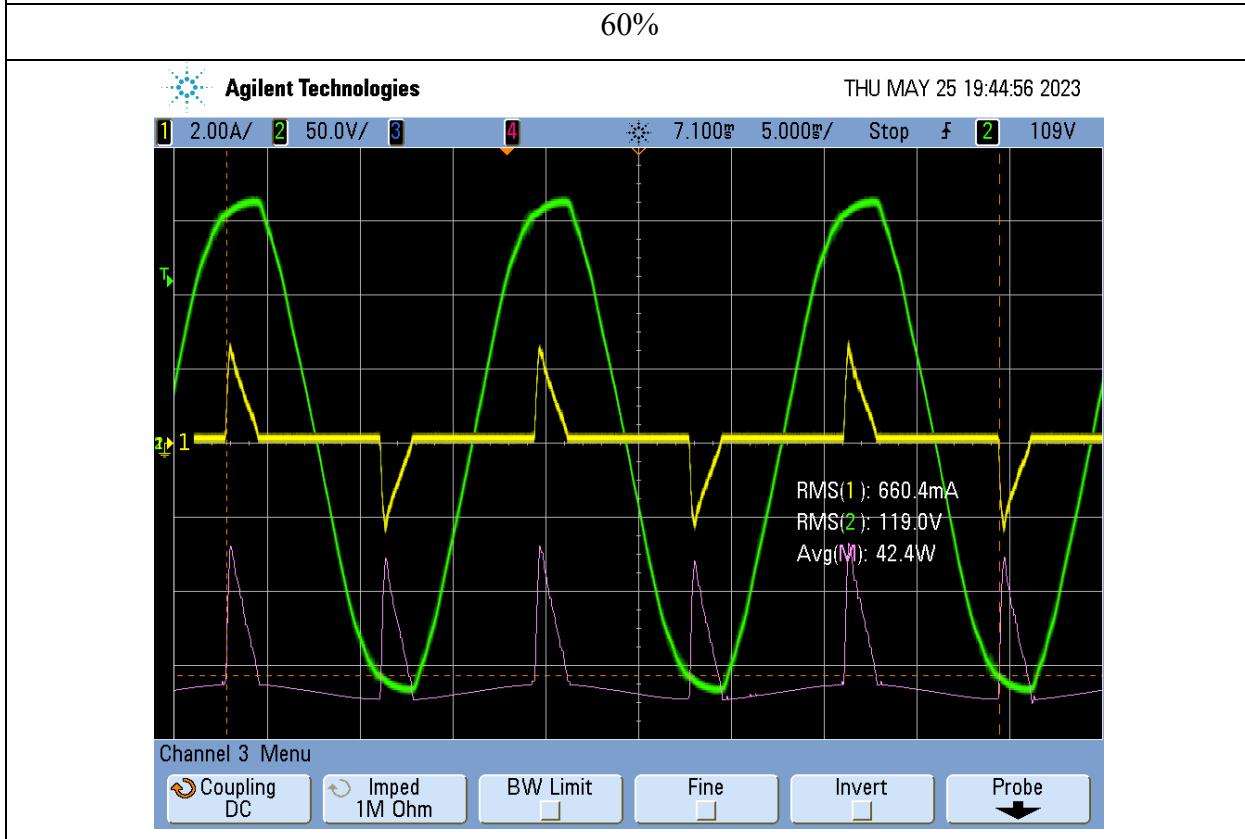
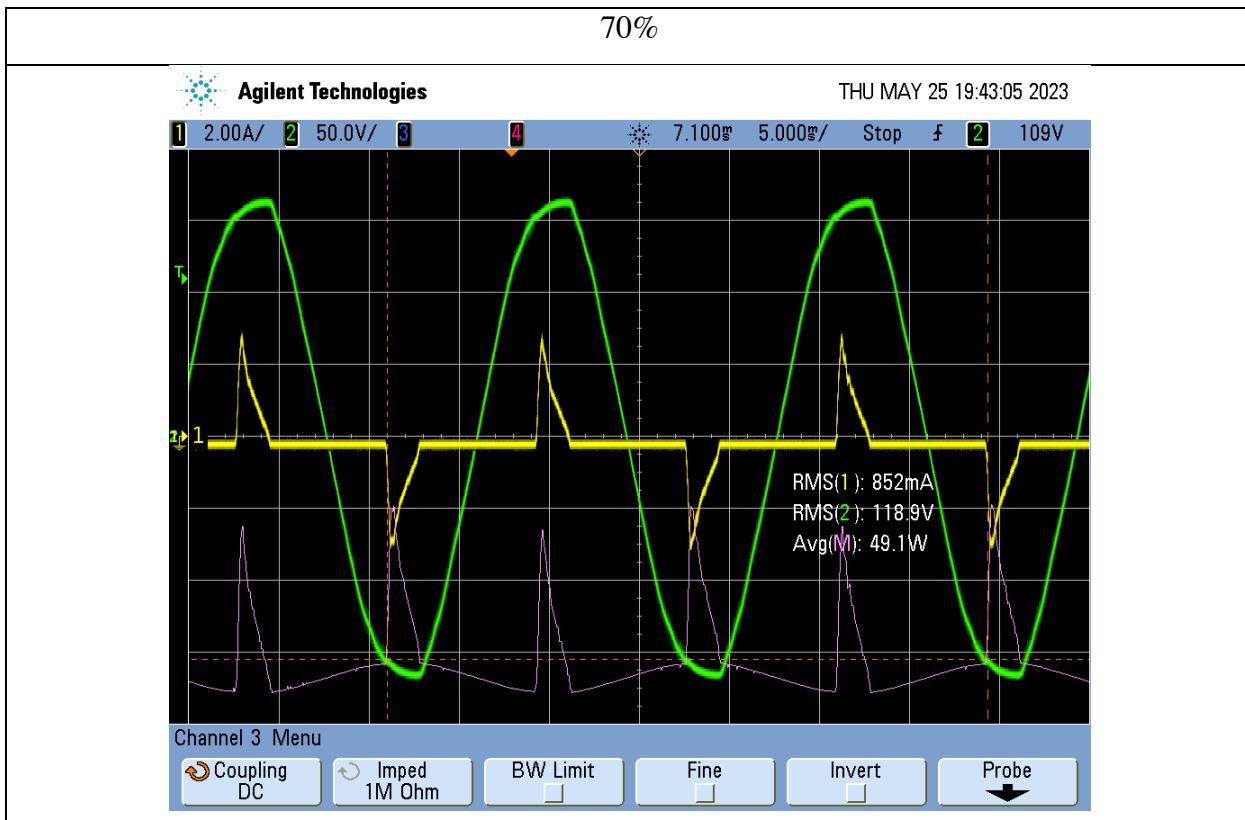
CH1: Input Current, No Power factor correction

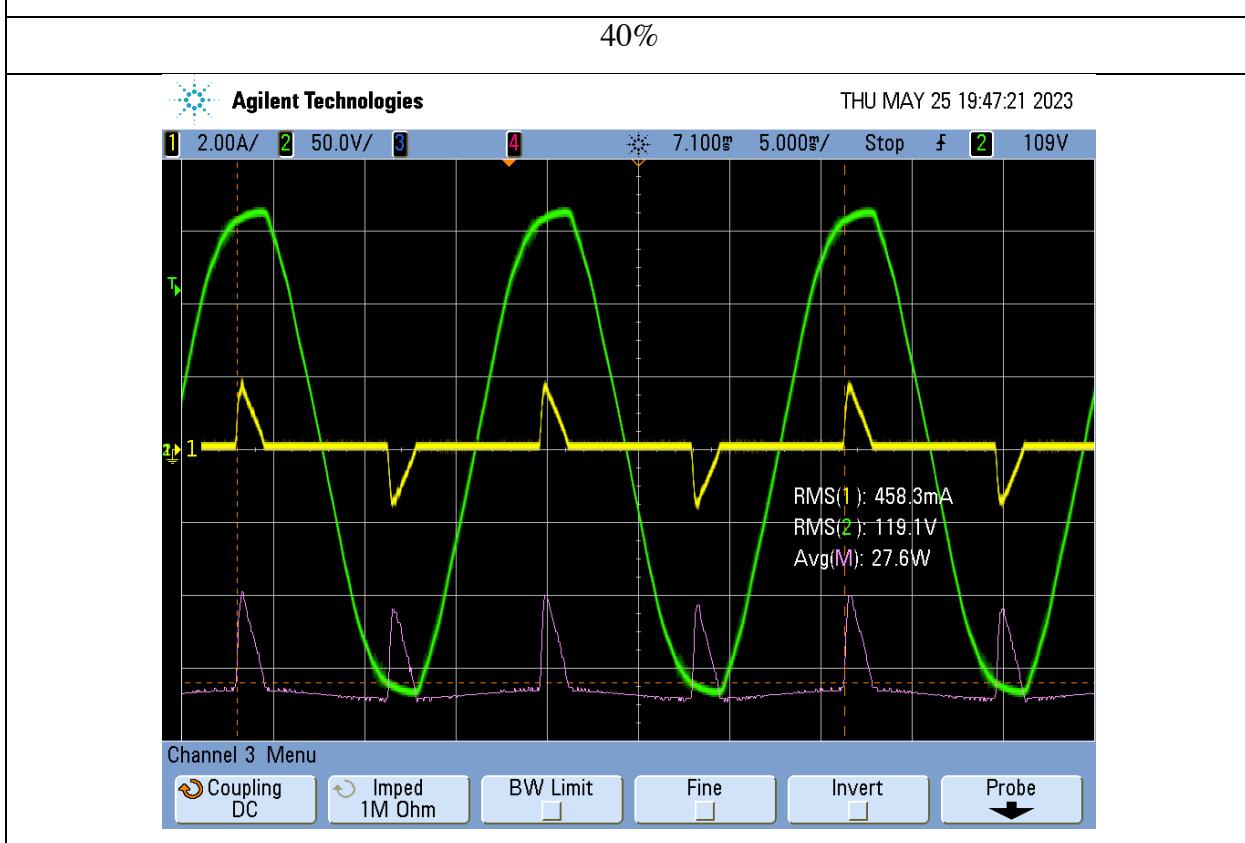
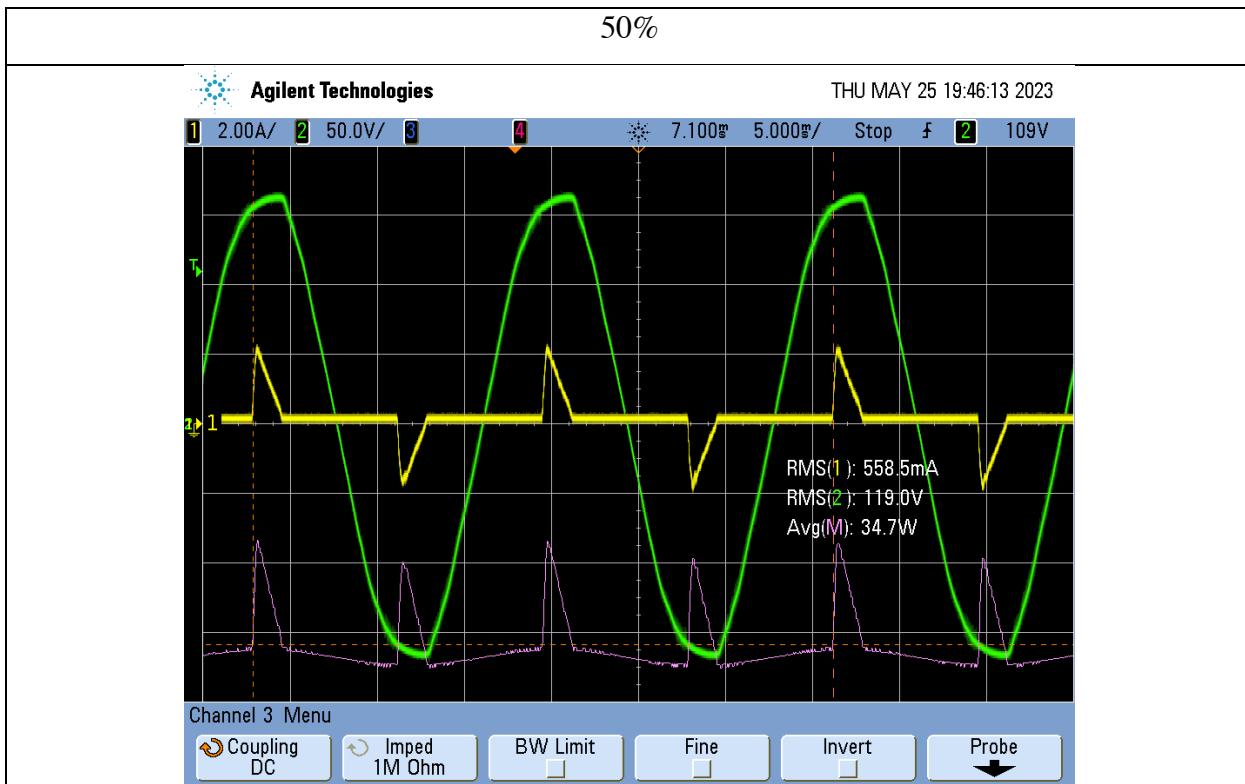
CH2: Input Voltage, AC utility power 60Hz

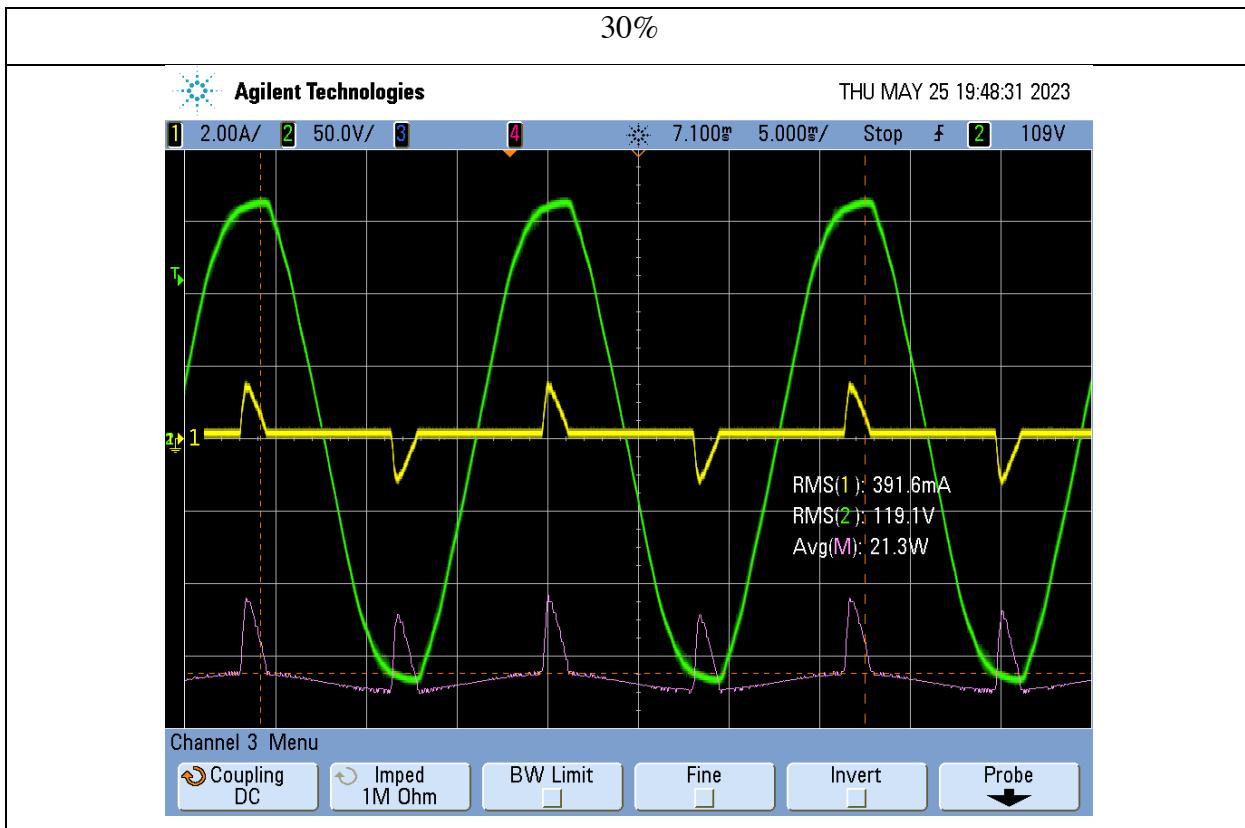
M: CH1 * CH2







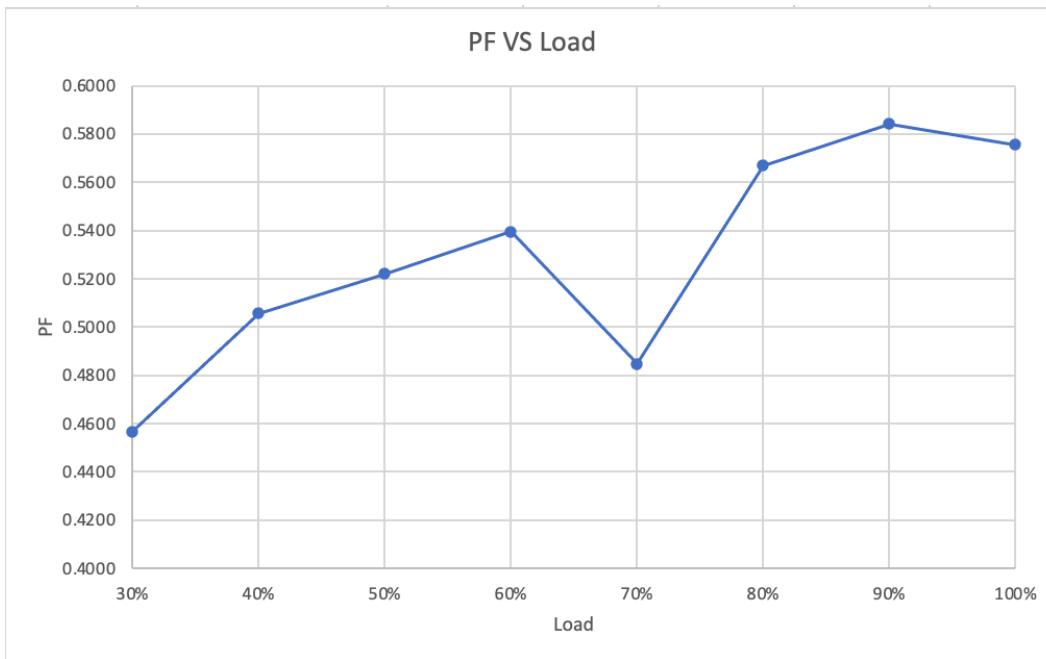
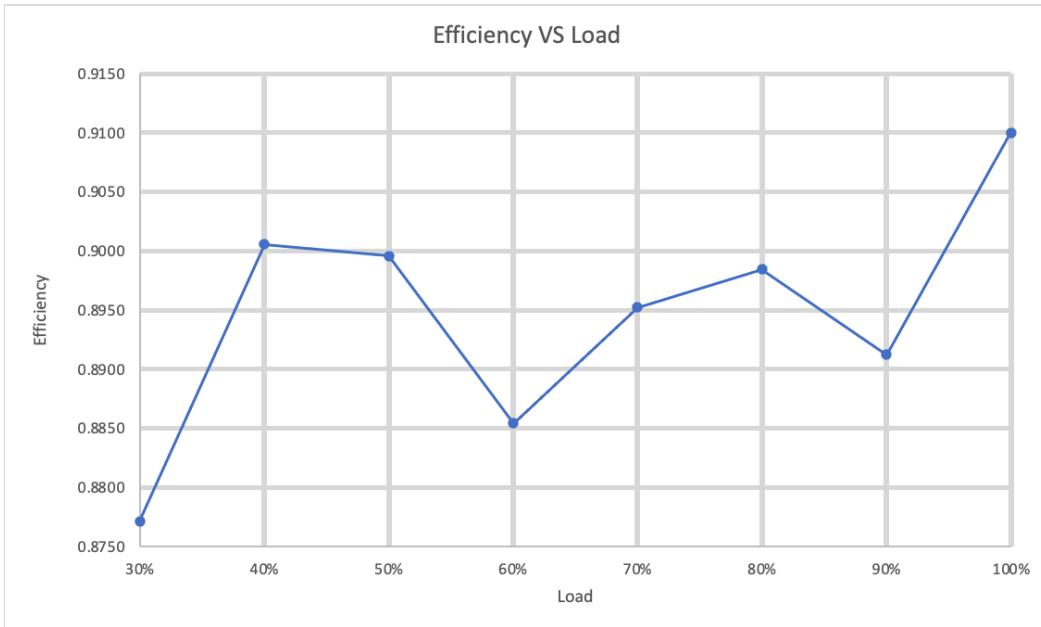




Data Tables: Efficiency = Pout/Pin

Load(%)	Load1/Load2(Ω / Ω)	Pin(W)	P1(W)	P2(W)	Pout(W)	Efficiency
100%	7.5/7.5	69.4	29.637	33.518	63.155	0.9100
90%	8.3/8.3	63.4	26.446	30.057	56.503	0.8912
80%	9.4/9.4	55.7	23.572	26.472	50.044	0.8985
70%	10.7/10.7	49.1	20.813	23.142	43.955	0.8952
60%	12.5/12.5	42.4	17.848	19.694	37.542	0.8854
50%	15/15	34.7	14.897	16.318	31.215	0.8996
40%	18.8/18.8	27.6	11.904	12.952	24.856	0.9006
30%	25/25	21.3	8.9679	9.7155	18.6834	0.8772

Load(%)	Load1/Load2(Ω / Ω)	Pin(W)	Vin(V)	Iin(A)	Vin*Iin	PF
100%	7.5/7.5	69.4	118.2	1.02	120.564	0.5756
90%	8.3/8.3	63.4	118.6	0.915	108.519	0.5842
80%	9.4/9.4	55.7	119.1	0.825	98.2575	0.5669
70%	10.7/10.7	49.1	118.9	0.852	101.3028	0.4847
60%	12.5/12.5	42.4	119	0.6604	78.5876	0.5395
50%	15/15	34.7	119	0.5585	66.4615	0.5221
40%	18.8/18.8	27.6	119.1	0.4583	54.58353	0.5056
30%	25/25	21.3	119.1	0.3916	46.63956	0.4567



PF graph shown because input current and voltage are not sine waves with the same phase, there is reactive power in the input power, so $V_{in,RMS} \times I_{IN,RMS} = S \neq P$.

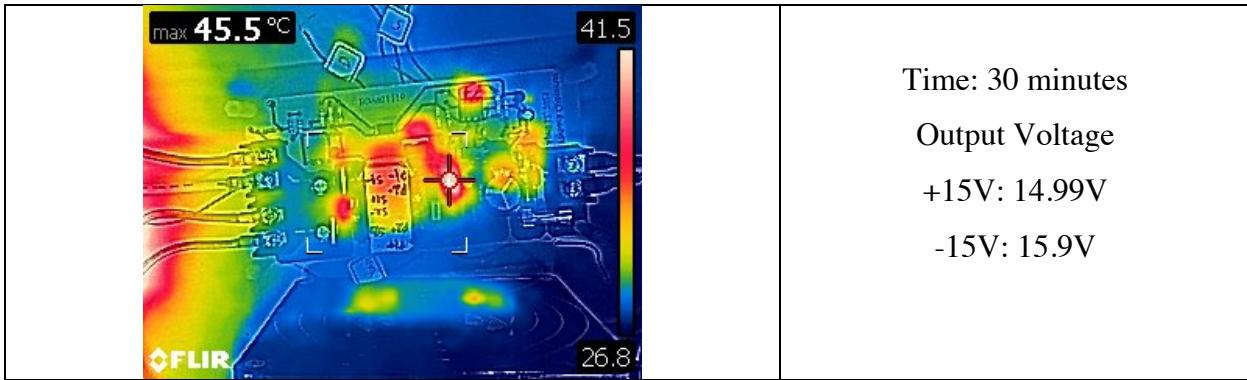
$$PF = \frac{P_{IN}}{V_{IN,RMS} \times I_{IN,RMS}}$$

For our efficiency, it is fairly consistent at around 0.87 to 0.91 for all load.

Looking at power factor vs load, closer to a full load will yield the highest power factor which means it will be more power efficient. The trend of both is really similar with more percentage of load, it will have a more efficient output power. We can clearly see the relations in $P = V^2 / R$.

Burn In

Burn In Photo	Data
	<p>Time 0:00 Output Voltage +15V: 15V -15V: 15.9V</p>
	<p>Reach 70-80 Degrees Time: 7:15 Output Voltage +15V: 14.99V -15V: 15.89V</p>
	<p>Time: 10 minutes Output Voltage +15V: 14.99V -15V: 15.89V</p>
	<p>Time: 20 minutes Output Voltage +15V: 14.99V -15V: 15.91V</p>



- a. Reach 70 degrees Celsius in 7 min 15 seconds.
- b. Add fan after that and reach around 45 Celsius for the rest of the test.

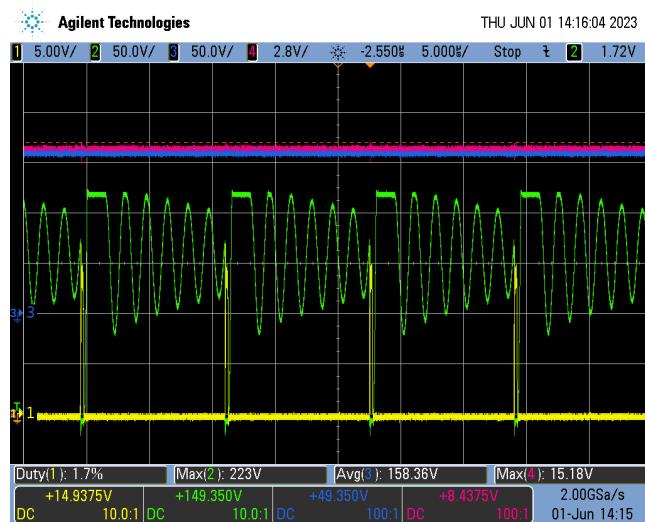
0-70 without fan: 7:15

Stable under fan: 45 degrees Celcius

No-Load Starting

CH1: V_{GS} CH2: V_{DS}

CH3: V_{RECT} CH4: V_{OUT}



V_{GS} has a very small duty, V_{DS} shows that it operates in DCM with the oscillations because it has no/very light load.

The control circuit have to regulate the output voltage will damage the output capacitor. The circuit still input power to the magnetizing inductance and IC. V_{out} is at 15.18V. V_{rect} is at around 158.36V.

Load Transient

Load 1 : 2A (100% Load)

$T_1 = 5\text{ms}$

Rise(Slew Rate): 2A/us

CH1(yellow): $V_{\text{out}}(+15\text{V})$ AC

CH3: V_{DS} (not needed, just for checking it works)

Load 2 : 1A (50% Load)

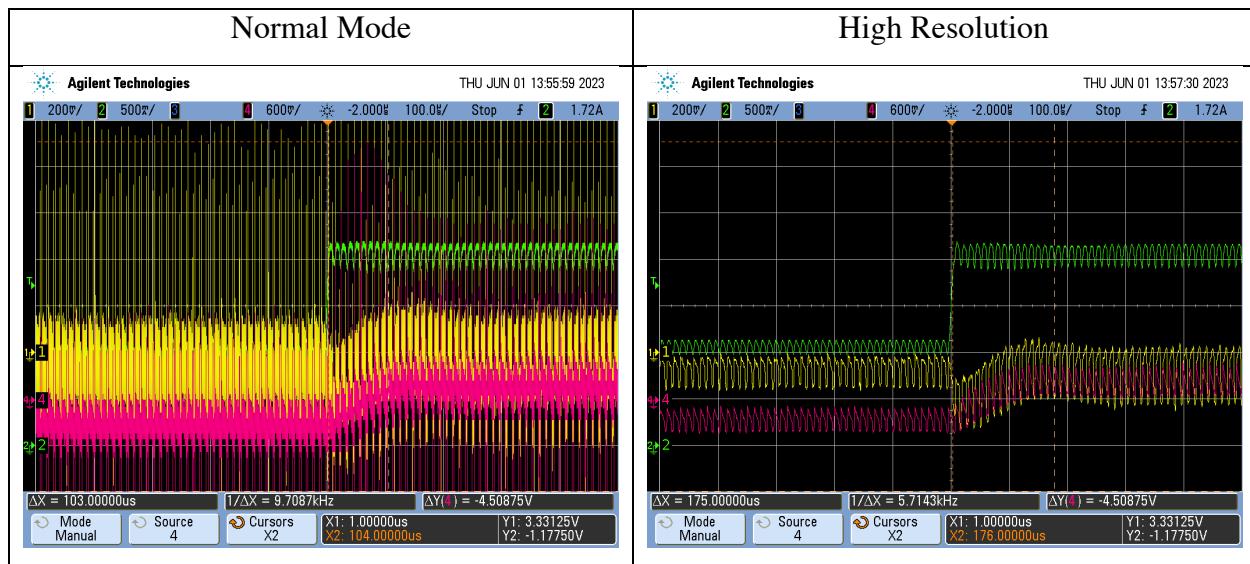
$T_2 = 5\text{ms}$ (sufficient of rise and fall)

Fall(Slew Rate): 2A/us

CH2(Green): $I_{\text{out}}(+15\text{V})$

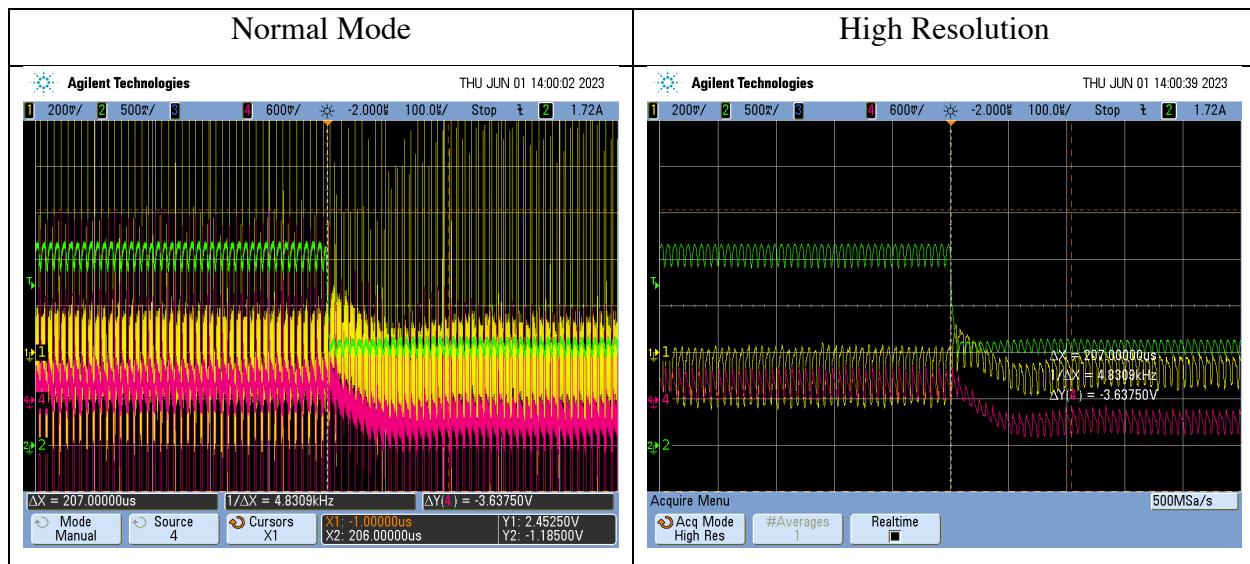
CH4(red): $V_{\text{out}}(-15\text{V})$ AC

Rise



Numerical Measurement: The rise time is 175us.

Fall



Numerical Measurement: The falling time is 207us.

Rising Analysis:

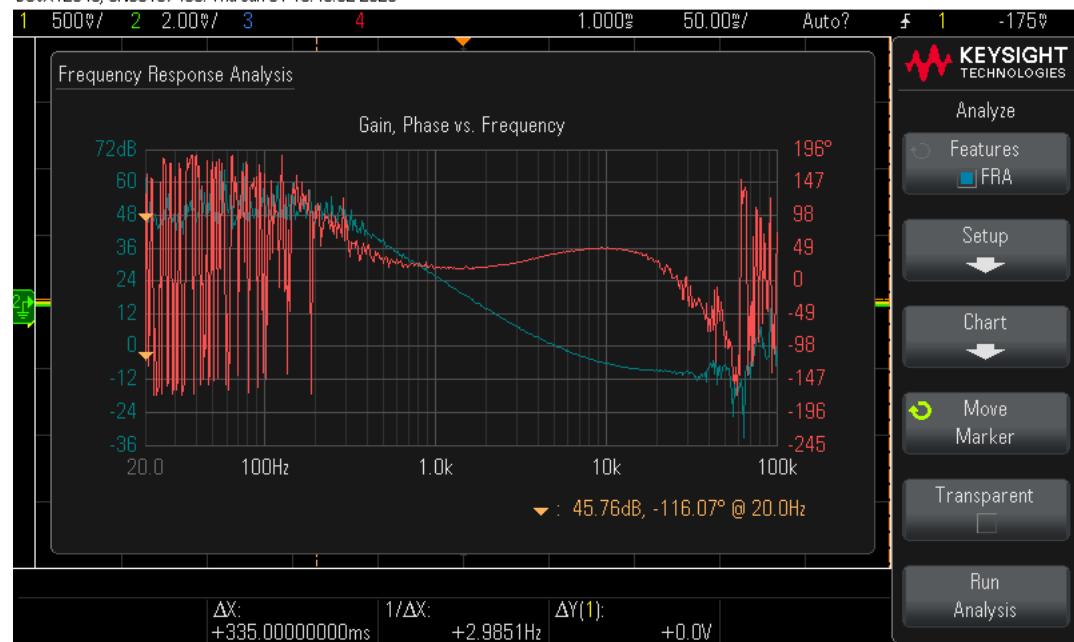
When load change from light to heavy, the output voltage (yellow) decrease a bit. The duty is increased accordingly to output more load. So the -15V(red) rise a little. A sudden increase in load makes the output current increase. After 175us, the circuit reach steady state operation again seen in the output voltages.

Falling Analysis:

When load change from heavy to light, the output voltage (yellow) increase a bit. The duty is decreased accordingly to output less load. So the -15V(red) decrease a little. A sudden decrease in load makes the output current decrease. After 207us, the circuit reach steady state operation again seen in the output voltages.

Frequency Response Analysis

DSOX1204G, CN60167485; Thu Jun 01 15:46:52 2023



Input : CH1

Output : CH2

Frequency: 20Hz to 100kHz

Amplitude: 1Vpp

Points: 500 points

Output Load: 500 points

The recorded **LC double pole frequency** is around 200 to 300Hz.

The **bandwidth** recorded is around 5.0kHz, where the DC gain is 45.76dB. The bandwidth is from when the gain reaches 0dB, which is around 5kHz.

Difficulties Encountered Along the Way and Solutions:

1. When I was soldering my components onto the board, I noticed that one hole is a little smaller than the pin, so the component cannot fit into the whole. This part took me around 30 minutes to solve because I was afraid I had to redo everything. The solution that I did was to use a sharp item to carve out the side to make the hole bigger, and try to push the pin into the hole. At the end, I went to change the hole size in my easyEDA as well.
2. When I first start to do the open loop test, I was confused on how to connect my power supply, load, and setup the oscilloscope. I watched the tutorial video and worked on it at the same time. As I move on with closed loop, start up, soft start, load transient, I got quicker with the setup and made fewer mistakes.
3. When I was doing my Load transient test, my fuses burst. After checking, we found out that two of my diodes is broken. I resolder the two new diode and its done.
4. I used the USB in the lab and it was gone. My data of soft start and start up was inside. I found time during the buffer week to go redo it, although I didn't measure Vcomp....
5. When I was working on my no load starting, I couldn't measure my Vrect or it output a really weird waveform. I couldn't figured out why because I connected everything correctly. After searching for the problem for so long, I figured out that I connected the measuring probe onto the rubber part of the wire....

Review and Feedback:

First, I feel like there are so many videos on NTU Cool to watch, especially the ones where TA explains the circuit. I think it is pretty useful because when I am working on the experiment, it actually shows the same result. For 實作 videos, I usually watch it the same time when I am working on the experiment because it is way faster.

During Experiment: