Lab ?: ??????????

# Design Explanation

## NAND Implement Lawrence

1. Design Concepts
2. Schematic Graph

## NAND Implement Ariel

## Ripple Adder

## Decode and Execute

## Carry Lookahead Adder

1. Design Concepts

We divide CLA (Carry Lookahead Adder) into 3 modules, adder unit, 4-bit CLA generator, 2-bit CLA generator.

First, the adder unit process inputs into p (propagate) flag and g (generate) flag. Second, 4-bit CLA process p flag and g flag into c (carry) flags. 4-bit CLA would also condense p flags and g flags. Last, 2-bit CLA generator process the condensed p flags and g flags into c flag.

Such procedure could significantly reduce the latency from gates to gates, we will dig into the benefits in following discussion.

1. Schematic Graph
2. Benefits
3. How it works?
4. Circuits Explanation

## 4-bit Multipler

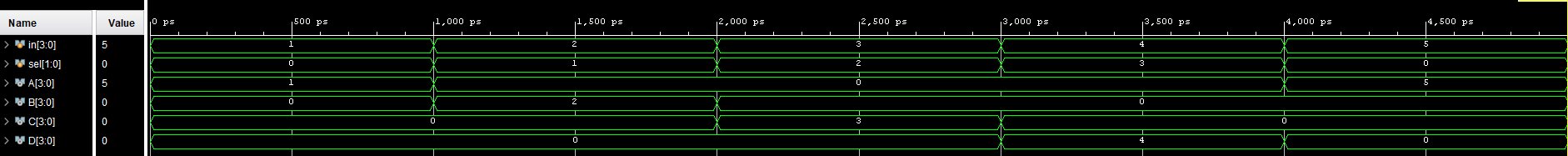
1. How it works?
2. Schematic Graph

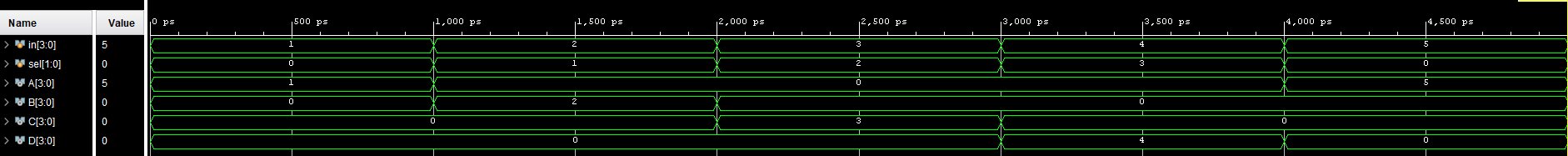
## Exhausted Testbench

# Design Verification

## DMUX

Enumerate all possible inputs, and verify the outputs manually. The pictures below are the representation with verification.





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# Contribution

## Lawrence Wu

## Ariel Chang

# What have we learned?