Implementations of Multiple Controlled-X (MCX) Circuit

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1 Part A: 3 Different Implementations of 5 Control and 1 Target Qubits

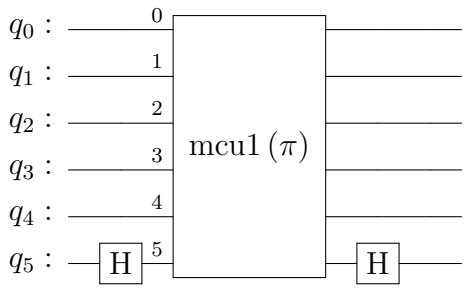
1.1 Minimized Width

In the first implementation, we try to minimize width by adding an optimization parameter "width". The result is the MCX circuit with the lowest number of qubits: five control; one target.
Without transpilation,

- depth: 63
- width: 6

With transpilation,

- depth: 117
- width: 6



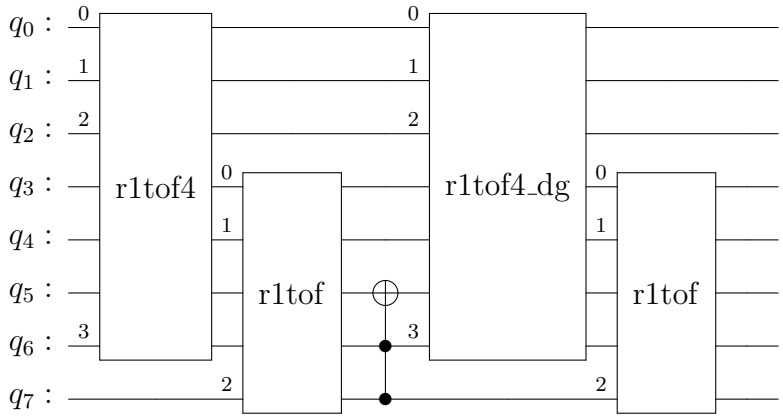
1.2 Minimized Depth

In the second implementation, we use another optimization parameter "depth". We achieve the MCX circuit with the lowest number of gates. Note that as the number of gates decreases, more qubits are demanded.
Without transpilation,

- depth: 47
- width: 8

With transpilation,

- depth: 34
- width: 8



1.3 Arbitrary Width & Depth

Lastly we create a MCX circuit with arbitrary values for width and depth, creating an arbitrary number of qubits and gates. For this implementation, we can easily verify that values are in fact between the minimum width and depth.
We pass

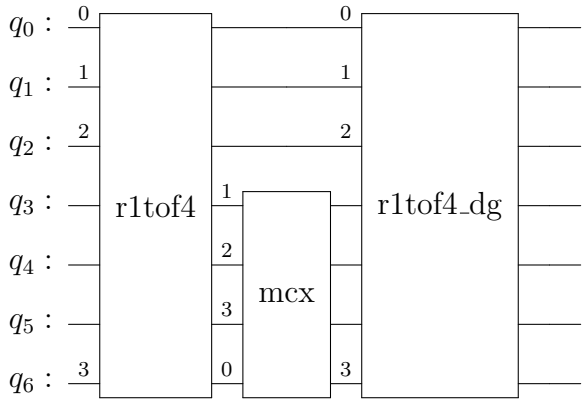
- 7 as maximum width
- 70 as maximum depth

to obtain

- depth: 63
- width: 7

without transpilation.
With transpilation,

- depth: 51
- width: 7



2 Part B: 2 Different Implementations of 20 Control and 1 Target Qubits

2.1 Minimized Width

This part requires a circuit with 20 control and 1 target qubits. This optimizes the width. With 21 qubits, we can expect an increase in the number of gates or depth.
Without transpilation,

- depth: 2277
- width: 22

As we can see below, there are too many gates without transpilation-

- H: 512
- P: 600
- CX: 992
- CU1: 216
- U2: 192
- U1: 384

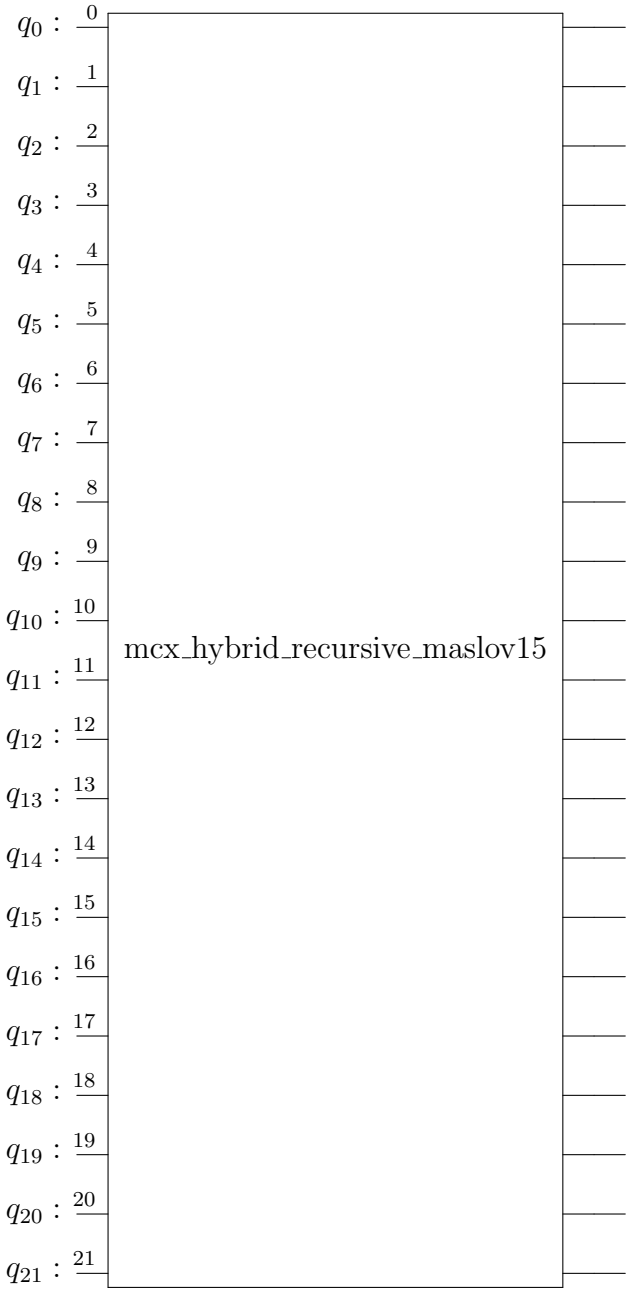
With transpilation,

- depth: 1894
- width: 22

The gates with transpilation-

- U: 1501
- CX: 1424

This circuit is indeed more complicated and contains more gates with the constraint on the width. We simply cannot express all of those gates in this file.


q_0 : 0
q_1 : 1
q_2 : 2
q_3 : 3
q_4 : 4
q_5 : 5
q_6 : 6
q_7 : 7
q_8 : 8
q_9 : 9
q_{10} : 10
q_{11} : 11
q_{12} : 12
q_{13} : 13
q_{14} : 14
q_{15} : 15
q_{16} : 16
q_{17} : 17
q_{18} : 18
q_{19} : 19
q_{20} : 20
q_{21} : 21
mcx_hybrid_recursive_maslov15

2.2 Minimized Depth

This section indicates an optimization of depth for the MCX circuit which means we will use the lowest number of gates. As we have observed before, this leads to an increase in the number of qubits.
Without transpilation,

- depth: 119
- width: 30

The number of qubits are increased to compensate the reduced depth. The reduced depth means it needs fewer gates compared to the above implementation. The gates without transpilation-

- H: 74
- T: 76
- CX: 114
- TDG: 75

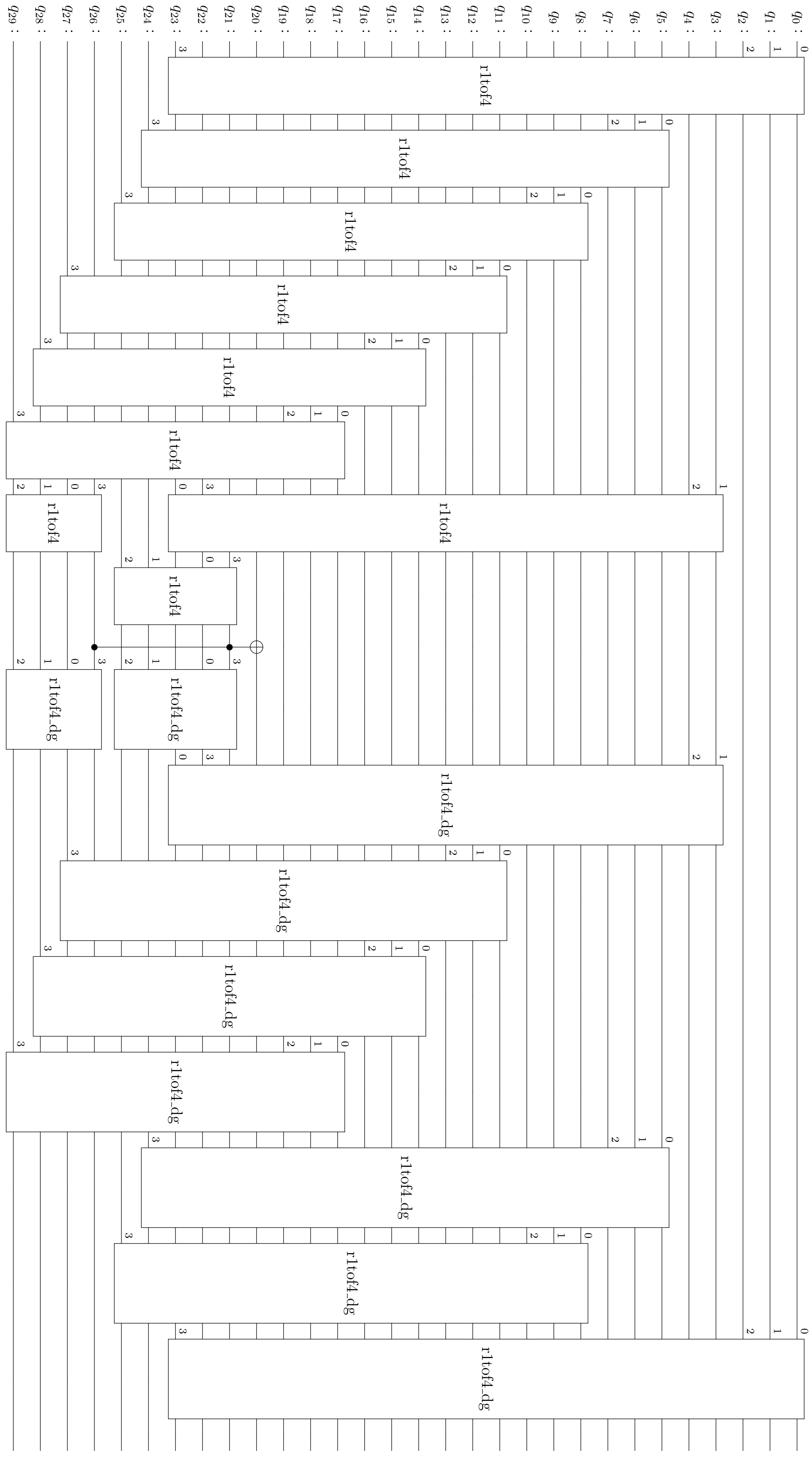
With transpilation,

- depth: 66
- width: 30

The gates with transpilation-

- U: 132
- CX: 114

Although the circuit eliminates much complexity, there is a scalability issue because it is more difficult to maintain more qubits.



q_0 : q_1 : q_2 : q_3 : q_4 : q_5 : q_6 : q_7 : q_8 : q_9 : q_{10} : q_{11} : q_{12} : q_{13} : q_{14} : q_{15} : q_{16} : q_{17} : q_{18} : q_{19} : q_{20} : q_{21} : q_{22} : q_{23} : q_{24} : q_{25} : q_{26} : q_{27} : q_{28} : q_{29} :
r1tof4
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