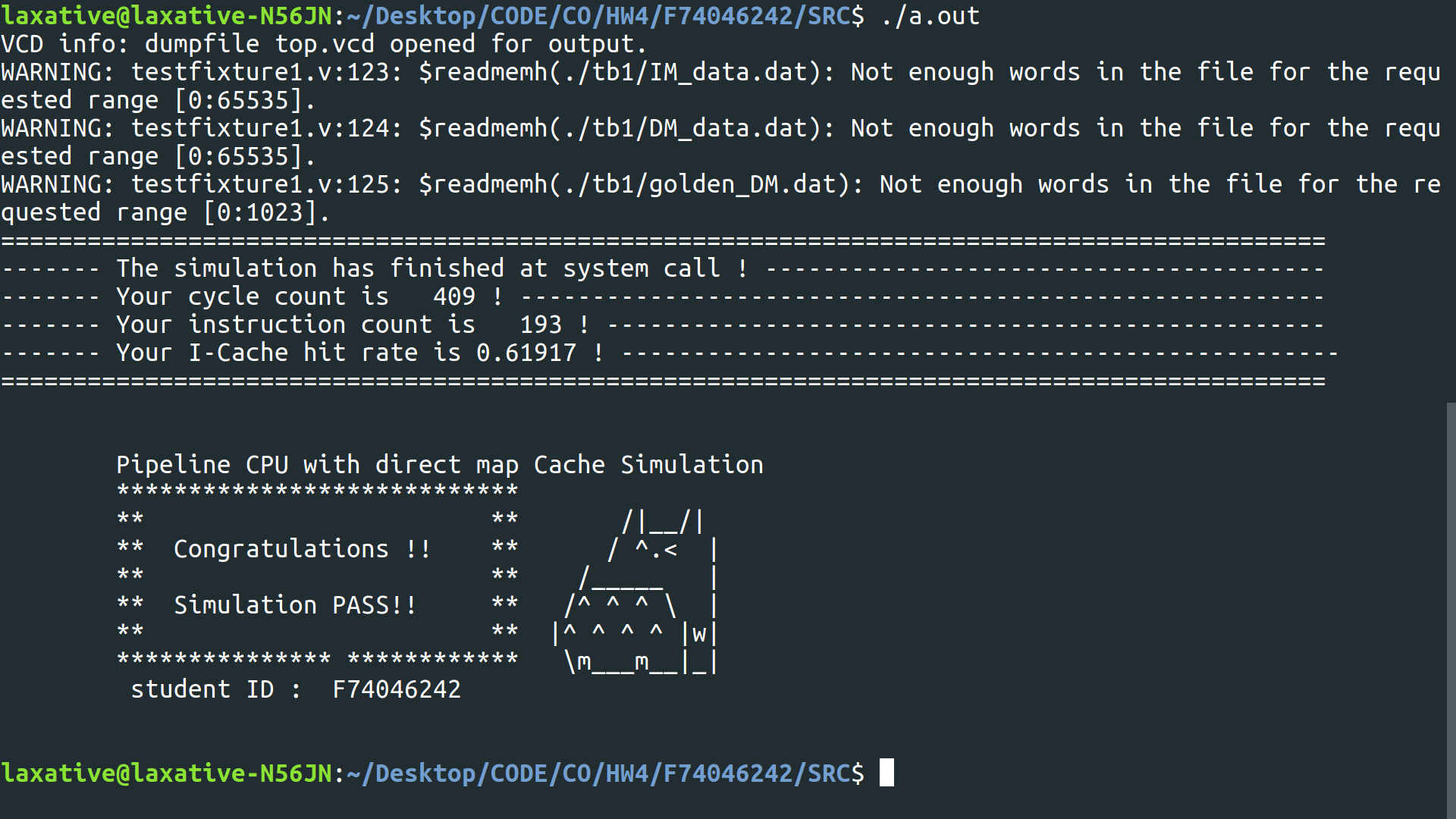
**Computer Organization 2017**

**HOMEWORK IV**

系級: 資訊108 學號: F74046242 姓名: 謝耀賢

**實驗結果圖(snapshot of result)**

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**The I-Cache hit rate of your simulation & your reason:**

**指令波型圖( Instruction waveform of some situations)**

(Please explain why your snapshot is correct, including the wires, signals.)

1. I-Cache Miss



Description:

If I-Cache hit = 0 => I-Cache Miss, get the data from the memory and place the data into the cache.

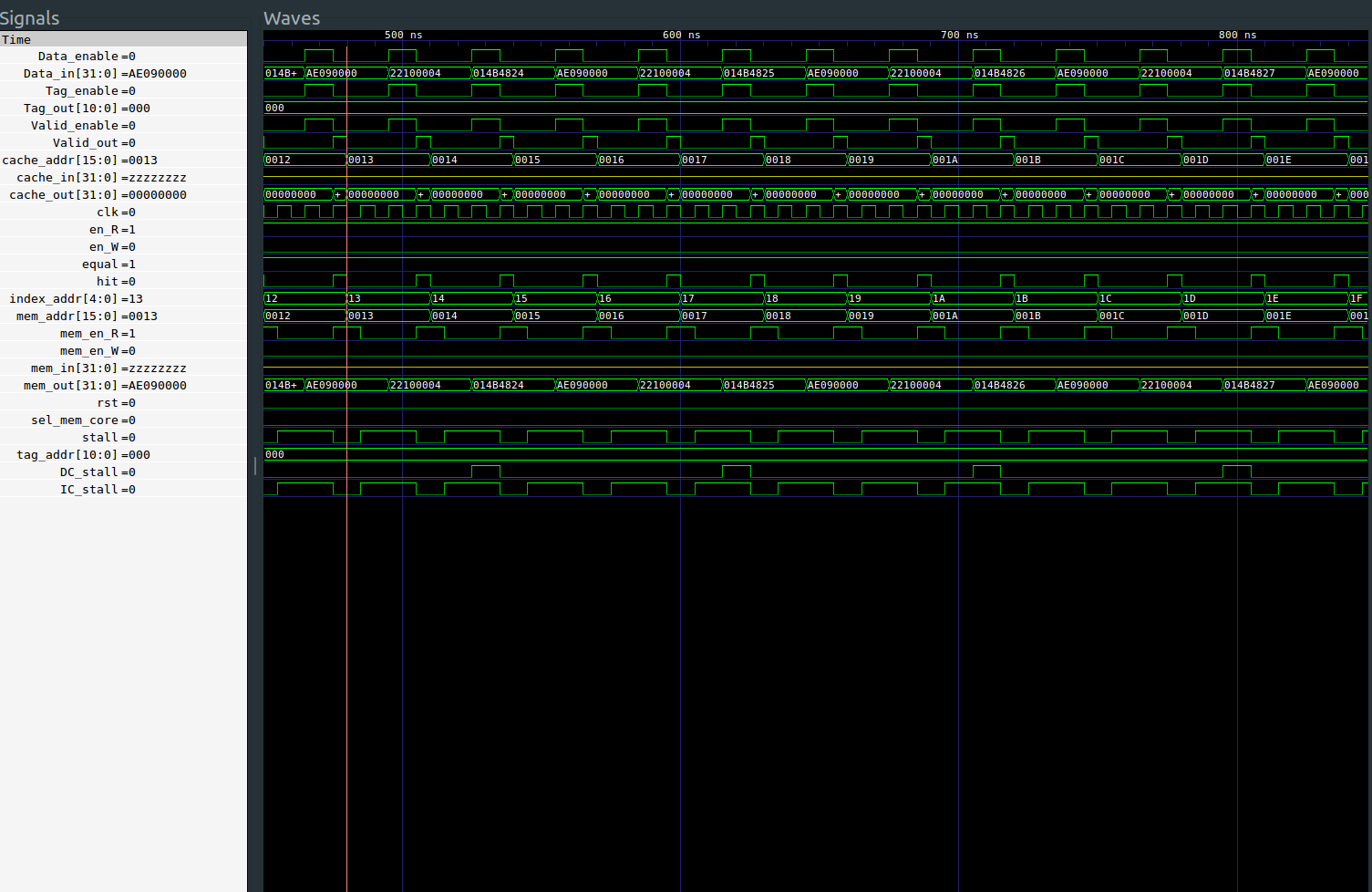
1. I-Cache Hit:



Description:

If I-Cache hit = 1 => I-Cache Hit, read data from cache.

1. CPU stall:



Description:

If stall = 1, then stall cpu and wait for data.

**心得(Report)**

**這次的作業跟上次相比，並沒有增加很多東西(大概是因為大部分的module在作業下載時已經寫好了)，所以需要寫的部份只有cache\_control,core,修改HDU,以及新增DC\_readEnable這個signal而已，而花比較多的時間，在於寫cache\_control中read部份的FSM(其實也還好，因為有IM作為參考)，整體來說，寫這份作業還蠻順利的(大概花了2個多小時吧)**