CS223

Miniproject_Report

Project-2 : Processor design in Logisim

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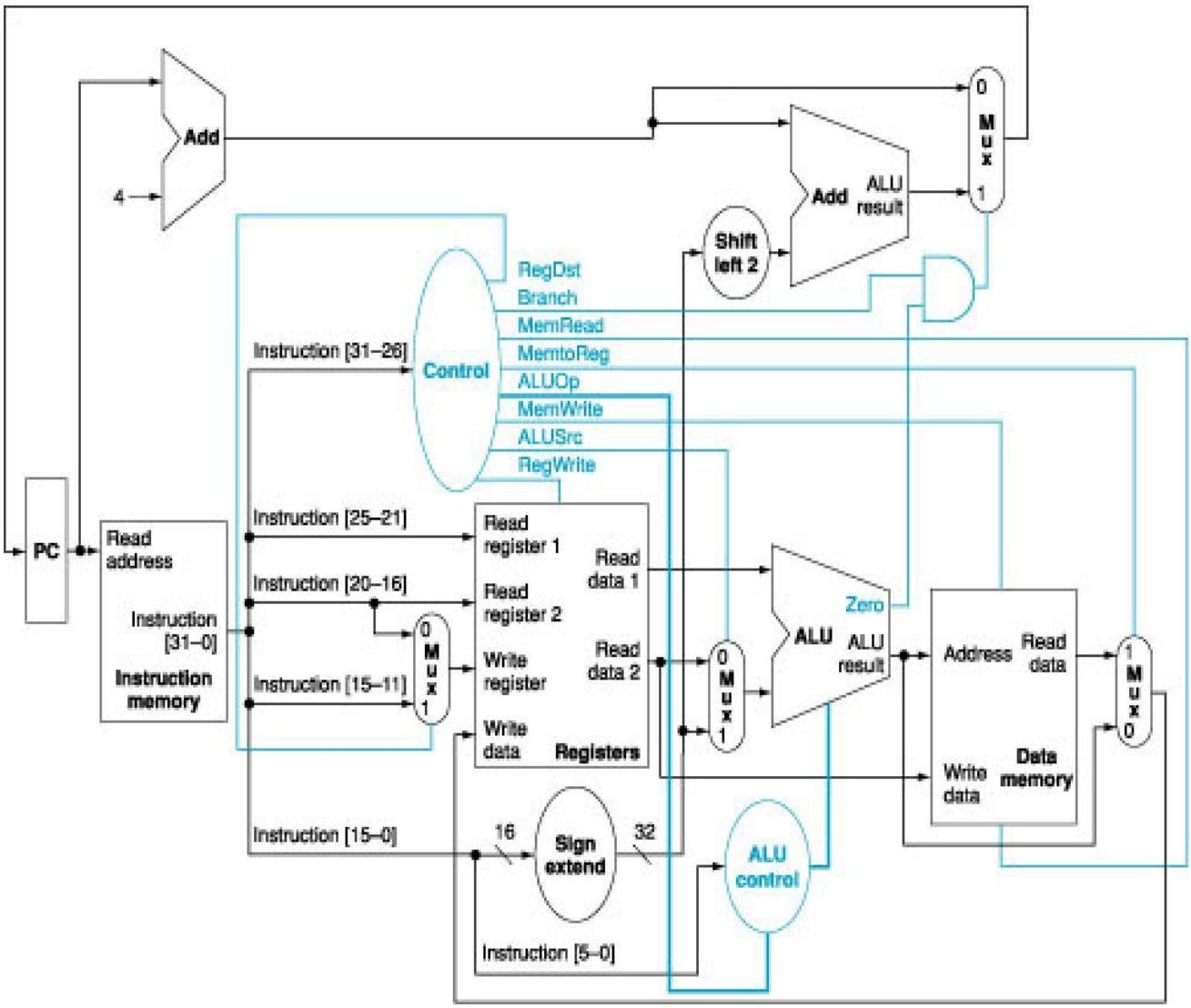
>>1.Project 2

Simulate the following architecture in Logic sim (implement add, sub , LW , SW, BEQ,ADDI, Jump instructions).A microarchitecture that executes instructions in a single cycle is shown in figure. The structure shows the datapath , connecting the state elements with combinational logic that can execute the various instructions. Control signals determine which specific instruction is carried out by the datapath at any given time. The controller contains combinational logic that generates the appropriate control signals based on the current instruction.



I am following given table for construct CONTROL_UNIT , ALUOpc and ALU control.

Step 1.

14 of 20 100%

All control inputs

Instruction	Opcode	Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
Rtype	000000	1	1	0	0	0	0	0	0
Sw	101011	X	0	1	1	0	X	0	0
Lw	100011	0	1	1	0	1	1	0	0
Beq	000100	X	0	0	0	0	X	1	0
J	000010	X	0	X	0	0	X	X	1

Step 2.

15 of 20 100%

Encoding opc

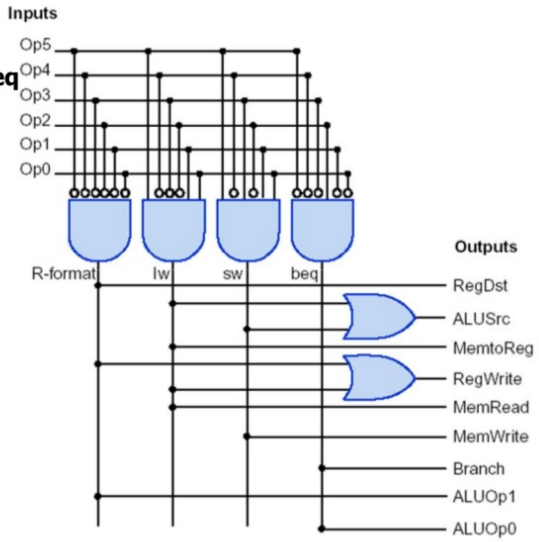
Ins	Opcode	OPC	Rdst	RW	Asrc	MW	MR	M2R	Brn	Jmp
R	000000	10	1	1	0	0	0	0	0	0
Sw	101011	00	X	0	1	1	0	X	0	0
Lw	100011	00	0	1	1	0	1	1	0	0
Beq	000100	01	X	0	0	0	0	X	1	0
J	000010	XX	X	0	X	0	0	X	X	1

Step 3.

17 of 20 100%

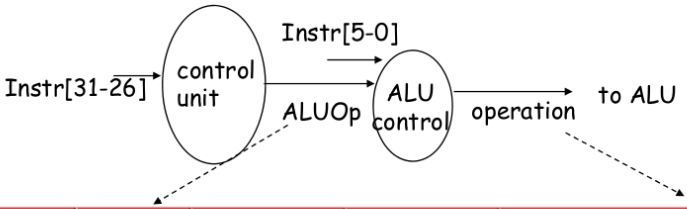
Control Unit PLA Implementation

	Signal name	R-format	lw	sw	beq
Inputs	Op5	0	1	1	0
	Op4	0	0	0	0
	Op3	0	0	1	0
	Op2	0	0	0	1
	Op1	0	1	1	0
	Op0	0	1	1	0
Outputs	RegDst	1	0	x	x
	ALUSrc	0	1	1	0
	MemtoReg	0	1	x	x
	RegWrite	1	1	0	0
	MemRead	0	1	0	0
	MemWrite	0	0	1	0
	Branch	0	0	0	1
	ALUOp1	1	0	0	0
	ALUOP2	0	0	0	1



19 of 20 100%

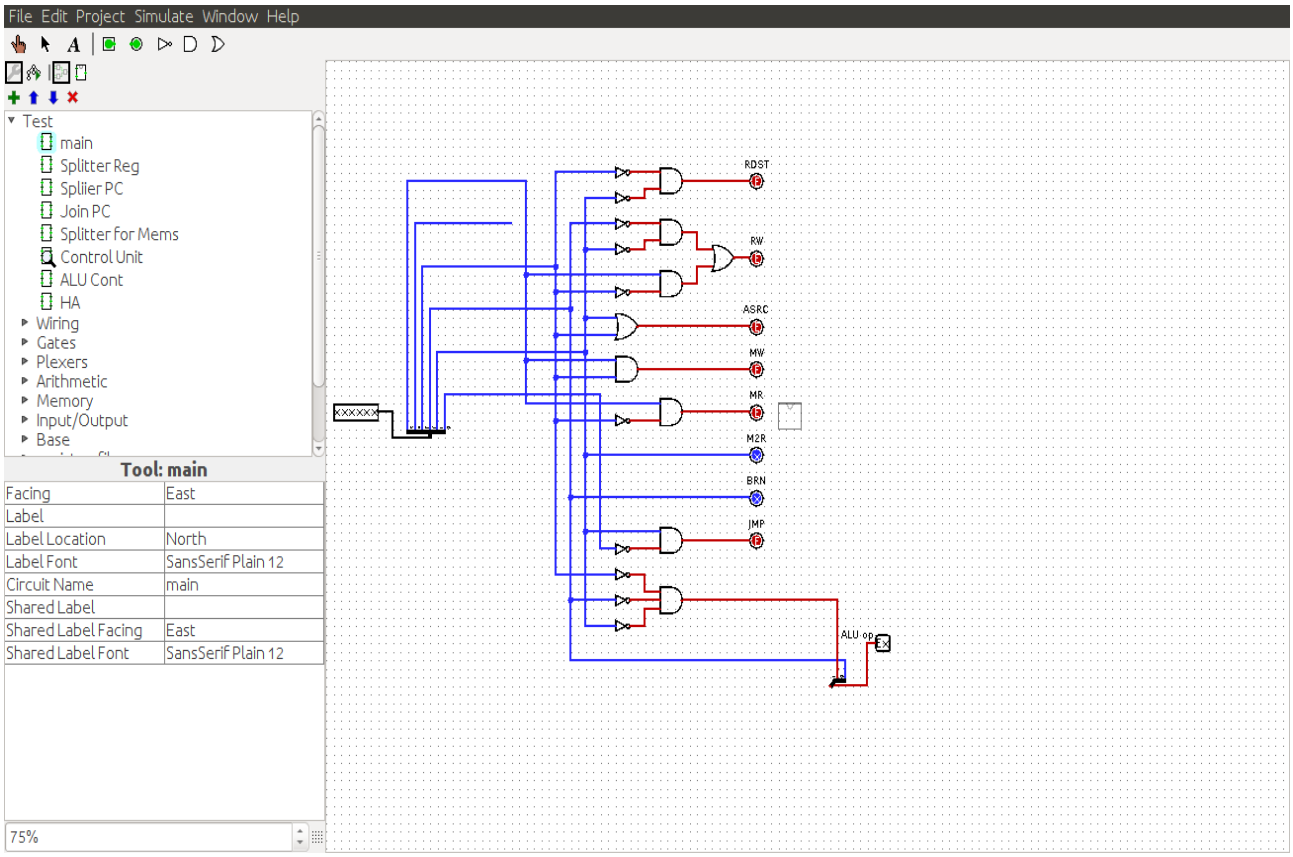
Single Cycle Control Unit: ALU control



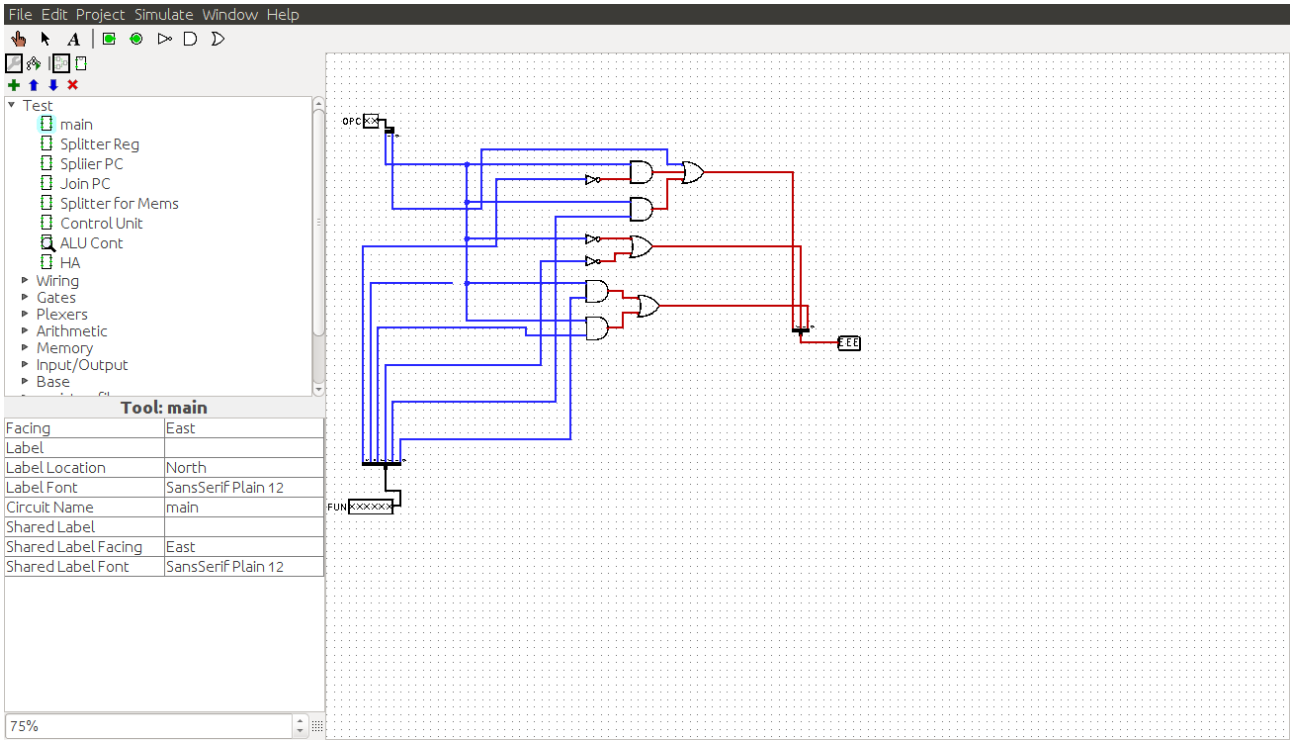
Type	OPC	INS	FUN	Action	OP
R-Type	10	Add	100000	Add	010
R-Type	10	Sub	100010	Sub	110
R-Type	10	And	100100	And	000
R-Type	10	Or	100101	Or	001
R-Type	10	SLT	101010	SetOnLess	111
Sw	00	Sw	Xxxxxx	Add	010
Lw	00	Lw	Xxxxxx	Add	010
Beq	01	Beq	Xxxxxx	Sub	110
J	XX	J	Xxxxxx	Xxx	xxx

>> Some Screenshort of my Logisim pages..

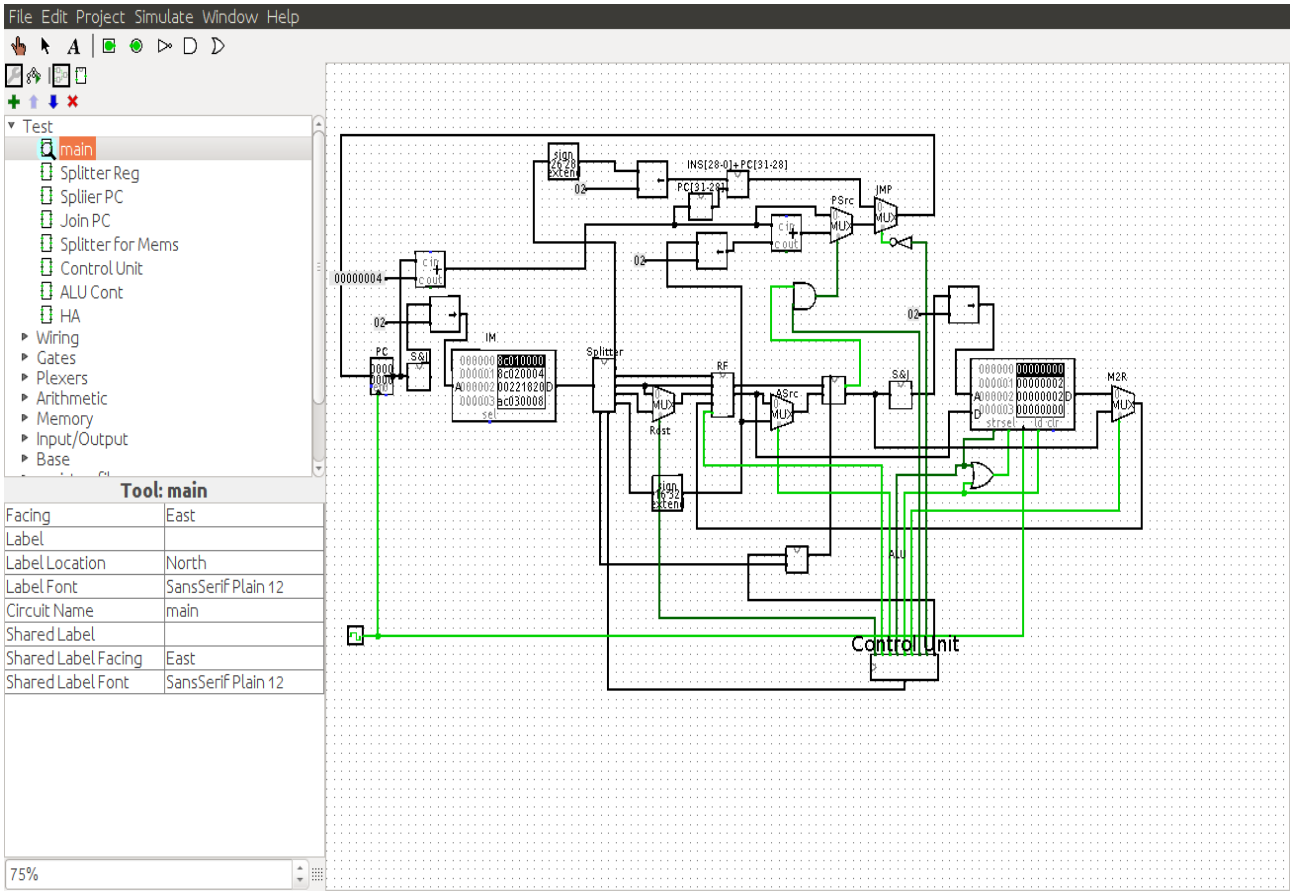
Control.



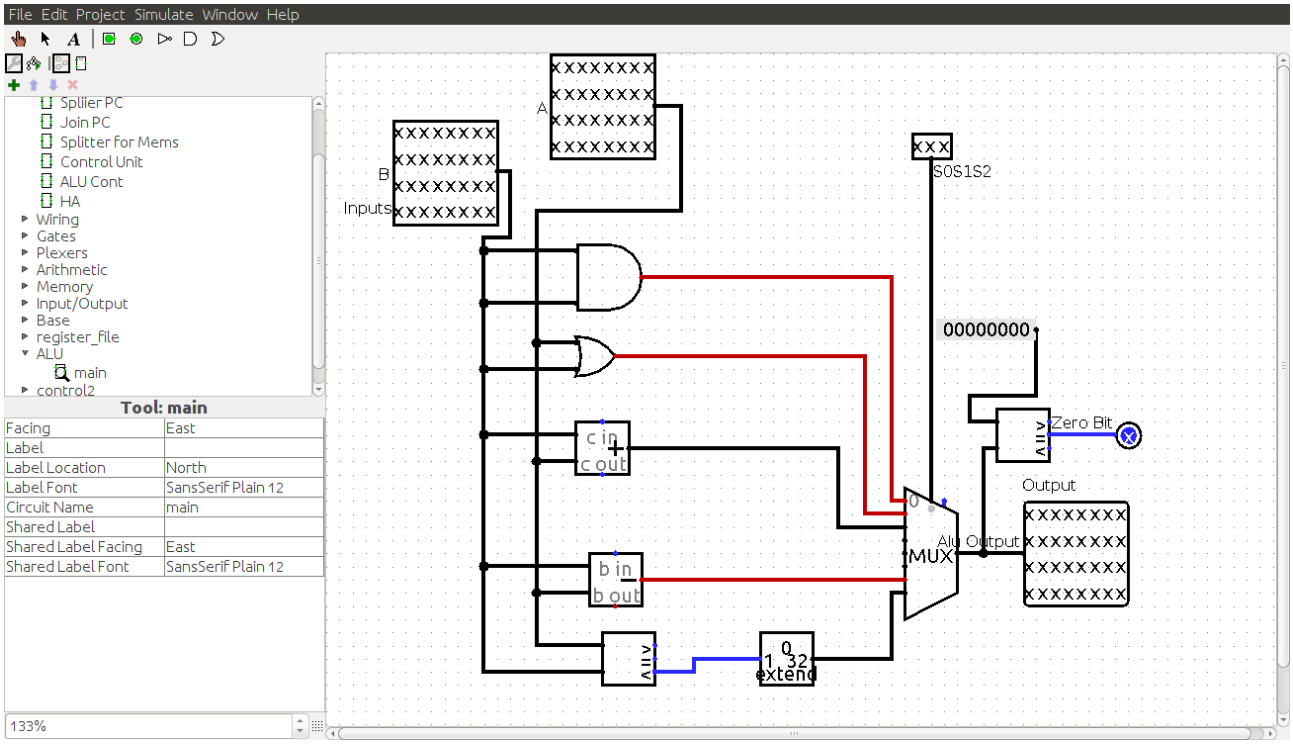
ALU Control



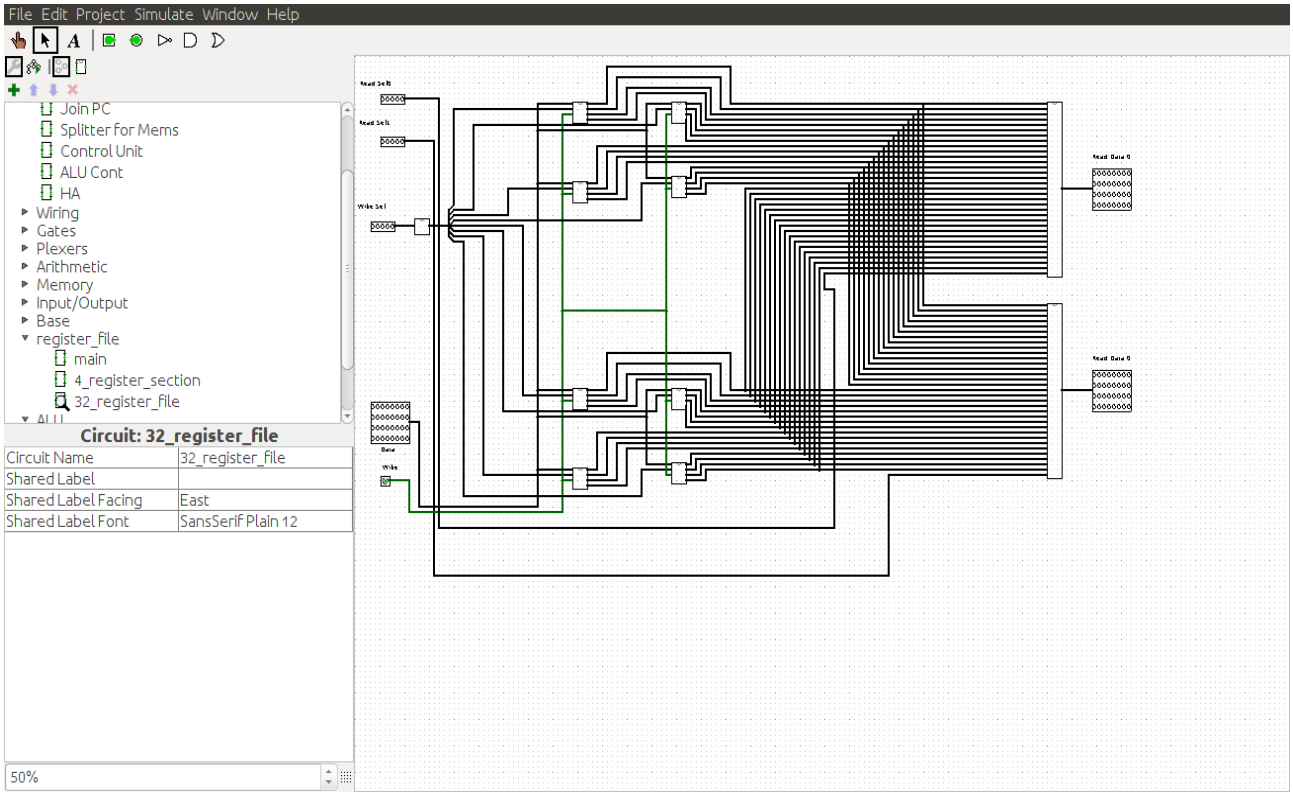
My Final Processor



ALU.



Register File.



Thankyou!!!