Module 1, Assignment 2

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1 Goal of the Assignment

In this assignment, you will implement a generic NAND gate in VHDL. You will investigate the elaborated design, i.e., the representation of the design with generic components, and the technology-mapped design, i.e., the design mapped to device-specific primitives.

2 Task Description

2.1 Implement a Generic NAND Gate

In Task 1, you have implemented an AND gate with two registered inputs and one registered output. Now, your task is to implement a generic NAND gate with registered inputs and a registered output. The inputs to the NAND gate are the 16 switches of the Nexys board, i.e., a 16-bit logic vector. The output will be assigned to LED 0 on the Nexys board. Use the constraints file (*constr_Nexys_A7.xdc*) provided in PANDA to assign the pins of your bock design to the correct pins of the FPGA package. The NAND gate will evaluate the logic function:

$$f(x_0, x_1, ..., x_{N-1}) = \overline{x_0 \wedge x_1 \wedge ... \wedge x_{N-1}} \qquad 2 \leq N \leq 16 \quad (1)$$

In other words, implement a module which performs a logical NAND on the N LSBs of the input vector and provides the result at its output. Make N a configurable parameter in your VHDL code.

Hint: To make your design generic, you could, for example, use the for-generate statement.

For the following schematics, assume gates with two inputs to be used by Vivado.

Draw the schematic you expect for the elaborated design with $N = 4$:

How many logical gates are you expecting to be used with $N = 4$? 4

Draw the schematic you expect for the elaborated design with $N = 7$:

How many logical gates are you expecting to be used with $N = 7$? 7

Draw the schematic you expect for the elaborated design with $N = 16$:

How many logical gates are you expecting to be used with $N = 16$? 16

Verify the correctness of your design by comparing your expected schematic to the schematic generated by Vivado. Do you see structural differences in the schematics? If yes, why?

There are no differences in the expected and generated schematic.

2.2 Simulate the Design

Create a test bench and verify the design's correctness with a behavioral simulation.

2.3 Synthesize the Design

Determine the parameter K (#inputs per LUT) for the LUTs used in the FPGA of the Nexys board: 6

Draw the schematic you expect for the synthesized design with $N = 4$:

How many LUTs are you expecting to be used with $N = 4$? 1

Draw the schematic you expect for the synthesized design with $N = 7$:

How many LUTs are you expecting to be used with $N = 7$? 2

Draw the schematic you expect for the synthesized design with $N = 16$:

How many LUTs are you expecting to be used with $N = 16$? 3

Synthesize the design and compare your schematic to the schematic after synthesis. Do the schematics differ from each other? If yes, why?

There are no differences in the expected and generated schematic after synthesis.

2.4 Implement the Design, Generate the Bitstream, and Program the FPGA

Implement the design, generate the bitstream, program the FPGA, and test your design on the hardware.