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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [ ] Show output file after run
- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

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testbench.sv

```
1  // Code your testbench here
2  // or browse Examples
3  module tb_fourbit_RCA;
4    logic [3:0]a,b;
5    logic Cin;
```

```
  wire [3:0]s;
  wire Cout;
  fourbit_RCA uut (.s(s),
                   .Cout(Cout),
                   .a(a),
                   .b(b),
                   .Cin(Cin));

  //fourbit_RCA uut (.s(s), .Cout(Cout), .a(a), .b(b), .Cin(Cin));
  reg clk =0;
  always #10 clk=~clk;
  initial begin
    a=4'b0000;
    b=4'b0000;
    Cin=0;
    #10 a=4'b0001; b=4'b0001; Cin=0;
    #10 a=4'b0011; b=4'b1001; Cin=1;
    #10 a=4'b1001; b=4'b0101; Cin=0;
    #10 a=4'b0011; b=4'b0011; Cin=0;
    #10 a=4'b0011; b=4'b0101; Cin=1;
    #10 $finish;
  end


  initial begin

    #5 $display("a=%b,b=%b,Cin=%b,s=%b,Cout=%b,time=%0t", a, b, Cin,s,Cout,$time);
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end
endmodule
```

design.sv

SV/Verilog Design

```
// Code your design here
module fourbit_RCA(s,Cout,a,b,Cin);
  output reg [3:0]s;
  output reg Cout;
  input [3:0]a;
  input [3:0]b;
  input Cin;
  wire c1,c2,c3;
  FA X0(s[0], c1, a[0],b[0],Cin);
  FA X1(s[1], c2, a[1],b[1],c1);
  FA X2(s[2], c3, a[2],b[2],c2);
  FA X3(s[3], Cout, a[3],b[3],c3);

endmodule
module FA(s,c,x,y,z);
  input x,y,z;
  output s,c;
  wire s1,c1,c2;
  HA m1(s1,c1,x,y);
  HA m2(s,c2, s1,z);
  or o(c, c1,c2);
endmodule
module HA( s, c, x, y);
  input x,y;
  output s,c;
  xor x1(s,x,y);
  and m(c,x, y);
endmodule
```

```
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```

Log | Share

```
[2023-09-20 17:00:44 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv  && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_fourbit_RCA."
MESSAGE "$root top modules: tb_fourbit_RCA."
SUCCESS "Compile success 0 Errors 0 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debu
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ns.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 20 (83.33%) primitives and 4 (16.67%) other processes in SLP
# SLP: 78 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is red
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4671 kB (elbread=427 elab2=4109 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: a=0000,b=0000,Cin=0,s=0000,Cout=0,time=5
# RUNTIME: Info: RUNTIME_0068 testbench.sv (26): $finish called.
# KERNEL: Time: 60 ns,  Iteration: 0,  Instance: /tb_fourbit_RCA,  Process: @INITIAL#17_1@.
# KERNEL: stopped at time: 60 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
```

```
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-20 17:00:47 UTC] Opening EPWave...
Done
```