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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [ ] Show output file after run
- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

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testbench.sv

```
1
2 module tb_fourbit_cla();
3   reg [3:0] a, b;
4   reg c0;
5   wire [3:0] s;
```

```
  wire c4;

  // Instantiate the fourbit_cla module
  fourbit_cla uut (
    .s(s),
    .c4(c4),
    .a(a),
    .b(b),
    .c0(c0)
  );


  initial begin
    // Test Case 1
    a = 4'b0001;
    b = 4'b0101;
    c0 = 1'b0;
    #10;

    // Test Case 2
    a = 4'b1010;
    b = 4'b1100;
    c0 = 1'b1;
    #10;


    $finish;
  end



  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end

endmodule

```

design.sv

SV/Verilog Design

```
// Code your design here
module fourbit_cla(s,c4,a,b,c0);
  output c4;
  output [3:0]s;
  input c0;
  input [3:0]a,b;
  wire [3:0]p,g;
  wire c1,c2,c3;
  //generate carry propagator pi=ai^bi
  genvar i;
  generate
    for (i = 0; i < 4; i = i + 1) begin
      assign p[i] = a[i] ^ b[i];
      assign g[i] = a[i] & b[i];
    end
  endgenerate
  /*assign p[0]=a[0]^b[0];
  assign p[1]=a[1]^b[1];
  assign p[2]=a[0]^b[2];
  assign p[3]=a[0]^b[3];
  //generate carry generator gi=ai&bi
  assign g[0]=a[0]&b[0];
  assign g[1]=a[1]&b[1];
  assign g[2]=a[2]&b[2];
  assign g[3]=a[3]&b[3];*/

```

```
  //generate carry ci+1=g1+pici
  assign c1=g[0]|p[0]&c0;
  assign c2=g[1]|p[1]&c1;
  assign c3=g[2]|p[2]&c2;
  assign c4=g[3]|p[3]&c3;

  //generate sum si=pi|ci
  assign s[0]=p[0]|c0;
  assign s[0]=p[0]|c0;
  assign s[0]=p[0]|c0;
  assign s[0]=p[0]|c0;
endmodule

```

Log Share

```
[2023-09-26 19:24:52 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv  && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_fourbit_cla."
MESSAGE "$root top modules: tb_fourbit_cla."
SUCCESS "Compile success 0 Errors 0 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debug
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ns.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 0 primitives and 18 (100.00%) other processes in SLP
# SLP: 15 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.2 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is redu
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
```

```
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 576 kB (elbread=427 elab2=14 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# RUNTIME: Info: RUNTIME_0068 testbench.sv (32): $finish called.
# KERNEL: Time: 20 ns,  Iteration: 0,  Instance: /tb_fourbit_cla,  Process: @INITIAL#18_0@.
# KERNEL: stopped at time: 20 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-26 19:24:56 UTC] Opening EPWave...
Done
```