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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [ ] Show output file after run

Output File Name

Output Filename

- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

205

testbench.sv

```
1 // Code your testbench here
2 // or browse Examples
```

```
module tb_decoder_3x8;
  reg [7:0]y;
  reg [2:0]x;
  decoder_3x8 uut (
    .y(y),
    .x(x)
  );
  /*reg clk=0;
  always begin
   #5 clk=~clk;
  end*/

  initial begin
    x=3'b000;
    #10 x=3'b001;
    $display("x-%b, y-%b",x,y);
    #10 x=3'b011;
    $display("x-%b, y-%b",x,y);
    #10 x=3'b101;
    $display("x-%b, y-%b",x,y);
    $finish;
  end
  /*always @(posedge clk) begin
    $display("x-%b, y-%b",x,y);
  end*/

  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end
endmodule
```

design.sv

SV/Verilog Design

```
// Code your design here
module decoder_3x8(y,x);
  output [7:0]y;
  input [2:0]x;
  wire w;
  wire [3:0]y1;
  wire [3:0]y2;
  wire [1:0]x1;
  not g1(w,x[2]);
  decoder_2x4 m1(y1,x,w);
  decoder_2x4 m2(y2,x1,x[2]);
  assign y={y2,y1};
  assign x={x[2],x1};
endmodule

module decoder_2x4(y,x,e);
  output [3:0]y;
  input [1:0]x;
  input e;
  wire w1,w2,w3,t;
  not g1(t,e);
  not g2(w2,x[0]);
  not g3(w3,x[1]);
  nand g4(y[0],w1,w2,w3);
  nand g5(y[1],w1,x[0],w3);
  nand g6(y[2],w1,w2,x[1]);
  nand g7(y[3],w1,x[0],x[1]);
```

```
28 endmodule
```

Log | Share

```
[2023-09-21 17:23:55 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv  && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
WARNING VCP5228 "Input port x<wire> is used as lvalue." "design.sv" 13  11
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_decoder_3x8."
MESSAGE "$root top modules: tb_decoder_3x8."
SUCCESS "Compile success 0 Errors 1 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debu
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ns.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Warning: design.sv (10): Length of connection (3) does not match the length of port "x" (2)
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 15 (78.95%) primitives and 4 (21.05%) other processes in SLP
# SLP: 22 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is red
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4668 kB (elbread=427 elab2=4106 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: x-001, y-xxxx111x
# KERNEL: x-011, y-xxxx11x1
# KERNEL: x-101, y-xxxxx111
```

```
# RUNTIME: Info: RUNTIME_0068 testbench.sv (23): $finish called.
# KERNEL: Time: 30 ns,  Iteration: 0,  Instance: /tb_decoder_3x8,  Process: @INITIAL#15_0@.
# KERNEL: stopped at time: 30 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-21 17:23:58 UTC] Opening EPWave...
Done
```