Read only memory | Random access memory

↳ Combinational ckt | ↳ sequential ckt

↳ No feedback | ↳ feedback

↳ Designed using basic gates | ↳ Using flipflops

8×2 ROM → No. of bits stored in each location

↳ No. of memory locations

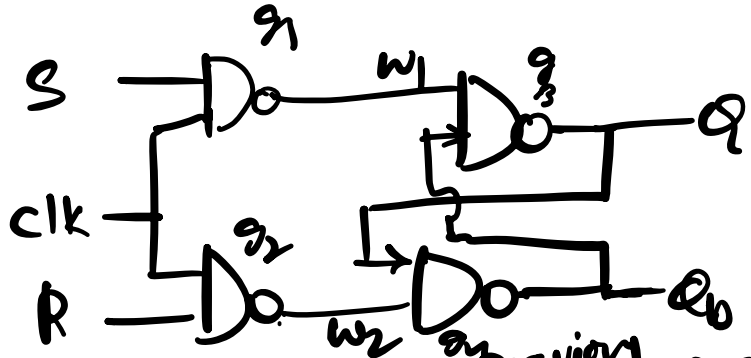
If we need to store 00 in location 5, 100 is selected

Sequential circuits:

nand

0 0	1
0 1	1
1 0	1
1 1	0

Clocked SR flipflop:-



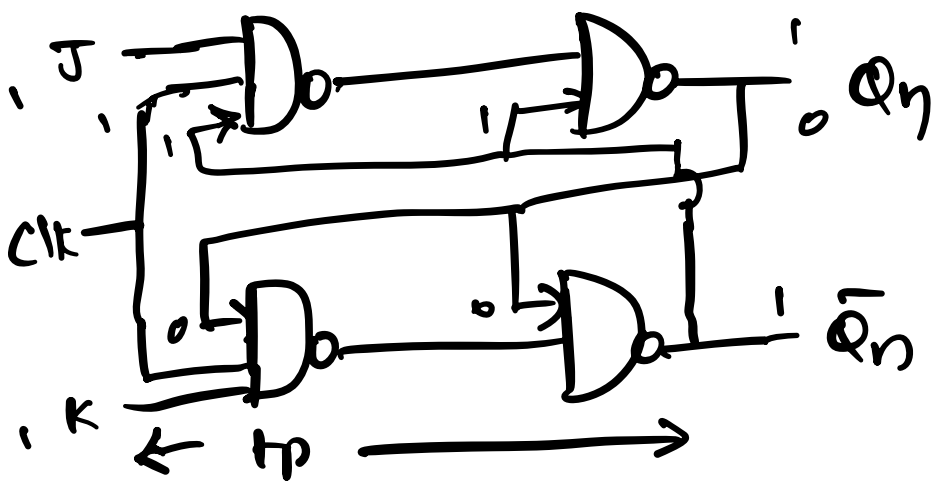
clk=1	S	R	Q_n (previous)	Q_{n+1} (present)	
	0	0	0	0	Q_n
	0	0	1	1	Q_n
	0	1	0	0	Reset
	0	1	1	0	Reset
	1	0	0	1	set
	1	0	1	1	set
	1	1	0	x	ambiguous state.
	1	1	1	x	ambiguous state.

If clk = 0, FF remains in previous state

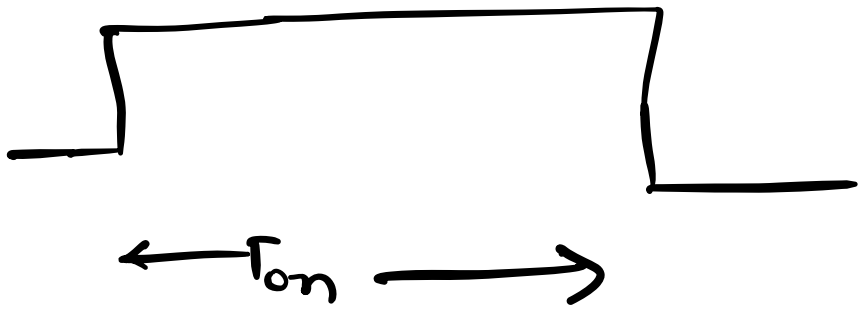
JK flip flop

if clk = 0
F.F remains
in previous
state

clk=1	J	K	Q_n	Q_{n+1}	
	0	0	0	0	Q_n
	0	0	1	1	
	0	1	0	0	Reset
	0	1	1	0	
	1	0	0	1	Set
	1	0	1	1	
	1	1	0	1	$\bar{Q}_n$
	1	1	1	0	



There is
a problem
of race
around
condition



Consider initial, $J=1, K=1, Q_n=0$

after t_p sec, $J=1, K=1, Q_n=1$

after t_p sec, $J=1, K=1, Q_n=0$

Repeat because $T_p < T_{on}$

it will given 0, 1, 0, 1, 0, 1 ....

until total $T_p > T_{on}$

This is called race around condition

to avoid this, we need to make

either ① $t_p > T_{on}$ (practically

imposible because $t_p = ps$, then

Clock frequency should be m GHz

② Master-slave F.F (edge triger F.F)

Master-slave JK flip flop