Brought to you by DOULOS (http://www.doulos.com)

Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [x] Show output file after run

Output File Name

Output Filename

- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

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testbench.sv

```
1
2 module tb_sr_ff();
```

```
3
4
5   reg s, r, clk;
6   wire q, qb;
7
8
9   sr_ff uut (
10    .q(q),
11    .qb(qb),
12    .s(s),
13    .r(r),
14    .clk(clk)
15  );
16
17
18  reg clk_period = 10;
19  always #((clk_period/2)) clk = ~clk;
20
21
22  initial begin
23
24    s = 0;
25    r = 0;
26    clk = 0;
27
28
29    #5 s = 1; // Set S to 1
30    #5 r = 1; // Set R to 1
31    #5 s = 0; // Set S to 0
32    #5 r = 0; // Set R to 0
33
34
35    $finish;
36  end
37
38
39  always @(posedge clk) begin
40    $display("Time=%0t s=%b r=%b q=%b qb=%b", $time, s, r, q, qb);
41  end
42  initial begin
43    $dumpfile("dump.vcd");
44    $dumpvars;
45  end
46  initial begin
47    #100;
48    $finish;
49  end
50
51 endmodule
52
```

design.sv

SV/Verilog Design

```
1  // Code your design here
2  module sr_ff(q,qb,s,r,clk);
3    output q,qb;
4    input s,r;
5    input clk;
6    wire w1,w2;
7    nand g1(w1,s,clk);
8    nand g2(w2,r,clk);
9    nand g3(q,w1,qb);
10   nand g4(qb,w2,q);
11 endmodule
12 module jk_ff(q,qb,j,k,clk);
13   output q,qb;
14   input j,k;
```

```
  input clk;
  wire w1,w2;
  nand g1(w1,j,qb,clk);
  nand g2(w2,k,q,clk);
  nand g3(q,w1,qb);
  nand g4(qb,w2,q);
endmodule

```

Log Share

masterslave_ff

0 views and **0** likes

Public (anyone with the link can view)

Save

B I H | | | | | | | (https://simplemde.com/markdown-guide)

A short description will be helpful for you to remember your playground's details

lines: 1 words: 0 0:0