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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [ ] Show output file after run
- [ ] Download files after run

Examples

using EDA Playground (/playgrounds?searchString=EDAPEX&language=&simulator=&methodologies=&_libraries=on&_svx=on&_easierUVM=on&curated=true&_c
VHDL (/playgrounds?searchString=&language=VHDL&simulator=&methodologies=&_libraries=on&_svx=on&_easierUVM=on&curated=true&_cura
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Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

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testbench.sv

SV/Verilog Testbench

```
25  // Test stimulus
26  initial begin
27    // Test case 1
28    a = 4'b0010;
29    b = 4'b0101;
30    m = 0;
31    cin = 0;
32    #10 $display("Test Case 1:");
33    #10 $display("a=%b, b=%b, m=%b, cin=%b", a, b, m, cin);
34    #10 $display("s=%b, cf=%b", s, cf);
35
36    // Test case 2
37    a = 4'b1111;
```

```
    b = 4'b0001;
    m = 1;
    cin = 1;
    #10 $display("\nTest Case 2:");
    #10 $display("a=%b, b=%b, m=%b, cin=%b", a, b, m, cin);
    #10 $display("s=%b, cf=%b", s, cf);

    // Add more test cases if needed...

    // End simulation
    #10 $finish;
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end

endmodule
```

design.sv

```
  wire [3:0]g,p,q,r;
  wire cout,t,f;
  xor x1(p[3],m,b[3]);
  xor x2(p[2],m,b[2]);
  xor x3(p[1],m,b[1]);
  xor x4(p[0],m,b[0]);
  not n1(t,cout);
  and l1(f,t,m);
  xor x5(r[3],f,q[3]);
  xor x6(r[2],f,q[2]);
  xor x7(r[1],f,q[1]);
  xor x8(r[0],f,q[0]);
  assign g[0]=0;
  assign g[1]=0;
  assign g[2]=0;
  assign g[3]=0;
  fourbit_RCA m1(q,cout,a,p,m);
  fourbit_RCA m2(s,cf,r,g,f);
  //fourbit_RCA m1(cout,q,a,p,m);
  //fourbit_RCA m2(cf,s,f,r,g);
endmodule

module fourbit_RCA(s,Cout,a,b,Cin);
  output reg [3:0]s;
  output reg Cout;
  input [3:0]a;
  input [3:0]b;
  input Cin;
  wire c1,c2,c3;
  FA X0(s[0], c1, a[0],b[0],Cin);
  FA X1(s[1], c2, a[1],b[1],c1);
  FA X2(s[2], c3, a[2],b[2],c2);
  FA X3(s[3], Cout, a[3],b[3],c3);

endmodule
module FA(s,c,x,y,z);
  input x,y,z;
  output s,c;
  wire s1,c1,c2;
```

```
  HA m1(s1,c1,x,y);
  HA m2(s,c2, s1,z);
  or o(c, c1,c2);
endmodule
module HA( s, c, x, y);
  input x,y;
  output s,c;
  xor x1(s,x,y);
  and m(c,x, y);
endmodule
```

Log Share

```
[2023-09-20 20:28:47 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv  && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_fourbit_addorsub."
MESSAGE "$root top modules: tb_fourbit_addorsub."
SUCCESS "Compile success 0 Errors 0 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debu
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ns.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 50 (89.29%) primitives and 6 (10.71%) other processes in SLP
# SLP: 163 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is red
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
```

```
# Allocation: Simulator allocated 4674 kB (elbread=428 elab2=4111 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: Test Case 1:
# KERNEL: a=0010, b=0101, m=0, cin=0
# KERNEL: s=0111, cf=0
# KERNEL:
# KERNEL: Test Case 2:
# KERNEL: a=1111, b=0001, m=1, cin=1
# KERNEL: s=1110, cf=0
# RUNTIME: Info: RUNTIME_0068 testbench.sv (48): $finish called.
# KERNEL: Time: 70 ns,  Iteration: 0,  Instance: /tb_fourbit_addorsub,  Process: @INITIAL#26_0@.
# KERNEL: stopped at time: 70 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-20 20:28:50 UTC] Opening EPWave...
Done
```