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## Languages & Libraries

**Testbench + Design**

SystemVerilog/Verilog

**UVM / OVM** (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

**Other Libraries** (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

## Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

**Compile Options** (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

**Run Options** (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

**Run Time:** 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [ ] Show output file after run
- [ ] Download files after run

## Examples

## Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

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testbench.sv

```
1  // Code your testbench here
2  // or browse Examples
3  module tb_FA;
4    logic x,y,z,s,c;
5    FA uut(.x(x), .y(y), .z(z), .s(s), .c(c));
```

```
  initial begin
    x=0;
    y=0;
    z=0;
    #5 x=1; y=0; z=0;
    #5 x=0; y=1; z=0;
    #5 x=1; y=1; z=0;
    #5 x=1; y=1; z=1;
    #5 $finish;
  end
  initial begin
    $display("x=%b, y=%b, z=%b s=%b, c=%b", x, y, z, s, c);
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end
endmodule
```

design.sv

SV/Verilog Design

```
// Code your design here

module FA(s,c,x,y,z);
  input x,y,z;
  output s,c;
  wire s1,c1,c2;
  HA m1(s1,c1,x,y);
  HA m2(s,c2, s1,z);
  or o(c, c1,c2);
endmodule
module HA( s, c, x, y);
  input x,y;
  output s,c;
  xor x1(s,x,y);
  and m(c,x, y);
endmodule
```

Log Share

```
[2023-09-19 19:25:14 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv  && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_FA."
MESSAGE "$root top modules: tb_FA."
SUCCESS "Compile success 0 Errors 0 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debu
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
```

```
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ns.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 5 (62.50%) primitives and 3 (37.50%) other processes in SLP
# SLP: 21 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is red
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4668 kB (elbread=427 elab2=4106 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: x=0, y=0, z=0 s=x, c=x
# RUNTIME: Info: RUNTIME_0068 testbench.sv (14): $finish called.
# KERNEL: Time: 25 ns,  Iteration: 0,  Instance: /tb_FA,  Process: @INITIAL#6_0@.
# KERNEL: stopped at time: 25 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-19 19:25:17 UTC] Opening EPWave...
Done
```