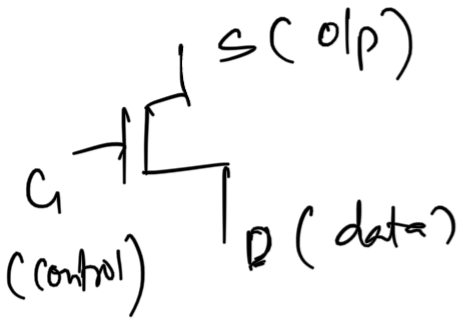
Verilog modelling:

P-Spice: obtain electrical calculations accurately.

verilog:

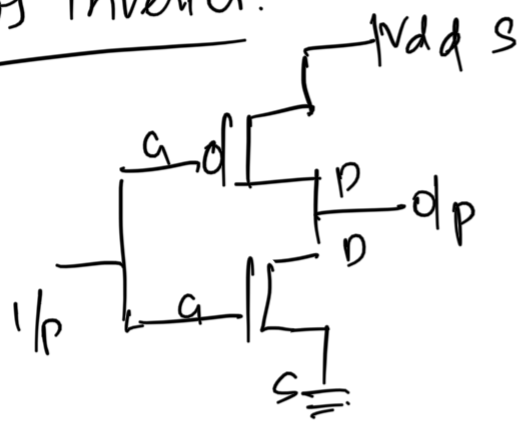


Two primitives (source, drain, gate)

nmos n(output, data, control)

pmos p(output, data, control)

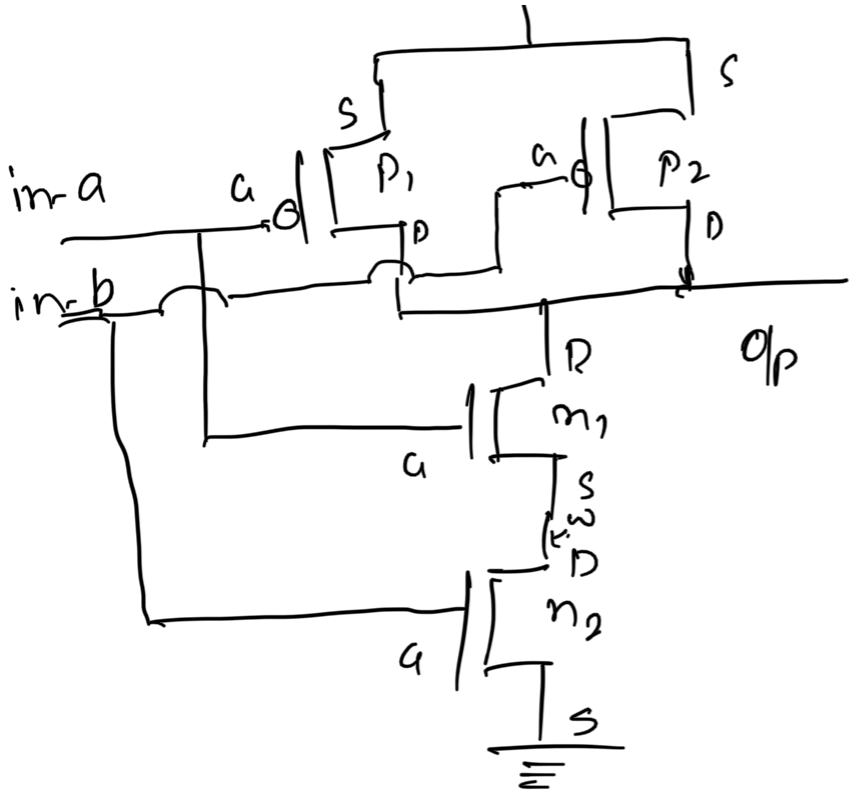
CMOS inverter:




```
module cmos_inv
        (o/p, i/p);
output o/p;
input i/p;
supply0 gnd;
supply1 Vdd;
pmos p(Vdd, o/p, i/p)
nmos n(gnd, o/p, i/p)
endmodule
```

CMOS - NAND:

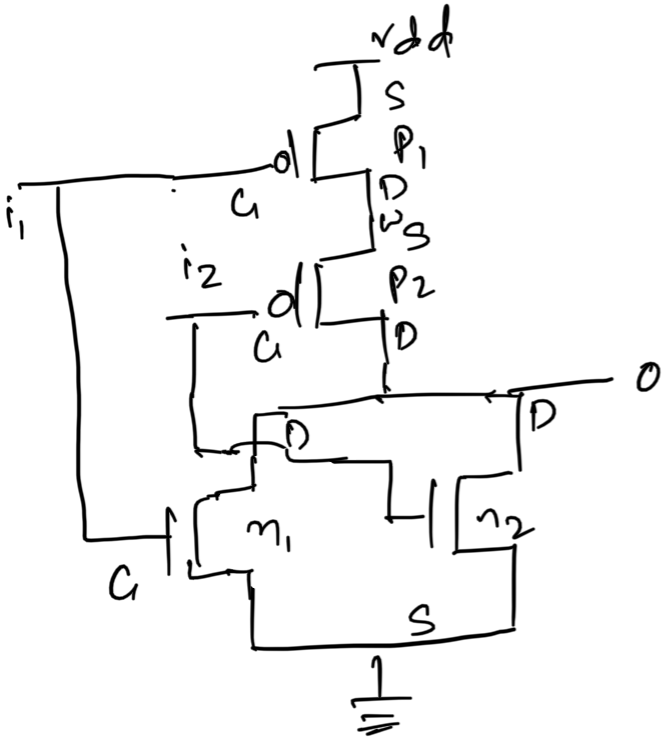

```
module cmos_NAND
        (o/p, in_a, in_b);
```




```
output o/p;
input in_a, in_b;
 wire w;
 supply0 gnd;
 supply1 vdd;
pmos P1(vdd, o/p, in_a);
pmos P2(vdd, o/p, in_b);
nmos n1(w, o/p, in_a);
nmos n2(gnd, w, in_b);
```

end module.

CMOS NOR:



i_1	i_2	O
0	0	1
0	1	0
1	0	0
1	1	0

```
module cmos_nor (o, i1, i2);
    output o;
    input i, i2;
    wire w;
    supply0 g;
    supply1 v;
    pmos p1 (v, w, i1);
    pmos p2 (w, o, i2);
    nmos n1 (g, o, i1);
    nmos n2 (g, o, i2);
endmodule.
```