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▼ Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM ⓘ (<http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies>)

None

Other Libraries ⓘ (<http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies>)

None
OVL 2.8.1
SVUnit 2.11

- ☐ Enable TL-Verilog ⓘ (<http://www.redwoodeda.com>)
- ☐ Enable Easier UVM ⓘ (<http://www.doulos.com/easier>)
- ☐ Enable VUnit ⓘ (<https://vunit.github.io/index.html>)

▼ Tools & Simulators ⓘ (<http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators>)

Aldec Riviera Pro 2022.04

Compile Options ⓘ (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options ⓘ (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time:

10 ms

- ☐ Use **run.do** Tcl file
- ☐ Use **run.bash** shell script
- ☒ Open **EPWave** after run
- ☐ Show output file after run
- ☐ Download files after run

► Examples

▼ Community

 Collaborate

 Forum (<https://groups.google.com/forum/#!forum/eda-playground>)

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testbench.sv



```
1
2 `timescale 1ns/1ps
3
4 module tb_cmos_inverter;
5
```

SV/Verilog Testbench

EPWave

```
6
7 parameter PERIOD = 10;
8 parameter HALF_PERIOD = PERIOD / 2;
9
10
11 reg i;
12 wire o;
13
14
15 cmos_inverter uut (
16     .o(o),
17     .i(i)
18 );
19
20
21 initial begin
22     i = 0; #HALF_PERIOD;
23     i = 1; #HALF_PERIOD;
24
25
26     $finish;
27 end
28
29
30
31 always @(posedge o) begin
32     $display("Time=%0t, i=%b, o=%b", $time, i, o);
33 end
34 initial begin
35     $dumpfile("dump.vcd");
36     $dumpvars;
37 end
38
39 endmodule
40
```

design.sv



```
1 // Code your design here
2 module cmos_inverter(o,i);
3     output o;
4     input i;
5     supply0 g;
6     supply1 v;
7     pmos p(v,o,i);
8     nmos n(g,o,i);
9 endmodule
```

Log

Share

[2023-09-26 02:55:20 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.

EPWave

```
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_cmos_inverter."
MESSAGE "$root top modules: tb_cmos_inverter."
SUCCESS "Compile success 0 Errors 0 Warnings Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debu
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsysf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 2 (40.00%) primitives and 3 (60.00%) other processes in SLP
# SLP: 6 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is red
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4667 kB (elbread=427 elab2=4106 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# RUNTIME: Info: RUNTIME_0068 testbench.sv (27): $finish called.
# KERNEL: Time: 10 ns, Iteration: 0, Instance: /tb_cmos_inverter, Process: @INITIAL#21_0@.
# KERNEL: stopped at time: 10 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-26 02:55:23 UTC] Opening EPWave...
Done
```