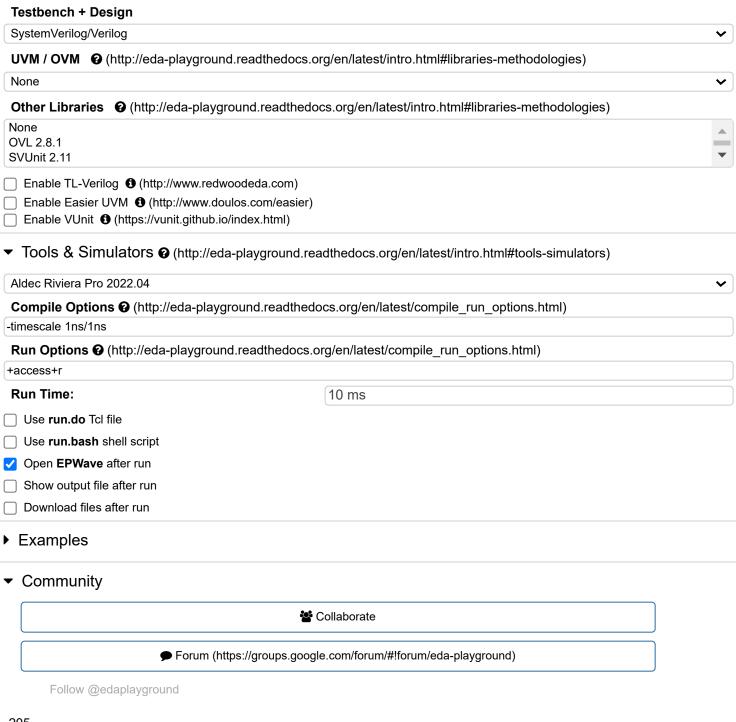
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▼ Languages & Libraries



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```
7
     parameter PERIOD = 10;
     parameter HALF_PERIOD = PERIOD / 2;
8
9
10
11
     reg i;
12
     wire o;
13
14
     cmos_inverter uut (
15
       .0(0),
16
17
       .i(i)
     );
18
19
20
21
     initial begin
22
       i = 0; #HALF_PERIOD;
23
       i = 1; #HALF_PERIOD;
24
25
26
       $finish;
27
28
     end
29
30
31
     always @(posedge o) begin
       $display("Time=%0t, i=%b, o=%b", $time, i, o);
32
     end
33
     initial begin
34
35
       $dumpfile("dump.vcd");
36
       $dumpvars;
37
38
39
   endmodule
40
```

```
design.sv
        \oplus
  1 // Code your design here
    module cmos_inverter(o,i);
      output o;
  3
  4
      input i;
      supply0 g;
 5
  6
      supply1 v;
  7
      pmos p(v,o,i);
      nmos n(g,o,i);
    endmodule
```

```
[2023-09-26 02:55:20 UTC] vlib work && vlog '-timescale' 'lns/lns' design.sv testbench.sv && vsim AVSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.

EPWave
```

♣ Share

Log

```
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_cmos_inverter."
MESSAGE "$root top modules: tb_cmos_inverter."
SUCCESS "Compile success 0 Errors 0 Warnings Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debu
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ps.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 2 (40.00%) primitives and 3 (60.00%) other processes in SLP
# SLP: 6 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is red
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4667 kB (elbread=427 elab2=4106 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# RUNTIME: Info: RUNTIME_0068 testbench.sv (27): $finish called.
# KERNEL: Time: 10 ns, Iteration: 0, Instance: /tb_cmos_inverter, Process: @INITIAL#21_0@.
# KERNEL: stopped at time: 10 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-26 02:55:23 UTC] Opening EPWave...
Done
```

EPWave