Brought to you by DOULOS (http://www.doulos.com)

Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [x] Show output file after run

Output File Name

Output Filename

- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

205

testbench.sv

```
1 // Code your testbench here
2 // or browse Examples
```

```
module tb_HA;
  logic x,y,s,c;
  HA uut(.x(x), .y(y), .s(s), .c(c));
  initial begin
    x=0;
    y=0;
    #5 x=1; y=0;
    #5 x=0; y=1;
    #5 x=1; y=1;
    #5 $finish;
  end
  initial begin
    $display("x=%b, y=%b, s=%b, c=%b", x, y, s, c);
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end
endmodule
```

design.sv

SV/Verilog Design

```
// Code your design here
module HA( s, c, x, y);
  input x,y;
  output s,c;
  xor x1(s,x,y);
  and m(c,x, y);
endmodule

```

Log Share

half_adder design and verification

0 views and **0** likes

Public (anyone with the link can view)

Save

B I H | | | | | | | (https://simplemde.com/markdown-guide)

A short description will be helpful for you to remember your playground's details

lines: 1 words: 0 0:0