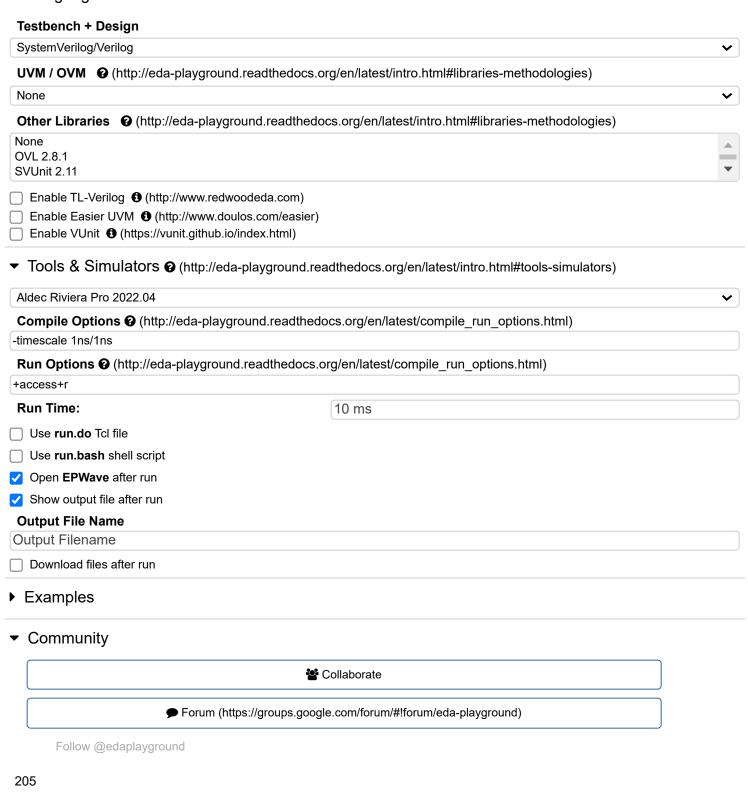
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▼ Languages & Libraries



1 // Code your testbench here
2 // or browse Examples

 \oplus

testbench.sv

```
3 module tb_HA;
      logic x,y,s,c;
      HA uut(.x(x), .y(y), .s(s), .c(c));
  5
      initial begin
  6
 7
        x=0;
        y=0;
 8
        #5 x=1; y=0;
 9
        #5 x=0; y=1;
 10
        #5 x=1; y=1;
 11
        #5 $finish;
 12
      end
 13
      initial begin
 14
        $display("x=%b, y=%b, s=%b, c=%b", x, y, s, c);
 15
      end
 16
      initial begin
 17
        $dumpfile("dump.vcd");
 18
        $dumpvars;
 19
      end
 20
    endmodule
 21
        \oplus
design.sv
                                                                                            SV/Verilog Design
  1 // Code your design here
    module HA(s, c, x, y);
      input x,y;
 3
 4
      output s,c;
 5
      xor x1(s,x,y);
 6
      and m(c,x, y);
    endmodule
  7

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                    half_adder design and verification
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                                           Save
                                                   0
                                                 (https://simplemde.com/markdown-
                             1
2
3
                                     8 |
                                                 guide)
   A short description will be helpful for you to remember your playground's details
```