Brought to you by DOULOS (http://www.doulos.com)

Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [ ] Show output file after run
- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

205

testbench.sv

```
1  // Code your testbench here
2  // or browse Examples
3  module tb_mux;
4
5    reg [3:0] i;
```

```
  reg [1:0] s;
  wire y;

  mux_4x1 uut (
    .y(y),
    .i(i),
    .s(s)
  );

  initial begin
    i = 4'b0000;
    s = 2'b00;
    $display("s = %b, i = %b, y = %b", s, i, y);

    // Apply test cases
    #10 s = 2'b01;
    #10 i = 4'b1010;
    $display("s = %b, i = %b, y = %b", s, i, y);
    #10 s = 2'b10;
    #10 s = 2'b11;
    $display("s = %b, i = %b, y = %b", s, i, y);
    #10 i = 4'b1100;
    #10 s = 2'b00;


    $finish;
  end
  initial begin
    $dumpfile("dump.vcd");
    $dumpvars;
  end

endmodule
```

design.sv

SV/Verilog Design

```
// Code your design here

module mux_4x1(y,i,s);
  output y;
  input [3:0]i;
  input [1:0]s;
  wire [1:0]w;
  wire [1:0]m1;
  wire [1:0]m2;
  mux_2x1 A(w[0],m1,s[0]);
  mux_2x1 B(w[1],m2,s[0]);
  mux_2x1 C(y,w,s[1]);
  assign i={m2,m1};
endmodule



/*module mux_2x1_buffer(y,i,s);
  output y;
  input [1:0]i;
  input s;
  wire w;
  bufif1 B1(y,w,i[0]);
  bufif1 B2(y,s,i[1]);
endmodule */


module mux_2x1(y,i,s);
  output y;
  input [1:0]i;
```

```
  input s;
  wire w1,w2,w3;
  not g1(w1,s);
  and g2(w2,w1,i[0]);
  and g3(w3,s,i[1]);
  or g4(y,w2,w3);
endmodule

/*module mux_4x1(y,i,s);
  output y;
  input [3:0]i;
  input [1:0]s;
  wire w1,w2;
  wire [3:0]p;
  not G1(w1,s[0]);
  not G2(w2,s[1]);
  and g3(p[0],w1,w2,i[0]);
  and g4(p[1],s[0],w2,i[1]);
  and g5(p[2],w1,s[1],i[2]);
  and g6(p[3],s[0],s[1],i[3]);
  or g7(y,p[0],p[1],p[2],p[3]);
endmodule*/
```

Log | Share

```
 [2023-09-21 20:20:10 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv  && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
MESSAGE "Pass 3. Processing behavioral statements."
WARNING VCP5228 "Input port i<wire> is used as lvalue." "design.sv" 13  11
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: tb_mux."
MESSAGE "$root top modules: tb_mux."
SUCCESS "Compile success 0 Errors 1 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debu
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# KERNEL: PLI/VHPI kernel's engine initialization done.
# PLI: Loading library '/usr/share/Riviera-PRO/bin/libsystf.so'
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ns.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
```

```
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 12 (80.00%) primitives and 3 (20.00%) other processes in SLP
# SLP: 27 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is red
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4668 kB (elbread=427 elab2=4107 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: s = 00, i = 0000, y = x
# KERNEL: s = 01, i = 1010, y = x
# KERNEL: s = 11, i = 1010, y = x
# RUNTIME: Info: RUNTIME_0068 testbench.sv (31): $finish called.
# KERNEL: Time: 60 ns,  Iteration: 0,  Instance: /tb_mux,  Process: @INITIAL#15_0@.
# KERNEL: stopped at time: 60 ns
# VSIM: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
./dump.vcd
[2023-09-21 20:20:13 UTC] Opening EPWave...
Done
```