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Languages & Libraries

Testbench + Design

SystemVerilog/Verilog

UVM / OVM (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None

Other Libraries (http://eda-playground.readthedocs.org/en/latest/intro.html#libraries-methodologies)

None
OVL 2.8.1
SVUnit 2.11

- [ ] Enable TL-Verilog (http://www.redwoodeda.com)
- [ ] Enable Easier UVM (http://www.doulos.com/easier)
- [ ] Enable VUnit (https://vunit.github.io/index.html)

Tools & Simulators (http://eda-playground.readthedocs.org/en/latest/intro.html#tools-simulators)

Aldec Riviera Pro 2022.04

Compile Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

-timescale 1ns/1ns

Run Options (http://eda-playground.readthedocs.org/en/latest/compile_run_options.html)

+access+r

Run Time: 10 ms

- [ ] Use **run.do** Tcl file
- [ ] Use **run.bash** shell script
- [x] Open **EPWave** after run
- [ ] Show output file after run
- [ ] Download files after run

Examples

Community

Collaborate

Forum (https://groups.google.com/forum/#!forum/eda-playground)

Follow @edaplayground

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testbench.sv

1

design.sv

SV/Verilog Design

```
// Code your design here

module seq_detector(y,x,clk);
  output y;
  input x;
  input clk;
  wire j0,j1,k0,k1,q0,q1;
  buf l1(j0,x);
  and l2(j1,x,q0);
  not l3(k1,x);
  not l(qb,q1);
  or l4(k0,k1,qb);
  jk_ff l5(q0,jo,k0,clk);
  jk_ff l6(q1,j1,k1,clk);
endmodule


//jk_flipflop verilog code
module jk_ff(q,j,k,clk);
  output reg q;
  input j,k,clk;
  always@(posedge clk)
    case ({j,k})
      2'b00: q<=q;
      2'b01: q=1'b0;
      2'b10: q=1'b1;
      2'b11:q<=!q;
    endcase
endmodule
```

Log Share

```
[2023-09-27 03:29:06 UTC] vlib work && vlog '-timescale' '1ns/1ns' design.sv testbench.sv  && vsim
VSIMSA: Configuration file changed: `/home/runner/library.cfg'
ALIB: Library "work" attached.
work = /home/runner/work/work.lib
MESSAGE "Pass 1. Scanning modules hierarchy."
MESSAGE "Pass 2. Processing instantiations."
```

```
MESSAGE_SP VCP2876 "Implicit net declaration, symbol qb has not been declared in module seq_detecto
MESSAGE_SP VCP2876 "Implicit net declaration, symbol jo has not been declared in module seq_detecto
MESSAGE "Pass 3. Processing behavioral statements."
MESSAGE "Running Optimizer."
MESSAGE "ELB/DAG code generating."
MESSAGE "Unit top modules: seq_detector."
MESSAGE "$root top modules: seq_detector."
SUCCESS "Compile success 0 Errors 0 Warnings  Analysis time: 0[s]."
ALOG: Warning: The source is compiled without the -dbg switch. Line breakpoints and assertion debug
done
# Aldec, Inc. Riviera-PRO version 2022.04.117.8517 built for Linux64 on May 04, 2022.
# HDL, SystemC, and Assertions simulator, debugger, and design environment.
# (c) 1999-2022 Aldec, Inc. All rights reserved.
# ELBREAD: Elaboration process.
# ELBREAD: Elaboration time 0.0 [s].
# KERNEL: Main thread initiated.
# KERNEL: Kernel process initialization phase.
# ELAB2: Elaboration final pass...
# ELAB2: Create instances ...
# KERNEL: Time resolution set to 1ns.
# ELAB2: Create instances complete.
# SLP: Started
# SLP: Elaboration phase ...
# SLP: Elaboration phase ... done : 0.0 [s]
# SLP: Generation phase ...
# SLP: Generation phase ... done : 0.1 [s]
# SLP: Finished : 0.1 [s]
# SLP: 5 (71.43%) primitives and 2 (28.57%) other processes in SLP
# SLP: 19 (100.00%) signals in SLP and 0 interface signals
# ELAB2: Elaboration final pass complete - time: 0.1 [s].
# KERNEL: SLP loading done - time: 0.0 [s].
# KERNEL: Warning: You are using the Riviera-PRO EDU Edition. The performance of simulation is redu
# KERNEL: Warning: Contact Aldec for available upgrade options - sales@aldec.com.
# KERNEL: SLP simulation initialization done - time: 0.0 [s].
# KERNEL: Kernel process initialization done.
# Allocation: Simulator allocated 4665 kB (elbread=427 elab2=4103 kernel=134 sdf=0)
# KERNEL: ASDB file was created in location /home/runner/dataset.asdb
# KERNEL: Simulation has finished. There are no more test vectors to simulate.
# VSIM: Simulation has finished.
Finding VCD file...
```