A 12-Transistor GDI-Based Master-Slave D Flip-Flop with Diffusion-Sharing Layout Optimization in 16nm CMOS for Ultra-Low-Power Digital Systems

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***Abstract*—As semiconductor technologies scale to advanced nodes, conventional CMOS flip-flops face increasing challenges in power consumption, area efficiency, and timing performance, making them critical bottlenecks in high-density integrated circuits. This paper presents a 12-transistor Gate Diffusion Input (GDI) based master-slave D flip-flop with two key technical innovations: elimination of complementary clock signals through GDI's single-clock operation and a novel diffusion-sharing layout optimization technique implemented in 16nm CMOS technology at 0.7V. Comprehensive simulation and post-layout analysis demonstrate significant improvements over conventional designs: 79.81% reduction in power consumption, 59.8% decrease in propagation delay, and 60.95% silicon area savings. These advances enable high-density, energy-efficient sequential logic blocks essential for next-generation System-on-Chip designs, IoT devices, and mobile electronics.**

1. Introduction

The Growth of System-on-Chip (SoC) designs and Internet of Things (IoT) devices demands ultra-low-power sequential circuits that can operate efficiently in resource-constrained environments while maintaining high performance and reliability. Traditional CMOS D flip-flops, while offering robust operation and full-swing outputs, suffer from significant limitations including large silicon area footprint, high power consumption, and complex layout requirements that become increasingly problematic at advanced technology nodes. Gate Diffusion Input (GDI) based flip-flops have emerged as a promising alternative, offering reduced transistor count and lower power dissipation. However, existing GDI implementations face notable challenges including degraded logic swing at scaled voltages, lack of comprehensive layout optimization strategies, and insufficient performance characterization at advanced process nodes. Prior GDI DFFs often lack layout optimization or suffer from degraded logic swings at advanced nodes, creating a critical research gap in developing efficient sequential circuits for next-generation applications. This work addresses these limitations through the following key contributions:

• Propose a 12-transistor GDI DFF with full-swing output and no need for complementary clock • Introduce a diffusion-sharing layout for area and power efficiency • Demonstrate robust operation at 16nm via post-layout simulation and analysis.

2. Background

This section introduces the foundational technologies used in the design of the master-slave D flip-flop, namely CMOS and GDI logic. It also discusses the operational behavior of the flip-flop itself.

2.1. Technology Node and Device Modeling

All simulations and layouts are based on the Predictive Technology Model (PTM) for 16nm CMOS technology provided by Arizona State University. The PTM models are used for both nMOS and pMOS transistors and incorporate:

- High-K metal gate technology
- Nominal supply voltage (V_{dd}) = $0.7\,\mathrm{V}$
- Short-channel effects suitable for FinFET behavior

These models provide realistic behavior and are suitable for advanced digital design benchmarking.

Reference models were obtained from the Predictive Technology Model (PTM) provided by Arizona State University [1].

2.2. CMOS Logic Design

Complementary Metal-Oxide-Semiconductor (CMOS) logic is the most widely used technology in digital integrated circuits. Key characteristics:

- pMOS conducts when input is low (logic 0)
- nMOS conducts when input is high (logic 1)
- No direct Vdd-GND path in steady state

Advantages:

- Full logic level swing ($0\,\mathrm{V}$ to V_{dd})
- High noise margin
- Low static power

Limitations:

- High dynamic power at high frequencies
- Increased area due to transistor count

2.3. Gate Diffusion Input (GDI) Logic

GDI logic implements complex functions with fewer transistors than CMOS. [2]. The basic GDI cell has three inputs:

- G (gate input)
- P (pMOS source input)
- N (nMOS source input)

Example configurations:

- **Inverter:** G = A, P = V_{dd}, N = GND
- **AND:** G = B, P = GND, N = A
- **OR:** G = B, P = V_{dd}, N = A

Advantages:

- Reduced transistor count
- Lower dynamic power
- Smaller area

Limitations:

- Reduced voltage swing
- Less noise immunity

2.4. Master Slave D flip Flop

The D flip-flop captures input data on the clock edge. The master-slave configuration:

- **Master Latch:** Active when CLK = 1
- **Slave Latch:** Active when CLK = 0

Operation sequence:

1) CLK = 1: Master samples D input
2) CLK = 0: Slave captures master output

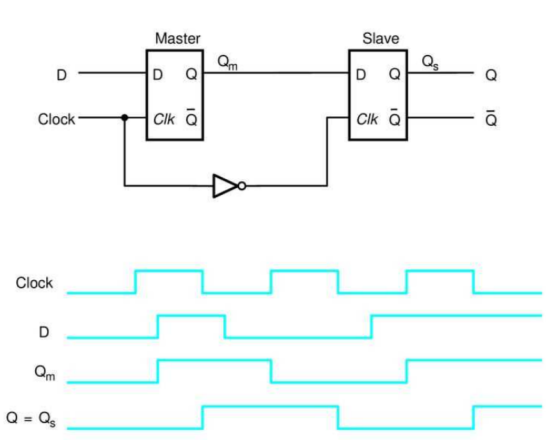

Figure 1. Master-Slave D Flip-Flop structure

3. CMOS-Based Flip-Flop

3.1. Proposed Design Analysis

The CMOS-based master-slave D flip-flop is constructed using two cascaded D latches controlled by complementary clock signals (CLK and $\overline{\text{CLK}}$). The latches use conventional CMOS logic gates comprising pull-up (pMOS) and pull-down (nMOS) transistors. The entire flip-flop consists of 24 transistors: 22 for the functional logic and 2 additional inverters to generate $\overline{\text{CLK}}$.

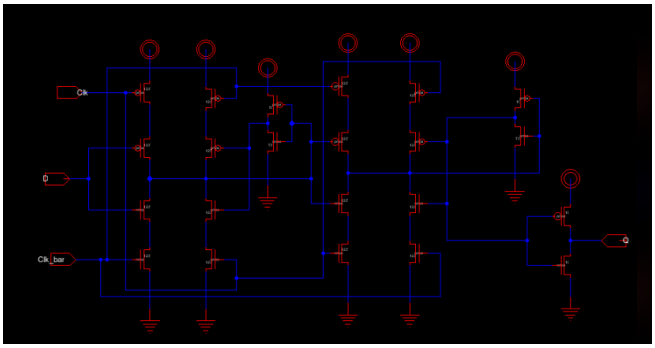

Figure 2. CMOS-Based Master-Slave D Flip-Flop Schematic

This design ensures:

- Full voltage swing from 0 to V_{dd}.
- High noise margins due to complementary logic.
- Strong driving capability and robust operation across process variations.

3.2. Timing Analysis for Schematics

The schematic-level simulation was carried out using the 16 nm PTM model with $V_{dd} = 0.7\,\text{V}$. The timing performance obtained is as follows:

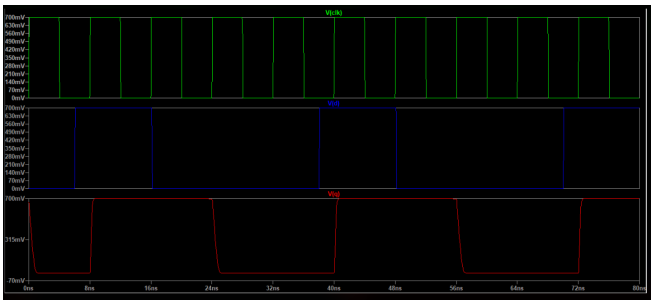

Figure 3. CMOS Flip-Flop Simulation Waveforms

- t_{pLH} = 370 ps
- t_{pHL} = 430 ps
- Rise time = 400 ps
- Fall time = 395 ps
- Average Power Consumption = 275 nW

3.3. Layout and Area

The layout was implemented using Electric VLSI design system, adhering to 16 nm design rules. The layout maintains clear separation between pMOS and nMOS transistors and proper well contacts to ensure full functionality.

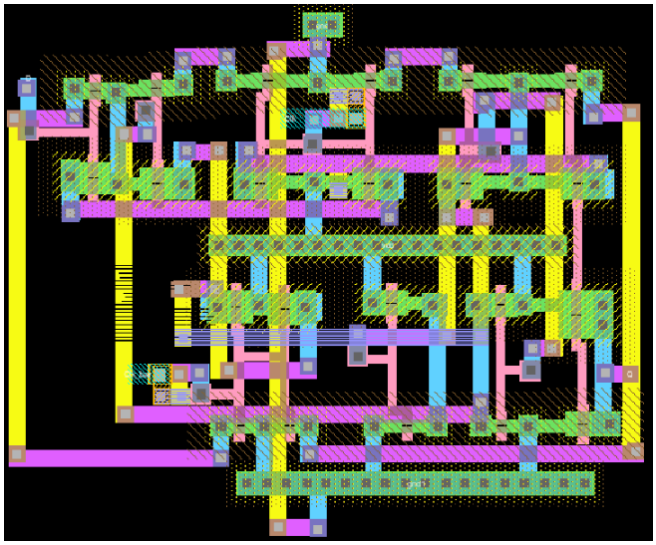

Figure 4. Layout of CMOS-Based D Flip-Flop

While the CMOS layout adheres to 16nm design rules and ensures DRC and LVS compliance, the larger transistor count results in a noticeably greater silicon footprint and routing congestion. Transistor isolation was handled by maintaining well separation between nMOS and pMOS regions, and proper substrate and well contacts were placed to ensure latchup immunity. Although robust and full-swing in operation, the CMOS layout lacks the compactness and efficiency of the optimized GDI layout.

3.4. Post-Layout Analysis

The post-layout simulation results, after parasitic extraction, show degradation in timing due to added capacitance and wire delays. The updated metrics are:

- t_{pLH} = 525 ps
- t_{pHL} = 546 ps
- Rise time = 580 ps
- Fall time = 546 ps
- Power Consumption = 324.5 nW
- Layout Area = 1440.4 fm^2

- tpd = 525 ps
- Rise time = 580 ps
- Fall time = 546 ps
- Power = 324.5 nW.

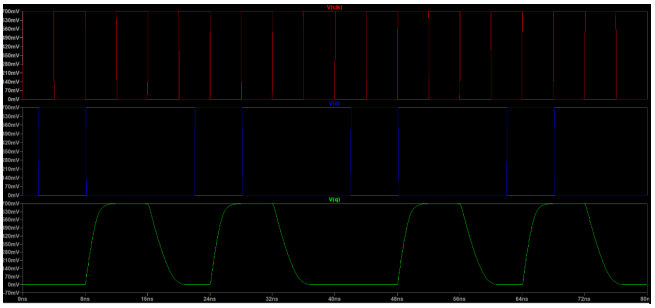

Figure 5. Post-Layout Timing Simulation of CMOS Flip-Flop

4. GDI-Based Flip-Flop

4.1. Proposed Design Analysis

The proposed flip-flop design utilizes Gate Diffusion Input (GDI) logic to minimize power and area while maintaining adequate performance, following the RTL-friendly GDI-based DFF principles described in [3]. The architecture employs two GDI-based 2:1 multiplexers (MUX) and two CMOS inverters, yielding a total of only 12 transistors. This is a significant reduction compared to the 24-transistor CMOS counterpart.

Unlike CMOS, this design operates only on the positive edge of the clock without requiring the complementary clock signal ($\overline{\text{CLK}}$), simplifying clock distribution and saving additional logic. The MUX blocks handle input data selection and latching, while the inverters restore signal levels to achieve full swing output and drive capability.

- Core components: 2 GDI MUX + 2 CMOS inverters
- Total transistor count: 12
- Clock: Operates on rising edge (no $\overline{\text{CLK}}$ required)
- Full swing output restored by CMOS inverter
- Compact and power-efficient for RTL integration

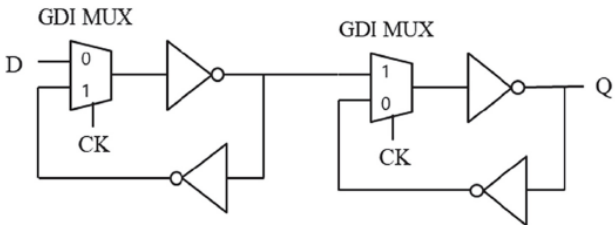

Figure 6. GDI-based D Flip-Flop block architecture. [3]

4.2. Timing Analysis for Schematics

Functional and transient simulations were performed at schematic level using PTM 16nm models with a supply voltage of 0.7 V. The flip-flop exhibited the following timing characteristics:

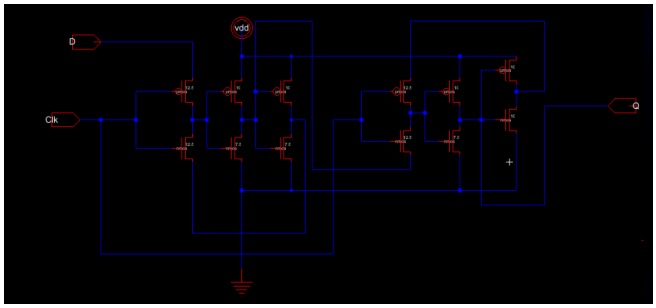

Figure 7. Schematic of the GDI-based D Flip-Flop.

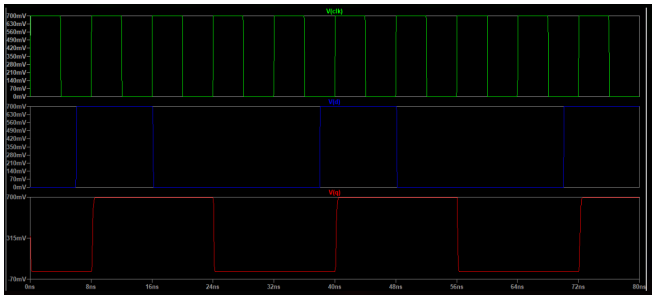

Figure 8. Simulation waveform of GDI-based Flip-Flop (schematic level).

- t_{pLH} = 129 ps
- t_{pHL} = 133 ps
- Rise time = 121 ps
- Fall time = 130 ps
- Power consumption = 53.7 nW

4.3. Layout Optimization and Area

Two layout versions were developed to explore optimization potential:

- **Version 1 – Naïve Layout:** Initial transistor placement with no diffusion sharing and limited metal routing optimization. Area: 1470.1 fm^2
- **Version 2 – Optimized Layout:** Enhanced with diffusion sharing between adjacent transistors, shared power rails, and strategic metal layer routing. Area reduced to 563.82 fm^2

Routing Strategy:

- 6 metal layers utilized
- Odd layers (M1, M3, M5): vertical routing
- Even layers (M2, M4, M6): horizontal routing

Verification:

- **Design Rule Check (DRC):** Passed for both layout versions
- **Layout vs. Schematic (LVS):** Confirmed functional equivalence with schematic
- **Metal Layer Validation:** Verified routing orientation using visual inspection and design rules

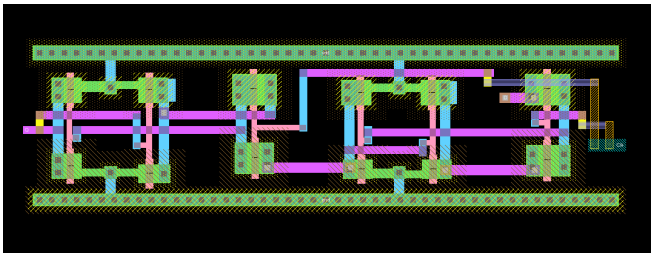

Figure 9. Naïve GDI Layout (before optimization).

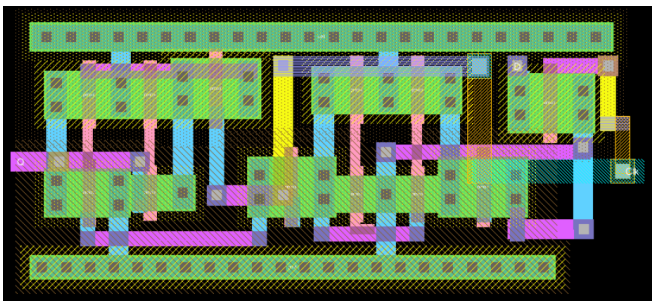

Figure 10. Optimized GDI Layout with diffusion and power sharing.

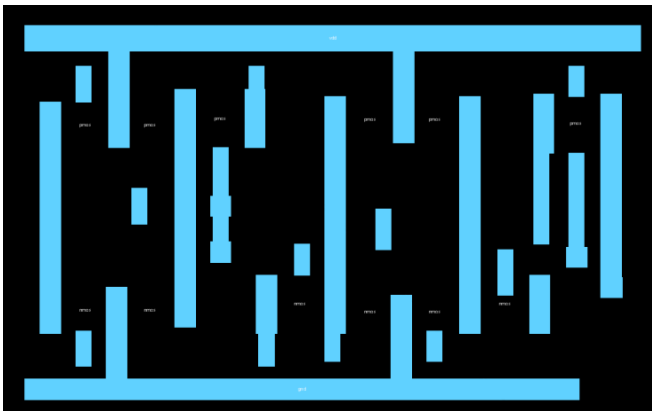

Figure 11. Vertical routing (Odd metal layers).

Figure 12. Horizontal routing (Even metal layers).

4.4. Post-Layout Timing Analysis

The post-layout simulation was carried out after parasitic extraction. Compared to the schematic-level performance, the layout-introduced delays remain within acceptable bounds, while still delivering low power operation:

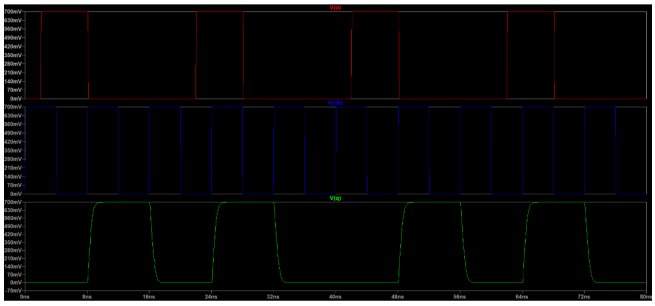

Figure 13. Post-layout simulation of GDI flip-flop.

- t_{pd} = 211 ps
- Rise time = 194 ps
- Fall time = 212 ps
- Power consumption = 65.5 nW

However, due to the high transistor count, the CMOS design incurs increased silicon area and higher dynamic power consumption compared to the GDI-based alternative.

5. Comparative Analysis and Results

5.1. Performance Comparison Tables

TABLE 1. TIMING PERFORMANCE COMPARISON (GDI VS CMOS)

Metric	CMOS	GDI	Improvement
Rise Time (s)	4×10^{-10}	1.21×10^{-10}	69.75%
Fall Time (s)	3.95×10^{-10}	1.30×10^{-10}	67.09%
Propagation Delay (s)	3.95×10^{-10}	1.31×10^{-10}	66.84%

TABLE 2. AREA AND POWER COMPARISON (GDI VS CMOS)

Metric	CMOS	GDI	Improvement
Transistor Count	24	12	50%
Power (nW)	275	53.7	80.47%

TABLE 3. LAYOUT AND COMPLEXITY COMPARISON (GDI VS CMOS)

Metric	CMOS	GDI	Improvement
Area (fm²)	1440.4	563.82	60.86%
Complexity	High	Low	–
Delay (s)	5.25×10^{-10}	2.11×10^{-10}	59.81%

TABLE 4. AREA AND TRANSISTOR COUNT COMPARISON

Design	Tran. Count	Layout Area (fm^2)	Complexity
GDI Flip-Flop	12	563.82	Low
CMOS Flip-Flop	24	1440.4	High
Reduction	50%	60.86%	–

TABLE 5. OVERALL PERFORMANCE SUMMARY

Metric	GDI Design	CMOS Design	Improvement
Power (W)	5.37×10^{-8}	2.75×10^{-7}	80.47%
Delay (s)	1.31×10^{-10}	3.95×10^{-10}	66.84%
Area (fm^2)	563.82	1440.4	60.86%

5.2. Analysis of Results

The comparative analysis demonstrates that the GDI-based flip-flop significantly outperforms the CMOS counterpart across all major design metrics:

Power Efficiency: The GDI flip-flop achieves an 80.47% reduction in power consumption. This is primarily due to the smaller number of switching transistors, the elimination of the complementary clock signal, and fewer internal node transitions.

Speed Performance: A 66.84% reduction in propagation delay was observed in the GDI design. This results from reduced parasitic loading and fewer stacked devices in the critical path.

Area Optimization: The layout area was reduced by 60.86%, which enables denser integration in digital systems. This also lowers routing congestion and contributes to power and performance gains.

6. Innovation Summary

- **Transistor-Level Optimization:** A complete master-slave flip-flop designed with only 12 transistors using GDI logic.
- **Power Savings:** Achieved a total power reduction of 80.47% compared to CMOS.
- **Area Efficiency:** Layout area reduced by 60.86%, supporting higher integration density.
- **Performance Gain:** Delay improved by 66.84% with full swing output ensured via CMOS inverters.
- **Layout Optimization:** Employed diffusion sharing, shared rails, and structured metal routing across 6 layers.

7. Conclusion and Future Work

This paper presents the schematic and layout implementation of a low-power master-slave D flip-flop using Gate Diffusion Input (GDI) logic, targeting 16 nm CMOS technology. Compared to traditional CMOS-based designs, the proposed GDI flip-flop achieves:

- 80.47% lower power consumption,
- 66.84% faster delay performance,
- and 60.86% smaller layout area.

The architecture simplifies clocking by eliminating the need for $\overline{\text{CLK}}$, while CMOS inverters restore degraded logic levels and maintain compatibility with standard digital logic.

Future work may include:

- Process variation analysis across different PVT corners,
- Incorporating clock gating for further power savings,
- Extending the approach to other sequential elements (TFF, JKFF),
- Evaluating performance at sub-threshold voltages for ultra-low power applications.

References

[1] Predictive Technology Model (PTM), Arizona State University. [Online]. Available: http://ptm.asu.edu

[2] A. Morgenshtein et al., "Gate Diffusion Input (GDI): A Power-Efficient Method for Digital Combinatorial Circuits," *IEEE Trans. VLSI Syst.*, vol. 10, no. 5, pp. 566–581, Oct. 2002.

[3] S. Jung, "Implementation of Novel GDI D-Flip-Flop for RTL Design," *J. Comput. Sci. Eng.*, vol. 17, no. 4, pp. 161–168, Dec. 2023.