Low Power Comparator Logic circuit

Rana Musa -1210007, Shaymaa Dawabsha – 1191708, Leyan Buirat - 1211439

Electrical & Computer Engineering Department, Birzeit University
Ramallah, Palestine
1191708@student.birzeit.edu

***Abstract*—**
It has been observed that technology is growing at an exponential rate, including the growing density of an integrated circuit chip, reducing the design area, but this rapid change did not reflect on the battery life of the devices, such that the battery life increased slowly. So, the most targeting objective in the IC design now, become to be in introducing designs with low power consumption with small area and delay. The purpose of this project is to develop an efficient comparator logic circuit design. Comparator logic circuits are among the most important components of electronic devices. They are the main component of ALUs, which are the basis of all modern electronics. In order to implement and verify the design, we will use LTspice XVII tool for functional verification, and Electric EDA tool for layout design, with 22nm as the rule. The smaller the rule, the better the power.

***Keywords*— low power, small area, small delay, comparator circuit, 1-Bit Comparator, 4-Bit Comparator, 8-Bit comparator, XOR, 2X1MUX, GDI.**

I. INTRODUCTION

According to moor's law the number of transistors on single chip is doubled every two years while the size of the chip remain the same, the existence of the transistors within a small area and small space, means that the device will be faster and faster. So by this way we can decrease the area of the design and have a low delay. Also with these we can reduce the power consumption, but this reduction is small, and the need of power saving increases rapidly with the wide use of the electronic devices like laptops, mobile phone, etc.. so power consumption have become an important issues not only for the designers but also for the customers which represent almost if not all people in the world. Hence the main challenge now for the designers is to introduce design that consumes less power 'save battery life'. For this purpose a lot of researches and suggestion are introduced, making a wide range of techniques that can be used in IC design, like clock gating, power gating, multi-voltage technique[1], gate diffusion input 'GDI' technique, AVLS technique, reducing the number of transistors by optimizing the logical function of the signals and so on.

In this project we will implement the comparator logic circuit starting with one-bit comparator circuit, and then build 4-bit and 8-bit comparator circuit using cascading style. In our implementation We will use different techniques to reduce the power in the design like GDI technique and reducing the number of transistors, in addition to that We will consider a small area and small delay for the design.

II. RELATED WORK 'EXITING WORK'

Our implementation, and design of the comparator logic circuit, was based on a previous design 'VLSI Design of Low Power 4 Bit Magnitude Comparator Using GDI Technique 'Sujata S. Chiwandea, Minal L. Keote, Shilpa S. Katre and Shruti H. Bhagwate. Elamaran' [2]. In this research paper the authors tend to introduce a new design for the 4-bit and 8-bit comparator logic circuit, which consumes less power, their assumption for a less power circuit was based on reducing the number of needed transistors in the design, which was obvious in the circuit of the XNOR gate.

The whole logic was to consider a design for the equal function, which done using XNOR gate, and for the greater than function which done using NAND gate. The signal of the less than function was done by a NOR gate that used in the final stage 'equal signal NOR greater than signal', and this will have an obvious effect when cascading the 1-bit comparator circuit to implement 4-bit comparator circuit and so on.

The structural model used in implementing a 4-bit and 8-bit comparator circuit was based on the cascading technique such that using four 1-bit comparator we can build a 4-bit comparator circuit, and using two 4-bit comparator we can build a 8-bit comparator. and in each design the less than function will be calculating in the final 1-bit comparator, to save the area, and hence the power.

III. GDI TECHNIQUE

GDI (Gate Diffusion Input) is a new technique of low power digital circuit design. This technique allows reducing power consumption, delay, and area of digital circuit, in addition is maintain a low complexity of the logic design. [3]

The following figure shows the simplest circuit that depends on the GDI technique, and the next table illustrate all logical functions that can be implemented by different combination of this circuit

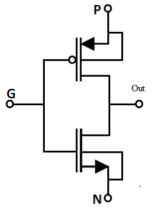

Figure 1 : GDI Basic Cell

N	Ss	P	Sp	G	D	FUNCTIONS
0	0	1	1	A	A'	INVERTER
A	A	0	A	B	AB	AND
1	0	A	D	B	A+B	OR
A'	0	A	1	B	A'B+AB'	XOR
A	0	A'	1	B	AB+A'B	XNOR
0	0	B	B	A	A'B	FUNCTION 1
B	0	1	1	A	A'+B	FUNCTION 2
C	0	B	1	A	A'B+AC	MUX

Figure 2 : Some logic Functions Using The Circuit in Fig1

IV. 1-BIT COMPARATOR LOGIC CIRCUIT

A 1-Bit comparator circuit, is a hardware device that takes two input each of 1-bit, and produces three output signals, Greater than 'GT', Less Than 'LT', and Equal to 'EQ'. one of these three signal can be active at a time, while the others are zeros.

The following describe the function of each output signal, and how I improved the design of each function.

A. Greater Than Signal 'GT'

Greater than will be one if the first binary one in the first number will appear before the first one in the second number, so to find it's logical function, We have used the K-Map as shown in the below figure.

Table 1 K-Map of Greater Than Signal

A / B	0	1
0	0	1
1	0	0

As concluded from the above table, the logical function of the greater than signal is ➔ GT = AB`= A AND B` = A` NOR B. In the previous design the authors used NAND gate to implement the grater than function, which in this case will cost 8 transistors (4 for the NAND, 2 for the first invertor of B, and 2 for the invertor of the NAND gate). But it can be implemented with the NOR gate which will cost in this case 6 transistors, and this step of optimization called logical optimization. and as the aim of the project is to get minimal power, area, and delay, hence We have thought in implementing the greater than function using the GDI technique, such that from Figure2 we can notice that using simple circuit with the GDI technique as in Figure1 we can get the logical function AB`, by considering the connection that specified in the first row in the Figure. Hence this will minimize the area of the design, the delay, and the power.

B. Less Than Signal 'LT'

Less than signal is totally the opposite of the greater than signal, and the following table illustrate the k-map of the less than signal.

Table 2K-Map of Less Than Signal

A / B	0	1
0	0	0
1	1	0

C.

As concluded the logical function of the less than signal is LT = A`B = A` AND B = A NOR B. In our design, the less than signal is represented as GT NOR EQ, as only one of the three signals can be present at a time. Using this approach will yield to a small area since the number of transistors in the 1-input NOR gate is 4, the reason behind not using A`B as in the device in the greater than signal is that the aim of our design is to use the one bit comparator in cascading way for implementing a comparator with higher degree for the inputs, so using the circuit of A`B will enforce me to use it in every single one-bit comparator, while using GT NOR EQ will be very help full when cascading the 1-Bit comparator to implement a comparator for large range of inputs, because we just need to calculate the less than signal once in the final stage of the design, so all what we need in this case is 4 transistors, instead of 8 transistors in case of 4-bit comparator, and 16 transistors in case of 8-bit comparator..

D. Equal To Signal 'EQ'

Equal to means checking if the two inputs have the same sequence of bits, if they have then they are equal else they are not equal. So to find the logical function of the signal, We have used the K-Map which is represent in the below table

Table 3 K-Map for the Equal Signal

A / B	0	1
0	1	0
1	0	1

As conclude from the above table the logical function of the equal signal is è EQ = A`B` + AB = A XNOR B. The equal signal is the most expensive signal, since it achieved by using XNOR gate. We will need 14 transistors to implement XNOR gate using conventional CMOS logic, which requires a large area, a long delay, and high power. Therefore, in XNOR gates, we can optimize better to achieve better results in terms of cost. We can achieve high performance with the XNOR gate by using the GDI logic style, which is one of the best choices for the XNOR gate. This is the same as the one illustrated in the research paper, which has five transistors, model three, and uses GDI logic called 'Gate diffusion input logic'. This technique help us in getting small design for the needed function with small number of transistors, but an important problem in this design is the degradation in the output, since it's not based on the conventional CMOS style,

We have used an XOR gate with the GDI technique for the equal signal, which will be used for an input to the next 1-bit comparator in the case of an n-bit comparator. A MUX with high activation logic was then used to combine the resulting signals before passing them through a NOT gate. In this way, we will get the Equal signal as the output of the NOT gate, and also strengthen the signal to make it more accurate in the next step. By reordering the gates, we can accomplish all of this without adding any more devices.

The following will illustrate the design of the gates used for each signals illustrated above

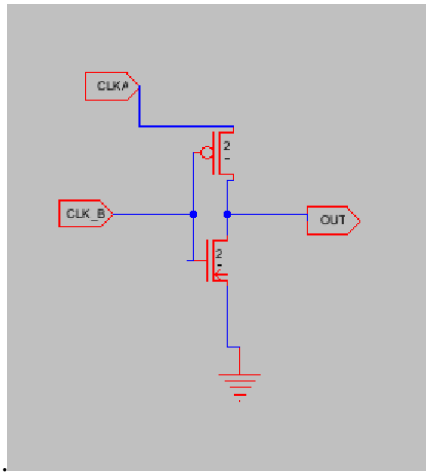

Figure 3 : AB` Circuit 'Greater Than signal circuit'

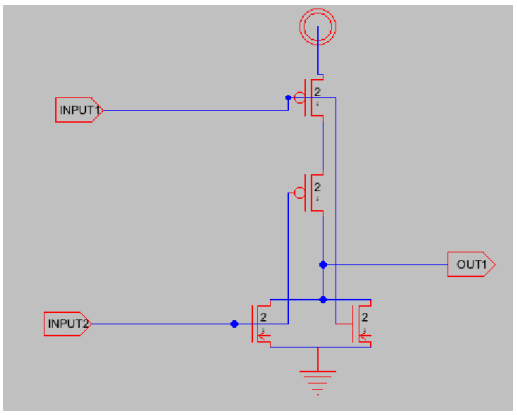

Figure 4: NOR gate

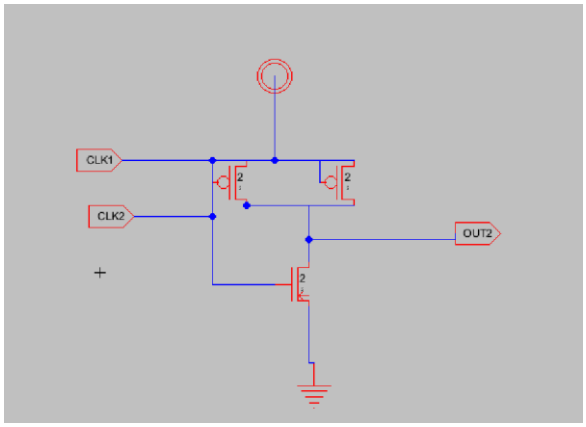

Figure 5 : Optimized XOR gate

E. 2X1-MUX

Using the same idea from the research paper, we have used a 2X1MUX with the previous equal signal as an enable to implement a one bit comparator with higher levels of inputs, but the difference between our design and that is the logic used in the 2X1MUX, which uses conventional CMOS logic, which will require about 12 transistors, and using the pass-transistor logic will cost 6 transistors, however, we used the GDI technique in our design to design the MUX, which only costs 2 transistors, so it can be very helpful in determining power efficiency, the area, and the delay as shown in Figure 6. The MUX in the previous work was enabled at high logic when the previous equal signal was high, while the MUX in our design is enabled at low logic when the greater than signal is high, and at high logic when the equal signal is high. The reason is that using a MUX with the GDI technique will yield to either weak zero or weak one, so to avoid the degradation in the needed logic We have implemented it in this way such that for the greater than signal we're considering to get strong 1 when the MUX is enabled and strong Zero when the MUX is disabled, we designed the mux to be enabled at low logic, with the signal connected to the P part of the MUX. However, since we are using an XOR gate without NOT before the MUX, we are considering getting string zero if the MUX is enabled and the signals are equal, else one, for which the MUX is enabled with high logic in this case, and the signal is connected to the N part of the MUX in order to achieve this.

The following are different implementations of the 2X1MUX

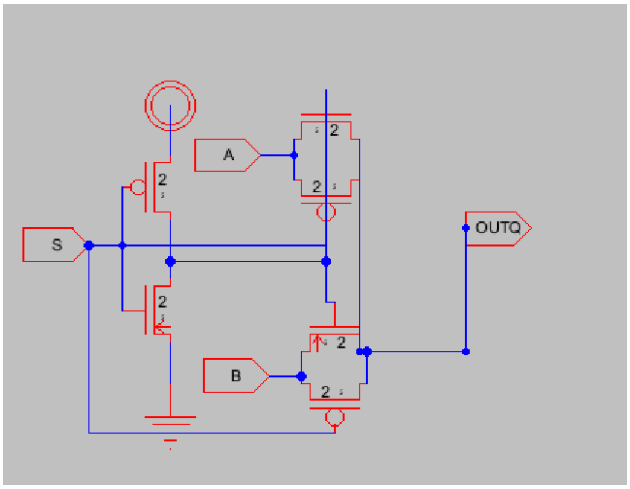

Figure 6 : 2X1-MUX Using Pass-Transistor Logic

The MUX in figure 7 is the one We have used, so in case of Greater Than MUX We have set B = 0, and in case of the Equal MUX We have set A = 1.

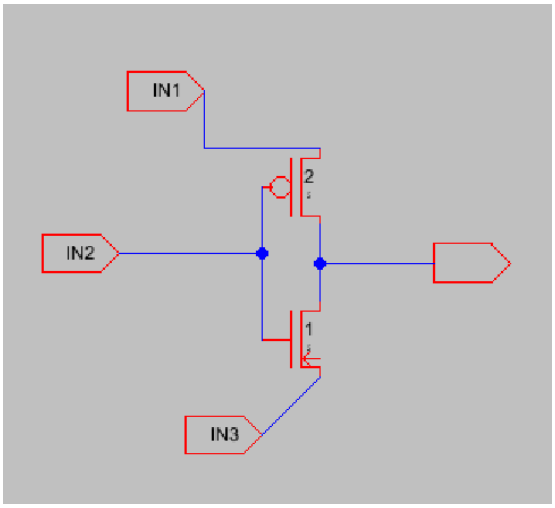

Figure 7 : 2X1-MUX Using GDI Technique

The following shown the functional verification for all the previous gates that We have used in our design. 'AB`, NOR, XOR, 2X1MUX.

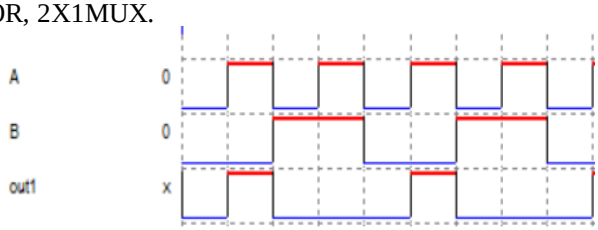

Figure 8 : simulation of AB` Circuit

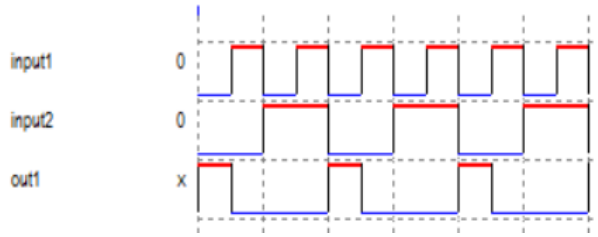

Figure 9 : Simulation of NOR gate

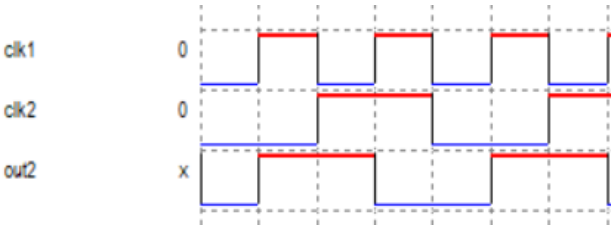

Figure 10 : Simulation of XOR gate

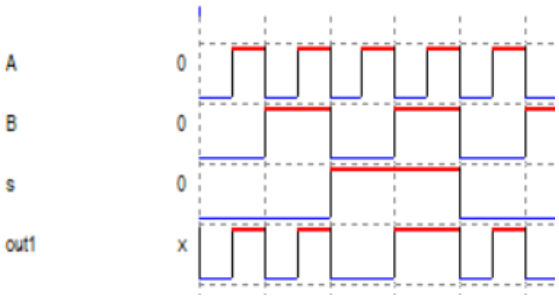

Figure 11 : Simulation of 2X1-MUX

The 1-Bit comparator was connected as explained before, the following are figures for the circuit, the block, and the simulation of the 1-Bit comparator, in addition to the layout.

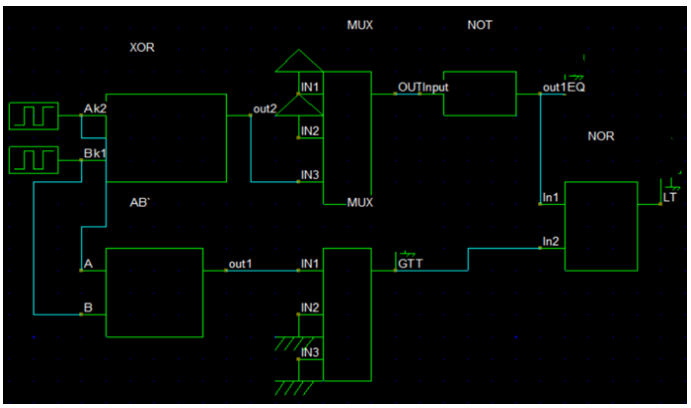

Figure 12 : 1-Bit Comparator Circuit

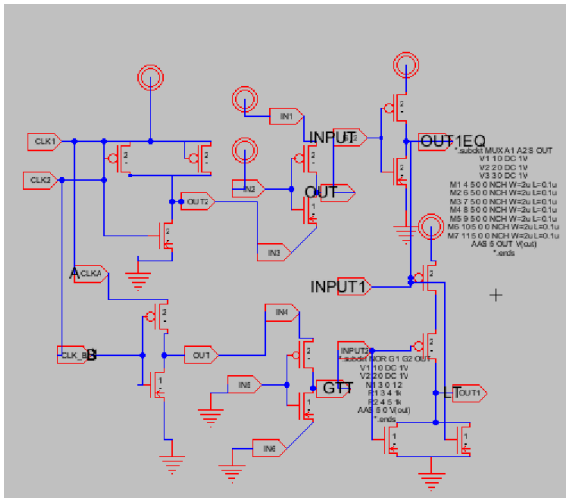

Figure 13 : 1-Bit Comparator Schematic

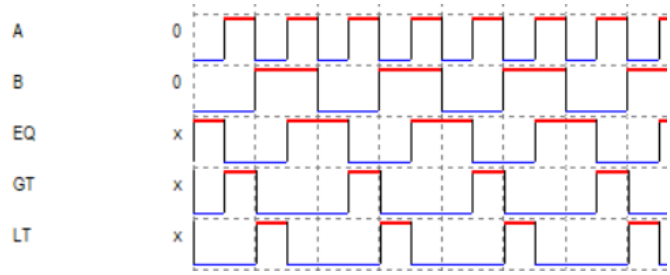

Figure 14 : Simulation of 1-Bit Comparator Circuit

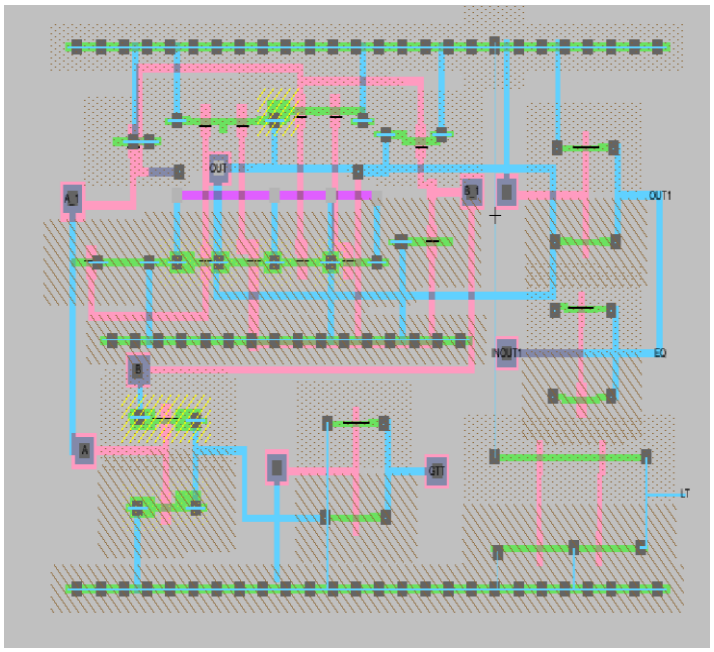

Figure 15 : One-Bit Comparator Layout

V. 4-Bit Comparator

The 4-Bit Comparator performs the same function as the 1-Bit Comparator, with the difference being that it has two inputs, each of size 4-bits, so we can build the 4-Bit Comparator by cascading 1-Bit Comparators. The idea in the cascading design is to use the equal signal from the previous design as an enable to a MUX, if the previous equal signal is 1 then the MUX will pass the result of the current 1-bit comparator else it will pass a zero for both the EQ signal and GT signal. Equal signal is the result of the last 1-bit comparator, whereas greater than signal is the output of the final greater than comparator resulted from each 1-bit comparator. And finally we can calculate the less than signal once after the final equal and greater than signal are ready by using the NOR gate.

The following shown the connection of the 4-Bit Comparator using 1-Bit Comparator, and the functional verification 'simulation' results from that connection, in addition to the layout design.

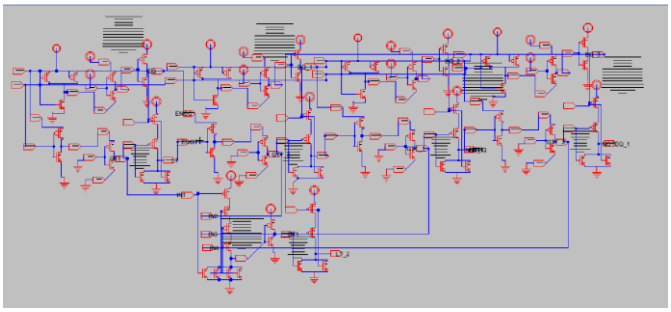

Figure 16 : 4-Bit Comparator Circuit

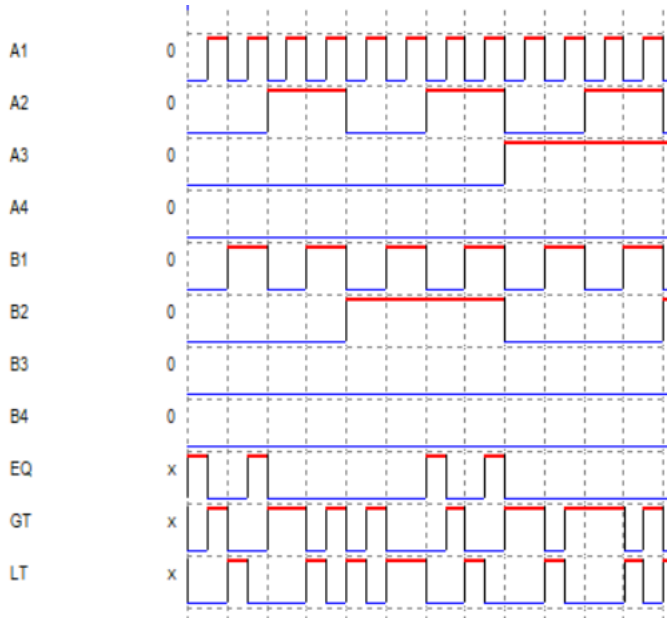

Figure 17 : Simulation of 4-Bit Comparator Circuit

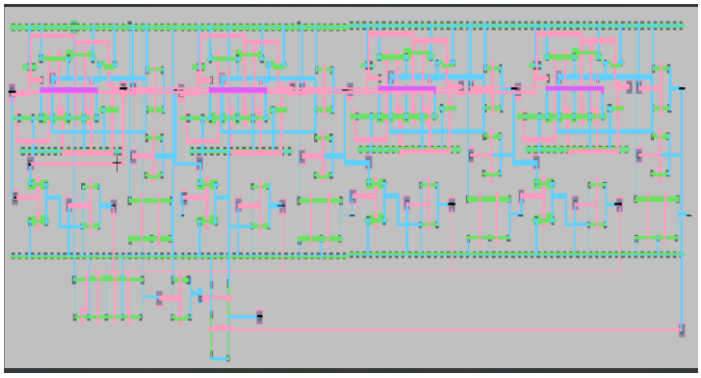

Figure 18 : Four-Bit Comparator Layout

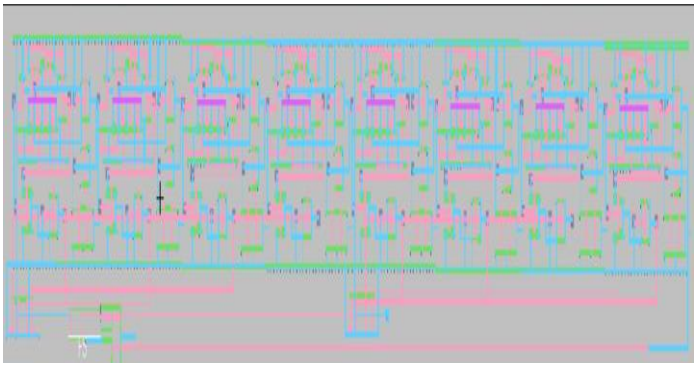

Figure 20-8: bit layout

VI. 8-Bit Comparator

With 8-Bit comparator we have two inputs each of 8-bit, the implementation of the 8-bit comparator can be done in the same way as the 4-bit... for the final result of the Greater than signal, we have an optimization that differ than the one in the research paper. Our optimization was done based on the logical optimization. Therefore, instead of using two 4-input OR gates and one 2-input OR gate to calculate the final greater than signal (the first 4-or gate for the first 4-bit comparator, the second for the second 4-bit comparator, and the 2-OR for the results from the previous two OR gates). In our design We have used two 4-Input NOR gate each one for one of the 4-Bit comparator and then combine the result using 2-Input NAND gate in this case it cost me 20 transistors at all, while the one in the research paper cost 26 transistors.

The following figures illustrate the connection of the 8-Bit Comparator circuit using 1-Bit Comparators, in addition to the functional verification of this connection.

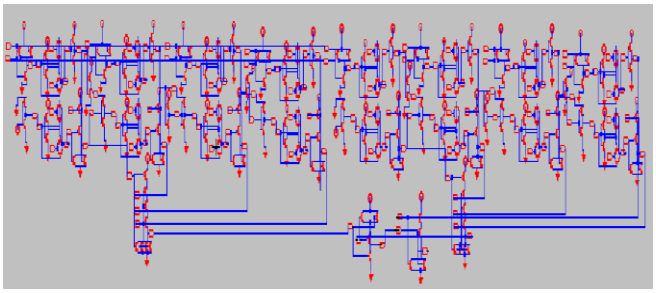

Figure 19 : 8-Bit Comparator schematic

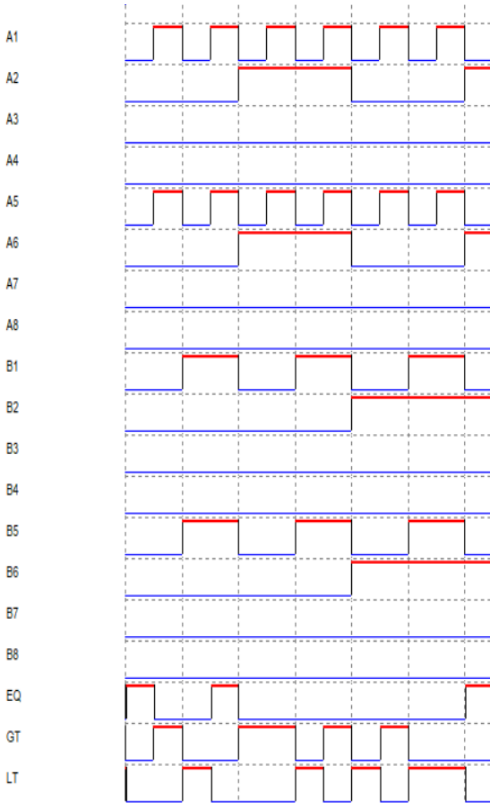

Figure 21 : Simulation of 8-Bit Comparator

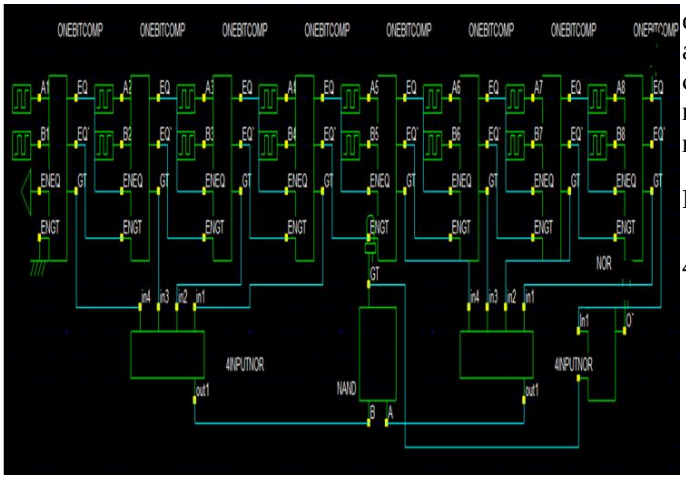

Figure 22 : 8-Bit Comparator Circuit

VII. Testing And Simulation

All the simulations done on layouts with 22nm as the rule, and a time scale equal to 1ns for the simulation window.

A. 1-Bit Comparator

The simulation window, and the concluded results for the 1-Bit Comparator layout are shown below.

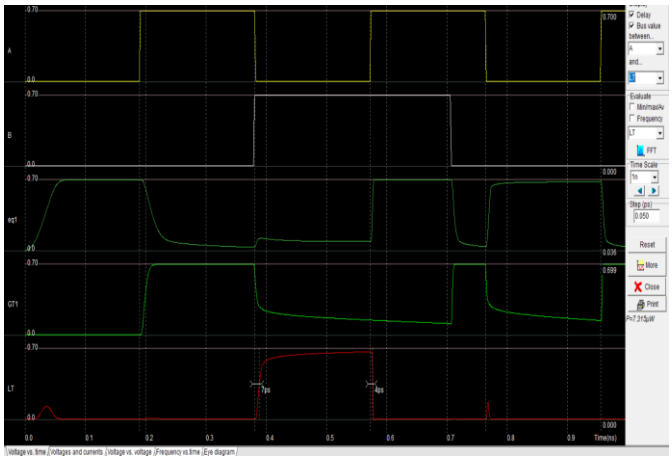

Figure 23 : Simulation Of 1-Bit Comparator Layout

Table 4 : 1-Bit Comparator Layout Design Results

Power	7.31 uW
Delay	4-7-8 ps
Width	0.8 0um
Height	1.10 0um
Area	0.8 um^2

Discussion

From the above results and simulation, I can noticed that the simulation in Figure 22 matches the functional verification at figure 14, which support the correctness of the connection, and of the logic. Also we conclude from the above table that the results are quit good, especially the result of the area ‘0.913 um^2, also the delay is accepted since it is not violating the logic of the layout. According to the power result it seems good and accepted .

B. 4-Bit Comparator

The simulation window, and the concluded results for the 4-Bit Comparator layout are shown below.

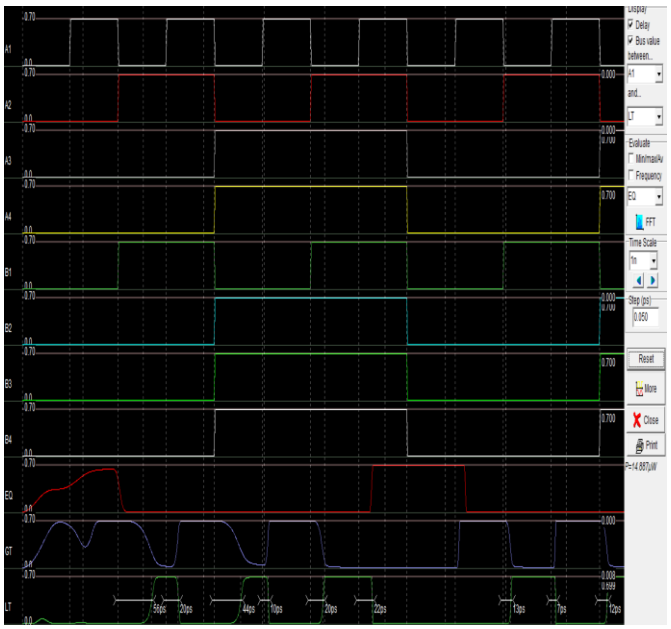

Figure 24 : Simulation of 4-Bit Comparator

Table 5 : 4-Bit Comparator Layout Design Results

Power	14.87 uW
Delay	17-21 ps
Width	2.5 0um
Height	1.5 0um
Area	3.7 um^2

Discussion

From the above results and simulation, I can see the match in he simulation between the one in figure 23 and that of figure 17, which support the correctness of the connection, in addition the obtained results are quit good, the area is perfect, the delay is accepted, and the power is very good .

C. 8-Bit Comparator

The Simulation window, and the concluded results for the 8-Bit Comparator layout are shown below.

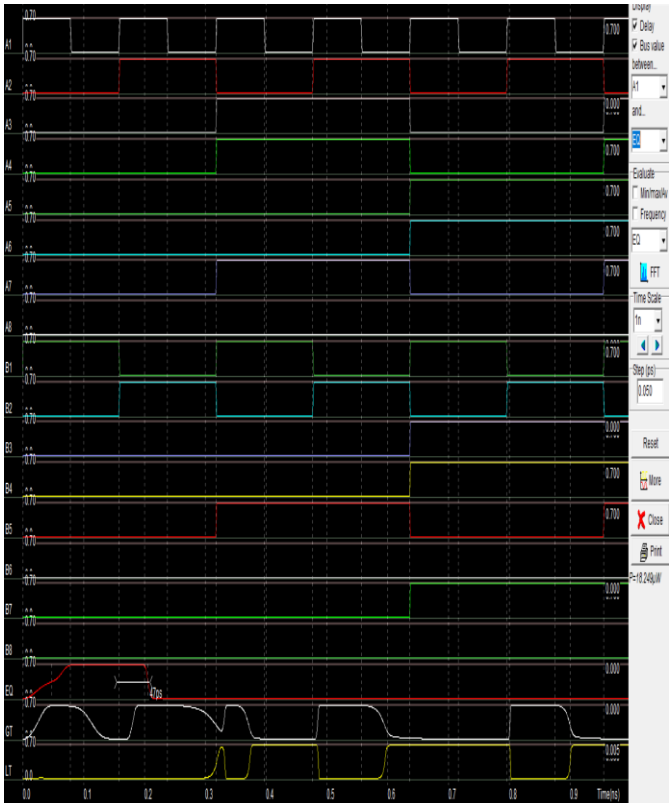

Figure 25 : Simulation of 8-Bit Comparator

Table 6 : 8-Bit Comparator LAyout Design Results

Power	18.249 uW
Delay	49 ps
Width	5.0 um
Height	1.6 um
Area	7.8 um^2

DISCUSSION

From the above results and simulation, I can see the match in the simulation between the one in figure 23 and that of figure 20, which support the correctness of the connection, in addition the obtained results are quit good, the area is perfect, the power is very good, and for the delay although it's high some how but it still good, since we talk about 8-Bit comparator.

VIII. CONCLUSIONS AND FUTURE WORK

In this project We have implemented many optimization on the previous design, depending on different strategies like GDI technique, reducing the number of transistors, using logical optimization and so on, and We have succeed in getting a sophisticated results, and unfortunately the previous design was done using 120nm as a rule for the design, but in the version of MICROWIND we have, this process does not exist, so we tend to select the smallest process so that I can optimize power consumption.

For future work, We will consider different circuits for the XNOR gate, but here due to time constraints We was unable to test all of them and choose the best, but the design we have chosen seems to be very good for power, area, and delay.

ACKNOWLEDGMENT

We feel privileged to thank Dr Khader Mohammad for the supervision in this project, and for the chance of trying new kind of projects. It was helpful, and challenging to try to optimize a previous design and get a sophisticated results..

REFERENCES

[1] What is Low Power Design ? Synoppsys WebSite

[2] K.S.S.K. Rajeash, S.Hari Hara Subamani and V. Elamaran 'CMOS VLSI Design Of Low Power Comparator Circuit' Departemtn Of ECE, School of EEE, SASTRA University, 613401, India

[3] Anjali Sharma, Pranshu Sharma '*Area and Power Efficient 4-Bit Comparator Design by Using 1-Bit Full Adder Module*' Department of Electronics and Communication Engineering, Univ APG Shimla, Shimla, hP, 171009, India.