ExamCompetition.com Computer Organization and Architecture

1. Micro program is

A. The name of source program in micro computers

B. The set of instructions indicating the primitive operations in a system

C. Primitive form of macros used in assembly language programming

D. Program of very small size

2. The CPU of a Computer takes instruction from the memory and executes them. This process is called

A. Load cycle B. Time sequence

C. Fetch-execute cycle D. None of these

3. When a program is being executed in an 8085 microprocessor, its Program Counter contains

A. Number of instructions in the current program that have already been executed

B. The total number of instructions in the program being executed

C. Memory address of the instruction that is being currently executed

D. Memory address of the instruction that is to be executed next

4. The control unit of computer

A. Performs ALU operations on the data

B. Controls the operation of the output devices

C. Both (a) and (b)

D. Directs the other unit of computers

5. The ALU of a computer normally contains a number of high speed storage elements called

A. Semi conductor memory **B. Registers**

C. Hard disk D. IC

6. _____ are used to overcome the difference in data transfer speeds of various devices .

a) Speed enhancing circuitory

b) Bridge circuits

c) Multiple Buses

d) Buffer registers

7. To extend the connectivity of the processor bus we use _____ .

a) PCI bus b) SCSI bus

c) Controllers d) Multiple bus

8. The key feature of the PCI BUS is

a) Low cost connectivity.

b) Plug and Play capability.

c) Expansion of Bandwidth.

d) Both a and c.

9. PCI stands for

a) Peripheral Component Interconnect.

b) Peripheral Computer Internet.

c) Processor Computer Interconnect.

d) Processor Cable Interconnect

10. The DMA transfer is initiated by _____

a) Processor

b) The process being executed

c) I/O devices

d) OS

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11. The technique where the controller is given complete access to main memory is

a) Cycle stealing b) Memory stealing

c) Memory Con **d) Burst mode**

12. In DMA transfers, the required signals and addresses are given by the

a) Processor b) Device drivers

c) DMA controllers d) The program itself

13. The DMA transfers are performed by a control circuit called as

a) Device interface **b) DMA controller**

c) Data controller d) Overlooker

14. In IEEE 32-bit representations, the mantissa of the fraction is said to occupy _____ bits.

a) 24 **b) 23**

c) 20 d) 16

15. The 32 bit representation of the decimal number is called as ____.

a) Double-precision **b) Single-precision**

c) Extended format d) None of the above

16. In IEEE 32-bit representations, the Exponent part is said to occupy _____ bits.

a) 8 b) 23

c) 7 d) 11

17. In the absolute addressing mode

A. Operand is inside the instruction

B. Address of the operand is outside the instruction

C. Register containing the address of the operand is speciied inside theinstruction

D. Location of the operand is implicit.

18. _____ are the different type/s of generating control signals.

a) Micro-programmed b) Hardwired

c) Micro-instruction **d) Both a and b**

19. word whose individual bits represent a control signal is _____.

a) Command word **b) Control word**

c) Co-ordination word d) Generation word

20. Highly encoded schemes that use compact codes to specify a small number of functions in each micro instruction is _____.

a) Horizontal organisation

b) Vertical organisation

c) Diagonal organisation

d) None of the above

21. Microprocessor 8085 is the enhanced version of ..... with essentially the same construction set

A. 6800 B. 68000

C. 8080 D. 8088

22. The sum of -6 and -13 using 2's complement addition is,

a) 11100011 b) 11110011

c) 11001100 **d) 11101101**

23. _____ refers to the operational units and their interconnection that realize the architectural specification

a) Computer Architecture

b) Computer Organization

c) Computer Design

d) Computer structure

24. With the _____, Intel introduce the use of superscalar techniques, which allow multiple instructions to execute in parallel

a) 80486 b) 8085

c) Pentium d) core 2 duo

25. Von Neumann architecture is based on

a) Data and instructions are stored in a single read-write memory.

b) the content of this memory are addressable by location, without regard to the type of data contained there.

c) Execution occurs in a sequential fashion from one instruction to the next.

d) All the above

26. Registers are located at

a) Processor b) cache

c) Main memory d) Secondary memory

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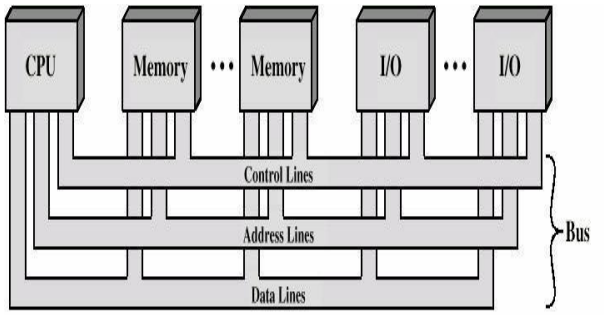
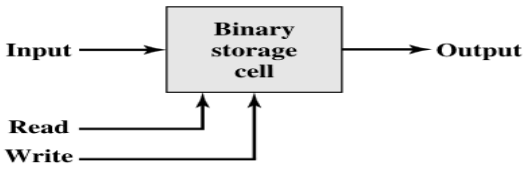
1. The following diagram shows a



a) Bas interconnection scheme
b) Memory interconnection scheme
c) I/O
d) Throughput

2. _____ refers to those attributes of a system visible to a programmer or, put another way, those attributes that have a direct impact on the logical execution of a program
a) computer organization
b) computer architecture
c) Microprocessor
d) Bus

3.the following diagram depicts a _____ cell.



a) storage
b) mobile
c) memory
d) register

4. _____ is the first intel x86 microprocessor with a dual core, referring to the implementation of two processors on a single chip.
a) core
b) core 2 duo
c) dual core
c) Centrino

5._____ chips are high speed processors that are known for their small die size and low power requirements. They are widely used in PDAs and other hand held devices, including games and phones as well as large variety of consumer products. It is probably the most widely used embedded processor architecture and indeed the most widely used processor architecture of any kind in the world
a) HAND
b) LEG
c) ARM
d) SUN

6. the major functions or requirements for an I/O module fall into which of the following categories ?
a) Control and timing.
b) Processor communication
c) Data buffering
d) All of these
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7.This was the first general purpose micro processor. It was designed to be the CPU of a general purpose micro- computer. It was faster, had a richer instruction set and a larger addressing capability. Which microprocessor are we discussing ?
a) 4004
b) 8008
c) 8080
d) All of these

8. the _____ is a popular high-bandwidth, processor independent bus that can function as a mezzanine or peripheral bus.
a) Peripheral component interconnect (PCI)
b) Peripheral component disconnect (PCD)
c) Input output connect
d) Array connect
9. Sequential, direct, random and associative are access methods and key characteristics of computer _____ system
a) Stack
b) counter
c) memory
d) core