NUMBER SYSTEM ExamCompetition.com

1. In which of the following base systems is 123 not a valid number?
(a) Base 10 (b) Base 16
(c)Base 8 **(d) Base 3**

2. Storage of 1 KB means the following number of bytes
(a) 1000 (b)964
(c)1024 (d) 1064.

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3. What is the octal equivalent of the binary number:10111101
(a)675 (b)275
(c) 572 **(d) 573.**

4. The binary code of $(21.125)_{10}$ is
(a) 10101.001 (b) 10100.001
(c) 10101.010 (d) 10100.111.

5. Excess-3 code is known as
(a) Weighted code (b) Cyclic redundancy code
(c) Self-complementing code (d) Algebraic code.

6. How many 1 are present in the binary representation of 15 x 256 + 5 x 16 + 3?
(a) 8 **(b) 9**
(c) 10 (d)11

7. The number of digits in octal system is
(a) 8 (b) 7
(c) 10 (d) none

8. The largest possible decimal number that can be represented by six binary digits (bits) is:
A. 256. B. 128.
C. 64. **D. 63.**

9. Convert the following binary number to decimal. 01011_2
A 11 B 35
C 15 D 10

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10. Convert the binary number 1001.0010_2 to decimal.
A 90.125 B **9.125**
C 125 D 12.5

11. One hex digit is sometimes referred to as a(n):
A byte **B nibble**
C grouping D instruction

12. Convert 59.72_{10} to BCD
A 111011 **B 01011001.01110010**
C 1110.11 D 0101100101110010

13. Convert the binary number 1100 to Gray code
A 0011 **B 1010**
C 1100 D 1001

LOGIC GATE

1. The output of an AND gate with three inputs, A, B, and C, is HIGH when _____.
A. A = 1, B = 1, C = 0 B. A = 0, B = 0, C = 0
C. A = 1, B = 1, C = 1 D. A = 1, B = 0, C = 1

2. If a signal passing through a gate is inhibited by sending a LOW into one of the inputs, and the output is HIGH,
A. AND **B. NAND**
C. NOR D. OR

3. Output will be a LOW for any case when one or more inputs are zero for a(n):
A. OR gate B. NOT gate
C. AND gate D. NOR gate

4. The output of a NOR gate is HIGH if _____.
A. all inputs are HIGH B. any input is HIGH
C. any input is LOW D. all inputs are LOW

5. If the input to a NOT gate is A and the output is X, then _____.
A. X = A **B.** $X = \overline{A}$
C. X = 0 D. none of the above

6. Which of the following gates has the exact inverse output of the OR gate for all possible input combinations?
A. NOR B. AND
C. NAND D. None

7. The logic expression for a NOR gate is _____.
A. $X = \overline{A} + B$ B. $X = A + \overline{B}$
C. $X = A + B$ **D.** $X = \overline{A + B}$

8. A 2-input NOR gate is equivalent to a _____
A negative-OR gate **B negative-AND gate**
C negative-NAND gate C none of the above

9. The output of an exclusive-NOR gate is HIGH if _____.
A the inputs are equal B one input is HIGH, and the other input is LOW
C the inputs are unequal D none of the above

10. A logic circuit that provides a HIGH output for both inputs HIGH or both inputs LOW is a(n):
A Ex-NOR gate B OR gate
C Ex-OR gate D NAND gate

11. Identify the type of gate below from the equation
$X = A \oplus B = \overline{A}B + A\overline{B}$
A Ex-NOR gate B OR gate
C **Ex-OR gate** D NAND gate

12. Which type of gate can be used to add two bits?
A Ex-OR B Ex-NOR
C Ex-NAND D NOR

13. A logic circuit that provides a HIGH output if one input or the other input, but not both, is HIGH, is a(n):
A Ex-NOR gate B OR gate
C Ex-OR gate D NAND gate

ExamCompetition.com ***K-Map & Combinational Circuit***

1. A graphical display of the fundamental products in a truth-table is known as
A. Mapping B. Graphing
C. T-map **D. karnaugh-map**

2. Consider following switching function:
f(w, x, y, z) = w'x' + w'x y'+ wx'z'+ wxy
For this function, which of the following is list of essential prime impicants ?
A. w' x', w' y', x' y', wxy B. wxy, wyz'
C. w' x', w' y', x' z', , wyz D. w' x', w' y', x' z, wxy'

3. The simplified form of the boolean expression
$(X + \bar{Y} + Z)(Z + \bar{Y} + \bar{Z})(X + Y + Z)$ is
A. $\bar{X}Y + \bar{Z}$ **B.** $X + \bar{Y}Z$
C. X D. $XY + \bar{Z}$

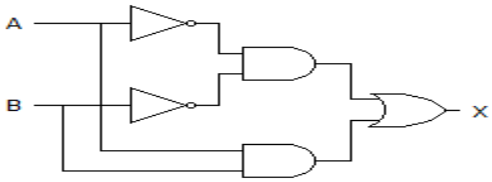
3. Which of the following expressions is in the sum-of-products (SOP) form?
[A] AB + CD
[B] AB(CD)
[C] (A + B)(C + D)
[D] (A)B(CD)

4. The simplest equation which implements the K-map shown below is:

	$\bar{C}$	C
$\bar{A}\bar{B}$	0	0
$\bar{A}B$	1	1
AB	1	1
$A\bar{B}$	0	1

A. $X = AC + B$ B. $X = A\bar{B}$
C. $AB\bar{C} + ABC + A\bar{B}C$ D. $AB + \bar{A}B$

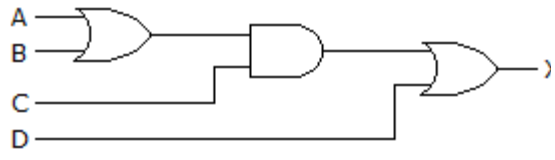
Which of the following logic expressions represents the logic diagram shown?



A. $X = A\bar{B} + \bar{A}B$
B. $X = \overline{A\bar{B}} + AB$
C. $X = \overline{A\bar{B}} + \bar{A}\bar{B}$
D. $X = \bar{A}\bar{B} + AB$

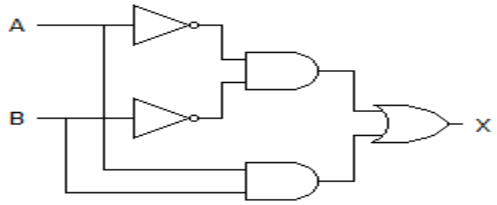
6. Which statement below best describes a Karnaugh map?
A. A Karnaugh map can be used to replace Boolean rules.
B. The Karnaugh map eliminates the need for using NAND and NOR gates.
C. Variable complements can be eliminated by using Karnaugh maps.
D. Karnaugh maps provide a visual approach to simplifying Boolean expressions.

Solve the network in the figure given below for *X*.



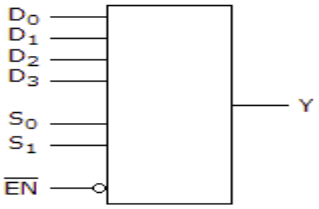
A. $A + BC + D$
B. $((A + B)C) + D$
C. $D(A + B + C)$
D. $(AC + BC)D$

8. What type of logic circuit is represented by the figure shown below?



A. XOR **B. XNOR**
C. AND D. NAND

The device shown here is most likely a _____.



A. Comparator
B. Multiplexer
C. Demultiplexer
D. parity generator

11. How many outputs are on a BCD decoder?
A. 4 B. 16
C. 8 **D. 10**

12. How many data select lines are required for selecting eight inputs?

A. 1 B. 2
C. 3 D. 4

C.J = 0, K = 1 **D.J = 0, K = 0**

ExamCompetition.com ***Sequential circuit***

1. Popular application flip-flop are ?
[A] Counters
[B] Shift registers
[C] Transfer registers
[D] All of above

2. SR Flip flop can be converted to T-type flip-flop if ?
[A] S is connected to Q
[B] R is connected to Q
[C] Both S and R are shortend
[D] S and R are connected to Q and Q' respectively

4. A simple flip-flop
[A] is 2 bit memory
[B] is 1 bit memory
[C] is a four state device
[D] has nothing to do with memory

5. An SR flip flop cannot accept the following input entry
[A] Both input zero
[B] zero at R and one at S
[C] zero at S and one at R
[D] Both inputs one

6. The main difference between JK and RS flip-flop is that?
[A] JK flip-flop does not need a clock pulse
[B] there is feedback in JK flip-flop
[C] JK flip-flop accepts both inputs as 1
[D] JK flip-flop is acronym of junction cathode multivibrator

7. How is a J-K flip-flop made to toggle?
A. J = 0, K = 0
B. J = 1, K = 0
C. J = 0, K = 1
D. J = 1, K = 1

8. How many flip-flops are required to produce a divide-by-128 device?
A. 1 B. 4
C. 6 D. 7

9. Which of the following is correct for a gated D flip-flop?
A. The output toggles if one of the inputs is held HIGH.
B. Only one of the inputs can be HIGH at a time.
C. The output complement follows the input when enabled.
D. Q output follows the input D when the enable is HIGH

10. A J-K flip-flop is in a "no change" condition when _____.
A. J = 1, K = 1 B.J = 1, K = 0

11. The symbols on this flip-flop device indicate _____.
A. triggering takes place on the negative-going edge of the CLK pulse
B. triggering takes place on the positive-going edge of the CLK pulse
C. triggering can take place anytime during the HIGH level of the CLK waveform
D. triggering can take place anytime during the LOW level of the CLK waveform
INCOMPLETE QUESTION

12. What is one disadvantage of an S-R flip-flop?
A. It has no enable input.
B. It has an invalid state.
C. It has no clock input.
D. It has only a single output.

13. How many flip-flops are required to make a MOD-32 binary counter?
A.3 B.45
C.5 D.6

14. A MOD-16 ripple counter is holding the count 10012. What will the count be after 31 clock pulses?
A.10002 B.10102
C.10112 D.11012

15. How many flip-flops are required to construct a decade counter?
A.10 B.8
C.5 **D.4**

16. How many different states does a 3-bit asynchronous counter have?
A.2 B.4
C.8 D.16

17. A 4-bit up/down binary counter is in the DOWN mode and in the 1100 state. To what state does the counter go on the next clock pulse?
A.1101 **B.1011**
C.1111 D.0000

18. A ripple counter's speed is limited by the propagation delay of:
A. each flip-flop
B. all flip-flops and gates
C. the flip-flops only with gates
D. only circuit gates

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19. In a 6-bit Johnson counter sequence there are a total of how many states, or bit patterns?
A.2 B.6
C.12 D.24

20. A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains _____.
A.0000 B.1111
C.0111 D.1000

21. Assume that a 4-bit serial in/serial out shift register is initially clear. We wish to store the nibble 1100. What will be the 4-bit pattern after the second clock pulse? (Right-most bit first.)
A.1100 B.0011
C.0000 D.1111

ExamCompetition.com ***LOGIC FAMILY***

1. Which of the following summarizes the important features of emitter-coupled logic (ECL)?
A. low noise margin, low output voltage swing, negative voltage operation, fast, and high power consumption
B. good noise immunity, negative logic, high-frequency capability, low power dissipation, and short propagation time
C. low propagation time, high-frequency response, low power consumption, and high output voltage swings
D. poor noise immunity, positive supply voltage operation, good low-frequency operation, and low power

2. Which of the following logic families has the shortest propagation delay?
A. CMOS B. TTL
C. ECL D. DTL

3. What is the major advantage of ECL logic?
A. very high speed
B. wide range of operating voltage
C. very low cost
D. very high power

4. The time needed for an output to change from the result of an input change is known as:
A. noise immunity B. fan-out
C. propagation delay D. rise time

5. Which family of devices has the characteristic of preventing saturation during operation?
A. TTL **B. CMOS**
C. ECL D. DTL

6. What is the standard TTL noise margin?
A. 5.0 V B. 0.0 V
C. 0.8 V **D. 0.4 V**

7. Which logic family is characterized by a multiemitter transistor on the input?
A. ECL B. CMOS
C. TTL D. None of the above

MEMORY & CONVERTER

1. How many address bits are needed to select all memory locations in the 16K × 1 RAM?
A. 8 B. 10
C. 14 D. 16

2. The storage element for a static RAM is the _____.
A. diode B. resistor
C. capacitor **D. flip-flop**

3. Select the statement that best describes Read-Only Memory (ROM).
A. nonvolatile, used to store information that changes during system operation
B. nonvolatile, used to store information that does not change during system operation
C. volatile, used to store information that changes during system operation
D. volatile, used to store information that does not change during system operation

4. How many 2K × 8 ROM chips would be required to build a 16K × 8 memory system?
A. 2 B. 4
C. 8 D. 16

5. Which of the following best describes EPROMs?
A. EPROMs can be programmed only once.
B. EPROMs can be erased by UV.
C. EPROMs can be erased by shorting all inputs to the ground.
D. All of the above.

6. The difference between a PLA and a PAL is:
A. The PLA has a programmable OR plane and a programmable AND plane, while the PAL only has a programmable AND plane.
B. The PAL has a programmable OR plane and a programmable AND plane, while the PLA only has a programmable AND plane.
C. The PAL has more possible product terms than the PLA.
D. PALs and PLAs are the same thing.

7. What is a digital-to-analog converter?
A. It allows the use of cheaper analog techniques, which are always simpler.
B. It takes the digital information from an audio CD and converts it to a usable form.
C. It converts direct current to alternating current.
D. It stores digital data on a hard drive.

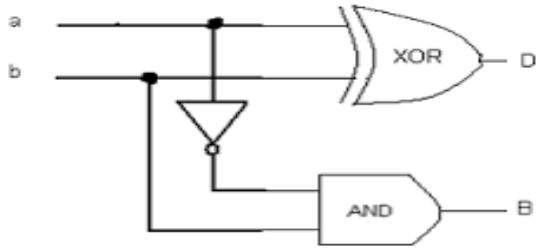
ExamCompetition.com ***KVS 2013***

1. consider an arbitrary number system with the independent digits as 0, 1 and X. what is the radix of this number system ?
a) 1 b) 2
c) 3 d) 4

2. the following diagram shows a

a) Exclusive –NOR gate b) NAND gate
c) AND gate d) OR gate

3. the folloeing diagram shows a

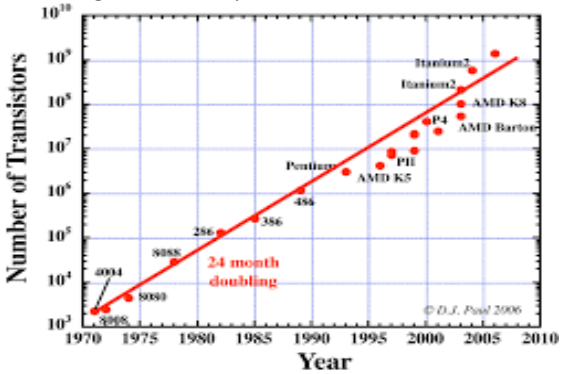


a) half adder **b) half subtractor**
c) full adder d) full subtactor

4. A/an …… also called a data selector, is a combinational circuit with more than one input line, one output line and more than one selection line.
a) de multiplexer **b) multiplexer or MUX**
c) operational amplifier d) integrated circuit

5. A……. multivibrator circuit is one in which LOW and HIGH output states are stable
a) Monostable **b) bistable**
c) Multistable d) Tristable

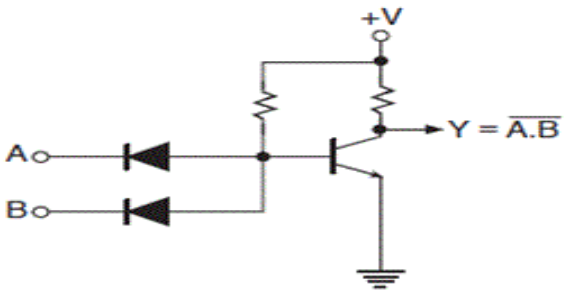
6. the diagram below represents



a) Moore's law b) Netwon Raphson method
c) Boyle's law d) Gregor law

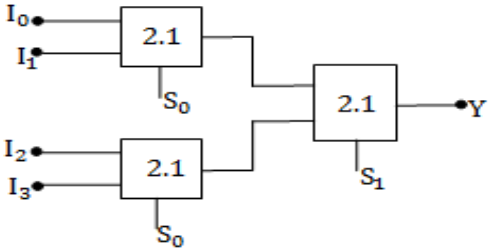
7. _____ memory is intended to give memory speed approaching that of the fastest memories available, and at the same time provide a large memory size at the price of less expensive types of semiconductor memories.
a) Register b) Counter
c) Flip flop **d) Cache**

8. the following diagram depicts _____ logic.



a) diode b) transistor
c) diode-transistor d) resistor

9. Determine the function performed by the combinational circuit of the given figure.



a) 4 to 1 multiplexer b) 8 to 1 multiplexer
c) 16 to 1 multiplexer d) 32 to 1 multiplexer

10. The percentage resolution of an eight bit D/A converter is
a) 0.39% b) 0.38%
c) 0.50% d) 0.51%

11. Determine the size of PROM required for the implementing the 16-to-1 multiplexer.
a) 1M X 1 b) 2M X 1
c) 8M X 1 d) 32M X 1

12. Determine the number of programmable inter-connections in the following programmable logic device PAL device with eight input variables, 16 AND gates and four OR gates.
a) 384 b) 512
c) 256 **d) 128**

13. The reduced expression for the following expression using a Karnaugh Map F(W,X,Y,Z) = ∑(0, 4, 8, 12) is
a) YZ **b) Y'Z'**
c) Y+Z d) Y'+Z'