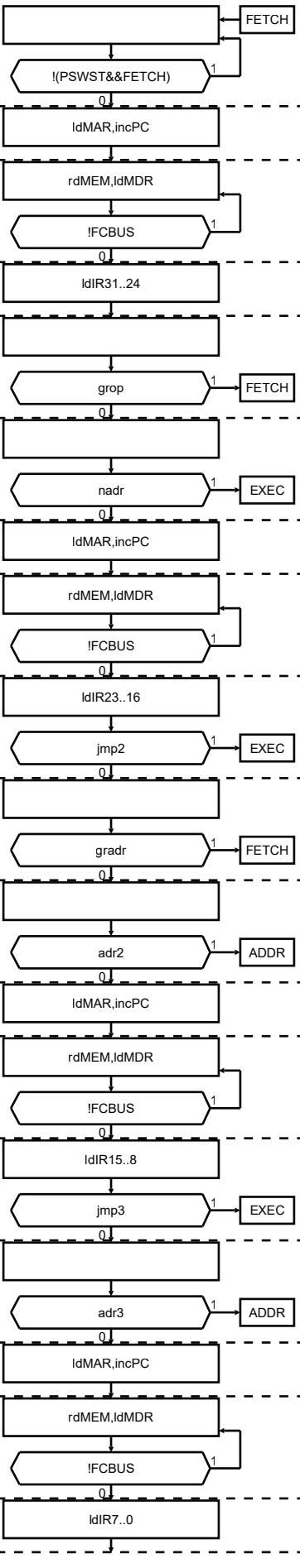
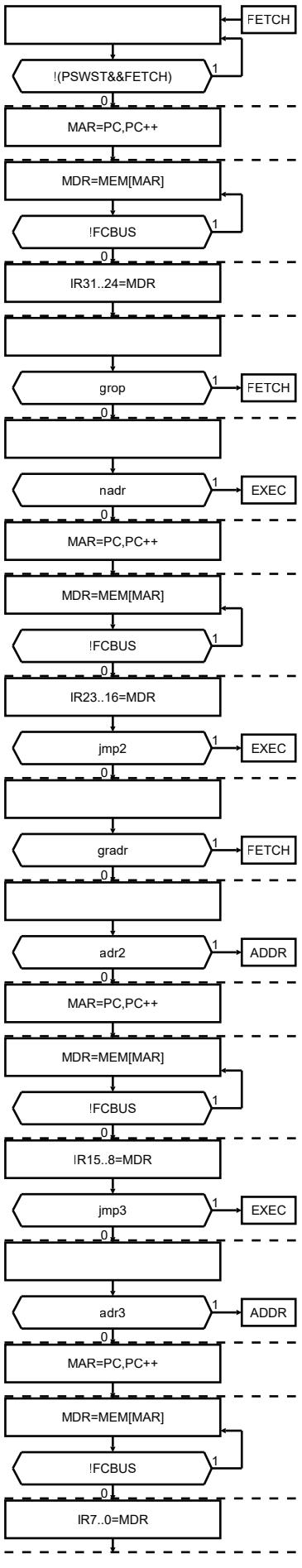


Дијаграм тока
микрооперација

Дијаграм тока
управљачких сигнала

Секвенца управљачких
сигнала



00 FETCH: brief $\neg(\text{PSWST} \& \text{FETCH})$ then this (00)

01 IdMAR, incPC

02 rdMEM, IdMDR brief $\neg(\text{FCBUS})$ then this (02)

03 IdIR31..24

04 brief grop then FETCH (00)

05 brief nadr then EXEC (13)

06 IdMAR, incPC

07 rdMEM, IdMDR brief $\neg(\text{FCBUS})$ then this (07)

08 IdIR23..16 brief jmp2 then EXEC (13)

09 brief gradr then FETCH (00)

0A brief adr2 then ADDR (12)

0B IdMAR, incPC

0C rdMEM, IdMDR brief $\neg(\text{FCBUS})$ then this (0C)

0D IdIR15..8 brief jmp3 then EXEC (13)

0E brief adr3 then ADDR (12)

0F IdMAR, incPC

10 rdMEM, IdMDR brief $\neg(\text{FCBUS})$ then this (10)

11 IdIR7..0



Дијаграм тока микрооперација	Дијаграм тока управљачких сигнала	Секвенца управљачких сигнала
		12 ADDR: clFETCH,stADDR br FETCH (00)
		13 EXEC: clFETCH,stEXEC br FETCH (00)
		00 ADDR: brif !ADDR then this (00)
		01 brcase immed,memdir,regdir,memind,preincr, postdec,regindpom then IMMED (02), MEMDIR (03),REGDIR (04),MEMIND (06), PREINCR (0C),POSTDEC (0D),REGINDPOM (0F)
		02 IMMED: IdB15..8,idB7..0 br EXEC (15)
		03 MEMDIR: IdMAR,mxMAR0 br LOAD (10)
		04 REGDIR: brif STORE then EXEC (15)
		05 IdB15..8,idB7..0,mxB1 br EXEC (15)
		06 MEMIND: IdMAR,mxMAR0
		07 rdMEM,idMDR brif !FCBUS then this (07)
		08 IdB7..0,mxB0,incMAR
		09 rdMEM,idMDR brif !FCBUS then this (09)
		0A IdB15..8,mxB0
		0B IdMAR,mxMAR1 br LOAD (10)
		0C PREINCR: mxOFS0,ldMAR, mxMAR0,mxMAR1,idGPR br LOAD (10)
		0D POSTDEC: IdMAR,mxMAR0,mxMAR1
		0E mxOFS1,ldGPR br LOAD (10)



