Samsung

ARTIK™ Modules

7

710 PCB Design Guide

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VERSION HISTORY

Revision	Date	Description	Maturity
1.0	October 19, 2016	ARTIK 710 PCB Design Guide	Release

ARTIK 710 Overview

ARTIK 710 Features

Table 1 shows an overview of the most important features of the Samsung ARTIK™ 710 Module.

Table 1. ARTIK 710 Module Features

Processor and Boot Mode	
SOC	Nexell S5P6818
Cache	L1 : 32KB I-Cache, 32KB D-Cache
	L2 : 1MB Shared Cache
Co-Processor	VFP(Vector Floating Point Processor), Neon Processor
Chipset	ARM® Cortex®-A53 OCTA(1.4GHz)
Boot Mode Support :	NAND, SPI Flash/EEPROM, NOR, SD(eMMC), USB, UART
ARTIK 710 scenario :	eMMC → SD0 → USB Device
Memory	
Memory/Max. Memory	On Board 1GB
Memory Type	DDR3(up to 800MHz)
Memory Modules	2 x 512MB
Network Tools	
WLAN	
Supports	802.11 a/b/g/n/ac
Antenna	1 X 1
Interface	SDIO
Bluetooth	
Supports	Bluetooth® 4.1
Interface	UART
ZIGBEE®	
Supports	2.4GHz Only
Interface	UART
	+3dBm normal mode output power, up to 8dBm
Storage	
eMMC	
Vendor	Samsung
Supports	eMMC Specification Ver 4.5 (Support 4-bit SDR mode up to 50MHz only)
Capacity	4GB
Security Solution	
Interface	Serial(UART)
Chip	S3FT9MF
Display and External Graphics	
LVDS	
Available max resolution	1920x1080 @60fps
	6 LVDS output channels (5 data channels, 1 clock channel)
MIPI	
Available max resolution	WUXGA (1920x1200)
HDMI	1.4a
Support video format	480p/480i @59.94Hz/60Hz, 576p/576i@50Hz
	720p/720i @50Hz/59.94Hz/60Hz
	1080p/1080i @50Hz/59.94Hz/60Hz
I/O Interface	
SD/MMC Controller	3 x SD/MMC Controller (SD 3.0, SDIO 3.0(WLAN), MMC 4.41, eMMC 4.5(Storage))
	SD_0 available

Ethernet	IEEE 802.3az-2010, for Energy Efficient Ethernet(EEE)
	1000M-bit Ethernet MAC
USB	1 x USB 2.0 port, 1 x USB 2.0 OTG port, 1 x USB HSIC Host
I^2C	3 x I2C Bus Controller (100kbit/s Standard-mode, 400kbit/s Fast-mode)
	I2C_0, I2C_1, I2C_2 available
SPI	3 x SPI Controller
	Master Mode : 50MHz(Receive Data 20MHz) Slave Mode : 8MHz
	SPI_0, SPI_2 available
UART	6 x UART Controller
	Using UART_0 : ZigBee® UART_1 : Bluetooth, UART_2 : eSE
	UART_3, UART_4, UART5 available
PWM	3 x PWM
	Using PWM_1 : eSE
	PWM_0, PWM2 available
ADC	8 x ADC
	ADC 0-5 available
JTAG	1 x JTAG(ARM 20pin)
GPIO	42 x Normal GPIO
	2 x Alive GPIO
ZigBee JTAG	For F/W download 1ea(10pin)
Audio and Camera	
Sound	
Data Interfaces	I2S_0, I2S_1, PCM
Camera	
Interface	MIPI CSI(Support 4 channel virtual channel or data interleave)
Max. Resolution(Still cut)	5M
Video Capture Resolution	1080P

BLOCK DIAGRAM

Figure 1 and *Figure 2* show the ARTIK 710 Module and the ARTIK 710 Development Kit block schematics respectively.

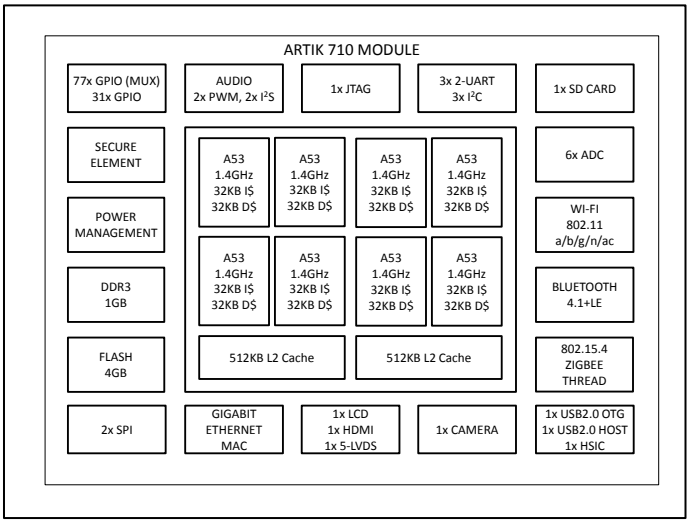

Figure 1. Module Block Diagram

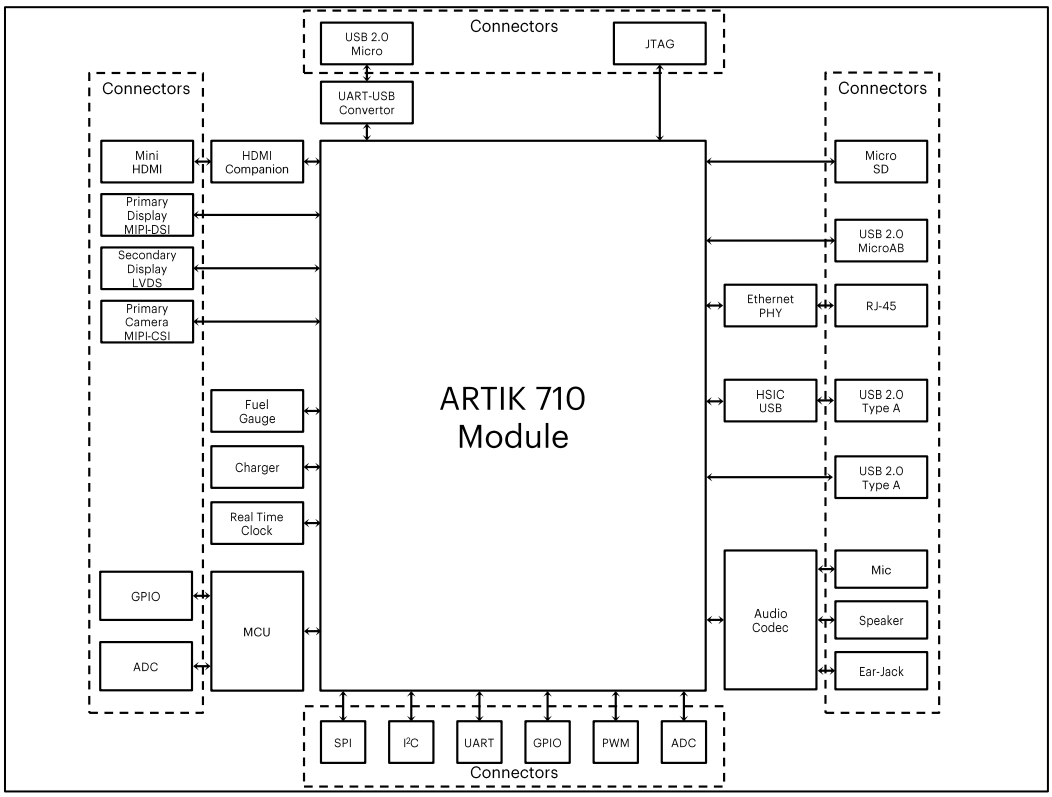

Figure 2. ARTIK 710 Development Kit Block Diagram

MECHANICAL DIMENSIONS & IO FUNCTION DESCRIPTION

MECHANICAL DIMENSION

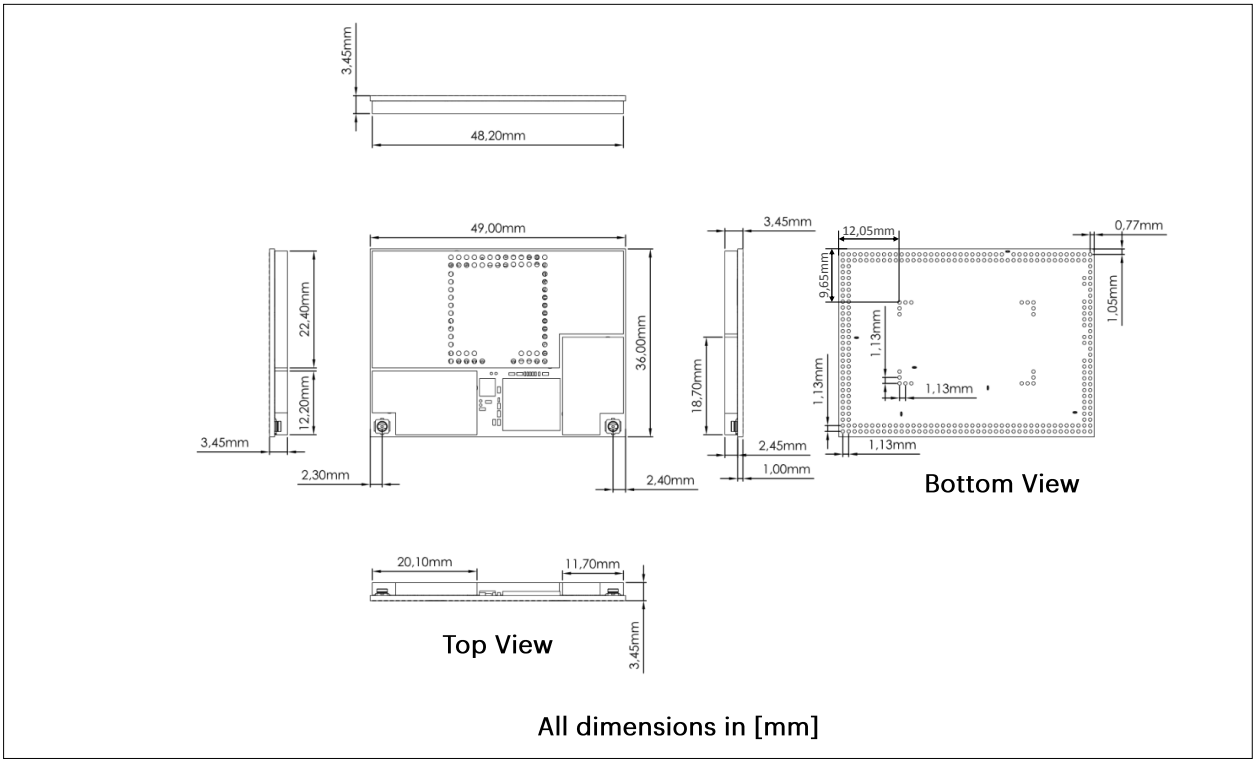

Figure 3. Mechanical Dimensions

Ball Map (Top View)

PA1	PA2	PA3	PA4	PA5	PA6	PA7	PA8	PA9	PA10	PA11	PA12	PA13	PA14	No Ball	PA16	PA17	PA18	PA19	PA20	PA21	PA22	PA23	PA24	PA25	PA26	PA27	PA28	PA29	PA30	PA31	PA32	PA33	PA34	PA35	PA36	PA37	PA38	PA39	PA40	PA41	PA42	PA43
PB1	PB2	PB3	PB4	PB5	PB6	PB7	PB8	PB9	PB10	PB11	PB12	PB13	PB14	PB15	PB16	PB17	PB18	PB19	PB20	PB21	PB22	PB23	PB24	PB25	PB26	PB27	PB28	PB29	PB30	PB31	PB32	PB33	PB34	PB35	PB36	PB37	PB38	PB39	PB40	PB41	PB42	PB43
PC1	No Ball																																								PC42	PC43
PD1	No Ball																																								PD42	PD43
PE1	PE2																																								PE42	PE43
PF1	PF2																																								PF42	PF43
PG1	No Ball																																								PG42	PG43
PH1	No Ball																																								PH42	PH43
PJ1	PJ2									TP282	TP283	TP284																		TP285	TP286	TP287									PJ42	PJ43
PK1	PK2									TP301																						TP288									PK42	PK43
PL1	PL2									TP300																						TP289									PL42	PL43
PM1	PM2																																								PM42	PM43
PN1	PN2																																								PN42	PN43
PP1	No Ball																																								PP42	PP43
PR1	PR2																																								PR42	PR43
PT1	PT2																																								PT42	PT43
PU1	No Ball																																								PU42	PU43
PV1	No Ball																																								PV42	PV43
PW1	PW2																																								PW42	PW43
PY1	PY2																																								PY42	PY43
PAA1	PAA2									TP299																						TP290									PAA42	PAA43
PAB1	PAB2									TP298																						TP291									PAB42	PAB43
PAC1	PAC2									TP297	TP296	TP295																		TP294	TP293	TP292									PAC42	PAC43
PAD1	PAD2																																								PAD42	PAD43
PAE1	PAE2																																								PAE42	PAE43
PAF1	PAF2																																								PAF42	PAF43
PAG1	PAG2																																								PAG42	PAG43
PAH1	PAH2																																								PAH42	PAH43
PAJ1	PAJ2																																								PAJ42	PAJ43
PAK1	PAK2	PAK3	PAK4	PAK5	PAK6	PAK7	PAK8	PAK9	PAK10	PAK11	PAK12	PAK13	PAK14	PAK15	PAK16	PAK17	PAK18	PAK19	PAK20	PAK21	PAK22	PAK23	PAK24	PAK25	PAK26	PAK27	PAK28	PAK29	PAK30	PAK31	PAK32	PAK33	PAK34	PAK35	PAK36	PAK37	PAK38	PAK39	PAK40	PAK41	PAK42	PAK43
PAL1	PAL2	PAL3	PAL4	PAL5	PAL6	PAL7	PAL8	PAL9	PAL10	PAL11	PAL12	PAL13	PAL14	PAL15	PAL16	PAL17	PAL18	PAL19	PAL20	PAL21	PAL22	PAL23	PAL24	PAL25	PAL26	PAL27	PAL28	PAL29	PAL30	PAL31	PAL32	PAL33	PAL34	PAL35	PAL36	PAL37	PAL38	PAL39	PAL40	PAL41	PAL42	PAL43

Figure 4. Ball MAP Top View

I/O Function Description

Ball List Table

Table 2. ARTIK 710 Module Ball List

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA01	GMAC_TXEN	S	IO	N	GPIOE11	GMAC_TXEN		
PA02	GMAC_TXD1	S	IO	N	GPIOE8	GMAC_TXD1		
PA03	GMAC_TXD3	S	IO	N	GPIOE10	GMAC_TXD3		
PA04	GND	G	-	N				
PA05	GMAC_GTXCLK	S	IO	N	GPIOE24	GMAC_GTXCLK		
PA06	GMAC_RXDV	S	IO	N	GPIOE19	GMAC_RXDV	SPITXD1	
PA07	GMAC_RXD2	S	IO	N	GPIOE16	GMAC_RXD2		
PA08	GMAC_RXD0	S	IO	N	GPIOE14	GMAC_RXD0	SPICLK1	
PA09	GND	G	-	N				
PA10	AP_MIPICSI_DNCLK	S	IO	N	AP_MIPICSI_DNCLK			
PA11	AP_MIPICSI_DN0	S	IO	N	AP_MIPICSI_DN0			
PA12	AP_MIPICSI_DN1	S	IO	N	AP_MIPICSI_DN1			
PA13	AP_MIPICSI_DN2	S	IO	N	AP_MIPICSI_DN2			
PA14	AP_MIPICSI_DN3	S	IO	N	AP_MIPICSI_DN3			
PA15	NC	-	-	-				
PA16	AP_MIPIDSI_DNCLK	S	IO	N	AP_MIPIDSI_DNCLK			
PA17	AP_MIPIDSI_DN0	S	IO	N	AP_MIPIDSI_DN0			
PA18	AP_MIPIDSI_DN1	S	IO	N	AP_MIPIDSI_DN1			
PA19	AP_MIPIDSI_DN2	S	IO	N	AP_MIPIDSI_DN2			
PA20	AP_MIPIDSI_DN3	S	IO	N	AP_MIPIDSI_DN3			
PA21	GND	G	-	N				
PA22	AP_LVDS_TN0	S	IO	N	AP_LVDS_TN0			
PA23	AP_LVDS_TN1	S	IO	N	AP_LVDS_TN1			
PA24	AP_LVDS_TN2	S	IO	N	AP_LVDS_TN2			
PA25	AP_LVDS_TNCLK	S	IO	N	AP_LVDS_TNCLK			
PA26	AP_LVDS_TN3	S	IO	N	AP_LVDS_TN3			
PA27	AP_LVDS_TN4	S	IO	N	AP_LVDS_TN4			
PA28	GND	G	-	N				
PA29	AP_HDMI_CEC	S			AP_HDMI_CEC			
PA30	AP_HDMI_TX2N	S	O	N	AP_HDMI_TX2N			
PA31	AP_HDMI_TX1N	S	O	N	AP_HDMI_TX1N			
PA32	AP_HDMI_TX0N	S	O	N	AP_HDMI_TX0N			
PA33	AP_HDMI_TXCN	S	O	N	AP_HDMI_TXCN			
PA34	GND	G	-	N				
PA35	AP_OTG_DM	S	IO	N	AP_OTG_DM			
PA36	AP_USBH_DM	S	IO	N	AP_USBH_DM			
PA37	AP_GPA13	S						
PA38	AP_HSIC_STROBE	S	IO	N	AP_HSIC_STROBE			
PA39	AP_GPA14	S	IO	N	GPIOA14	DISD13		
PA40	AP_GPA9	S	IO	N	GPIOA9	DISD8		
PA41	AP_GPA15	S	IO	N	GPIOA15	DISD14		
PA42	AP_GPA12	S	IO	N	GPIOA12	DISD11		
PA43	GND	G	-	N				
PAA1	AP_ADC2	S	IO	N	AP_ADC2			
PAA2	AP_ADC3	S	IO	N	AP_ADC3			
PAA42	VBAT_MAIN	P		N				
PAA43	VBAT_MAIN	P		N				
PAB1	GND	G	-	N				
PAB2	GND	G	-	N				

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAB42	VBAT_MAIN	P		N				
PAB43	VBAT_MAIN	P		N				
PAC1	AP_TCK	S	IO	PD	TCLK	GPIOE28		
PAC2	AP_TMS	S	IO	PU	TMS	GPIOE26		
PAC42	GND	G	-	N				
PAC43	GND	G	-	N				
PAD1	AP_TDO	S	IO	N	TDO	GPIOE29		
PAD2	AP_TDI	S			TDI	GPIOE27		
PAD42	VCC3P3_LDO8	P		N				
PAD43	VCC3P3_LDO8	P		N				
PAE1	AP_NTRST	S	IO	PU	NTRST	GPIOE25		
PAE2	AP_AGP2_RTC_INT_N	S	IO	N	ALIVEGPIO2			
PAE42	GND	G	-	N				
PAE43	VCC3P3_LDO8	P		N				
PAF1	AP_PWRKEY	S	IO	N	ALIVEGPIO0			
PAF2	AP_AGP1_HOMEKEY	S	IO	N	ALIVEGPIO1			
PAF42	GND	G	-	N				
PAF43	GND	G	-	N				
PAG1	AP_NRESET	S	I	N	NRESET			
PAG2	AP_GPA25_BACKKEY	S	IO	N	GPIOA25	DISVSYNC		
PAG42	AP_GPB11	S	IO	N	CLE0	CLE1	GPIOB11	
PAG43	AP_GPB18	S	IO	N	NNFWE0	NNFWE1	GPIOB18	
PAH1	AP_GPA26_VOLUP	S	IO	N	GPIOA26	DISHSYNC		
PAH2	AP_GPA0_MENUKEY	S	IO	N	GPIOA0	DISCLK		
PAH42	AP_GPC25	S	IO	PU	NSWAIT	GPIOC25	SPDIFTX	
PAH43	AP_GPE31	S	IO	PU	NSWE	GPIOE31		
PAJ1	AP_I2S0_LRCLK	S	IO	N	GPIOD12	I2SLRCLK0	AC97_SYNC	
PAJ2	AP_GPA27_VOLDOWN	S	IO	N	GPIOA27	DISDE		
PAJ42	BT_PCM_D_OUT	S	O	N	BT_PCM_OUT			
PAJ43	BT_PCM_LRCK	S	IO	N	BT_PCM_LRCK			
PAK01	AP_I2S0_DOUT	S	IO	N	GPIOD9	I2SDOUT0	AC97_DOUT	
PAK02	AP_I2S0_BCLK	S	IO	N	GPIOD10	I2SBCLK0	AC97_BCLK	
PAK03	AP_GPC11_SPI2_MISO	S	IO	N	SA11	GPIOC11	SPIRXD2	USB2.0OTG_ DRVVBUS
PAK04	AP_GPC9_SPI2_CLK	S	IO	N	SA9	GPIOC9	SPICLK2	
PAK05	AP_SPI0_MISO	S	IO	N	GPIOD0	SPIRXD0	PWM3	
PAK06	AP_SPI0_CLK	S	IO	N	GPIOC29	SPICLK0		
PAK07	AP_GPC14_PWM2	S	IO	N	SA14	GPIOC14	PWM2	VICLK2
PAK08	AP_GPD6_SCL	S	IO	N	GPIOD6	SCL2		
PAK09	AP_GPD4_SCL1	S	IO	N	GPIOD4	SCL1		
PAK10	AP_GPD2_SCL0	S	IO	N	GPIOD2	SCL0	ISO7816	
PAK11	AP_GPA23_HDMI_I2C_SCL	S	IO	N	GPIOA23	DISD22		
PAK12	ZB_JTMS	S	IO	N	ZB_JTMS			
PAK13	ZB_JTCK	S	IO	N	ZB_JTCK			
PAK14	ZB_PC0	S	IO	N	DIGITAL IO			
PAK15	ZB_PA4	S	IO	N	DIGITAL IO			
PAK16	GND	G	-	N				
PAK17	VCC3P3_SYS	P		N				
PAK18	VCC3P3_SYS	P		N				
PAK19	AP_NBATTF	S	I	N	NBATF			
PAK20	AP_GPE2	S	IO	N	GPIOE2	VID0_6	TSIDATA1_6	
PAK21	AP_GPE1	S	IO	N	GPIOE1	VID0_5	TSIDATA1_5	
PAK22	AP_UARTTX3	S	IO	N	GPIOD21	UARTTXD3		SDNCD1
PAK23	AP_UARTTX4	S	IO	N	SD13	GPIOB29	TSIDATA0_5	UARTTXD4
PAK24	AP_UARTTX5	S	IO	N	SD15	GPIOB31	TSIDATA0_7	UARRTTXD5

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAK25	AP_GPB0_VID1_1_I2SLRCK1	S	IO	N	GPIOB0	VID1_1	SDEX1	I2SLRCLK1
PAK26	AP_GPA28_I2SMCLK1	S	IO	N	GPIOA28	VICLK1	I2SMCLK2	I2SMCLK1
PAK27	AP_GPA30_VID1_0_I2SBCLK1	S	IO	N	GPIOA30	VID1_0	SDEX0	I2SBCLK1
PAK28	AP_SD0_CMD	S	IO	N	GPIOA31	SDCMD0		
PAK29	AP_SD0_D1	S	IO	N	GPIOB3	SDDAT0_1		
PAK30	AP_SD0_CLK	S	IO	N	GPIOA29	SDCLK0		
PAK31	NC	-	-	-				
PAK32	AP_GPB13_SD0_BOOT	S	IO	N	SD0	GPIOB13		
PAK33	AP_GPC17	S	IO	N	SA17	GPIOC17	TSIDP0	VID2_0
PAK34	AP_GPC0	S	IO	N	SA0	GPIOC0	TSERR0	
PAK35	AP_GPC26	S	IO	PU	RDNWR	GPIOC26		
PAK36	AP_GPB8	S	IO	N	GPIOB8	VID1_5	SDEX5	I2SDOUT2
PAK37	AP_GPB14	S	IO	N	RNB0	RNB1	GPIOB14	
PAK38	AP_GPA20	S	IO	N	GPIOA20	DISD19		
PAK39	AP_GPA18	S	IO	N	GPIOA18	DISD17		
PAK40	AP_GPA21	S	IO	N	GPIOA21	DISD20		
PAK41	AP_GPA10	S	IO	N	GPIOA10	DISD9		
PAK42	AP_GPA6	S	IO	N	GPIOA6	DISD5		
PAK43	BT_PCM_D_IN	S	I	N	BT_PCM_IN			
PAL01	AP_I2S0_DIN	S	IO	N	GPIOD11	I2SDIN0	AC97_DIN	
PAL02	AP_I2S0_MCLK	S	IO	N	GPIOD13	I2SMCLK0	AC97_NRST	
PAL03	AP_GPC12_SPI2_MOSI	S	IO	N	SA12	GPIOC12	SPITXD2	SDNRST2
PAL04	AP_GPC10_SPI2_CS	S	IO	PU	SA10	GPIOC10	SPIFRM2	
PAL05	AP_SPI0_MOSI	S	IO	N	GPIOC31	SPITXD0		
PAL06	AP_SPI0_CS	S	IO	N	GPIOC30	SPIFRM0		
PAL07	AP_GPD1_PWM0	S	IO	N	GPIOD1	PWM0	SA25	
PAL08	AP_GPD7_SDA	S	IO	N	GPIOD7	SDA2		
PAL09	AP_GPD5_SDA1	S	IO	N	GPIOD5	SDA1		
PAL10	AP_GPD3_SDA0	S	IO	N	GPIOD3	SDA0	ISO7816	
PAL11	AP_GPA24_HDMI_I2C_SDA	S	IO	N	GPIOA24	DISD23		
PAL12	ZB_JTDI	S	I	N	JTDI			
PAL13	ZB_JTDO	S	O	N	JTDO			
PAL14	ZB_RSTN	S	I	PU	NRESET			
PAL15	ZB_PA5	S	IO	N	DIGITAL IO			
PAL16	GND	G	-	N				
PAL17	VCC3P3_SYS	P		N				
PAL18	VCC3P3_SYS	P		N				
PAL19	AP_VDDPWRON	S	O	N	VDDPWRON			
PAL20	AP_GPE3	S	IO	N	GPIOE3	VID0_7	TSIDATA1_7	
PAL21	AP_GPE0	S	IO	N	GPIOE0	VID0_4	TSIDATA1_4	
PAL22	AP_UARTRX3	S	IO	N	GPIOD17	UARTRXD3		
PAL23	AP_UARTRX4	S	IO	N	SD12	GPIOB28	TSIDATA0_4	UARTRXD4
PAL24	AP_UARTRX5	S	IO	N	SD14	GPIOB30	TSIDATA0_6	UARTRXD5
PAL25	AP_GPD31	S	IO	N	GPIOD31	VID0_3	TSIDATA1_3	
PAL26	AP_GPB9_I2SDIN1	S	IO	N	GPIOB9	VID1_6	SDEX6	I2SDIN1
PAL27	AP_GPB6_VID1_4_I2SDOUT1	S	IO	N	GPIOB6	VID1_4	SDEX4	I2SDOUT1
PAL28	AP_SD0_D3	S	IO	N	GPIOB7	SDDATA0_3		
PAL29	AP_SD0_D2	S	IO	N	GPIOB5	SDDATA0_2		
PAL30	AP_SD0_D0	S	IO	N	GPIOB1	SDDATA0_0		
PAL31	AP_GPB4_VID1_3_BOOT	S	IO	N	GPIOB4	VID1_3	SDEX3	I2SLRCLK2
PAL32	AP_GPB15_SD1_BOOT	S	IO	N	SD1	GPIOB15		
PAL33	AP_GPD8	S	IO	N	GPIOD8	PPM		
PAL34	AP_GPE30	S	IO	PU	NSOE	GPIOE30		
PAL35	AP_GPC27	S	IO	PU	NSDQM	GPIOC27		
PAL36	AP_GPB22	S	IO	N	SD6	GPIOB22		

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAL37	AP_GPB16	S	IO	N	NNFOE0	NNFOE1	GPIOB16	
PAL38	AP_GPB23	S	IO	N	SD7	GPIOB23		
PAL39	AP_GPA22	S	IO	N	GPIOA22	DISD21		
PAL40	AP_GPA19	S	IO	N	GPIOA19	DISD18		
PAL41	AP_GPA17	S	IO	N	GPIOA17	DISD16		
PAL42	AP_GPA3	S	IO	N	GPIOA3	DISD2		
PAL43	BT_PCM_CLK	S	IO	N	BT_PCM_CLK			
PB01	GND	G	-	N				
PB02	GMAC_TXD0	S	IO	N	GPIOE7	GMAC_TXD0	VIVSYNC1	
PB03	GMAC_TXD2	S	IO	N	GPIOE9	GMAC_TXD2		
PB04	GMAC_MDC	S	IO	N	GPIOE20	GMAC_MDC		
PB05	GMAC_RXCLK	S	IO	N	GPIOE18	GMAC_RXCLK	SPIRXD1	
PB06	GMAC_RXD3	S	IO	N	GPIOE17	GMAC_RXD3		
PB07	GMAC_RXD1	S	IO	N	GPIOE15	GMAC_RXD1	SPIFRM1	
PB08	GMAC_MDIO	S	IO	N	GPIOE21	GMAC_MDIO		
PB09	GND	G	-	N				
PB10	AP_MIPICSI_DPCLK	S	IO	N	AP_MIPICSI_DPCLK			
PB11	AP_MIPICSI_DP0	S	IO	N	AP_MIPICSI_DP0			
PB12	AP_MIPICSI_DP1	S	IO	N	AP_MIPICSI_DP1			
PB13	AP_MIPICSI_DP2	S	IO	N	AP_MIPICSI_DP2			
PB14	AP_MIPICSI_DP3	S	IO	N	AP_MIPICSI_DP3			
PB15	GND	G	-	N				
PB16	AP_MIPIDSI_DPCLK	S	IO	N	AP_MIPIDSI_DPCLK			
PB17	AP_MIPIDSI_DP0	S	IO	N	AP_MIPIDSI_DP0			
PB18	AP_MIPIDSI_DP1	S	IO	N	AP_MIPIDSI_DP1			
PB19	AP_MIPIDSI_DP2	S	IO	N	AP_MIPIDSI_DP2			
PB20	AP_MIPIDSI_DP3	S	IO	N	AP_MIPIDSI_DP3			
PB21	GND	G	-	N				
PB22	AP_LVDS_TP0	S	IO	N	AP_LVDS_TP0			
PB23	AP_LVDS_TP1	S	IO	N	AP_LVDS_TP1			
PB24	AP_LVDS_TP2	S	IO	N	AP_LVDS_TP2			
PB25	AP_LVDS_TPCLK	S	IO	N	AP_LVDS_TPCLK			
PB26	AP_LVDS_TP3	S	IO	N	AP_LVDS_TP3			
PB27	AP_LVDS_TP4	S	IO	N	AP_LVDS_TP4			
PB28	GND	G	-	N				
PB29	AP_HDMI_HPD	S	I	N	AP_HDMI_HPD			
PB30	AP_HDMI_TX2P	S	O	N	AP_HDMI_TX2P			
PB31	AP_HDMI_TX1P	S	O	N	AP_HDMI_TX1P			
PB32	AP_HDMI_TX0P	S	O	N	AP_HDMI_TX0P			
PB33	AP_HDMI_TXCP	S	O	N	AP_HDMI_TXCP			
PB34	GND	G	-	N				
PB35	AP_OTG_DP	S	IO	N	AP_OTG_DP			
PB36	AP_USBH_DP	S	IO	N	AP_USBH_DP			
PB37	AP_OTG_ID	S	IO	N	AP_OTG_ID			
PB38	AP_HSIC_DATA	S	IO	N	AP_HSIC_DATA			
PB39	AP_GPA4	S	IO	N	GPIOA4	DISD3		
PB40	AP_GPA5	S	IO	N	GPIOA5	DISD4		
PB41	AP_GPA16	S	IO	N	GPIOA16	DISD15		
PB42	AP_GPA11	S	IO	N	GPIOA11	DISD10		
PB43	GND	G	-	N				
PC1	GND	G	-	N				
PC2	NC	-	-	-				
PC42	GND	G	-	N				
PC43	GND	G	-	N				
PD1	GND	G	-	N				

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PD2	NC	-	-	-				
PD42	VCC5P0_OTGVBUS	P		N				
PD43	VCC5P0_OTGVBUS	P		N				
PE1	GND	G	-	N				
PE2	GND	G	-	N				
PE42	VCC2P8_LDO7	P		N				
PE43	VCC2P8_LDO7	P		N				
PF1	GND	G	-	N				
PF2	GND	G	-	N				
PF42	VCC2P8_LDO7	P		N				
PF43	GND	G	-	N				
PG1	GND	G	-	N				
PG2	NC	-	-	-				
PG42	GND	G	-	N				
PG43	GND	G	-	N				
PH1	GND	G	-	N				
PH2	NC	-	-	-				
PH42	VCC_LDO5	P		N				
PH43	VCC_LDO5	P		N				
PJ1	GND	G	-	N				
PJ2	GND	G	-	N				
PJ42	VCC_LDO5	P		N				
PJ43	VCC_LDO2	P		N				
PK1	GND	G	-	N				
PK2	GND	G	-	N				
PK42	VCC_LDO2	P		N				
PK43	VCC_LDO2	P		N				
PL1	GND	G	-	N				
PL2	GND	G	-	N				
PL42	GND	G	-	N				
PL43	GND	G	-	N				
PM1	GND	G	-	N				
PM2	GND	G	-	N				
PM42	VCC_LDO1	P		N				
PM43	VCC_LDO1	P		N				
PN1	GND	G	-	N				
PN2	GND	G	-	N				
PN42	VCC_LDO1	P		N				
PN43	GND	G	-	N				
PP1	GND	G	-	N				
PP2	NC	-	-	-				
PP42	VCC1P2_LDO10	P		N				
PP43	GND	G	-	N				
PR1	GND	G	-	N				
PR2	GND	G	-	N				
PR42	VCC1P2_LDO10	P		N				
PR43	VCC1P2_LDO10	P		N				
PT1	VCC1P8_LDO4	P		N				
PT2	GND	G	-	N				
PT42	VCC_LDO9	P		N				
PT43	GND	G	-	N				
PU1	VCC1P8_LDO4	P		N				
PU2	NC	-	-	-				
PU42	VCC_LDO9	P		N				
PU43	VCC_LDO9	P		N				

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PV1	VCC1P8_LDO4	P		N				
PV2	NC	-	-	-				
PV42	VBAT_MAIN	P		N				
PV43	VBAT_MAIN	P		N				
PW1	AP_ADC4	S	IO	N	AP_ADC4			
PW2	AP_ADC5	S	IO	N	AP_ADC5			
PW42	VBAT_MAIN	P		N				
PW43	VBAT_MAIN	P		N				
PY1	AP_ADC0	S	IO	N	AP_ADC0			
PY2	AP_ADC1	S	IO	N	AP_ADC1			
PY42	VBAT_MAIN	P		N				
PY43	VBAT_MAIN	P		N				

Note:

1. Type definition – S:Signal ball, P:Power ball, G:GND ball
2. IO pad type definition – I:Input, O:Output. IO: Input/Output
3. Internal Pull Up/Down definition – PU:Pull Up, PD:Pull Down, N:No Pull

BALL LIST TABLE: SORTED BY FUNCTION

HDMI

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA29	AP_HDMI_CEC	S			AP_HDMI_CEC			
PA30	AP_HDMI_TX2N	S	O	N	AP_HDMI_TX2N			
PA31	AP_HDMI_TX1N	S	O	N	AP_HDMI_TX1N			
PA32	AP_HDMI_TX0N	S	O	N	AP_HDMI_TX0N			
PA33	AP_HDMI_TXCN	S	O	N	AP_HDMI_TXCN			
PB29	AP_HDMI_HPD	S	I	N	AP_HDMI_HPD			
PB30	AP_HDMI_TX2P	S	O	N	AP_HDMI_TX2P			
PB31	AP_HDMI_TX1P	S	O	N	AP_HDMI_TX1P			
PB32	AP_HDMI_TX0P	S	O	N	AP_HDMI_TX0P			
PB33	AP_HDMI_TXCP	S	O	N	AP_HDMI_TXCP			

LVDS

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA22	AP_LVDS_TN0	S	IO	N	AP_LVDS_TN0			
PA23	AP_LVDS_TN1	S	IO	N	AP_LVDS_TN1			
PA24	AP_LVDS_TN2	S	IO	N	AP_LVDS_TN2			
PA25	AP_LVDS_TNCLK	S	IO	N	AP_LVDS_TNCLK			
PA26	AP_LVDS_TN3	S	IO	N	AP_LVDS_TN3			
PA27	AP_LVDS_TN4	S	IO	N	AP_LVDS_TN4			
PB22	AP_LVDS_TP0	S	IO	N	AP_LVDS_TP0			
PB23	AP_LVDS_TP1	S	IO	N	AP_LVDS_TP1			
PB24	AP_LVDS_TP2	S	IO	N	AP_LVDS_TP2			
PB25	AP_LVDS_TPCLK	S	IO	N	AP_LVDS_TPCLK			
PB26	AP_LVDS_TP3	S	IO	N	AP_LVDS_TP3			
PB27	AP_LVDS_TP4	S	IO	N	AP_LVDS_TP4			

MIPI CSI

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA10	AP_MIPICSI_DNCLK	S	IO	N	AP_MIPICSI_DNCLK			
PA11	AP_MIPICSI_DN0	S	IO	N	AP_MIPICSI_DN0			
PA12	AP_MIPICSI_DN1	S	IO	N	AP_MIPICSI_DN1			
PA13	AP_MIPICSI_DN2	S	IO	N	AP_MIPICSI_DN2			
PA14	AP_MIPICSI_DN3	S	IO	N	AP_MIPICSI_DN3			
PB10	AP_MIPICSI_DPCLK	S	IO	N	AP_MIPICSI_DPCLK			
PB11	AP_MIPICSI_DP0	S	IO	N	AP_MIPICSI_DP0			
PB12	AP_MIPICSI_DP1	S	IO	N	AP_MIPICSI_DP1			
PB13	AP_MIPICSI_DP2	S	IO	N	AP_MIPICSI_DP2			
PB14	AP_MIPICSI_DP3	S	IO	N	AP_MIPICSI_DP3			

MIPI DSI

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA16	AP_MIPIDSI_DNCLK	S	IO	N	AP_MIPIDSI_DNCLK			
PA17	AP_MIPIDSI_DN0	S	IO	N	AP_MIPIDSI_DN0			
PA18	AP_MIPIDSI_DN1	S	IO	N	AP_MIPIDSI_DN1			
PA19	AP_MIPIDSI_DN2	S	IO	N	AP_MIPIDSI_DN2			
PA20	AP_MIPIDSI_DN3	S	IO	N	AP_MIPIDSI_DN3			
PB16	AP_MIPIDSI_DPCLK	S	IO	N	AP_MIPIDSI_DPCLK			
PB17	AP_MIPIDSI_DP0	S	IO	N	AP_MIPIDSI_DP0			
PB18	AP_MIPIDSI_DP1	S	IO	N	AP_MIPIDSI_DP1			
PB19	AP_MIPIDSI_DP2	S	IO	N	AP_MIPIDSI_DP2			
PB20	AP_MIPIDSI_DP3	S	IO	N	AP_MIPIDSI_DP3			

ETHERNET MAC

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA01	GMAC_TXEN	S	IO	N	GPIOE11	GMAC_TXEN		
PA02	GMAC_TXD1	S	IO	N	GPIOE8	GMAC_TXD1		
PA03	GMAC_TXD3	S	IO	N	GPIOE10	GMAC_TXD3		
PA05	GMAC_GTXCLK	S	IO	N	GPIOE24	GMAC_GTXCLK		
PA06	GMAC_RXDV	S	IO	N	GPIOE19	GMAC_RXDV	SPITXD1	
PA07	GMAC_RXD2	S	IO	N	GPIOE16	GMAC_RXD2		
PA08	GMAC_RXD0	S	IO	N	GPIOE14	GMAC_RXD0	SPICLK1	
PB02	GMAC_TXD0	S	IO	N	GPIOE7	GMAC_TXD0	VIVSYNC1	
PB03	GMAC_TXD2	S	IO	N	GPIOE9	GMAC_TXD2		
PB04	GMAC_MDC	S	IO	N	GPIOE20	GMAC_MDC		
PB05	GMAC_RXCLK	S	IO	N	GPIOE18	GMAC_RXCLK	SPIRXD1	
PB06	GMAC_RXD3	S	IO	N	GPIOE17	GMAC_RXD3		
PB07	GMAC_RXD1	S	IO	N	GPIOE15	GMAC_RXD1	SPIFRM1	
PB08	GMAC_MDIO	S	IO	N	GPIOE21	GMAC_MDIO		

UART

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAK22	AP_UARTTX3	S	IO	N	GPIOD21	UARTTXD3		SDNCD1
PAK23	AP_UARTTX4	S	IO	N	SD13	GPIOB29	TSIDATA0_5	UARTTXD4
PAK24	AP_UARTTX5	S	IO	N	SD15	GPIOB31	TSIDATA0_7	UARRTTXD5
PAL22	AP_UARTRX3	S	IO	N	GPIOD17	UARTRXD3		
PAL23	AP_UARTRX4	S	IO	N	SD12	GPIOB28	TSIDATA0_4	UARTRXD4
PAL24	AP_UARTRX5	S	IO	N	SD14	GPIOB30	TSIDATA0_6	UARTRXD5

I²C

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAK08	AP_GPD6_SCL	S	IO	N	GPIOD6	SCL2		
PAK09	AP_GPD4_SCL1	S	IO	N	GPIOD4	SCL1		
PAK10	AP_GPD2_SCL0	S	IO	N	GPIOD2	SCL0	ISO7816	
PAL08	AP_GPD7_SDA	S	IO	N	GPIOD7	SDA2		
PAL09	AP_GPD5_SDA1	S	IO	N	GPIOD5	SDA1		
PAL10	AP_GPD3_SDA0	S	IO	N	GPIOD3	SDA0	ISO7816	

SPI

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAK03	AP_GPC11_SPI2_MISO	S	IO	N	SA11	GPIOC11	SPIRXD2	USB2.0OTG_DRVVBUS
PAK04	AP_GPC9_SPI2_CLK	S	IO	N	SA9	GPIOC9	SPICLK2	
PAK05	AP_SPI0_MISO	S	IO	N	GPIOD0	SPIRXD0	PWM3	

PAK06	AP_SPI0_CLK	S	IO	N	GPIOC29	SPICLK0		
PAL03	AP_GPC12_SPI2_MOSI	S	IO	N	SA12	GPIOC12	SPITXD2	SDNRST2
PAL04	AP_GPC10_SPI2_CS	S	IO	PU	SA10	GPIOC10	SPIFRM2	
PAL05	AP_SPI0_MOSI	S	IO	N	GPIOC31	SPITXD0		
PAL06	AP_SPI0_CS	S	IO	N	GPIOC30	SPIFRM0		

PWM

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAK07	AP_GPC14_PWM2	S	IO	N	SA14	GPIOC14	PWM2	VICLK2
PAL07	AP_GPD1_PWM0	S	IO	N	GPIOD1	PWM0	SA25	

PCM (BT)

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAJ42	BT_PCM_D_OUT	S	O	N	BT_PCM_OUT			
PAJ43	BT_PCM_LRCK	S	IO	N	BT_PCM_LRCK			
PAK43	BT_PCM_D_IN	S	I	N	BT_PCM_IN			
PAL43	BT_PCM_CLK	S	IO	N	BT_PCM_CLK			

SD/MMC

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAK28	AP_SD0_CMD	S	IO	N	GPIOA31	SDCMD0		
PAK29	AP_SD0_D1	S	IO	N	GPIOB3	SDDAT0_1		
PAK30	AP_SD0_CLK	S	IO	N	GPIOA29	SDCLK0		
PAL28	AP_SD0_D3	S	IO	N	GPIOB7	SDDATA0_3		
PAL29	AP_SD0_D2	S	IO	N	GPIOB5	SDDATA0_2		
PAL30	AP_SD0_D0	S	IO	N	GPIOB1	SDDATA0_0		

USB 2.0 Host

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA36	AP_USBH_DM	S	IO	N	AP_USBH_DM			
PB36	AP_USBH_DP	S	IO	N	AP_USBH_DP			

USB 2.0 HSIC Host

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA38	AP_HSIC_STROBE	S	IO	N	AP_HSIC_STROBE			
PB38	AP_HSIC_DATA	S	IO	N	AP_HSIC_DATA			

USB 2.0 OTG

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PA35	AP_OTG_DM	S	IO	N	AP_OTG_DM			
PB35	AP_OTG_DP	S	IO	N	AP_OTG_DP			
PB37	AP_OTG_ID	S	IO	N	AP_OTG_ID			

I²S

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAJ1	AP_I2S0_LRCLK	S	IO	N	GPIOD12	I2SLRCLK0	AC97_SYNC	
PAK01	AP_I2S0_DOUT	S	IO	N	GPIOD9	I2SDOUT0	AC97_DOUT	
PAK02	AP_I2S0_BCLK	S	IO	N	GPIOD10	I2SBCLK0	AC97_BCLK	
PAL01	AP_I2S0_DIN	S	IO	N	GPIOD11	I2SDIN0	AC97_DIN	
PAL02	AP_I2S0_MCLK	S	IO	N	GPIOD13	I2SMCLK0	AC97_NRST	
PAK25	AP_GPB0_VID1_1_I2SLRCK1	S	IO	N	GPIOB0	VID1_1	SDEX1	I2SLRCLK1
PAK26	AP_GPA28_I2SMCLK1	S	IO	N	GPIOA28	VICLK1	I2SMCLK2	I2SMCLK1
PAK27	AP_GPA30_VID1_0_I2SBCLK1	S	IO	N	GPIOA30	VID1_0	SDEX0	I2SBCLK1
PAL26	AP_GPB9_I2SDIN1	S	IO	N	GPIOB9	VID1_6	SDEX6	I2SDIN1
PAL27	AP_GPB6_VID1_4_I2SDOUT1	S	IO	N	GPIOB6	VID1_4	SDEX4	I2SDOUT1

ADC

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAA1	AP_ADC2	S	IO	N	AP_ADC2			
PAA2	AP_ADC3	S	IO	N	AP_ADC3			
PW1	AP_ADC4	S	IO	N	AP_ADC4			
PW2	AP_ADC5	S	IO	N	AP_ADC5			
PY1	AP_ADC0	S	IO	N	AP_ADC0			
PY2	AP_ADC1	S	IO	N	AP_ADC1			

ALIVE GPIO

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAF1	AP_PWRKEY	S	IO	N	ALIVEGPIO0			
PAF2	AP_AGP1_HOMEKEY	S	IO	N	ALIVEGPIO1			
PAE2	AP_AGP2_RTC_INT_N	S	IO	N	ALIVEGPIO2			

JTAG (AP)

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAC1	AP_TCK	S	IO	PD	TCLK	GPIOE28		
PAC2	AP_TMS	S	IO	PU	TMS	GPIOE26		
PAD1	AP_TDO	S	IO	N	TDO	GPIOE29		
PAD2	AP_TDI	S			TDI	GPIOE27		
PAE1	AP_NTRST	S	IO	PU	NTRST	GPIOE25		

JTAG (ZIGBEE)

Ball	Name	Type	I/O	PU/PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
PAK12	ZB_JTMS	S	IO	N	ZB_JTMS			
PAK13	ZB_JTCK	S	IO	N	ZB_JTCK			

PAK14	ZB_PC0	S	IO	N	DIGITAL IO			
PAK15	ZB_PA4	S	IO	N	DIGITAL IO			
PAL12	ZB_JTDI	S	I	N	JTDI			
PAL13	ZB_JTDO	S	O	N	JTDO			
PAL14	ZB_RSTN	S	I	PU	NRESET			
PAL15	ZB_PA5	S	IO	N	DIGITAL IO			

NOT CONNECTED (NC)

Ball	Name
PA15, PAK31, PC2, PD2, PG2, PH2, PP2, PU2, PV2	NC

POWER: VDD

Ball	Name
PV42,PV43,PW42,PW43,PY42,PY43,PAA42,PAA43,PAB42,PAB43,	VBAT_MAIN
PAK17,PAK18,PAL17,PAL18	VCC3P3_SYS
PD42,PD43	VCC5P0_OTGVBUS
PM42,PM43,PN42	VCC_LDO1
PJ43,PK42,Pk43	VCC_LDO2
PT1,PU1,PV1	VCC1P8_LDO4
PH42,PH43,PJ42	VCC_LDO5
PE42,PE43,PF42	VCC2P8_LDO7
PAD42,PAD43,PAE43	VCC3P3_LDO8
PT42,PU42,PU43	VCC_LDO9
PP42,PR42,PR43	VCC1P2_LDO10

POWER: GND

Ball	Name
PA4,PA9,PA21,PA28,PA34,PA43,PAB1,PAB2,PAC42,PAC43,PAE42,PAF42,PAF43,PAK16,PAL16,PB01,PB09,PB15,PB21,PB28,PB34,PB43,,PC1,PC42,PC43,PD1,PE1,PE2,PF1,PF2,PF43,PG,PG42,PG43,PH1,PJ1,PJ2,PK1,PK2,PL1,PL2,PL42,PL43,PM1,PM2,PN1,PN2,PN43,PP1,PP43,PR1,PR2,PT2,PT43	GND

POWER DESIGN GUIDE

ELECTRICAL CHARACTERISTIC

ABSOLUTE MAXIMUM RATINGS

Exposure to the absolute maximum ratings may cause permanent damage and affect the reliability and safety of both device and system. The functional operation cannot be guaranteed beyond specified values given in the recommended operational conditions.

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VBAT_MAIN	Power Supply Voltage	-0.3	5.25*	V
T_{STO}	Storage Temperature	-55	100	˚C

***Note:** The maximum continuous voltage is 5.25V. Voltages up to 6.0V for up to 10 seconds, for a cumulative duration, over the lifetime of the device are allowed.

RECOMMENDED OPERATING CONDITIONS

Table 4. Recommended Operating Conditions

Symbol	Comment	Min	Typ	Max	Units
VBAT_MAIN	Power Supply Voltage	3.6	4.2	5.0	V
T_A	Commercial	0	–	70	˚C
	Industrial	-40	–	85	

INPUT POWER MANAGEMENT*

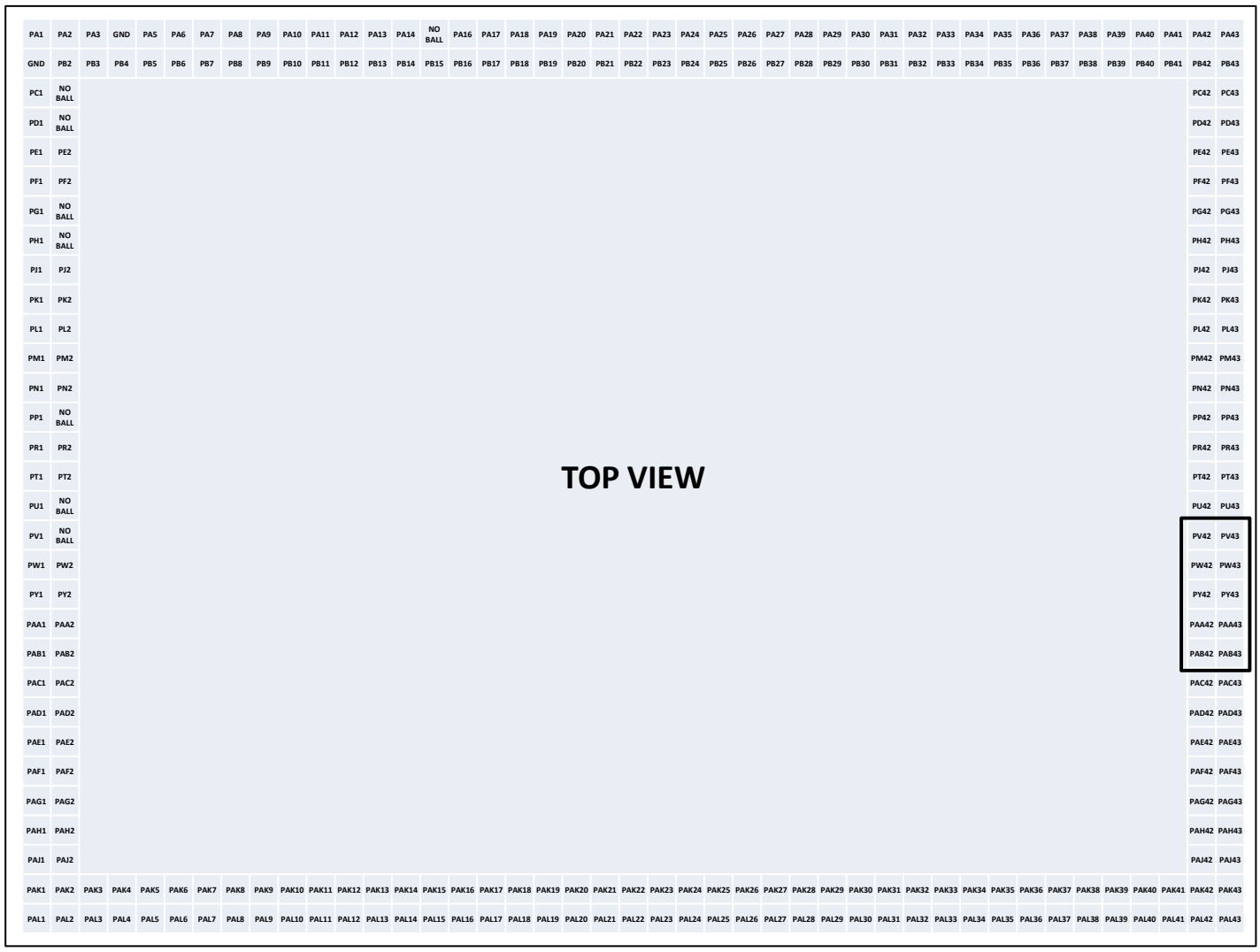

Figure 5. VBAT_MAIN Pin Locations on the ARTIK 710 Module

Power supply to VBAT_MAIN (Typ 4.2V) is needed to power up the ARTIK 710 Module. VBAT_MAIN is connected to a total of 10 pins (PV42, PV43, PW42, PW43, PY42, PY43, PAA42, PAA43, PAB42, PAB43).

REFERENCE SCHEMATIC

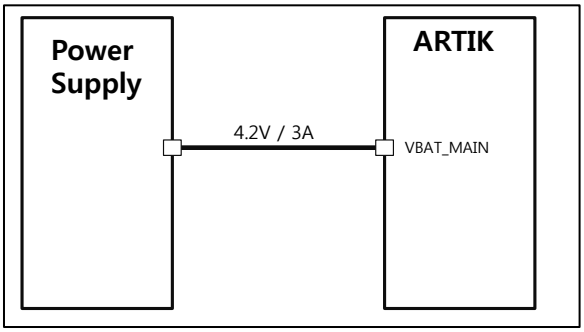

Figure 6. Direct Power Connection from Power Supply VBAT_MAIN

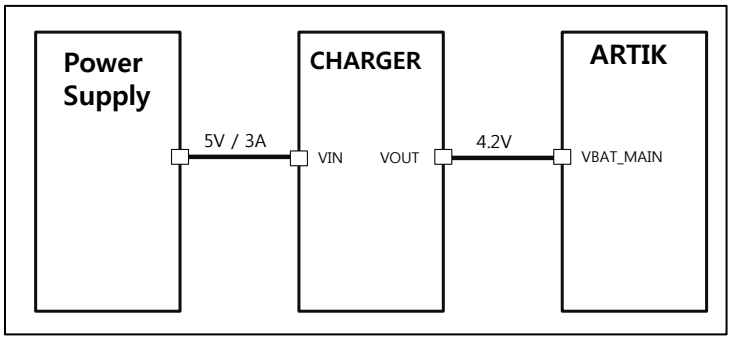

Figure 7. Power Connection through Charger IC

OUTPUT POWER MANAGEMENT

OUTPUT POWER FEATURE

Table 5. DCDC Converter Output

Output	Initial Voltage	Maximum Current	Description
VCC3P3_SYS	3.3V	1000mA	Internally used as IO power supply

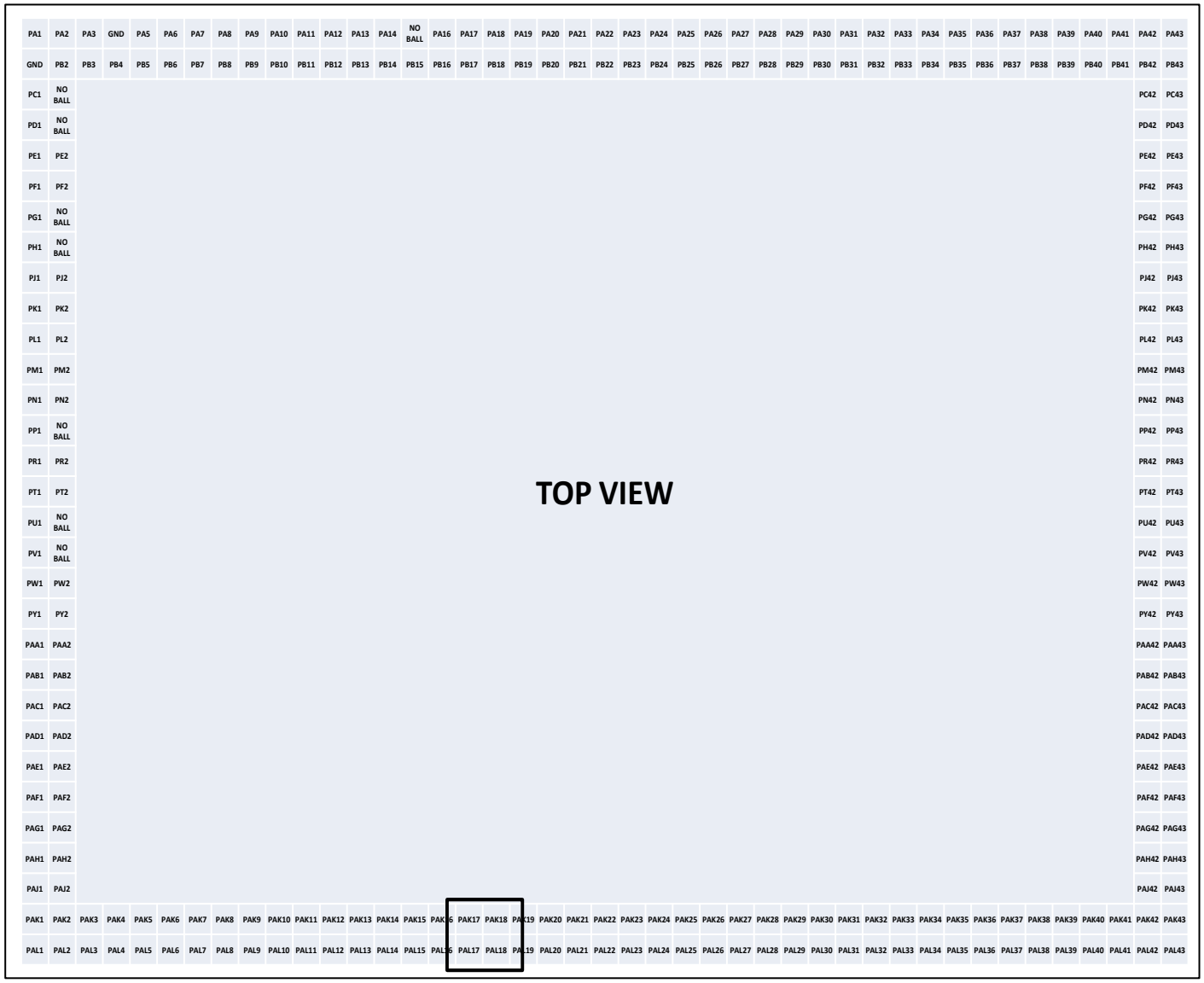

Figure 8. VCC3P3_SYS Pin Locations on the ARTIK 710 Module

Note: VCC3P3_SYS pins are total 4 pins. (PAK17, PAK18, PAL17, PAL18)

LDOs Output

Symbol	Initial Voltage	Control Range	Maximum Current	Pin Name	Description
LDO1	3.3V	0.9V~3.5V	300mA	PM42, PM43, PN42	User Control
LDO2	3.3V			PJ43, PK42, PK43	User Control
LDO3	1.8V			-	Reserved
LDO4	1.8V			PT1, PU1, PV1	User Control
LDO5	3.3V	0.6V~3.5V		PH42, PH43, PJ42	User Control
LDO6	3.3V			-	Reserved
LDO7	3.3V	0.9V~3.5V	200mA	PE42, PE43, PF42	User Control
LDO8	3.3V			PAD42, PAD43, PAE43	User Control
LDO9	1.8V			PT42, PU42, PU43	User Control
LDO10	1.2V			PP42, PR42, PR43	User Control

Note: Reserved LDOs are not connected to external pads. LDO outputs can be controlled using I^2C (AP_PMIC_SCL/SDA)

PCB DESIGN GUIDE

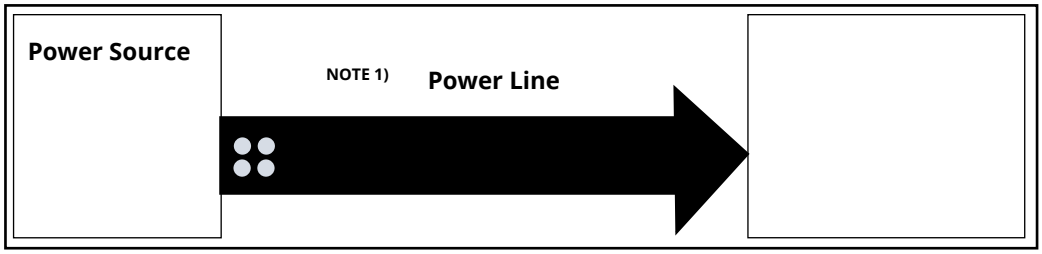

Figure 9. VBAT_MAIN Power Layout

Design Note:

1. Width of power line should be at least 80mil.
2. A via on each VBAT_MAIN pin is recommended.
3. Number of power vias on power source should be more than VBAT_MAIN power vias.

GENERAL PCB DESIGN GUIDELINES

GENERAL SPACING ON DIFFERENTIAL PAIRS

A general rule of thumb to properly layout differential pairs on the ARTIK 710 Module is given in *Figure 10* and *Figure 11*.

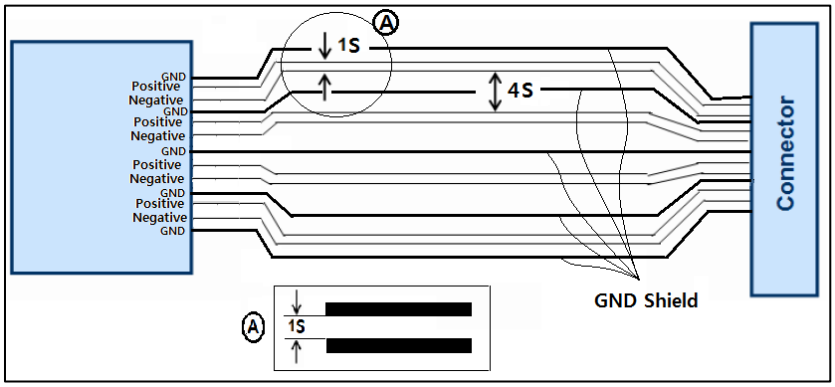

Figure 10. Physical separation between differential pairs should be adequate

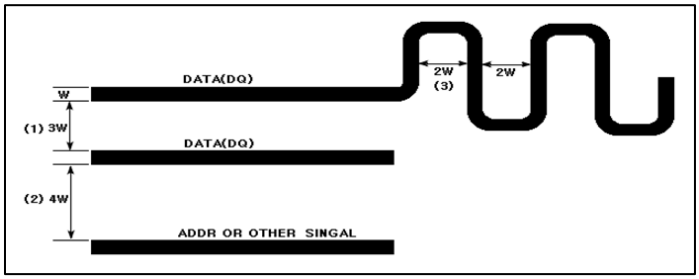

Figure 11. Spacing of Differential Pairs

SYMMETRICALLY ROUTING OF PASSIVE COMPONENTS

If passive components must be inserted into differential signal pairs, to match impedance, the best way to position them is as described in *Figure 12* and *Figure 13*.

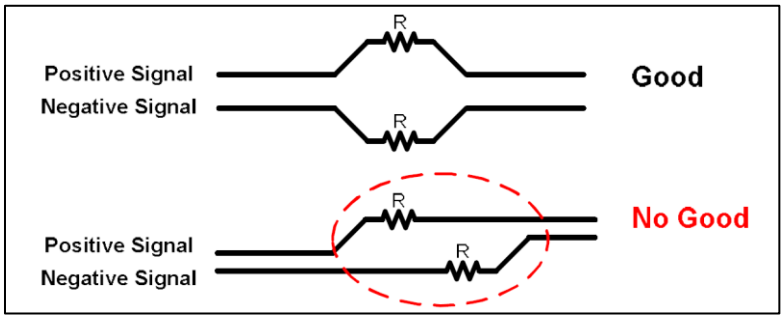

Figure 12. Symmetric Location of Passive Components

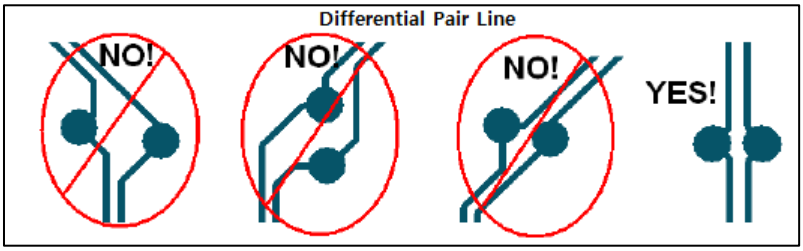

Figure 13. Symmetric Location of Passive Components

ROUTING A DIFFERENTIAL PAIR FROM MODULE TO DEVICE

When routing a differential pair from the module to the end device (connector) you need to make certain that the impedance is matched and as such the wiring needs to be as symmetrical as possible. *Figure 14* shows a variety of possible layouts from best to worst.

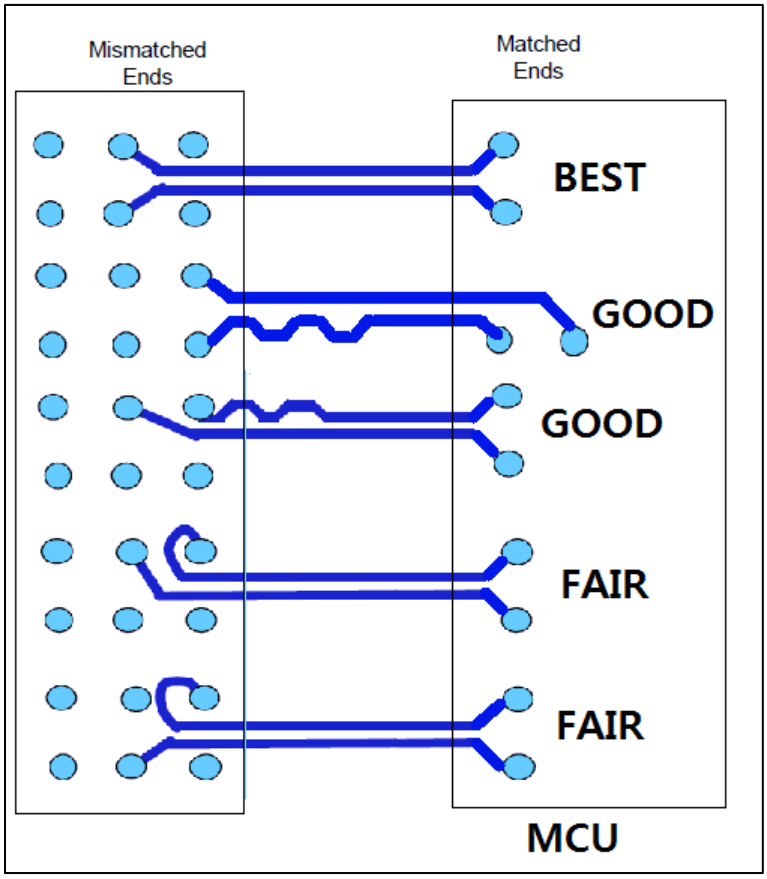

Figure 14. Differential Routing Suggestions

CHOOSING A PCB ARCHITECTURE

When cost is a concern, you might want to resort to a 6-Layer PCB as depicted in *Figure 15* versus an 8-Layer PCB design. When doing so it is best to route high speed Layer 3 and Layer 4 signal lines (LVDS type of signals) orthogonally to reduce the risk of cross talk and other interference patterns.

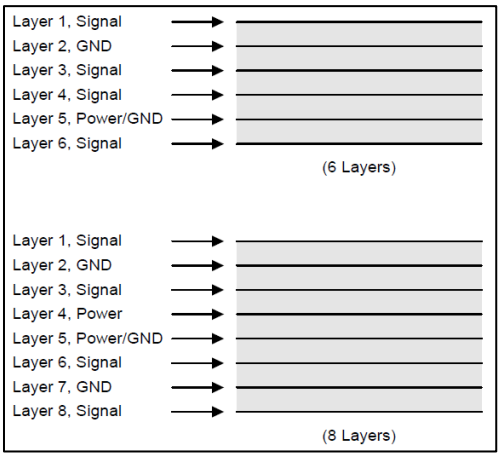

Figure 15. 6-Layer versus 8-Layer PCB

SD PCB Design Guidelines

Reference Schematic

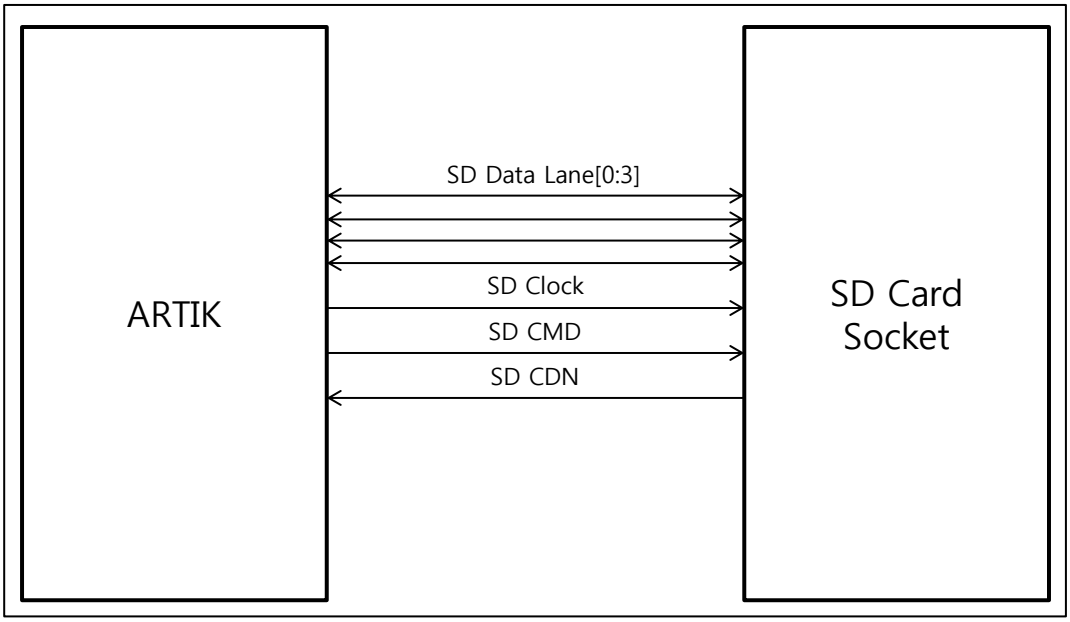

Figure 16. SD Reference Schematic

Note 1: To prevent ESD damage, it is recommended to attach a low capacitance ESD diode to each SD lane.
Note 2: To assure proper operation on the CDN (Card Detection Pin) pin, an always-on pull-up resistor is required.

PCB Design Guidelines

Table 6. PCB Design Guideline for SD

Layout	Comments	Parameter	Value
Length & Plane	Data and Clock signal length should be the same	Length Skew	±2mm

USB PCB Design Guidelines

Reference Schematic

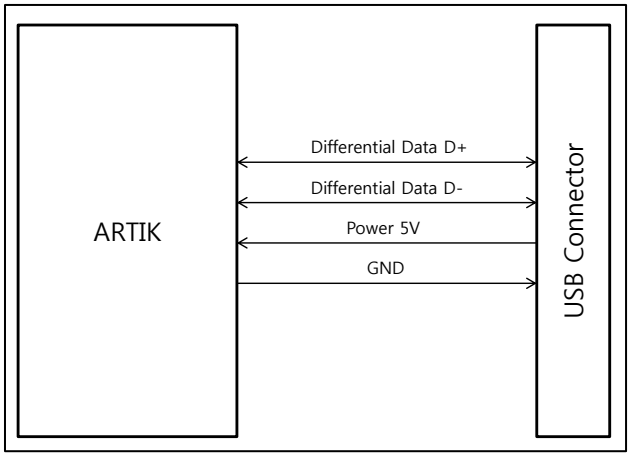

Figure 17. USB Reference Schematic

PCB Design Guidelines

Table 7. PCB Design Guideline for USB

Layout	Comments	Parameter	Value
Length & Plane	The line length of all USB related signal lines should be the same.	Length Skew	±0.25mm
	The pattern width and spacing is decided based on PCB stack-up information and 90Ω impedance matching.	Impedance Matching	90Ω±5% (Differential)
Spacing	In order to avoid interference with other high speed signals (ex : DDR3, USB device 2.0, X-tal, etc), please route the USB differential pairs as far away as possible.	Minimum Space	4S
GND Shield	Each differential pair should be shielded with GND.	GND Shield	Figure 18
Plane	Minimize vias for routing of the differential signal on the top layer as much as possible. In addition make sure that a GND (or VDD) layer in an undivided plane form is located below.	-	-
Via	Reduce the via hole count.	Maximum via Count	2

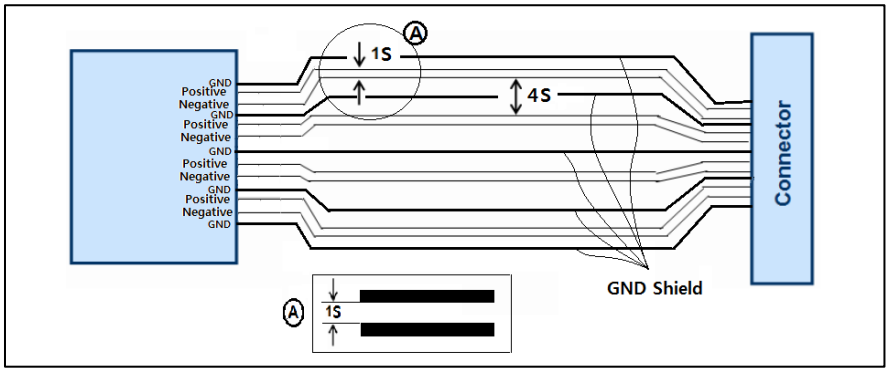

Figure 18. A differential signal pair should be adequately isolated from other differential pairs

HDMI PCB Design Guidelines

Reference Schematic

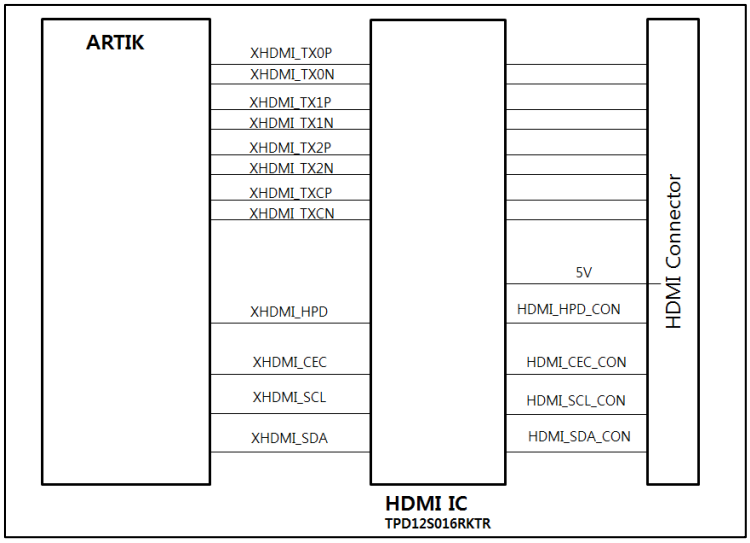

Figure 19. HDMI Reference Schematic

Note: Pull-up resistors are needed if the selected HDMI SoC does not have internal pull-ups.

PCB Design Guidelines

Table 8. PCB Design Guideline for HDMI

Layout	Comments	Value
Length & Plane	Impedance*	100Ω±5%
	Routing Length	Max 150mm
	Signal Separation (Coupled Line)	±0.3mm
	Signal Separation (Between each differential pair)	±0.3mm
Spacing	Spacing (Separation between other High speed signals)	4S
	Spacing (Separation between each differential pair signal)	4S
GND Shield	Each differential pair lines should be shielded with GND	
Via	The via hole count should be the same for all differential pairs	
	Reduce the via hole count	

Note: Pattern width and spacing is decided based on PCB stack-up information and a 100Ω impedance matching.
Note: Control signals are low speed and can adhere to a more cavalier routing scheme.

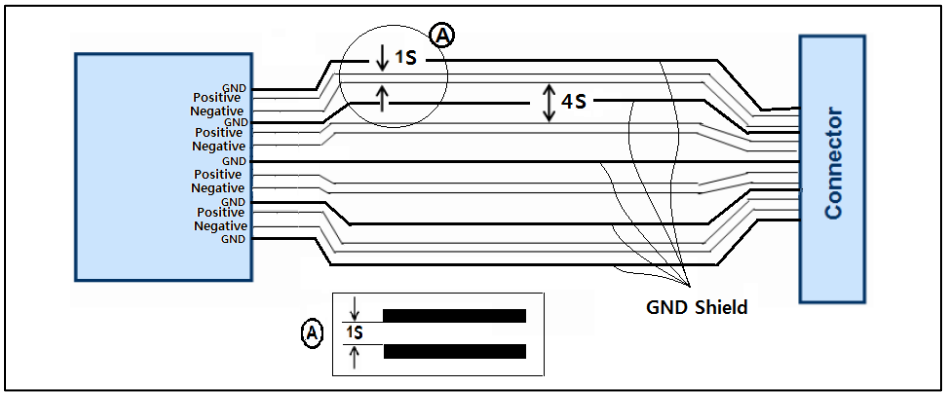

Figure 20. A differential signal pair should be adequately isolated from other differential pairs

LVDS PCB Design Guidelines

Reference Schematic

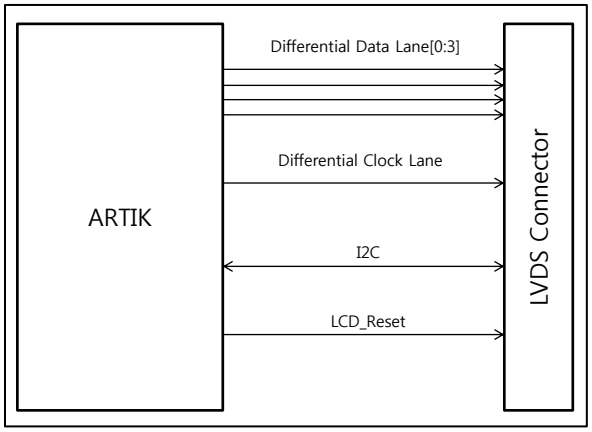

Figure 21. LVDS Reference Schematic

Note : Pattern width and spacing is decided based on PCB stack-up information and 100Ω impedance.

PCB Design Guidelines

Table 9. PCB Design Guideline for LVDS Differential Pairs

Layout	Comments	Parameter	Value
Length & Plane	The line length of all LVDS related signal lines should be the same.	Length Skew	±0.5mm
	The pattern width and spacing is decided based on PCB stack-up information and 100Ω impedance matching.	Impedance Matching	100Ω±5%
	Total length from the ARTIK 710 Module to device	Total Length	TBD
Spacing	In order to avoid interference with other high speed signals (ex : DDR3, USB device 2.0, X-tal, etc), please route the LVDS differential pairs as far away as possible.	Minimum Space	4S
	Minimum spacing to itself : 2S	Minimum Space	2S
	There should be sufficient spacing between each differential pair signals	Minimum Space	4S
GND Shield	Each differential pair should be shielded with GND	GND Shield	Figure 22
Via	Reduce the Via hole count	Maximum via count	2

Note: Control signals are low speed and can adhere to a more cavalier routing scheme.

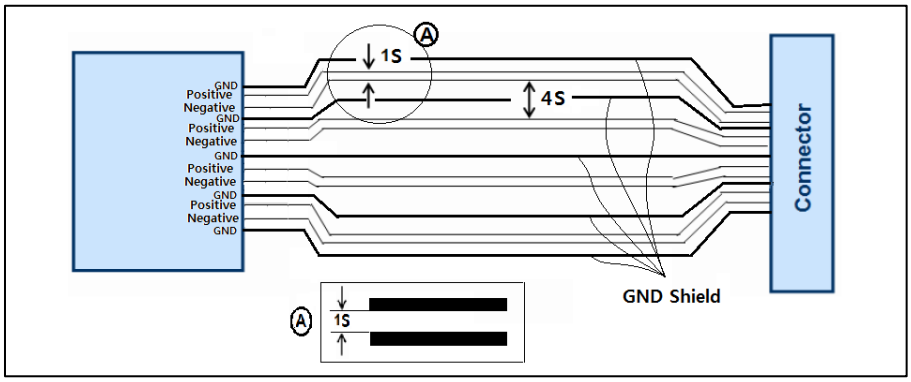

Figure 22. A differential signal pair should be adequately isolated from other differential pairs

MIPI PCB Design Guidelines

Reference Schematic

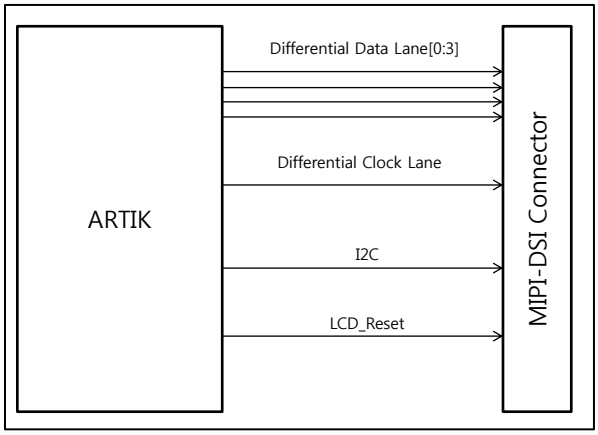

Figure 23. MIPI Reference Schematic

PCB Design Guidelines

Table 10. PCB Design Guidelines for MIPI Differential Pairs

Layout	Comments	Parameter	Value
Length & Plane	The line length of all MIPI related signal lines should be the same.	Length Skew	±0.5mm
	The pattern width and spacing is decided based on PCB stack-up information and 100Ω impedance matching.	Impedance Matching	100Ω±5%
	Total length from the ARTIK 710 Module to device	Total Length	TBD
Spacing	In order to avoid interference with other high speed signals (ex : DDR3, USB device 2.0, X-tal, etc), please route the MIPI differential pairs as far away as possible.	Minimum Space	4S
	Minimum spacing to itself : 2S	Minimum Space	2S
	There should be sufficient spacing between each differential pair signals	Minimum Space	4S
GND Shield	Each differential pair lines should be shielded with GND	GND Shield	Figure 24
Via	Reduce the Via hole count	Maximum via count	2

Note: Control signals such as I2C and LCD_Reset are low speed signals and can adhere to a more cavalier routing scheme.

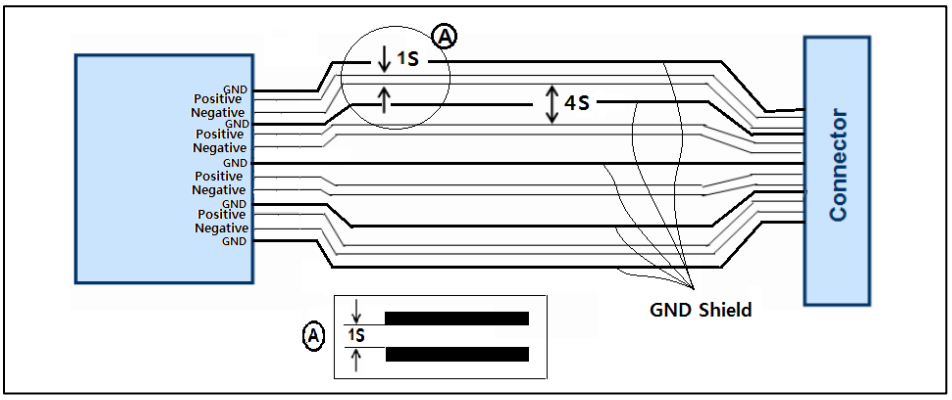

Figure 24. A differential signal pair should be adequately isolated from other differential pairs

GMAC PCB Design Guidelines

Reference Schematic

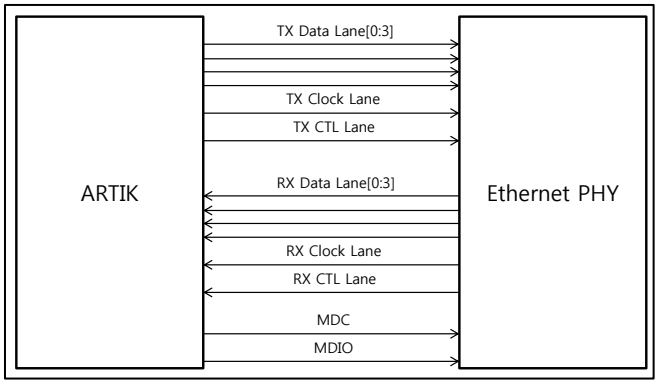

Figure 25. GMAC Reference Schematic

PCB Design Guidelines

Table 11. PCB Design Guidelines for GMAC

Layout	Comments	Parameter	Value
Length & Plane	Data and Clock signal length should be the same	Length Skew	±1mm

INTER CHIP COMMUNICATIONS PCB DESIGN GUIDELINES

REFERENCE SCHEMATIC (I²S, UART, SPI, I²C)

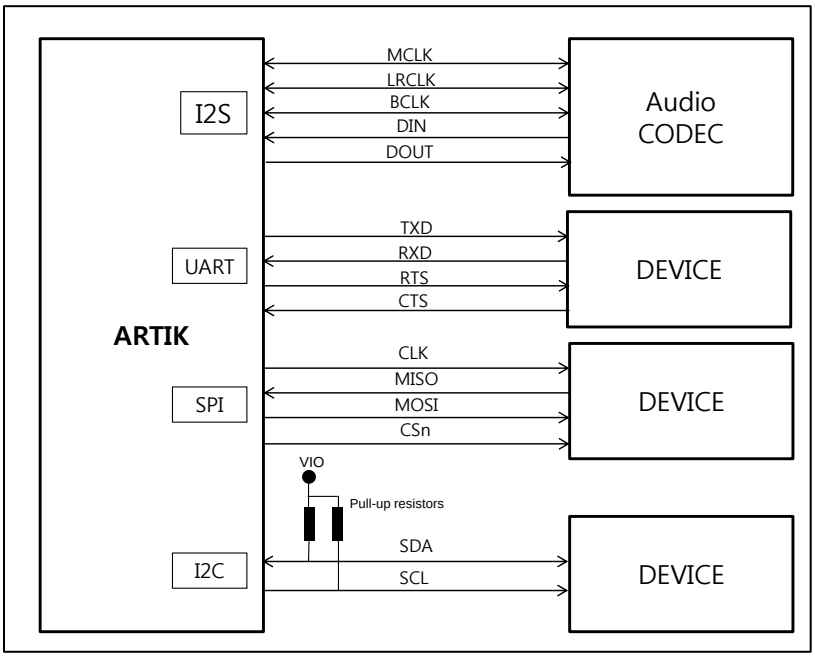

Figure 26. Inter Chip Communication Reference Schematic

PCB DESIGN GUIDELINES

Table 12. PCB Design Guidelines for Inter Chip Communication

IPs	Speed	Max Length (mm)	Length Skew (mm)	Swing Voltage (V)	Characteristic Impedance (Ω)	CL (pF)
HS-SPI	50MHz	300	30 (C-D)	3.3	50	-
HS-I2C	3.4Mbps	300	-	3.3	-	-

Note: C-D (Clock to Data)

GENERAL PURPOSE IO

SUSPEND MODE GUIDE

Table 13 shows the guidelines needed for proper suspend mode operation.

Table 13. Guidelines for Suspend Mode

GPIO State	External State	Suspend Guide		
		DIR	Drive	Pull-up/down
NC	-	Input	-	Enable
IN	Hi-Z	Input	-	Enable
	High/Low			Disable
OUT	Power off	Output	Low	Disable
	Power on		High/Low	Disable

INTERNAL PULL-UP/DOWN RESISTORS

An internal pull-up or pull-down resistor on each GPIO varies from 10KΩ to 50KΩ depending on its I/O type and its PVT (Process Voltage and Temperature) conditions.

Handling of Unused Pins

This chapter describes how to handle unused pins on the ARTIK 710 Module. NC (No Connect) can be handled as left floating.

The following groups are distinguished:

1. GPIO: Unused GPIO pins can be considered NC.
2. ADC: Unused ADC pins can be considered NC or can be connected to GND.
3. PWM: Unused PWM pins can be considered NC or can be connected to GND.
4. HDMI: Unused HDMI pins can be considered NC.
5. MIPI DPHY: Unused MIPI pins can be considered NC or can be connected to GND.

REFLOW PROFILE

TEMPERATURE PROFILE

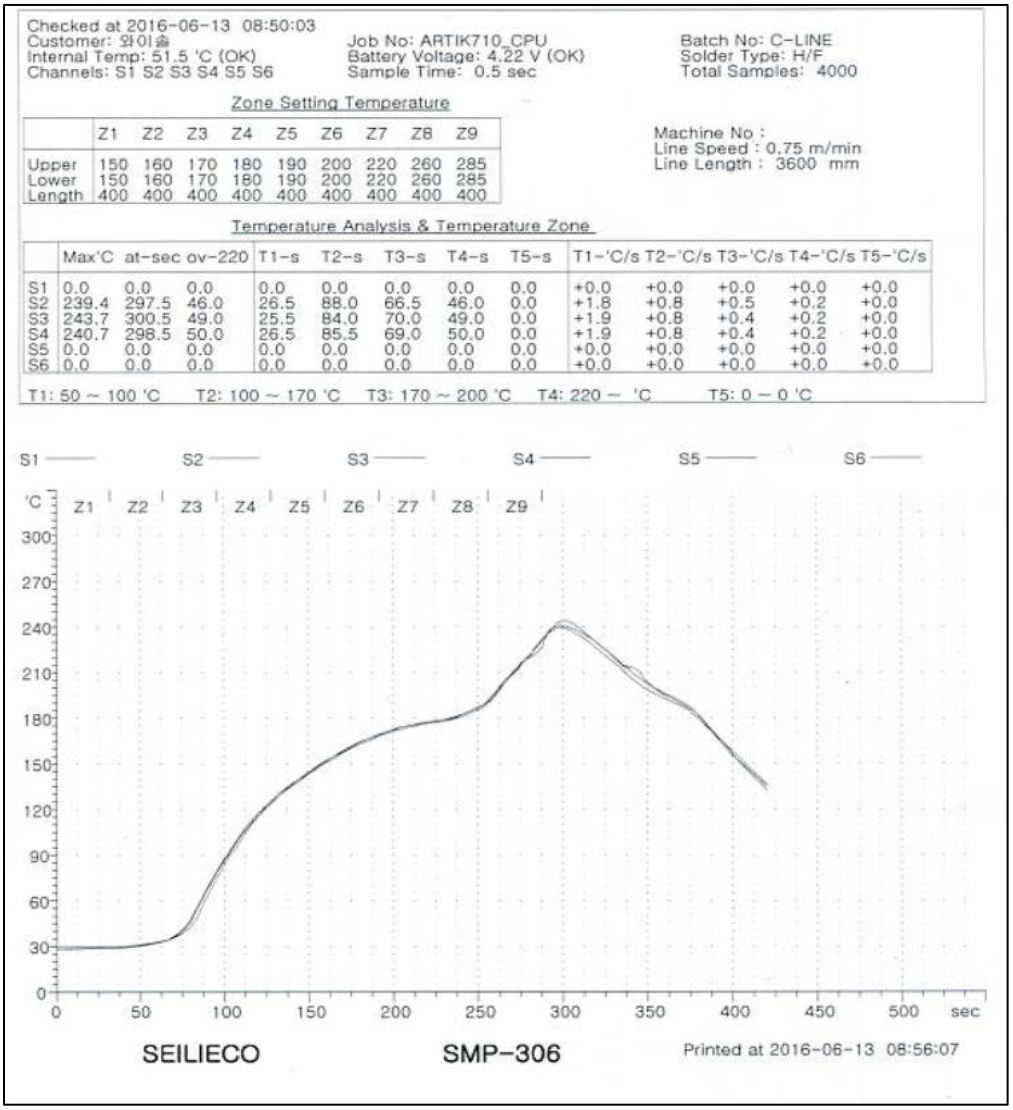

Figure 27. Reflow Temperature Profile

Table 14. Reflow Conditions

SPEC	Rising Temperature Condition	Pre-heating Condition	Reflow Condition	Peak
Temperature	50~100°C	100~170°C	Above 220°C	240°C
Tolerance	1~2°C/sec	60~100sec	30~50sec	±5°C

RECOMMENDED SOLDER PASTE

We recommend solder paste with the following properties:

1. Ingredient : Sn /Ag/ Cu
2. Particle size : 20~38um
3. Flux content : F11.5%

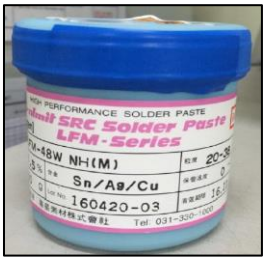

Figure 28. Recommended Solder Paste

Figure 28 shows a picture of the solder paste that we recommend. (Part Number: Hee LFM-48W NH(M) HF)

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