Digital Circuit Design

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Module 5

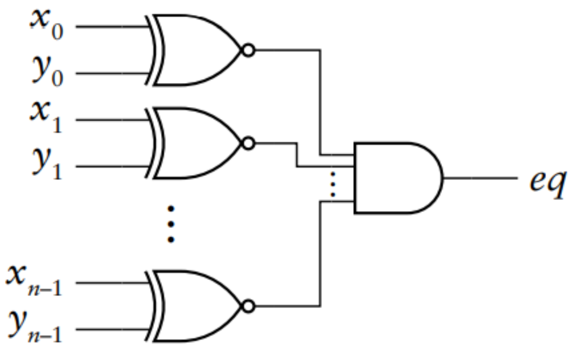
- Subtraction
- Two's complement
- Binary subtraction as addition
- https://www.edaplayground.com/x/bDf

Numer system rules

- In a base n system, n basic symbols or n digits are used.
- The value of a number is determined by the symbols and their positions within the description.
- For integers, the starting number (symbol) is zero (0).
- This class will initially focus on integer representations and not fractions.

Number comparison

- Equality x==y



x>y

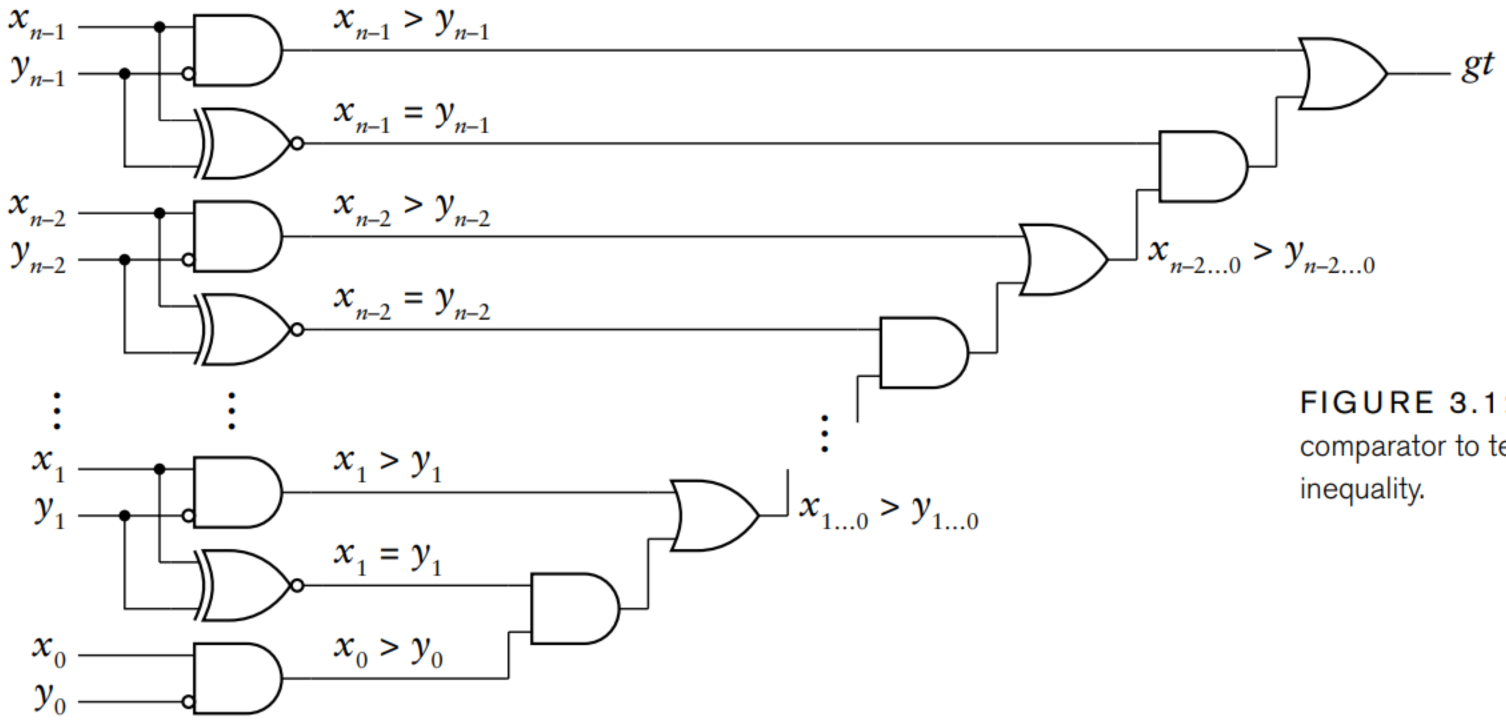


FIGURE 3.12 A magnitude comparator to test for greater than inequality.

Unsigned Number vs Signed number

- A n-bit Unsigned Number range is $(0, 2^n-1)$
- A n-bit signed Number range is $(-2^{(n-1)}, 2^{(n-1)}-1)$
- 2's complement: -x can be represented as ~x+1

Exercises

	0 0 0 0 0 0 0 0
72:	0 1 0 0 1 0 0 0
49:	0 0 1 1 0 0 0 1
121:	0 1 1 1 1 0 0 1

no overflow

	1 1 0 0 0 0 0 0
–63:	1 1 0 0 0 0 0 1
–32:	1 1 1 0 0 0 0 0
–95:	1 0 1 0 0 0 0 1

no overflow

	0 0 0 0 0 0 0 0
–42:	1 1 0 1 0 1 1 0
8:	0 0 0 0 1 0 0 0
–34:	1 1 0 1 1 1 1 0

no overflow

	0 1 0 0 1 0 0 0
72:	0 1 0 0 1 0 0 0
105:	0 1 1 0 1 0 0 1
	1 0 1 1 0 0 0 1

positive overflow

	1 0 0 0 0 0 0 0
–63:	1 1 0 0 0 0 0 1
–96:	1 0 1 0 0 0 0 0
	0 1 1 0 0 0 0 1

negative overflow

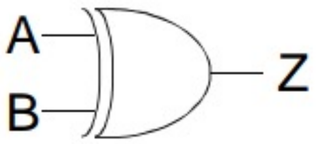
	1 1 1 1 1 0 0 0
42:	0 0 1 0 1 0 1 0
–8:	1 1 1 1 1 0 0 0
34:	0 0 1 0 0 0 1 0

no overflow

Signed Subtraction

$$x - y = x + (-y) = x + \overline{y} + 1$$

- Use a 2s-complement adder
  - Complement y and set $c_0 = 1$
- How to effectively complement y?

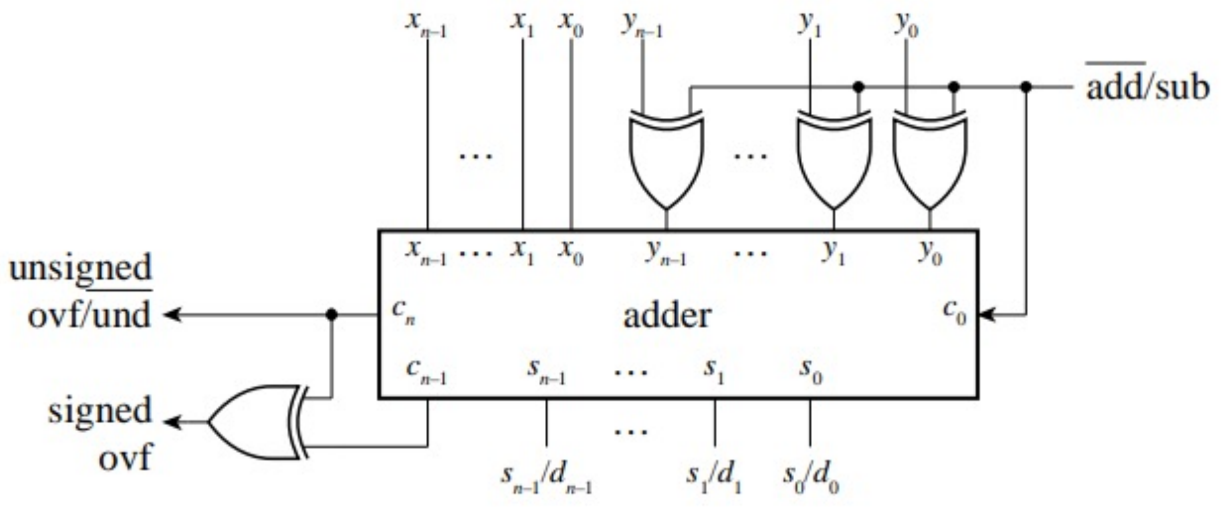


A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0

Add/Sub circuits

$$x - y = x + (-y) = x + \overline{y} + 1$$

- Use a 2s-complement adder
  - Complement y and set $c_0 = 1$



2's complement sign extension

- To extend a signed number from *n* bits to *m* bits:
  - add *m* – *n* bits to the msb side
  - fill the extra bits with the value of the original msb
- Examples 4 bits to 8 bits:

Number	4 bit				8 bit							
2	0	0	1	0	0	0	0	0	0	0	1	0
-2	1	1	1	0	1	1	1	1	1	1	1	0

Verilog using

- https://edaplayground.com/x/uuR5

- logic signed [7:0] test_sign_8