

The background features a dark, textured surface with numerous out-of-focus, warm-toned circular lights (bokeh) scattered across the upper half. A large, solid green shape, resembling a stylized leaf or a speech bubble, is positioned in the lower right quadrant. Inside this green shape, the title "Digital Circuit Design" is written in a white, elegant script font. Below the title, a thin white horizontal line is drawn.

Digital Circuit Design

Li Bai

Module 7

- Clock
- D flip-flop
 - Fix-point
 - Float-point
- Timing delays
 - Bit-wise multiplication
 - Shift operation (represent numbers as sum of multiple of 2^n)
 - Use multiplication IP core (block diagram instantiation)

Clock

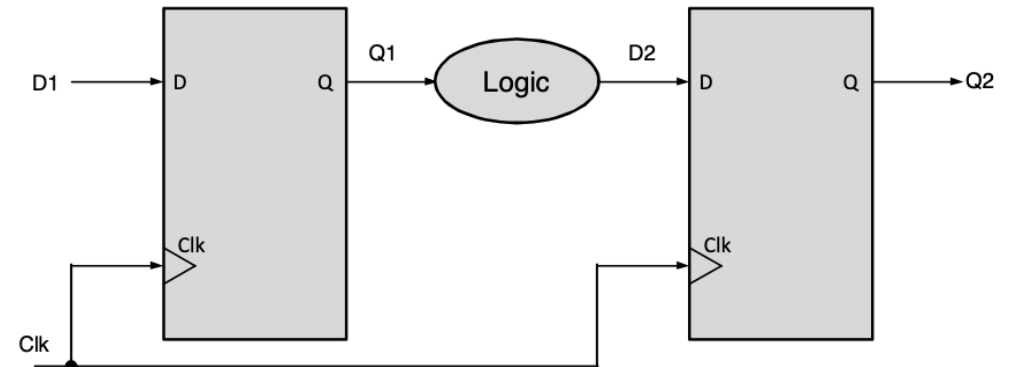
- Periodic signal, typically driving all sequential logic in a design. Some characteristics:
 - duty cycle
 - slew rate
 - rising edge, falling edge – high level, low level

$$SlewRate(S) = \frac{dV_0}{dt} = \frac{V_{0(90\%)} - V_{0(10\%)}}{t_{(90\%)} - t_{(10\%)}}$$



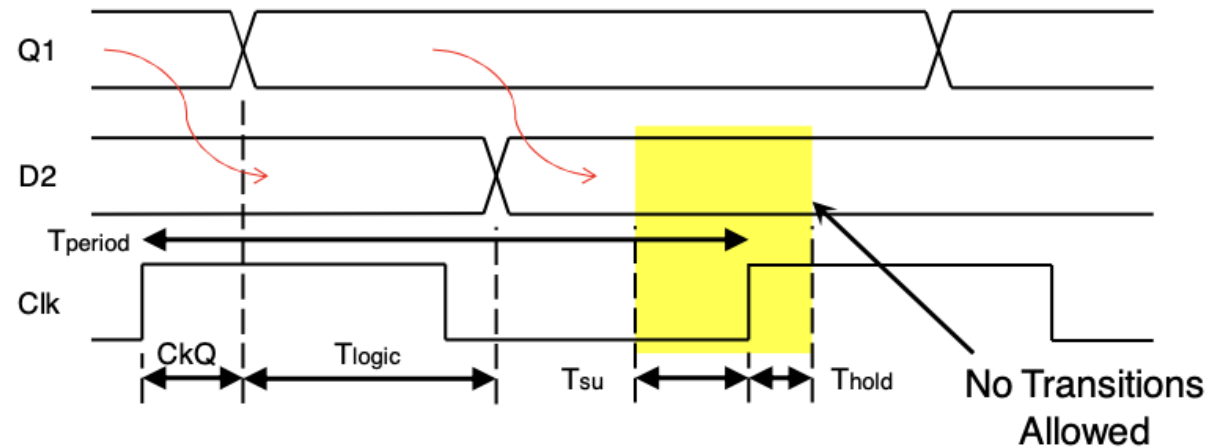
D Flip-Flop Specification

- Clock to Q – Time it takes after a clocking edge for the output Q to transition to a new state. There can be two different specifications – one for a positive transition for Q, and the other for a negative transition (not illustrated below).
- Setup time (before the clock changed, D1 has to maintain the same value)
- Hold time (after the clock changed, D1 cannot be changed)



Timing Analysis

- Setup Time Violation



Things work – as long as:

$$T_{period} > CkQ + T_{logic} + T_{su}$$

Failure is called a *Setup Time Violation*.