UWA ELEC5552

MEMS Testing Power Supply
Team 02

Author(s)
Liam Bettles (22815194)
Anders Christensen (22724462)
Nicholas Curwood-Wagner (22865518)
Pete Philip Paul (22702606)
Thomas Wilkinson (22239773)
Jason Zagari (21345828)

Final Report

Project Partners: Michal Zawierta, Australian National Fabrication Facility-WA
Dilusha Silva, Australian National Fabrication Facility-WA

UWA Supervisor: Hadi Afsharan

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Executive Summary

This report documents the comprehensive design, development, and testing of a digitally controlled PSU tailored for MEMS testing. The project was initiated in collaboration with the ANFF-WA and aims to meet specific technical and safety requirements for MEMS testing, including electrostatic actuation.

The power supply is designed to produce both DC and AC output voltages up to $200\,V$ and $200\,V_{RMS}$, respectively. It incorporates hardware interlocks for enhanced safety, fast output protection, and a user-friendly interface for easy programmability and computer-based control. The project has undergone rigorous testing to ensure it meets all technical specifications and safety protocols.

The design utilises a RPi MPU for digital control. User interaction is facilitated through a matrix keypad and visual feedback is provided via a display and LEDs. The project uses components that are readily available, ensuring sustainability and ease of replication.

The project successfully meets the majority of the initial requirements. It serves as a robust platform that can be further developed into a marketable product. For future versions, a formal approval process is suggested for industry compliance. Community briefings for user feedback and focused tenders on extending voltage and frequency ranges are recommended. Rigorous testing for long-term reliability and electromagnetic compatibility should also be established to enhance performance and market readiness.

1. Introduction

This report serves as the comprehensive documentation for a digitally controlled PSU, specifically tailored for Micro-Electromechanical Systems (MEMS) testing in association with the Australian National Fabrication Facility – WA node (ANFF-WA). Developed as part of the ELEC5552 course, the report covers the entire lifecycle of the project, from initial requirements to the final design. It aims to provide a thorough account of each stage, decision, and action taken, detailing the engineering principles, design methodologies, and validation processes employed.

1.1 Purpose

The primary aim of this document is to distinctly communicate the design journey and the rationale behind each decision made for the PSU. Serving as an integral part of the project's lifecycle, this report aims to provide a comprehensive overview from conceptualisation to implementation. It is intended to serve as a reference for stakeholders, including team members, instructors, and partners from the ANFF-WA. The report aims to provide them with a clear understanding of how the project progressed, the challenges faced, the solutions implemented, and how the final design meets and addresses the project's requirements and objectives.

1.2 Scope

This report provides a comprehensive review of the entire project, from its conceptualisation to its final implementation, focusing on the specific needs of MEMS testing in collaboration with the ANFF-WA.

Key aspects covered in this report include:

- Detailed design specifics for both DC and AC outputs tailored to meet the required criteria.
- In-depth analysis of safety protocols, including hardware interlocks, modulation controls, and protection mechanisms.
- A comprehensive look at the design requirements, their origins, and the steps taken to ensure they were addressed adequately.
- Discussion of project constraints, challenges encountered, and the corresponding solutions employed.

While the report aims to be exhaustive in its coverage of the project, it will not delve into the broader context of MEMS technology or the specific future applications of the power supply outside of intended use. These topics are considered outside the scope of this report.

1.3 Definitions, Acronyms, and Abbreviations

NOMENCLATURE:

Acronym/Abbreviation	Meaning
AC	Alternating Current
ADC	Analog to Digital Converter
ANFF-WA	Australian National Fabrication Facility
DC	Direct Current
DDS	Direct Digital Synthesis
DSI	Display Serial Interface
HV	High Voltage (>15V)
IC	Integrated Circuit
LED	Light Emitting Diode
LV	Low Voltage (0 to 5V)
MPU	Microprocessor
MEMS	Micro-Electromechanical System
MOSFET	Metal Oxide Silicon Effect Transistor
MV	Medium Voltage (5V to 15V)
NC	Normally Closed
NO	Normally Open
Op-amp	Operational Amplifier
PSU	Power Supply Unit
PWM	Pulse Width Modulation
RMS	Root Mean Square
RPi	Raspberry Pi
SFAIRP	So Far As Is Reasonably Practicable
SPDT	Single Pole Double Throw
TFT	Thin Film Transistor

DEFINITIONS:

Item	Definition
Micro-Electro-Mechanical Systems	A technology that integrates mechanical elements, sensors, actuators, and electronics on a common silicon substrate.
Australian National Fabrication Facility – Western Australia Node	A national network providing academia and industry with access to state-of-the-art fabrication facilities.
Hardware Interlock	A safety mechanism that prevents the system from operating under certain conditions to protect both the user and the system.
Modulation	The process of varying one or more properties of a periodic waveform, called the carrier signal, with a separate signal that contains information to be transmitted.

1.4 Background to the Project

This project was initiated in partnership with the ANFF-WA to address a critical need in the field of MEMS testing. MEMS technology has a wide array of applications, from medical devices to automotive sensors, and requires specialised power supplies for testing. The ANFF-WA sought a digitally controlled power supply capable of meeting specific technical and safety requirements for MEMS testing, including electrostatic actuation.

The project aims to deliver a power supply that not only meets these technical specifications but also adheres to safety protocols. Initial testing will be limited to $30V$, and any testing above this voltage will only occur under academic supervision. The project outcomes will be shared with ANFF-WA in the form of a GitHub repository containing all documentation and designs, under an open-source/open hardware license.

1.5 Responsibilities & Member Contribution

Member	Role	Contribution & Responsibilities
Liam Bettles	Project Administrator	Signal Modulation Design Architecture Stakeholder Engagement Ethical Considerations Final Costs of Design Software
Anders Christensen	Q/A Manager	Software & Code Display Overarching System & Subsystem Code Physical Interface System Testing System Building User Manual
Nicholas Curwood-Wagner	Client Liaison Manager	HV Amplification System Testing System Building Safety Issues Identification & Resolution System Troubleshooting System Demonstration
Pete Philip Paul	Project Controller	System Integration Overcurrent Protection Testing Procedures Risks & Mitigations Overcurrent Protection
Thomas Wilkinson	Q/A Manager	PCB Design Schematic Design Signal Generation System Testing System Building Process of Assembly Final Requirements Case Design Schematic Design
Jason Zagari	Project Configuration Manager	Report Formatting & Layout Interlock Design Design Outputs IO Register User Manual Final Requirements Software & Code Signal Generation

1.6 Report Summary

I. Final Requirements:
The report begins by highlighting the final set of requirements that guided the design process. These requirements are framed against client specifications, regulatory standards, and safety considerations.

II. Design Philosophy:
Following the requirements, the design philosophy of the project is presented. This section provides the rationale behind key design decisions, including component selection and system architecture.

III. High-Level Design Architecture:
The next section outlines the high-level architecture of the MEMS Testing Power Supply, breaking down the system into its major functional elements. Key design decisions are highlighted to provide a comprehensive understanding of the system's structure.

IV. Detailed Design Elements:
Each functional element of the design is then explored in detail. This includes circuit justifications, component selections, and how each element meets specific requirements and aligns with the overall design philosophy.

V. System Integration:
This section discusses how the MEMS Testing Power Supply is integrated as a complete system, detailing the interactions between various functional elements.

VI. Stakeholder Engagement:
Key stakeholder inputs, including client feedback and regulatory considerations, are highlighted to provide further validation for the proposed design.

VII. Risks, Safety, and Ethical Considerations:
The report then delves into the manufacturing method, safety issues, key risks and their mitigations, and ethical considerations related to the design.

VIII. Design Outputs and Final Costs:
Schematics, code snippets, component registers, and other key design outputs are provided. This section also includes a detailed cost breakdown of the project.

IX. Recommendations for Future Work:
The report concludes with recommendations for future works, including necessary approvals, potential tenders, and tests to be conducted for further refinement of the design.

IX. Final Design Implementation:
The final section shows functional proof of the built prototype including requirement and functional testing.

2. Final Design & Design Process

2.1 Project Requirements

The final set of requirements for the MEMS testing power supply project has undergone rigorous evaluation and prioritisation. The requirements are categorised based on their criticality to safety, functional importance, and stakeholder significance. The priority levels range from "Low" to "Safety Critical" with the description for each seen in the subsequent table (Table 2-1)

Table 2-1 Priority Rating & Description

Priority Categories	Priority Description
Safety Critical	Any requirement that **creates a hazard** if it is not met.
Critical	Any requirement that is key to achieving the functional requirements and must be included for a successful design delivery to occur
High	Any requirement that is key to achieving the required functionalities and must be included for client satisfaction
Medium	Any requirement that is ***not*** key to achieving the functional requirements of the design and is considered **high** importance to client satisfaction.
Low	Any requirement that is ***not*** key to the functional requirements of the design and is considered **low** importance to client satisfaction.

The ranking is calculated using a formula that considers whether the requirement is critical to safety, its functional rating, and its stakeholder rating. If a requirement is deemed critical to safety, it automatically receives the highest priority level of "Safety Critical".

The functional rating scale (1-5) assesses the impact of each requirement on the design's functionality, while the stakeholder rating scale (1-5) gauges the requirement's importance to key stakeholders. These ratings are summed to determine the final priority level for each requirement, unless it is critical to safety, in which case it is automatically classified as "Safety Critical."

Table 2-2 Priority Weightings

Stakeholder Rating (1-5)
1: This requirement does not benefit any stakeholders
2: This requirement has slight benefit to some stakeholders
3: This requirement has major benefit to some stakeholders OR slight benefit to important stakeholders
4: This requirement has major benefit to important stakeholders
5: This requirement has been specifically listed by important stakeholders
Functional Rating (1-5)
1: This requirement does not affect the functionality of the design
2: This requirement may affect the functionality of the design
3: This requirement will affect the functionality of the design
4: This requirement is critical to the functionality of the design
5: This requirement is critical to the functionality of the design & successful design delivery
Critical to Safety
Yes: Not meeting this requirement will create a hazard to person/s
No: Not meeting this requirement will not create any hazard

The subsequent table, Table 2-3, lists the finalised requirements in order of their calculated priority, providing a comprehensive view for project execution and stakeholder communication.

Table 2-3: Final Requirements (REQ), Prioritised

ID	Requirement Description	Priority
REQ-001	The design shall produce a DC output voltage of $0 - 200V$	Safety Critical
REQ-002	The design shall produce a DC output voltage that is hardware interlock limited to 100V	Safety Critical
REQ-003	The design shall produce an AC output voltage of $0 - 200V_{rms}$	Safety Critical
REQ-004	The design shall produce an AC output voltage with hardware interlock limiting it to $50V_{rms}$.	Safety Critical
REQ-005	The design shall produce a maximum output current of $10mA$	Safety Critical
REQ-006	The design shall have an adjustable output maximum current cutoff/trip limit tuneable in the range of $1 - 10mA$.	Safety Critical
REQ-007	The design shall protect the output from overcurrent by switching off the output in under 10 milliseconds.	Safety Critical
REQ-008	The design shall include a suitable, sealed case for safe handling.	Safety Critical
REQ-009	The design shall include a suitable case of a self-extinguishing material.	Safety Critical
REQ-010	The design shall undergo preliminary testing with output voltages not exceeding $30V$ (peak) for both DC and AC.	Safety Critical

REQ-011	The design shall comply with all relevant legal and regulatory requirements.	Safety Critical
REQ-012	The design shall consist of a visual indication light to show when the interlock is engaged or disengaged.	Safety Critical
REQ-013	The design shall utilise a computer or microcontroller.	Critical
REQ-014	The design shall utilise a physical interface to take in user inputs.	Critical
REQ-015	The design shall produce an AC output frequency of $50 - 300kHz$ sine wave.	Critical
REQ-016	The design shall produce a switchable output 100% amplitude modulated signal with a square wave signal for AC & DC outputs.	Critical
REQ-017	The design output connection shall be a BNC or high-voltage BNC.	Critical
REQ-018	The design shall have one output channel.	Critical
REQ-019	The design shall utilise a combination of a display and LEDs to indicate the status of the device.	High
REQ-020	The design shall allow for output voltage adjustments with steps of $0.05V$ or less over full range of voltages.	High
REQ-021	The design shall allow for output frequency adjustments with steps of $10kHz$ for the carrier frequency.	High
REQ-022	The design shall allow for current limit adjustments with steps of $2mA$.	High
REQ-023	The design shall produce a square wave signal with frequency range of 10-100Hz.	High
REQ-024	The design shall source input power from an external power supply adapter.	High
REQ-025	The output type (DC/AC), voltage, modulation (ON/OFF) and output enable shall all be controlled via a digital input.	High
REQ-026	The design shall minimise the voltage ripple as much as possible.	High
REQ-027	The design shall allow for output frequency adjustment with steps of 10 Hz for the square wave.	High
REQ-028	The design shall accept nominal input voltages in the range of $5 - 30\ V_{DC}$.	High
REQ-029	The design shall include a suitable case that allows for programming and computer-based control without disassembly.	Medium
REQ-030	All design files shall be uploaded to a Git repository with an open source / open hardware license for the project partner and other researchers.	Medium
REQ-031	The prototyping activities shall not exceed $350 for reimbursement purposes.	Medium
REQ-032	The design shall utilise components that are available in sufficient supply.	Medium
REQ-033	The design shall operate nominally in room temperature conditions.	Medium
REQ-034	The design shall have an expected lifetime of approximately 10 years.	Medium

REQ-035	The design shall be implemented on a PCB or protoboard if time constrained.	Medium
REQ-036	The design shall minimise electromagnetic interference produced as far as is practicable.	Medium
REQ-037	The design's size and weight shall be as low as possible.	Low
REQ-038	Frequency distortion of the sine wave shall be ≤ 2%	Medium
REQ-039	Step voltage ripple should be at least 10x smaller than the minimum step size ($5mV$)	Medium

2.2 Design Philosophy

2.2.1 Functional Philosophy

The architecture of the power supply system is designed to meet and exceed the "Safety Critical" and "Critical" requirements, as these are vital for functional success. Specifically, requirements REQ-001 to REQ-012 are pivotal, as they both possess the highest functional rating. These requirements dictate the output voltage and current specifications, making them non-negotiable for the system's functionality.

2.2.2 Safety Philosophy

Every "Safety Critical" requirement, such as REQ-001 to REQ-012, which involve voltage and current limitations, have been carefully addressed to ensure fail-safe operation. For example, hardware interlocks (REQ-002 and REQ-004) are implemented to limit the DC and AC output voltages, thereby minimising the risk of electrical hazards.

2.2.3 Component Selection Philosophy

The components for the design were selected based on a multi-faceted approach that aligns with the project's critical and high-priority requirements. Similarly, components were chosen to meet the adjustable output maximum current cutoff/trip limit (REQ-006) and to protect the output from overcurrent within 10 milliseconds (REQ-007). Additionally, the availability of components (REQ-032) was considered to ensure that the design could be easily replicated or scaled in the future. This philosophy ensures that each component not only meets the functional requirements but also contributes to the overall reliability and longevity of the system, as stipulated by REQ-034. Furthermore, the limited project budget specified in REQ-031 led to an additional factor of component selection for cost-effectiveness.

2.2.4 MPU and Modulation Philosophy

The use of a MPU in the design (REQ-013) serves multiple purposes, including but not limited to, control of output types (REQ-025), frequency adjustments (REQ-021, REQ-027), and current limit adjustments (REQ-022). The MPU allows for a more dynamic and flexible system, capable of real-time adjustments and monitoring. The modulation features, specifically the switchable 100% amplitude modulated signal for AC & DC outputs (REQ-016), were incorporated to offer a broader range of applications for the device. The MPU setup also manages the user interface of the device. As stipulated in REQ-019, the design has incorporated the combination of a display and LEDs to provide real-time status updates and operational feedback to the user.

2.2.5 Voltage and Current Control Philosophy

The use of a MPU in the design (REQ-013) serves multiple purposes, including but not limited to, control of output types (REQ-025), frequency adjustments (REQ-021, REQ-027), and current limit adjustments (REQ-022). The MPU allows for a more dynamic and flexible system, capable of real-time adjustments and monitoring. The modulation features, specifically the switchable 100% amplitude modulated signal for AC & DC outputs (REQ-016), were incorporated to offer a broader range of applications for the device. This aligns with the high-priority requirements and ensures that the design is not only functional but also versatile.

2.3 Overview of the Design Architecture

A high-level architectural design is presented in Figure 2-1 below. The figure illustrates the functionality of how the design is intended to work. See Appendix A – System Architecture for a detailed view of the below diagram.

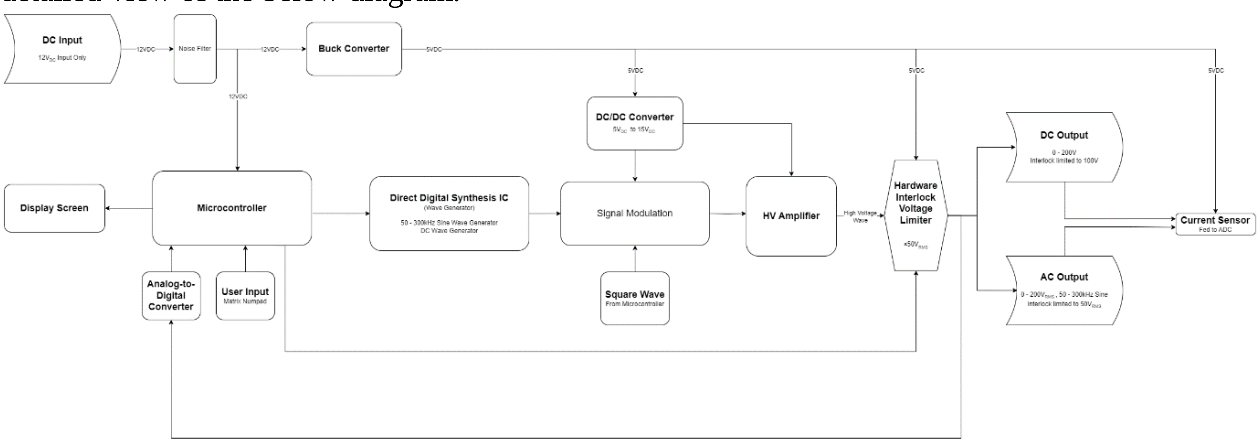

Figure 2-1: Design Architecture Overview

2.3.1 Power Supply and Conversion

The architecture incorporates a DC input of $12\ V$, aligned with the project brief's preference (REQ-028). This input undergoes noise filtering to ensure a cleaner power supply voltage. This filtered $12V$ supply is then converted to two $5V$ buses via a buck converter. This $5V$ bus serves multiple purposes, including powering the hardware interlock and the current sensor.

The $5V$ bus also feeds a $5V$ to $15V$ DC/DC converter, which provides the necessary voltage levels for signal modulation and the HV amplifier. This design choice is in line with the functionality philosophy, ensuring that the system can produce both AC and DC outputs at varying voltage levels (REQ-001, REQ-003).

2.3.2 MPU and User Interface

The system employs a MPU to manage various functionalities, fulfilling REQ-013 which mandates the use of a computer or microcontroller. The MPU is directly connected to a display screen and user input mechanisms, satisfying REQ-014 and REQ-019, which call for a physical interface for user inputs and a combination of display and LEDs for device status indication. The MPU is responsible for interfacing with the DDS IC, the hardware interlock system, digital potentiometers, and all other ICs that possess digital control.

2.3.3 Signal Generation and Modulation

A DDS IC chip is utilised for generating a wide range of frequencies. This component is essential for meeting REQ-015, which specify the frequency ranges for AC. The DDS IC chip is controlled by the MPU, aligning with the microcontroller and modulation philosophy that stresses the importance of precise, programmable control over signal generation. The signal modulation block represents the modulation IC which analogue multiplies the two incoming signals: the high frequency carrier, and the low frequency square wave from the MPU. This design element is pivotal for fulfilling REQ-016, which calls for a switchable output with 100% amplitude modulation for both AC and DC outputs. The output of the signal modulator feeds into the HV amplifier, which boosts the waveform amplitude to satisfy REQ-001 and REQ-003.

2.3.4 Safety and Output

The architecture incorporates a hardware interlock system connected to both the DC and AC outputs, fulfilling the safety-critical requirements of REQ-002 and REQ-004. These requirements specify hardware interlock limitations for DC and AC output voltages, ensuring that they do not exceed $100V$ and $50V_{rms}$, respectively. The hardware interlock is also connected to an ADC, which provides an additional layer of safety by monitoring the output parameters in real-time.

The current sensor is directly linked to the ADC and the MPU, in alignment with REQ-007, which mandates protection from overcurrent by switching off the output in under 10 milliseconds. The design also incorporates a visual indication light to show when the interlock is engaged or disengaged as per REQ-012.

The architecture also includes a sealed case made of self-extinguishing material, adhering to REQ-008 and REQ-009. These requirements are in line with the safety philosophy that emphasises robust physical protection and hazard mitigation.

The DC and AC outputs are designed to be separate but are both connected to the current sensor. This design choice follows REQ-018, which specifies a single output channel, and it aligns with the critical function philosophy that prioritises safety and reliability in output delivery.

2.4 Final design elements

2.4.1 DC Input & Filtering

2.4.1.1 Overview

The input power of the design is sourced from an external power adapter via a DC 2-pin barrel jack, to fulfill REQ-024. $12V_{DC}$ was chosen as the design input voltage as it provided an easier middle ground to buck and boost to other required voltage levels in the PSU design, such as $3.3V$, $5V$, $\pm 15V$ and $\pm 175V$. Furthermore, $12V_{DC}$ is a commonly accepted input voltage for buck/boost ICs in general, making part selection easier as well. This voltage level satisfies REQ-028.

Since the power source is external to the device, certain precautions must be taken to ensure that the input is stable and safe for the device to accept. One such precaution is to filter the input voltage to ensure a cleaner, stable voltage level close to the ideal $12V$. Common practice in electronics design is to use a decoupling capacitor close to the input pins, one pin connected to each of the DC barrel jack pins. This allows any incoming noise energy from the power input cable to be shunted through the capacitor. A comparatively large capacitance, and thus large noise energy absorption, $100\mu F$ high quality Panasonic capacitor was implemented in the design, as shown in Figure 2-2.

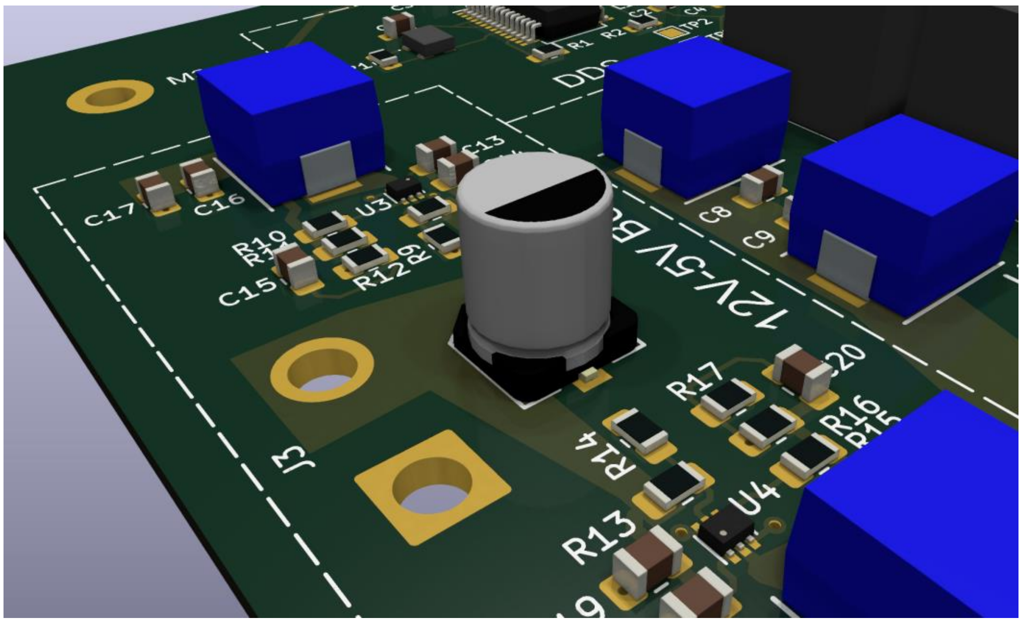

Figure 2-2: PCB render showing the decoupling capacitor located close to the 12V input connection point (J3)

2.4.1.2 Requirements Met

The design utilises an external power adapter with a $12V_{DC}$ input, meeting REQ-024 by sourcing its power externally and fulfilling REQ-028 by selecting a commonly accepted voltage level for buck/boost ICs.

2.4.2 Voltage Sources

2.4.2.1 Overview

The various electronics involved in the design are intended to operate at different voltage levels. A summary of the components at each voltage level is presented in Table 2-4. To facilitate these 5 voltage levels, various voltage sources have been implemented or sourced externally. $12V$ is sourced from the incoming DC line, as discussed in Section 2.4.1.

Table 2-4: Components and their associated supply voltages

Voltage	ICs / Components
$+3.3V$	DDS, DDS Crystal Oscillator, ADC, Digital Potentiometer Logic Supply
$+5V$	RPi, $\pm 15V$ Boost Converters, Current Sensor, Interlock Relay Coils
$+12V$	$+5V$ Buck Converters, Enclosure Fan
$\pm 15V$	Digital Potentiometer Power Supply, Modulator, LV Amplifier
$\pm 175V$	HV Amplifier

2.4.2.2 $+3.3\ V$ Source

The $+3.3\ V$ voltage level is sourced from the RPi's onboard $5V$ to $3.3V$ linear regulator IC. The maximum current draw from all of the connected ICs / components was found to be within safe margins of this regulator, and so the $3.3V$ pin from the RPi ribbon cable is used as a voltage source on the PCB.

2.4.2.3 $+5\ V$ Source

The $+5\ V$ voltage level is provided by two separate buck converter source circuits, both of which are supplied from the $+12V$ input. The buck converter source circuit is shown in Figure 2-3 and was designed using Texas Instrument's WEBENCH DC/DC Power Designer [1] to ensure correctly specified passive components were designed for the TPS564257DRL [2] buck converter IC.

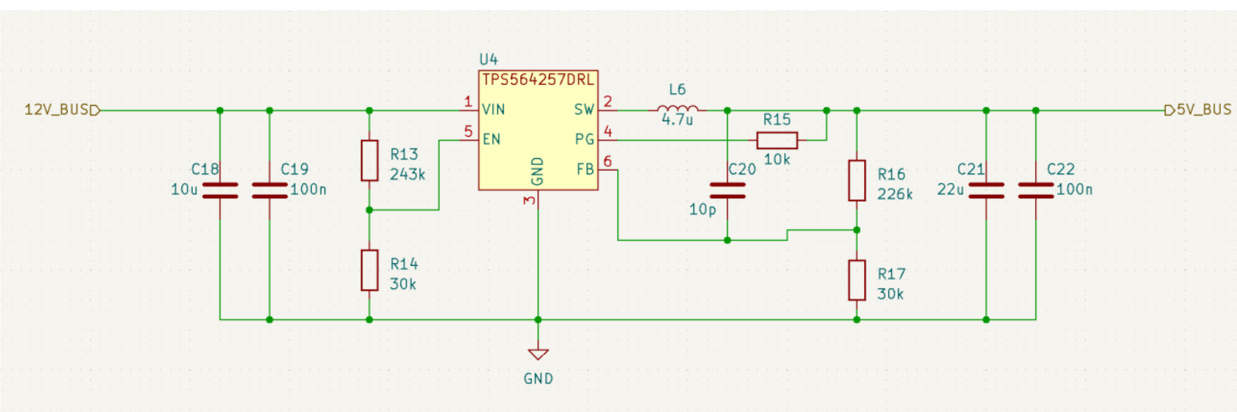

Figure 2-3: $12V$ to $5V$ Switching Regulator Buck Converter Circuit

One of these buck converter circuits is used to exclusively power the RPi, since it sinks $2.5A$ of current by itself, taking up a majority of the $4A$ capacity of this source circuit. The other buck converter circuit, contained in the 'Peripheral $5V$ Regulator' subsystem, is used to power the rest of the $+5V$ components mentioned in Table 2-4.

2.4.2.4 $\pm 15V$ Source

The digital potentiometer's power supply, modulator IC, and the LV amplifier all require positive and negative $15V$ voltage sources to allow them to accept and modify the bipolar sinusoidal signal. Two of the Murata CRE1S0515SC isolated DC-DC converters are used to convert the peripheral $5\,V$ regulated supply into positive and negative $15V$ voltage sources. The negative voltage is created by connecting the positive output pin of one of the converter ICs to common PCB ground, thus making the negative output pin $-15V$. This is also made possible due to the input-output isolation of the converter IC.

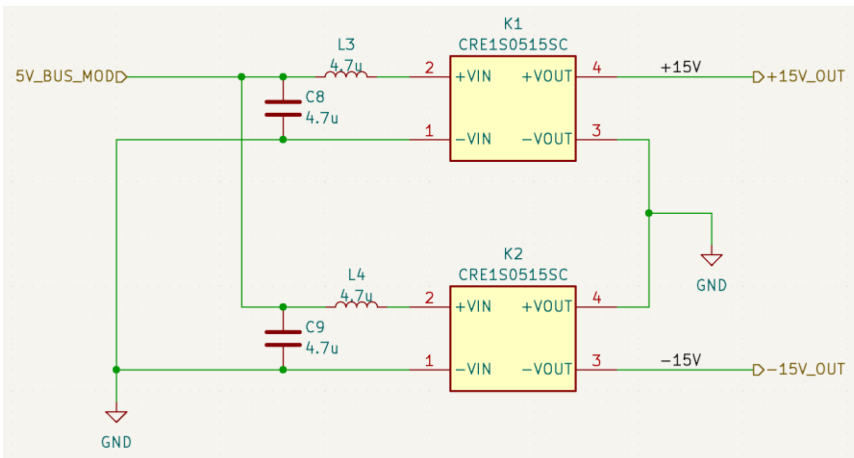

Figure 2-4: $5V$ to $\pm 15V$ Boost Converter Circuits

2.4.2.5 $\pm 175V$ Source

The $\pm 175V$ voltage levels required for the HV op-amp were found to be too costly to implement on the PCB. Due to this reason, the design decision was made early on to source cheaper boost converter daughterboards to provide these voltage levels, connected to the SMD HV op-amp via solder contacts on the PCB. These contact pads are shown in Figure 2-5. The external power supply was selected to be the SODIAL boost converter [3].

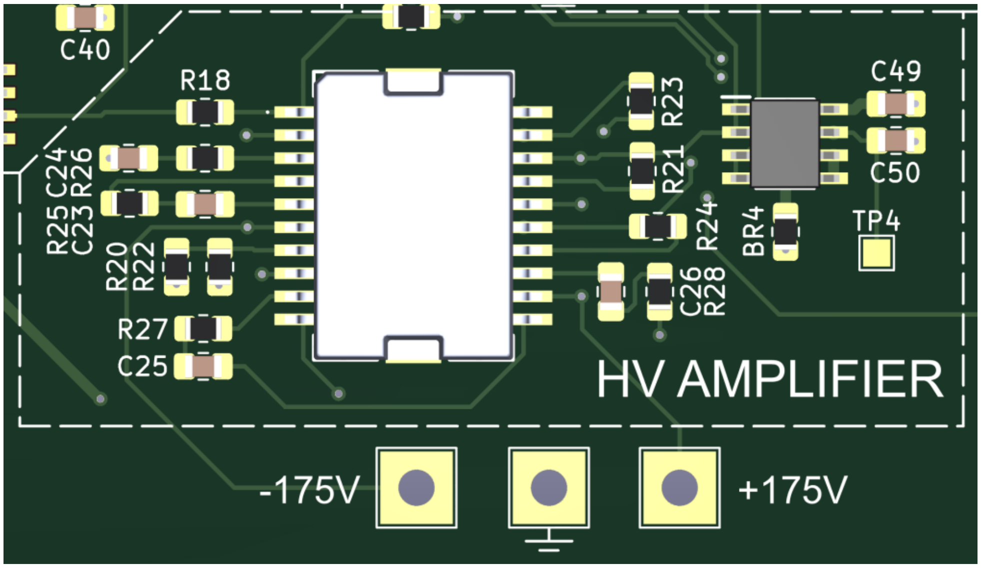

Figure 2-5: Contact pads (bottom) for connecting the external $\pm 175V$ voltage sources to the power op-amp (centre)

2.4.3 Signal Generation

2.4.3.1 Explanation

The signal generation circuit's purpose is to create the sinusoidal, or constant waveforms for AC & DC operating modes of the PSU, respectively. The system architecture outlined in Figure 2-1 provided the direction for signal generation, as research had shown that low peak-to-peak voltage signal generation ICs are easier to source than pre-amplified higher peak-to-peak voltage ICs. As per this direction, an Analog Devices AD9850 [4] DDS chip was selected. The chip is capable of generating sinusoidal, DC, sawtooth, and triangular waveforms, at frequencies up to $\sim 30MHz$ depending on the crystal oscillator's frequency that is paired with the IC, thus meeting REQ-015. Furthermore, the AD9850's high precision 32-bit frequency tuning word means that with the implemented $100MHz$ clock signal, an output frequency resolution of $0.03675Hz$ is possible. This is magnitudes more accurate than the required $10kHz$ steps, thus meeting REQ-021. Beside it meeting the specifications, the IC is also comparatively affordable at $56/piece and is consequently well documented online with many example schematics available. Based off these schematics, the signal generation DDS subsystem schematic was developed, as shown in Figure 2-6.

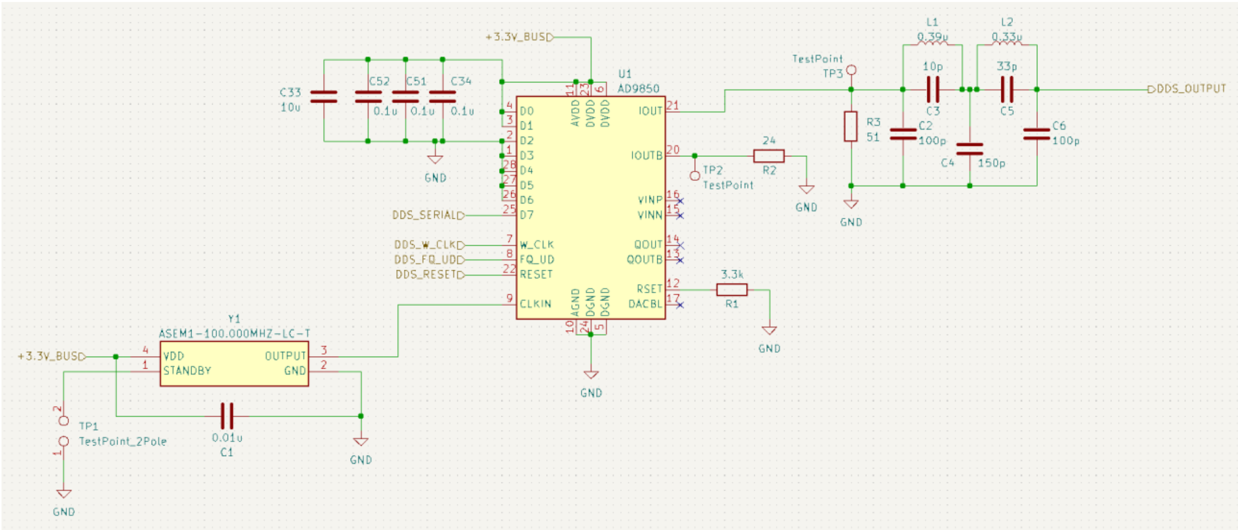

Figure 2-6: Signal generation DDS subsystem schematic with crystal oscillator included.

Due to difficulty with sourcing a $125MHz$ 7^{th} overtone crystal oscillator, the type recommended by the datasheet, a lower frequency 100MHz oscillator [5] was selected and implemented. A lowpass 5^{th} order elliptic filter is implemented on the output with a transition frequency of $\sim 400kHz$. This allows higher frequency harmonics that naturally occur from the AD9850's signal generation circuitry to be reduced in magnitude and ensures a cleaner, distortion-minimised signal to be generated for amplification. This contributes to meeting REQ-038 SFAIRP in the context of the DDS IC output.

2.4.3.2 Validation & Justification

No simulation was used for this subsystem as the supporting circuitry and passive components were built exactly to datasheet specifications.

2.4.3.3 Requirements Met

The design employs an Analog Devices AD9850 DDS chip for signal generation, capable of producing various waveforms up to ~30MHz, thereby satisfying REQ-015. The chip's high precision allows for an output frequency resolution of 0.03675Hz, far exceeding the required 10kHz steps and meeting REQ-021. Various voltage levels are sourced through different converters and regulators, aligning with REQ-028.

2.4.4 Signal Modulation

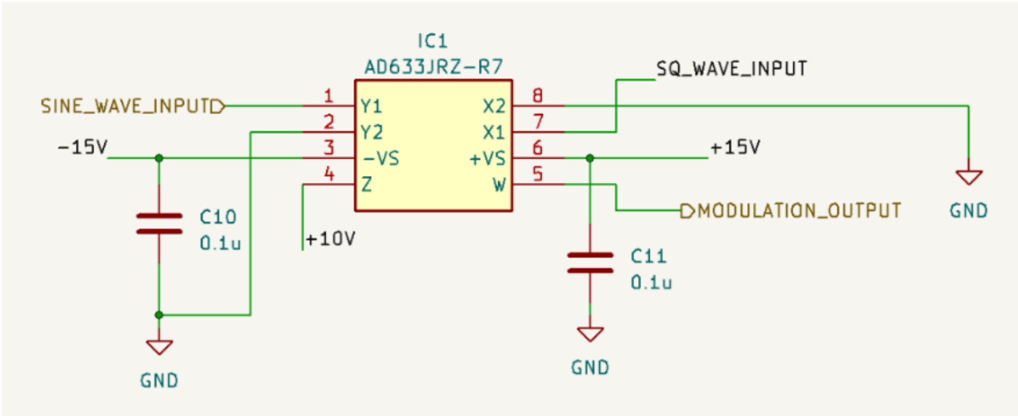

Figure 2-7: Signal modulation signal schematic

2.4.4.1 Explanation

The signal modulation circuit is specifically designed to perform analogue signal modulation as per the client's request. The user is able to select if they want the output signal to be modulated or not, noting that the modulation index is fixed at 1. There are four possible scenarios that the modulator will face within this design, these are:

I. AC input modulated with square wave,
II. AC input with no modulation,
III. DC input modulated with square wave, or
IV. DC input with no modulation.

The modulation square wave has a variable frequency which can be selected by the user as the RPi has a dedicated Pulse Width Modulation (PWM) GPIO which produces a $3.3V$ magnitude square wave. From this, a LM741 amplifier is used to step up the magnitude to $10V$.

Scenario I:AC Input Modulated with Square wave

In this scenario, the user generates AC wave with given input parameters. This wave is passed from the DDS to the "Sine_Wave_Input" pin as shown in Figure 2-7. Alongside this, the $10V$ square wave with the selected frequency is simultaneously passed into the modulator. The resulted output wave is a 100% (modulation index of 1) AC modulated wave. The resulting output waveform has a magnitude of approximately $0.5V$.

Scenario II: AC Input not Modulated.

This scenario closely resembles scenario I. Instead, here the square wave is given a duty cycle of 1. This results in a $3.3V_{DC}$ being passed into the LM471 amplifier. This leads to the output waveform of the modulator being a scaled version of the original input. The output magnitude is approximately around $0.5V$. Keeping this output consistent simplifies the HV amplification.

Scenario III: DC Input Modulated with Square wave

This scenario is similar to scenario I, except here the input signal is a DC waveform. The resulting output signal is essentially a scaled version of the input square wave. As expected, the output magnitude is approximately $0.5V$.

Scenario IV: DC Input not Modulated
This scenario is the most simplistic. Here, two DC signals are passed into the modulator. This simply results in a DC output voltage at around $0.5V$.

2.4.4.2 Requirements Met

This section of the overall design was implemented to explicitly meet REQ-16, which is critical to the function of the design. This design allows for a switchable modulation output signal for both AC and DC input signals.

2.4.4.3 Justification

To validate the proposed modulation circuit, PSpice for TI was used to simulate the functionality of the design.

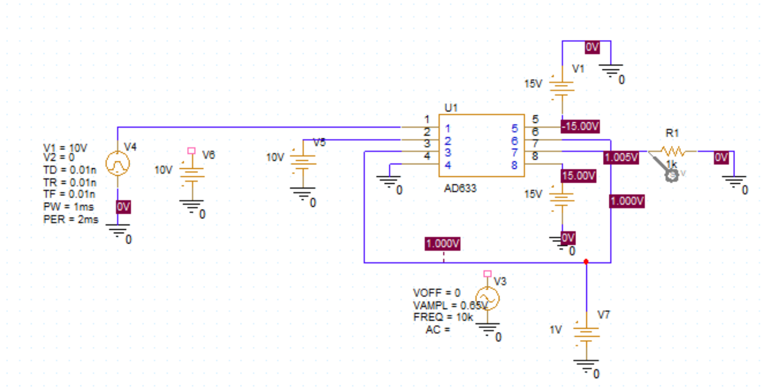

Figure 2-8: AD633 PSpice Model Architecture

Each of the scenarios described in 2.4.4.1 was then tested to observe how the AD633 should theoretically respond to the changes. To change the scenario, the voltage source is simply changed in each simulation. It is assumed that the output will stop before a new wave is passed into the AD633, hence the modelling has been conducted in the same manner. From the results presented below, the AD633 operates as intended and is a suitable component for this proposed design.

<u>Scenario I Simulation:</u>

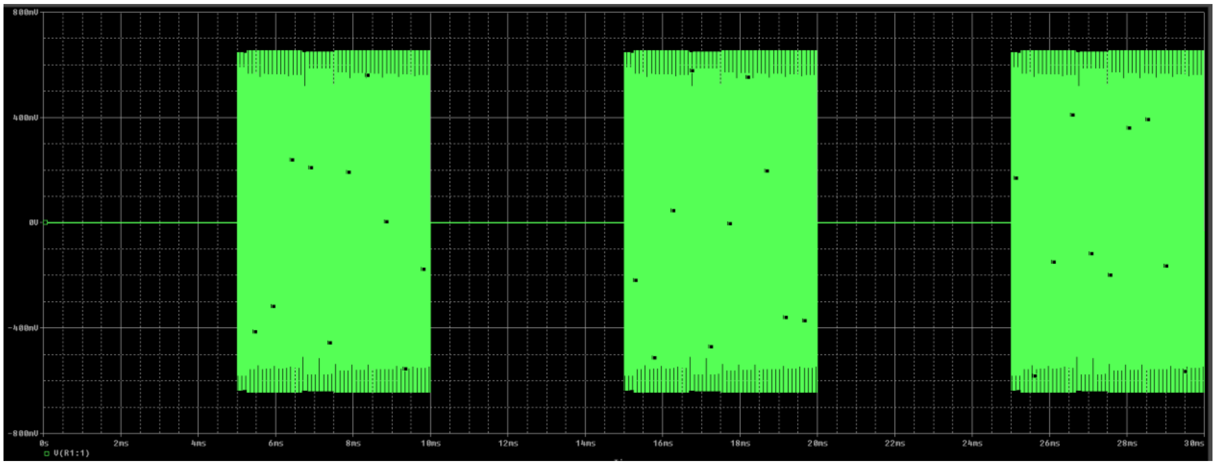

Figure 2-9: AD633 signal output for Scenario I test. The square wave frequency is 100 Hz *and the AC signal has a frequency of* 50 kHz.

<u>Scenario II Simulation:</u>

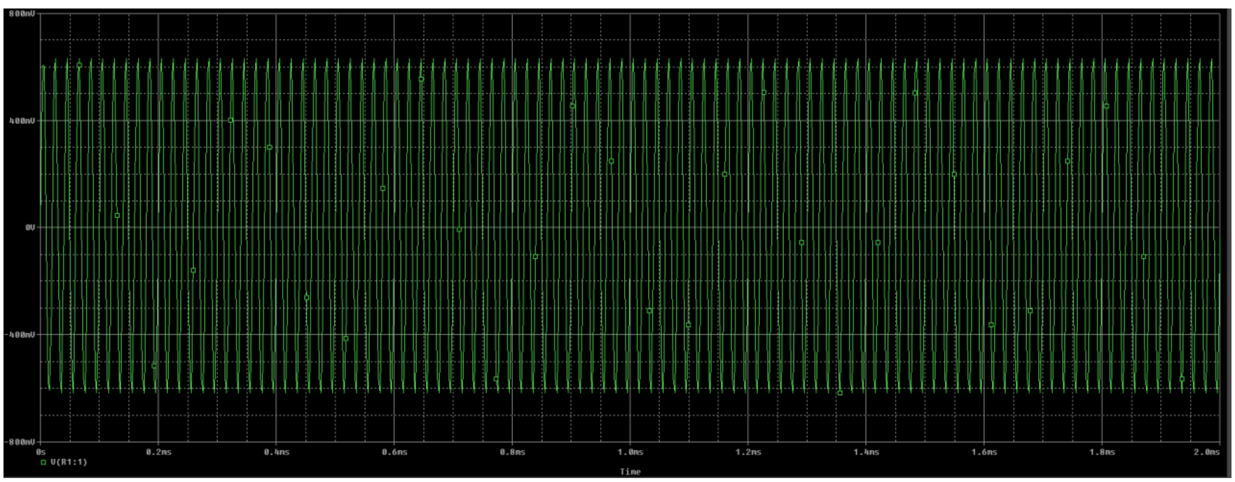

Figure 2-10: AD633 signal output for Scenario II test. The AC signal has a frequency of 50 kHz. *Note the reduced time scale used to better present the AC waveform.*

Scenario III Simulation:

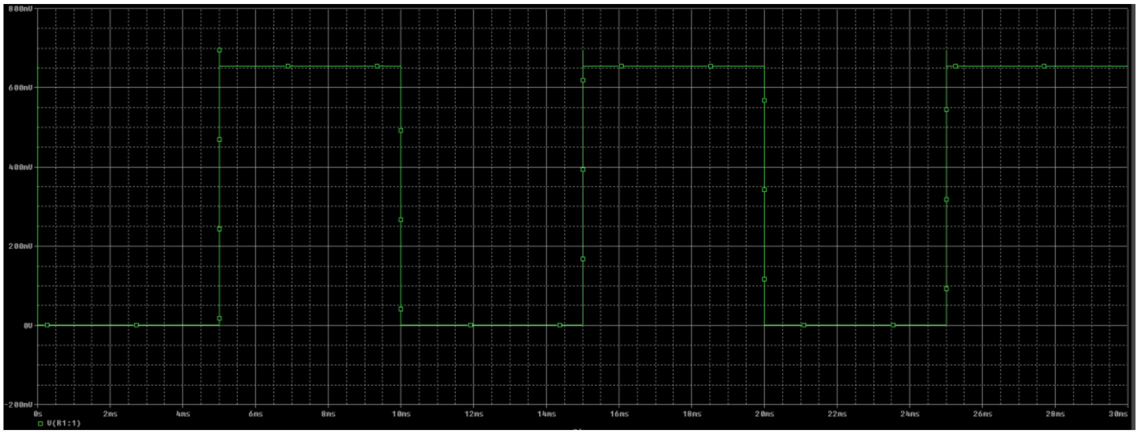

Figure 2-11: AD633 signal output for Scenario III test. The square wave frequency is $100\ Hz$.

Scenario IV Simulation:

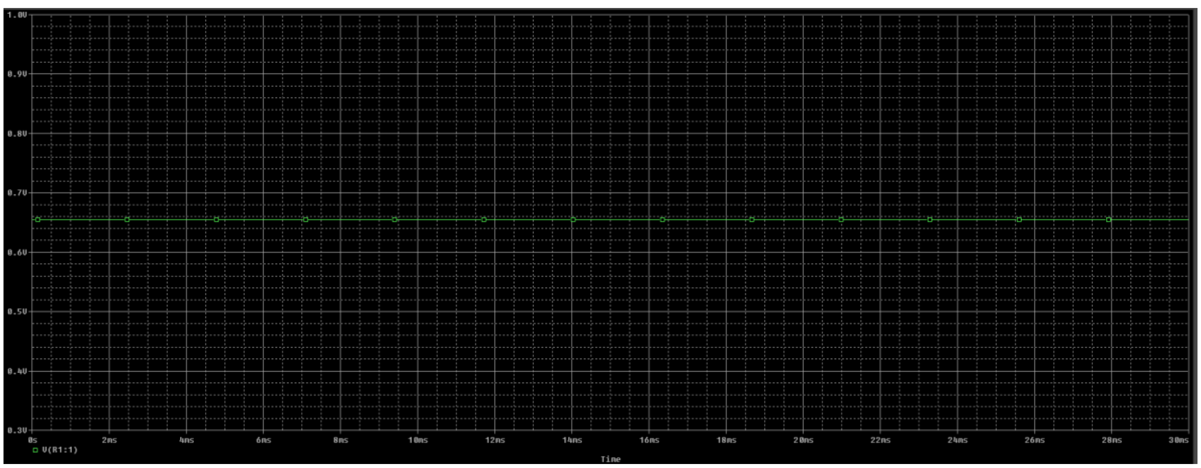

Figure 2-12:AD633 signal output for Scenario IV test.

2.4.4.4 Components

To successfully implement the signal modulation design element, the below IC components are required. These will ensure the sufficient power is supplied to the modulator as well as allowing a constant output voltage.

Component	Description	Output/Ratings
AD633JRZ	Four-quadrant, analogue multiplier	Supply Voltage: $\pm 18V$ Power: $500mW$ Operating Temperature: $0\ ℃\ to\ 70\ ℃$
CRE1S0515SC (x2)	DC-DC Converter	Input Voltage: $5V$ Output Voltage: $15V$ Output Current: $67mA$
LM741	General purpose operational amplifier	Max. Supply Voltage: $\pm 22V$ Power: $500mW$ Input Voltage: $15V$

2.4.5 HV Amplification

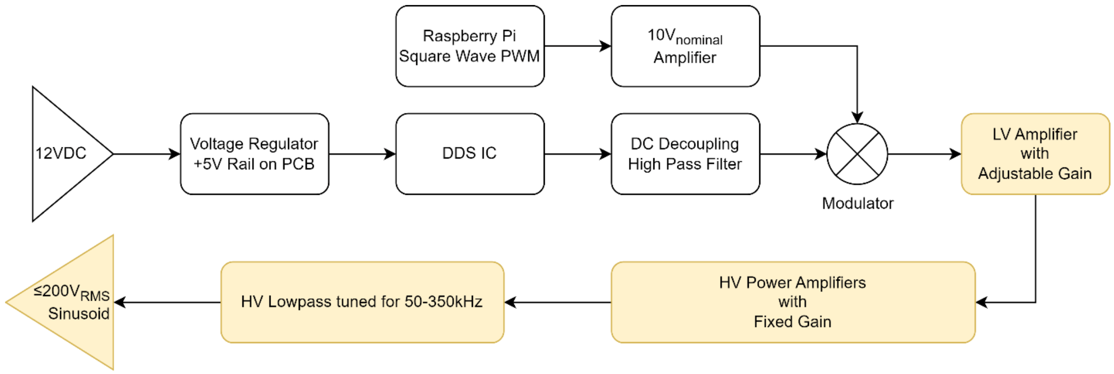

Figure 2-13: HV Amplification Architecture

The HV Amplification is a pivotal element in the MEMS Testing Power Supply project, designed to amplify signals to the required voltage levels for various applications. It consists of two main stages: the preconditioning amplification stage and the secondary amplification stage. The preconditioning amplification stage is user-controllable with a gain range of 0-8x, while the secondary amplification stage offers a fixed 20x gain. This design ensures that the system can handle a wide range of signal frequencies and amplitudes, meeting the project's stringent requirements. The final design for the HV amplification can be seen in Figure 2-14 below.

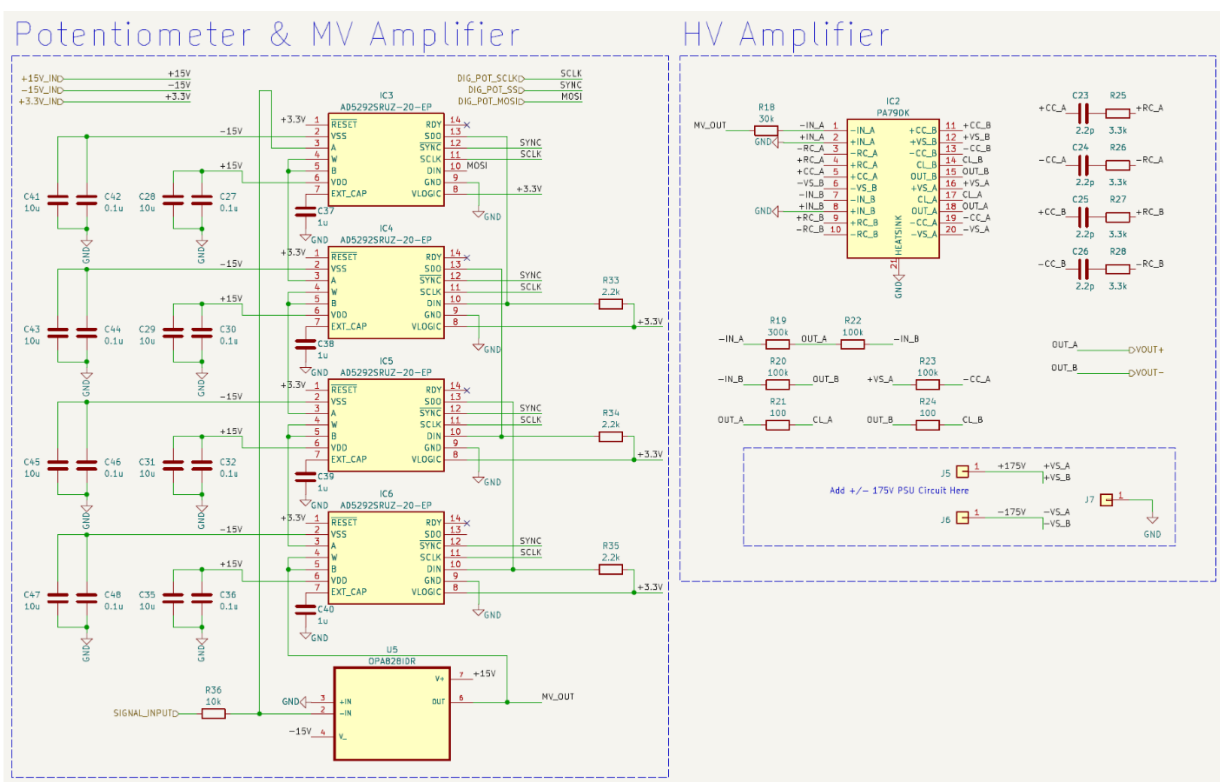

Figure 2-14: HV amplifier and MV amplifier with digital potentiometers

2.4.5.1 Explanation

Preconditioning amplification Stage:
The preconditioning amplification stage consists of four digital potentiometers, a resistor, and a precision operational amplifier. This stage is set up in an inverting gain configuration, crucial to meeting the requirements of the client. The MPU controls the digital potentiometers to adjust the resistor values, thereby altering the gain. Each potentiometer has 1024 resistive steps, providing a total of 4096 steps between the 0-8x gain range. This stage is essential for achieving the adjustable output voltage and frequency ranges specified in REQ-001, REQ-003, REQ-015, and REQ-020.

Secondary Amplification Stage:
The secondary amplification stage is designed with two operational amplifiers and offers a fixed gain of 20x. This stage can amplify signals up to $300kHz$ for AC and up to $215V_{rms}$, directly meeting REQ-003 and REQ-015. The design is based on the PA79 high voltage, high-speed op-amp, which is capable of delivering up to $200mA$ peak output current and has a slew rate of over $350V/\mu s$.

The HV amplification stage takes the output from the preamplification stage and steps it up to the final output level for the user. This two-stage design ensures that the system can meet a wide range of application requirements, from low to high voltage and frequency ranges, in compliance with REQ-005 and REQ-006.

The design of this circuit is a modified version from the PA79 datasheet [6], which provides guidelines for achieving high slew rates with low idle current. The PA79 is specifically designed as a high-speed pulse amplifier, making it an ideal choice for this application due to the high frequencies required as well as the high voltage.

2.4.5.2 Requirements Met

Requirement	Description
REQ-001	The design shall produce a DC output voltage of $0 - 200V$
REQ-003	The design shall produce an AC output voltage of 0 - $200\ V_{rms}$
REQ-015	The design shall produce an AC output frequency of 50-$300kHz$ sine wave
REQ-020	The design shall allow for output voltage adjustments with steps of $0.05V$ or less over full range of voltages.

2.4.5.3 Justification

To validate the proposed HV Amplification design, simulations were conducted using TINA [7]. These simulations aimed to verify that the design meets the client's requirements, particularly REQ-001, REQ-003, REQ-015, and REQ-020.

Preamplification Stage:

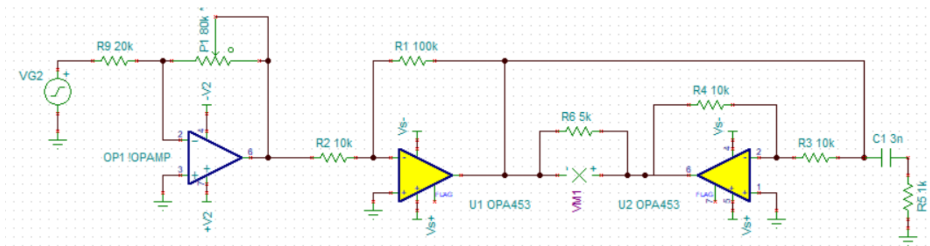

Figure 2-15: Preamplification Stage Simulation Schematic

The preamplification stage was simulated to confirm its ability to provide a gain range of 0-8x using a potentiometer. The simulation results in Figure 2-16 confirm that the stage operates as intended, allowing for precise control of gain.

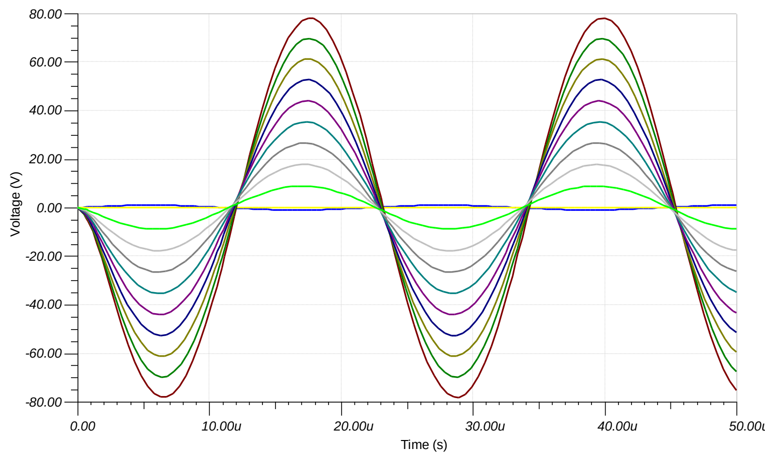

Figure 2-16 Preamplification stage tuneable voltage output range simulation

HV Amplification Stage:

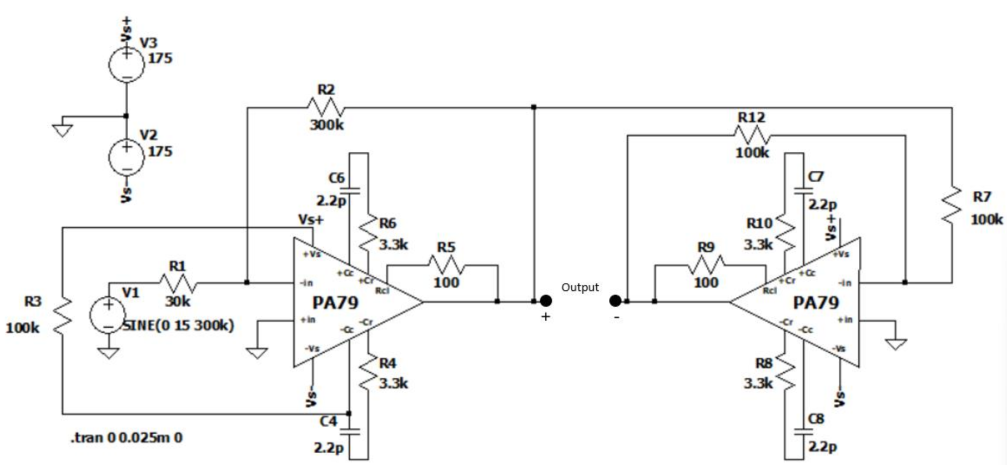

Figure 2-17: HV Amplification Stage Simulation Schematic

The HV Amplification stage was simulated to verify its fixed 20x gain and its capability to handle signals up to $300kHz$ and $215V_{rms}$. The simulation results align well with the theoretical expectations and confirm that the design meets REQ-003 and REQ-015. The 100Ω resistor was placed to ensure a maximum current draw of $20mA$.

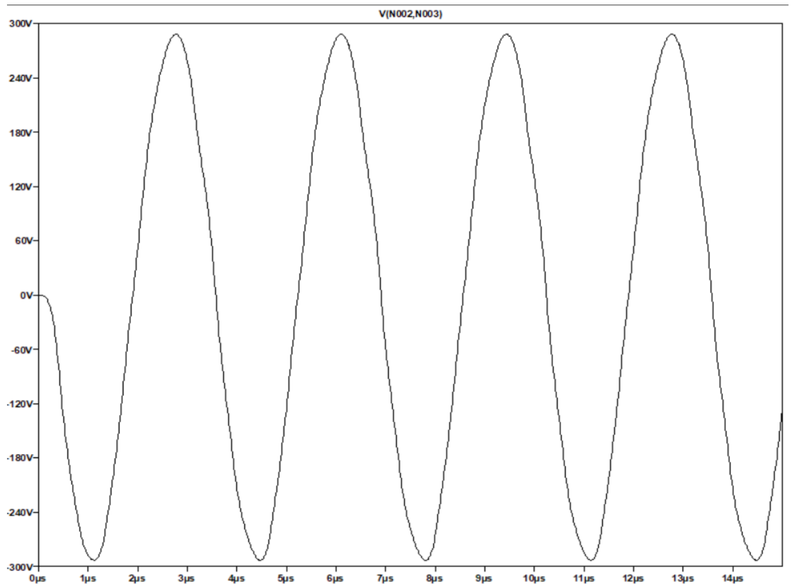

Figure 2-18: Total HV system simulation results

Overall System:

The complete HV Amplification system was also simulated to ensure that the two stages work cohesively to meet the overall system requirements. The results shown in Figure 2-18 indicate that the design is capable of providing the necessary voltage and frequency ranges, fulfilling REQ-001, REQ-003, REQ-015, and REQ-020.

2.4.5.4 Components

Component	Description	Output/Ratings
AD5292	Digital Potentiometer	Input Voltage: $\pm 16.5\ V$ Resistance: 0 - 20 $k\Omega$ 1024 Resistor Steps
PA79	2x Power Op-amp	Max. Supply Voltage: $\pm 175\ V$ Slew Rate: over $350\ V/\mu s$ Watt Dissipation Capability: $26\ W$ Power Bandwidth: $200\ kHz$ Output Current: $50\ mA$
OPA828	Precision Op-Amp	Max. Supply Voltage: $\pm 18\ V$ Slew Rate: $150\ V/\mu s$ Overload power limiter

2.4.6 Overcurrent Protection

The overcurrent protection circuit is designed to stop the output, once the output current is above the limit defined by the user. Overcurrent protection has been implemented using the following four steps:

1. Sense the current directly before the output terminal.
2. Send the output of the current sense IC to a circuit which removes the DC offset present.
3. Send the output of the DC offset remover circuit to an ADC.
4. Stop the output when the digital reading is above the allowable limit.

2.4.6.1 Current Sensing

The sensing of the current is done through ACS724 IC from the ACS family. The chip offers a current sensing range of $-2.5A$ to $2.5A$, which is significantly more than required as the design is for a max current of $10\ mA$. Furthermore, the sensitivity is specified as 800mV/A , which means the output will be $0.8mV$ per $1mA$ of sensed current. The working voltage of this IC is $297V_{rms}$, meaning that it's higher than the required maximum of $200\ V_{rms}$. This allows the output channel to be directly connected in series to this IC. Lastly, at zero current, the output of the IC will be $2.5V$, due to the inherently present DC offset. The schematic is shown in Figure 2-19.

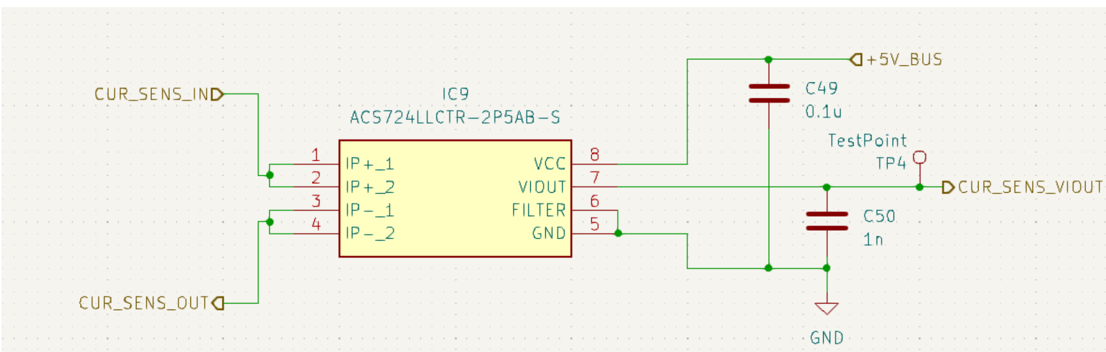

Figure 2-19: Current Sensing Module Schematic.

2.4.6.2 DC Offset Remover + Amplification Circuit

The offset needs to be removed because the design needs to measure very low current and therefore, the change in output of the current sensing IC will also be very low. Hence by removing the DC offset and only amplifying the output of the current sensing IC, the input into the ADC will span the whole 0 to $3.3V$ measuring range, allowing for accurate readings. The circuit is implemented using an Op-Amp, in a differential amplification setting. The schematic is shown in Figure 2-20, where the input 'VG1' is the 'CURR_SENS_VIOUT' from Figure 2-19.

For example, if the current through the ACS724 is 10mA, then the output will be $2.5080V$. Due to the differential configuration of the Op-Amp used in DC Offset Remover circuit, the difference between the input ($2.5080V$) and the reference ($2.49V$) will be $0.018V$. This voltage difference will then be amplified according to the closed loop gain, set by the resistors seen in Figure 2-20.

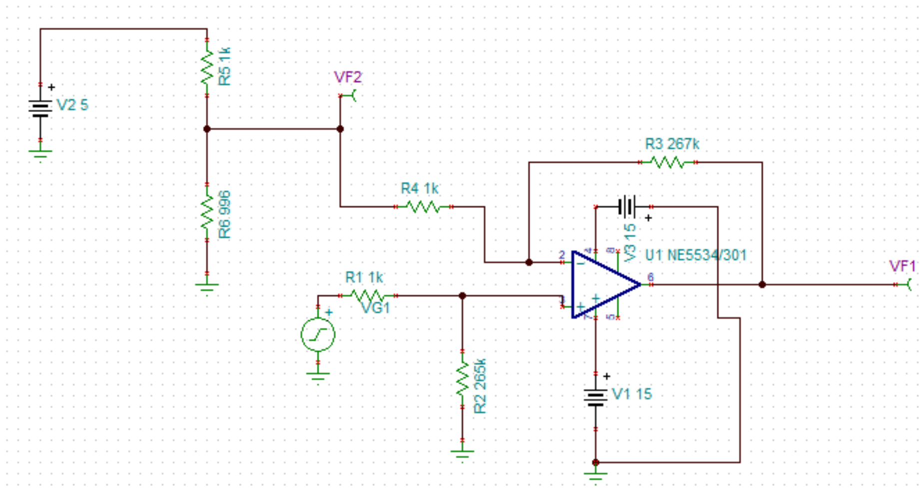

Figure 2-20: DC offset remover + Amplification circuit schematic.

2.4.6.3 Analog-To-Digital Converter (ADC)

The ADC is a component that converts the analogue output from DC offset remover amplifier circuit into a digital input into the MPU. This component converts the analog signal into a digital format, enabling the MPU to interpret the data. The selected ADC chip for this project is the AD7991, a 12-bit, four-channel device that communicates with the RPi via I2C protocol. The reference voltage for the ADC is set at 3.3V, which corresponds to the amplification circuit that maps the current sensing output between 0 and 3.3V. A schematic detailing this ADC configuration appears in Figure 2-21. Cost considerations led to the selection of an ADC with a communication speed limit of 400 kHz.

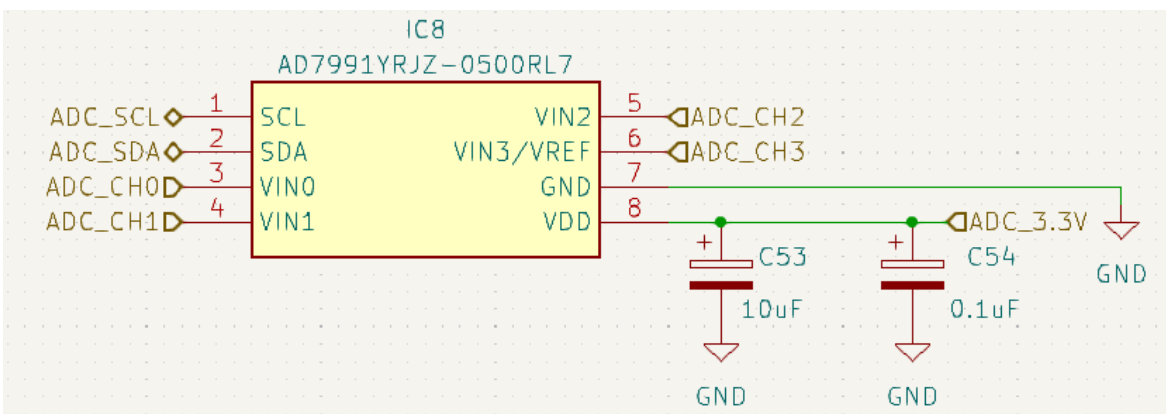

Figure 2-21: ADC schematic.

2.4.6.4 Requirements Met

The design uses an ACS724 IC for current sensing, which has a maximum current sensing range well above the design's maximum output current of 10mA, thereby meeting REQ-005. The overcurrent protection feature is designed to shut off the output rapidly when the sensed current exceeds the user-defined limit, aligning with REQ-007. The ADC chip AD7991 and the associated circuitry allow for precise current measurements, which can be used to implement current limit adjustments in steps, fulfilling REQ-022.

2.4.6.5 Justification

To validate the overcurrent protection design, an LTspice was used to simulate the ACS724, and Tina-Ti was used to simulate the DC offset remover plus amplification circuit. The schematic shown in Figure 2-22 was used to simulate the operation of the ACS724 in low current conditions.

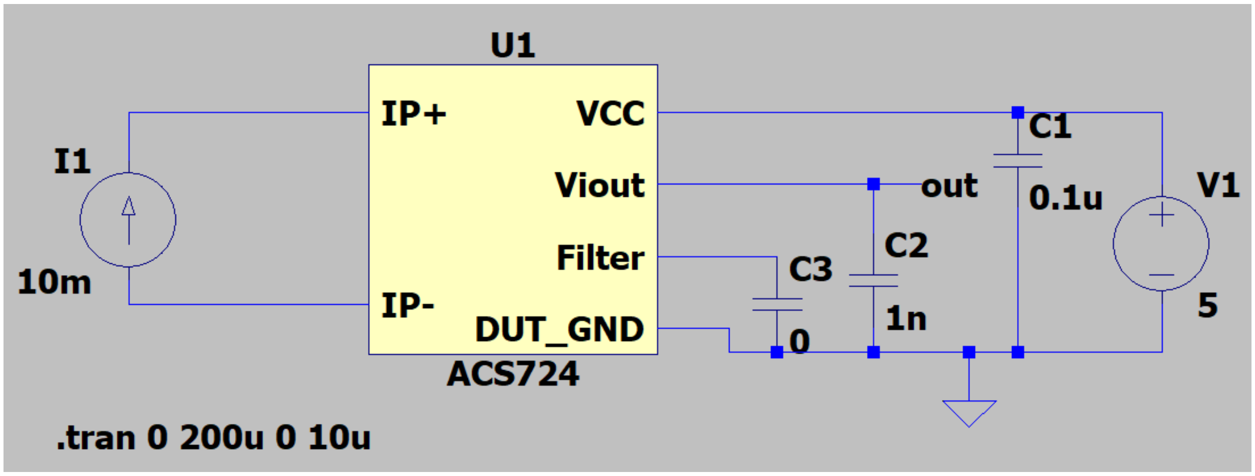

Figure 2-22: ACS724 simulation schematic.

Three simulation results are shown below showcasing the different operation modes of the power supply. The first simulation shown in Figure 2-23 shows the offset voltage in action, when the output is not connected to a load, i.e. no current is flowing, the current sensor output is $2.5V$.

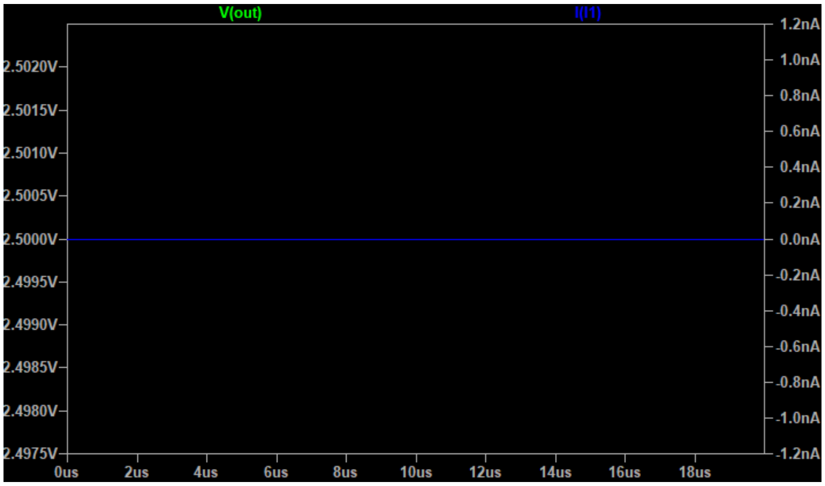

Figure 2-23: ACS724 DC offset simulation.

The second simulation shows when DC mode is selected by the user and hence, direct current is flowing the current sensor. This is shown in Figure 2-23. From Figure 2-24, the time difference is approximately $2\mu s$, showcasing the rise time. This is beneficial as it meets the requirement to shut down the output in under $10\ ms$. In Figure 2-25, a periodic pulse is generated, and the output is shown.

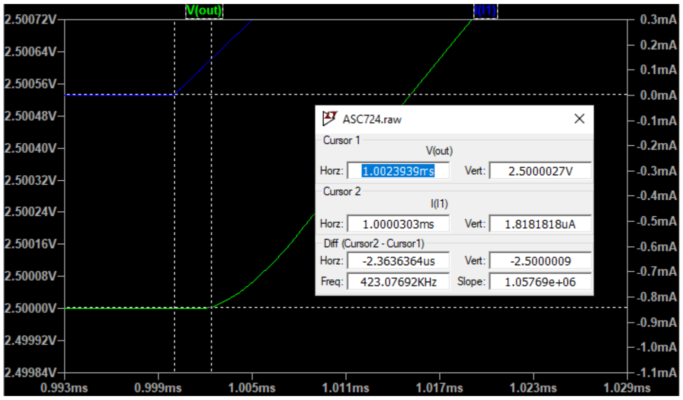

Figure 2-24: LTSpice simulation testing rise time.

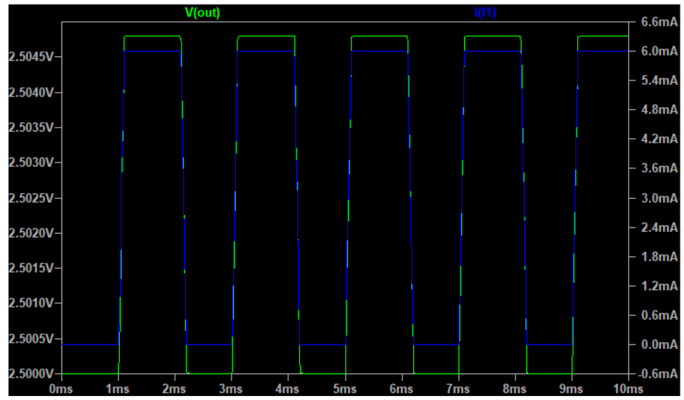

Figure 2-25: LTSpice simulation output of a applied DC pulse.

The last simulation is similar to the previous one, except the incident current is an AC. The rise time is similar to DC with a value of approximately $2\mu s$, however a design error is noticed. The simulation results are shown in Figure 2-26.

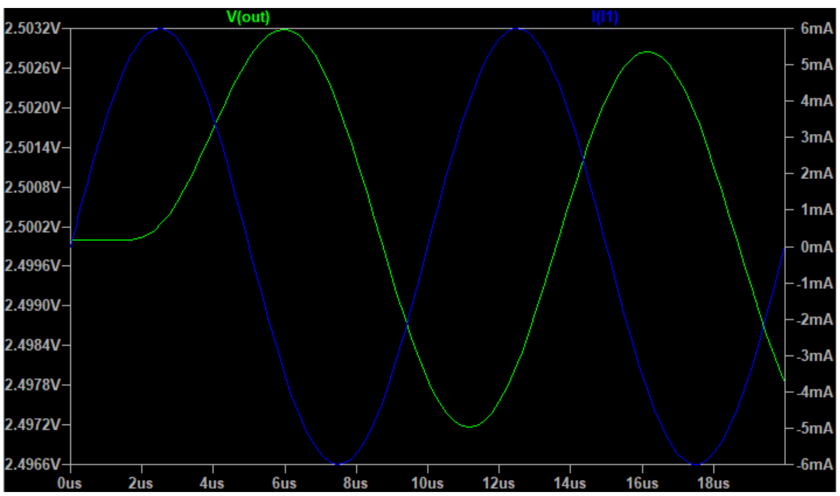

Figure 2-26: AC current sense output - Simulation

The peak-value of the output, when a 6mA current is flowing through the current sensing IC is $2.5048V$. However, this was not observed in Figure 2-26. The output signal is shown in green, and the peak-value is calculated to be 2.5026V. This is because the slew rate parameter was initially overlooked for the current sensing IC. The slew rate is crucial for high frequency outputs and this aspect is the primary reason for the error. This results in the design partially meeting the requirements shown in Section 2.4.6.4. However, for all DC outputs, the current sensing IC is a perfect fit, and no errors can be seen.

The simulation schematic for the DC offset remover circuit is shown in Figure 2-20, and the same three tests were applied as for the current sensing IC. Firstly, a $2.5V$ input is applied to the circuit to measure the output voltage when no current is flowing through the current sensing IC. Applying a $2.5\ V$ to the non-inverting end gives the resulting voltage output shown in Figure 2-27.

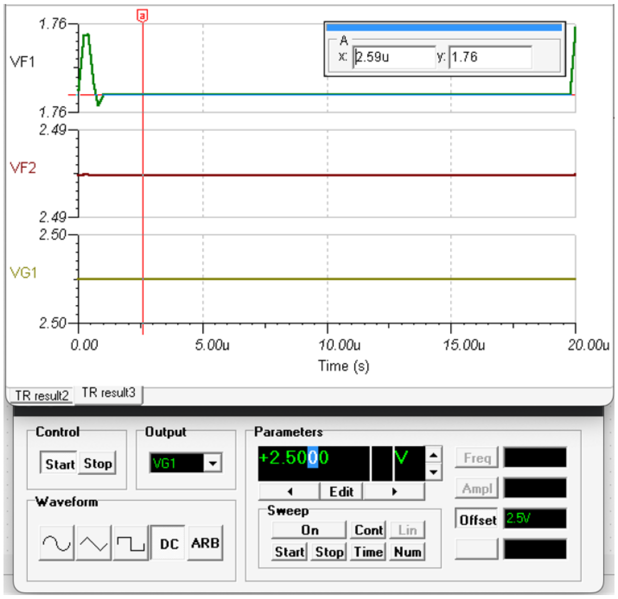

Figure 2-27: Showcasing output to the ADC when no current is flowing.

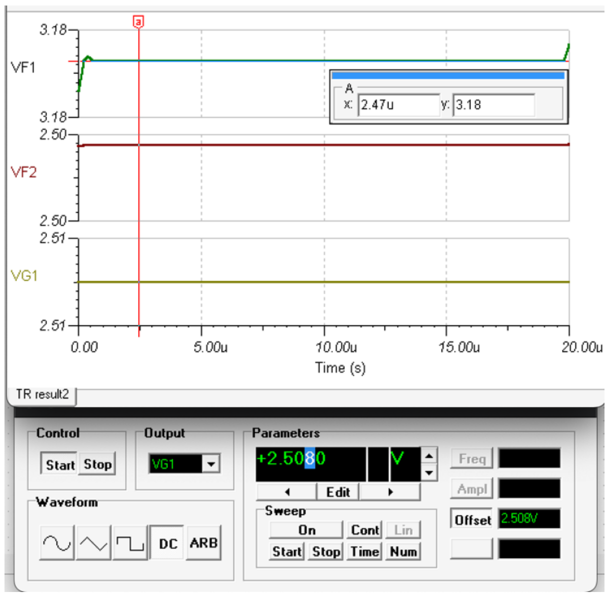

Figure 2-28: Simulation showcasing the output of DC offset remover circuit, when 10mA is flowing.

Secondly, when a DC current is applied to the current sensor IC, the output of ACS724 will also be DC. This output will be applied to the non-inverting pin (+) shown in Figure 2-20. When a 10mA current is flowing through the current sensing IC, the resulting voltage output will be $2.508V$, which is applied to the non-inverting pin. The resulting output of the DC offset remover circuit is shown in Figure 2-28. Lastly, when a AC signal is sensed by the current sensing IC, the output will also be AC. This output will be connected to the non-inverting pin of the NE5534 Op-Amp in DC offset remover circuit. The output of the DC offset circuit remover, when a AC signal is induced is shown in Figure 2-29. The output starts at $1.76V$ (labelled by the red cursor), mapping to zero current as seen in Figure 2-29, and rises upto the max of $3.18V$ (labelled by the blue cursor), when the input (VG1) is $2.508V$. In summary, the circuit is able to map the input voltage range of $2.492 - 2.508\ V$ from the current sensing IC to 1.76 - $3.18V$ from the DC offset remover circuit.

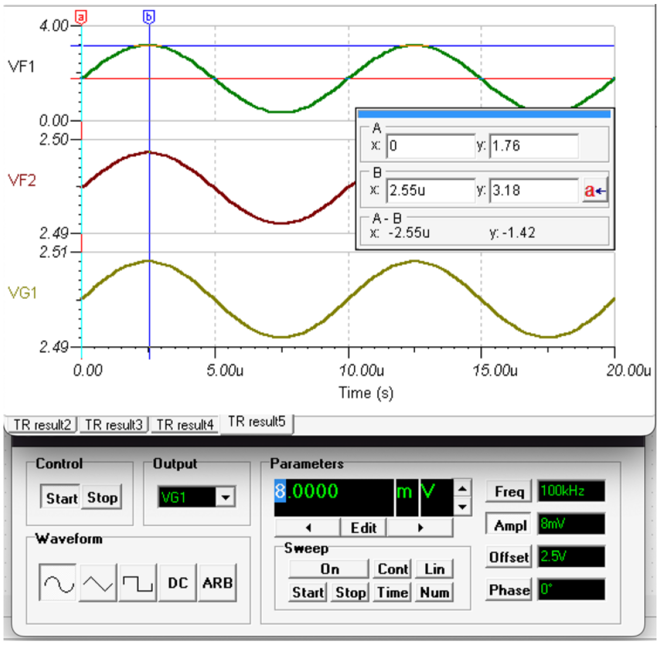

Figure 2-29: Simulation output of DC offset remover circuit when an AC signal is induced.

2.4.6.6 Components

To successfully implement the overcurrent protection design element, the below IC components are required. These will ensure the sufficient power is supplied to the current sensing IC, Op-Amp and ADC.

Component	Description	Ratings
ACS724	Automotive-Grade, Galvanically Isolated Current Sensor IC	Supply Voltage: $5V$ Primary Conductor Resistance: $1.2m\Omega$ Sensitivity: $800mV/A$
NE5534	Low-Noise Op-amp	Input Voltage: $\pm 15V$ Slew Rate: $13V/\mu s$ Input Current: $10mA$
AD7991	4-Channel, 12-Bit ADC with I^2C Compatible Interface	Reference Input/Supply: $3.3V$ Conversion Time: $1\mu s$ Operating Temperature: -40^oC to 125^oC

2.4.7 Hardware Interlock

The Hardware Interlock serves as a critical safety feature in the MEMS Testing Power Supply project, ensuring that voltage outputs are kept within safe limits. It provides multiple layers of control and safety mechanisms, from voltage limiting to user-controlled enable/disable functions. The final design for the hardware interlock can be seen in Figure 2-30 below.

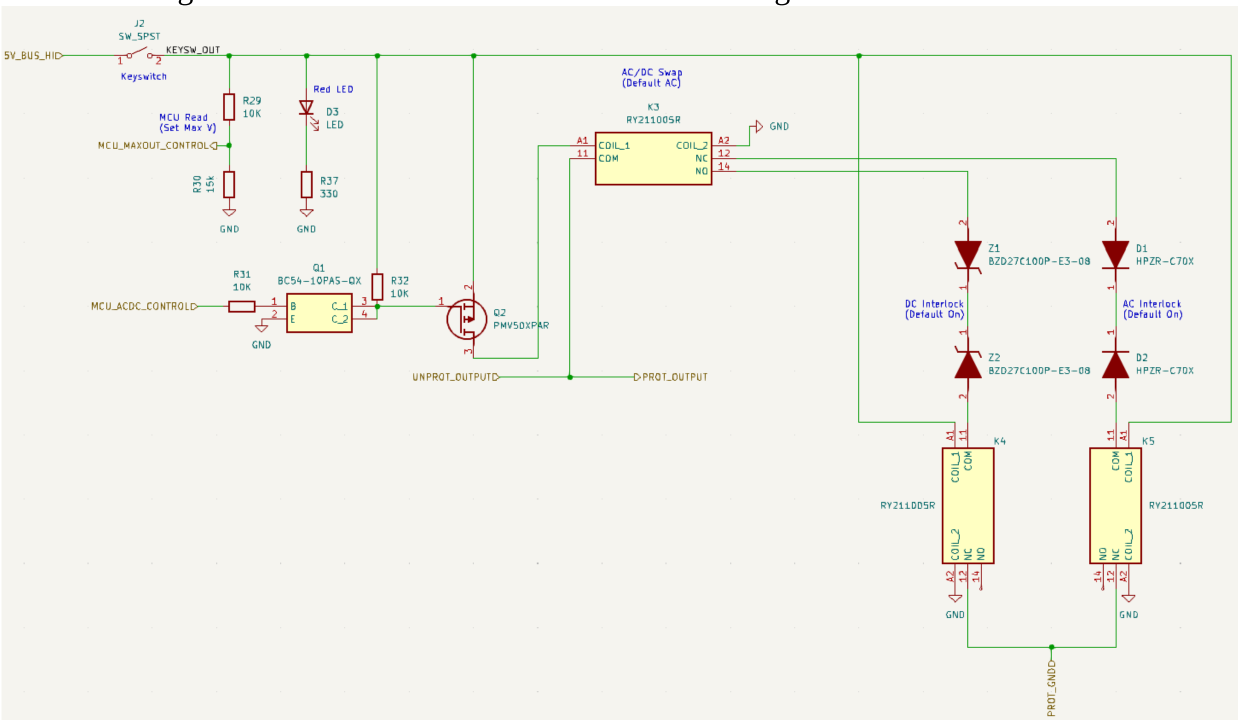

Figure 2-30: Hardware Interlock Schematic

2.4.7.1 Explanation

The hardware interlock is engineered to serve as a multi-faceted safety mechanism in the PSU. It is designed to limit the output voltage for both AC and DC outputs while providing the user with the ability to enable or disable this feature. The interlock operates under two main scenarios:

1. Interlock Enabled: When the key switch is turned on, the hardware interlock is disabled, allowing for higher voltage outputs.
2. Interlock Disabled: When the key switch is turned off, the hardware interlock is enabled, limiting the output voltage to safe levels as defined by the Zener diodes.

Key Switch & MPU:

The key switch is connected to a $5V$ bus. When enabled, it sends a high signal to a RPi MPU. A voltage divider is used to bring the $5V$ down to $3V$, within the MPU's $3.3V$ operating range.

LED Indicator:

An LED is also connected to the key switch circuit, lighting up when the key switch is closed, providing a visual indication of the interlock status.

Zener Diodes:
Two sets of back-to-back Zener diodes are used for voltage limiting. One set is rated at $70V$ for limiting AC voltage to $50\ V_{rms}$, and the other is rated at $100V$ for limiting DC voltage.

Single Pole Double Throw (SPDT) Relays:
Three SPDT relays are used in the design:

- One SPDT relay is positioned above the Zener's, with the AC side normally closed and the DC side normally open. This is due to the lower and therefore safer operating condition of the AC Interlock
- A second SPDT relay has its NC (Normally Closed) connected to ground and its NO (Normally Open) connected to the floating low side of the AC Zener's. Enabling the key switch swaps to the floating side and in turn disables the interlock.
- A third SPDT relay has its NC connected to ground and its NO connected to the floating low side of the DC Zener's. As with the AC setup, enabling the key switch disables the interlock.

MPU Output:
The RPi MPU has an additional output connected to an NPN transistor. The collector is connected to the gate pin of a P-MOS as well as the $5V$ bus, while the emitter is grounded. The P-MOS source is connected to the $5V$ bus, and its drain is connected to the AC-DC swapping relay. When a high signal is sent from the MPU, the P-MOS outputs a high voltage, and the relay draws the necessary current to swap to the DC Zener side.

Additional Safety Mechanism:
An input connection to the MPU serves as an additional safety feature. This prevents the user from inputting a voltage higher than the interlock limits when the interlock is enabled, serving as a backup safety measure.

2.4.7.2 Requirements Met

The hardware interlock is designed to meet multiple requirements from the project's requirements register. Specifically, it addresses REQ-02 and REQ-04 by utilising Zener diodes to limit the DC and AC output voltages to $100V$ and $50V_{rms}$, respectively. Additionally, the design incorporates a visual indication light as per REQ-12, which enhances user awareness of the interlock status. These features are crucial for ensuring the safety and reliability of the overall system.

2.4.7.3 Justification

To validate the proposed hardware interlock design, Falstad Circuit Simulator was used to simulate the functionality of the entire setup. The simulation was designed to emulate the real-world conditions as per the relay and datasheets, under which the hardware interlock would operate, including the key switch, MPU, LED indicator, Zener diodes, and SPDT relays.

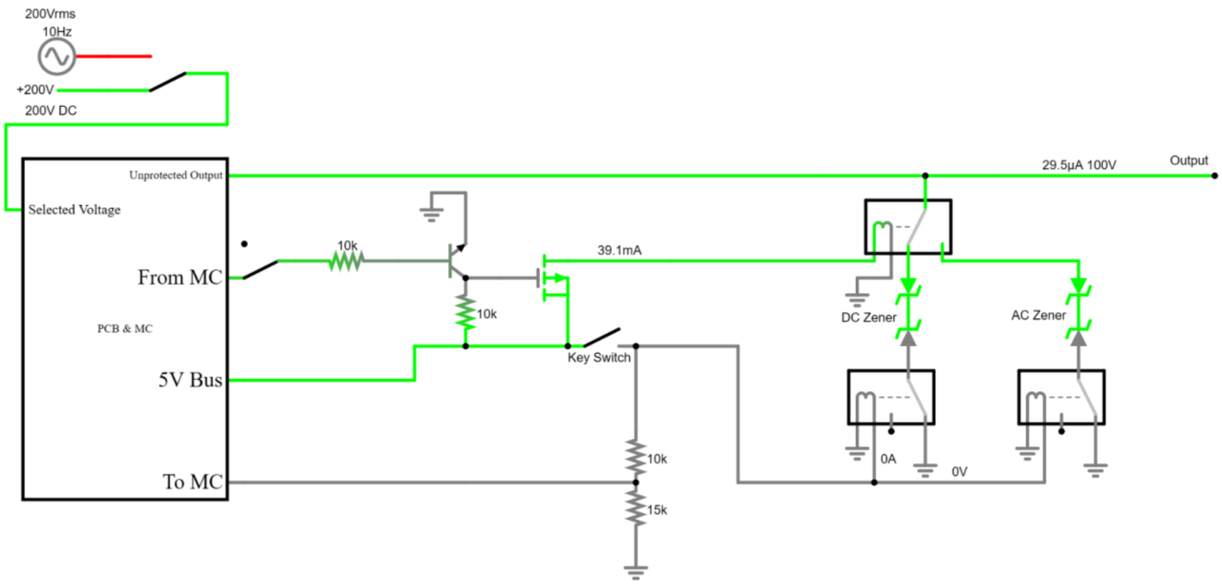

Figure 2-31: Falstad simulation schematic of the hardware interlock.

Key Switch & MPU Simulation:
The first simulation focused on the key switch and its interaction with the RPi microprocessor. When the key switch was enabled, the simulation confirmed that a high signal was sent to the m microprocessor. The voltage divider effectively brought the $5.5V$ down to $3V$, aligning with the microprocessor's operational limits. This can be seen in the simulation (Figure 2-32) below whereby a HV signal is sent when the keylock is closed.

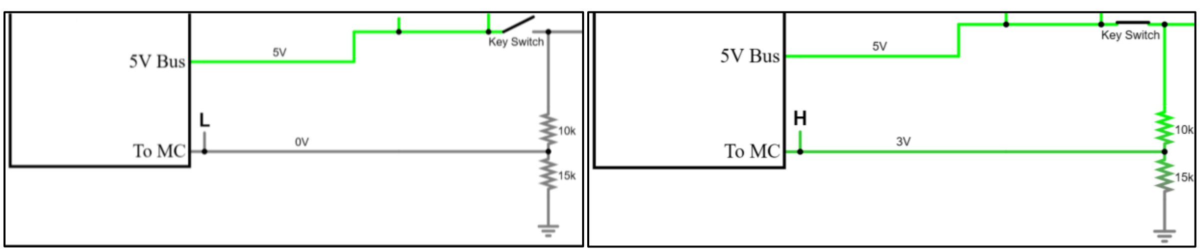

Figure 2-32: Falstad simulation showing key switch and MPU interaction. (OFF/Left, ON, Right)

Zener Diodes and SPDT Relays Simulation:
The simulation aimed to validate the functionality of the Zener diodes and SPDT relays in limiting the output voltage for both AC and DC modes, as per the design requirements.

DC Interlock Simulation:

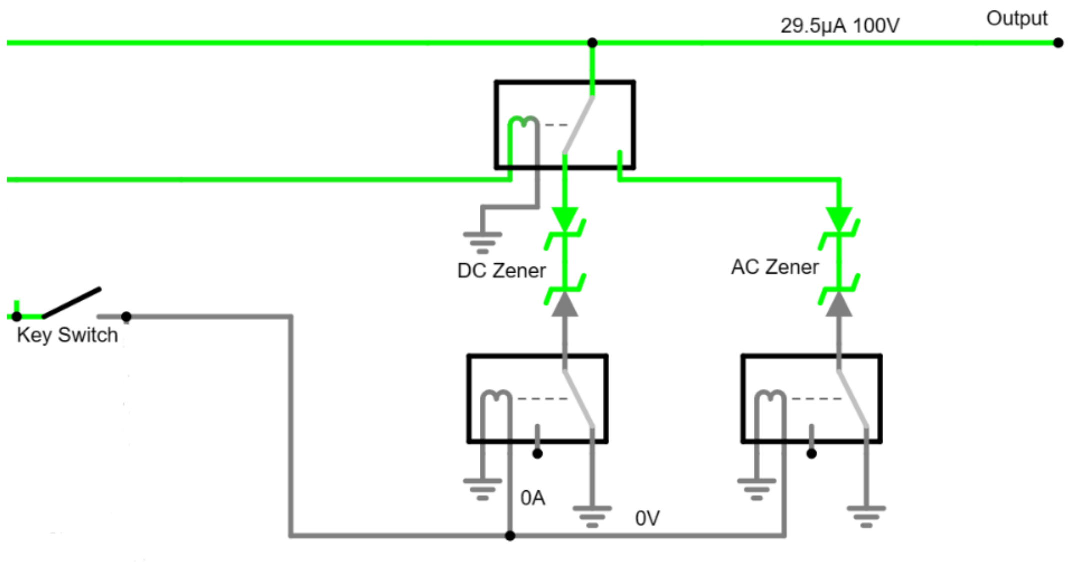

Figure 2-33: Circuit Simulation – DC Zener Enabled

The simulation circuit for the DC interlock was set up to test the $100V$ Zener diodes. A $200V$ DC input was applied to the circuit to assess the voltage-limiting capabilities of the diodes.

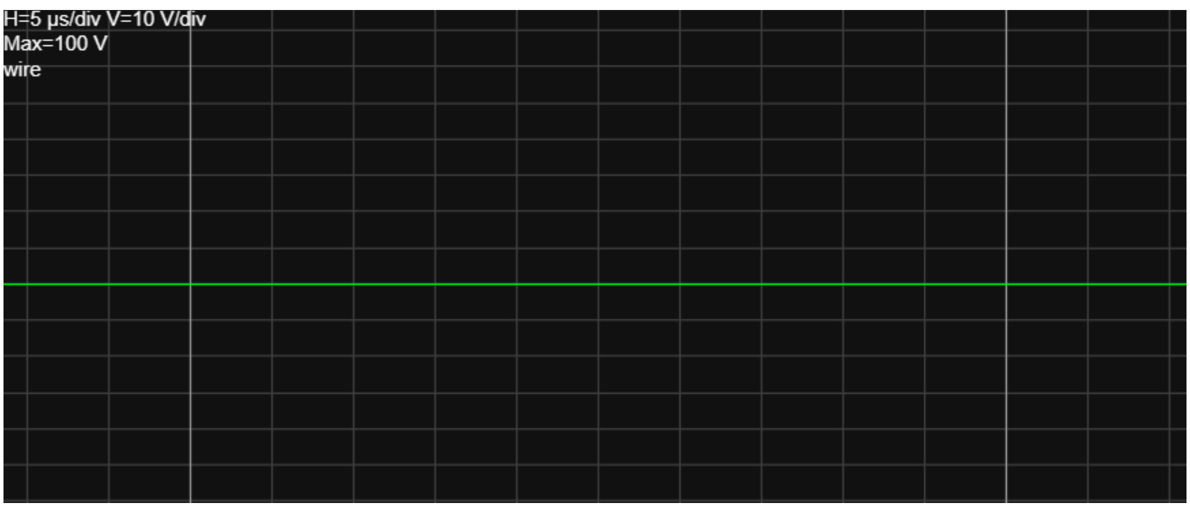

Figure 2-34: Output Plot - DC Zener Enabled

The output plot revealed that the Zener diodes effectively limited the output voltage to $100V$, confirming their role in the DC interlock mechanism.

AC Interlock Simulation:

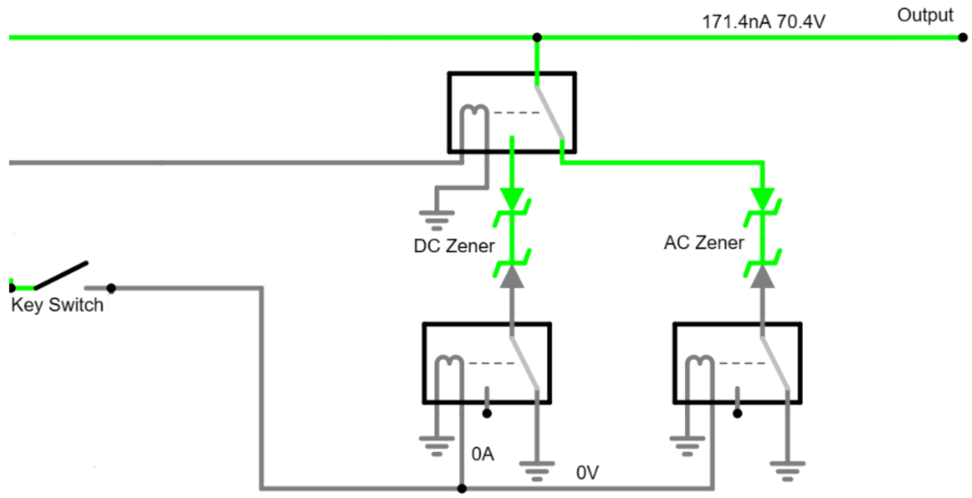

Figure 2-35: Circuit Simulation – AC Zener Enabled

For the AC interlock, the simulation was conducted at $300kHz$, which is the upper limit of the frequency range specified in the project brief. The circuit incorporated $70V$ Zener diodes to limit the AC voltage.

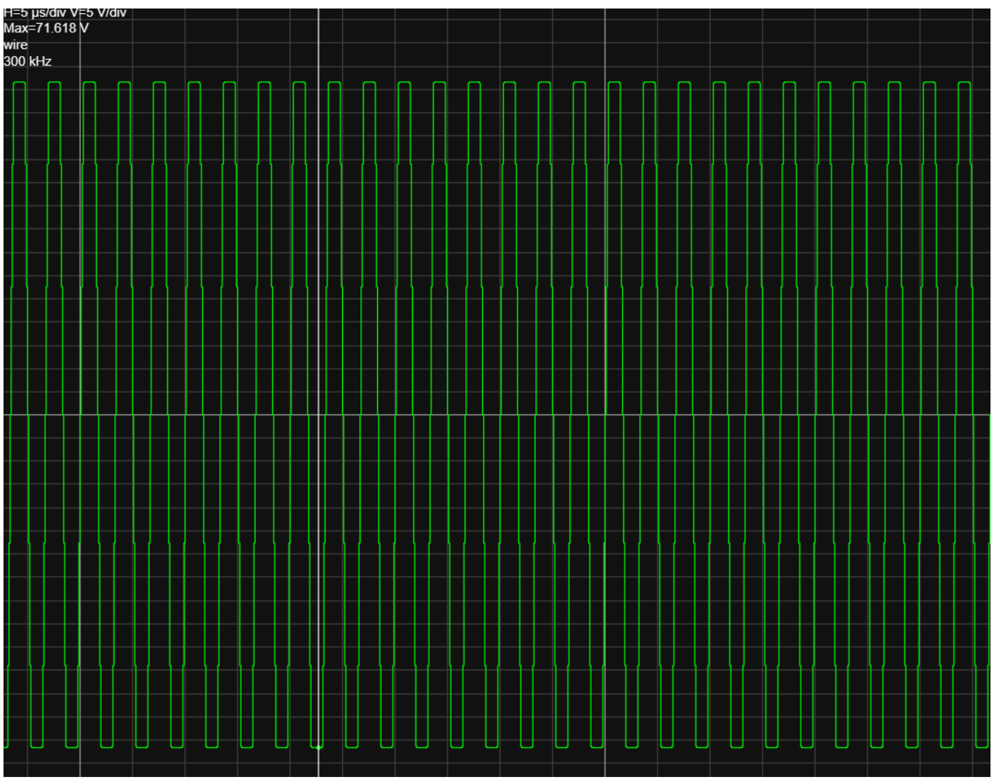

Figure 2-36: Output Plot – AC Zener Enabled

The output plot showed that the waveform retained its original shape but was limited to an amplitude of $71.618V$ peak. This translates to an RMS voltage of approximately $50.5V$, effectively meeting the requirement to limit the AC voltage to $50V_{rms}$.

These simulation results confirm that the Zener diodes and SPDT relays function as intended, successfully limiting the output voltages in both AC and DC modes. The SPDT relays were also verified to switch correctly between the AC and DC Zener diodes, controlled by the MPU's output.

MPU Select Simulation:
The third simulation focused on the additional output from the RPi MPU. When a high signal was sent from the MPU, the P-MOS outputted a high voltage, and the relay drew the necessary current to swap to the DC Zener side, confirming the design's functionality.

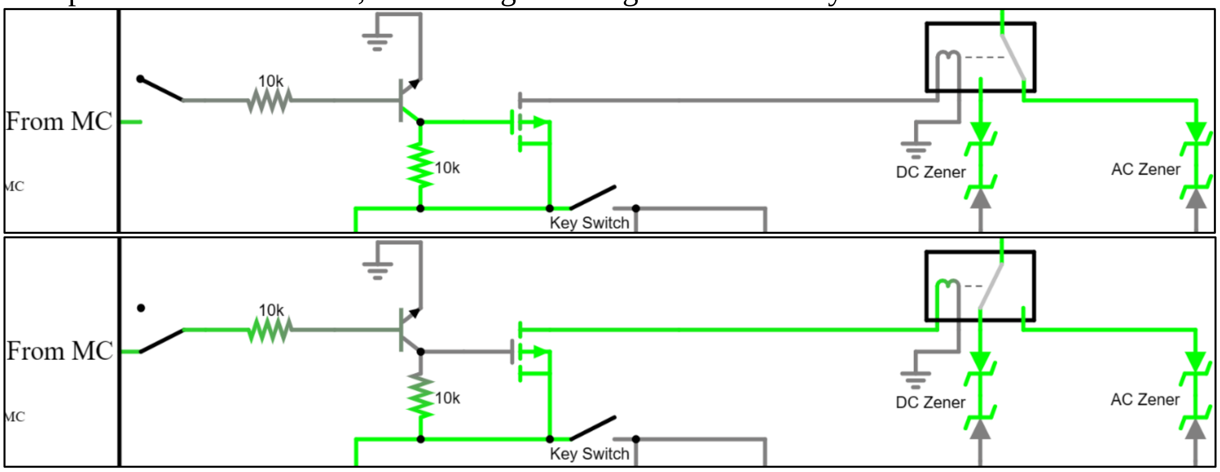

Figure 2-37: Falstad simulation showing microcontroller AC-DC output control.

Overall Functionality:
The simulation results confirm that the hardware interlock operates as intended, effectively controlling and limiting the output voltage and current based on the key switch's position. This validates the design's safety features and its ability to meet the project requirements.

2.4.7.4 Components

Component	Description	Purpose	Count
RY211005R	SPDT Relay Switch	Interlock Enable/Disable & Swap between AC & DC Zener Pathway	3
HPZR-C70X	70 V Zener Diode	AC Limiting Zener	2
BZD27C100P-E3-08	100 V Zener Diode	DC Limiting Zener	2
BC54-10PAS-QX	NPN Transistor	Controls the Gate Pin on the MOSFET	1
PMV50XPAR	P Type MOSFET	Swaps the AC/DC Relay (AC Low, DC High)	1
LED	Standard Red LED	On when Interlock Enabled	1

2.4.8 PCB Layout & Routing

2.4.8.1 Explanation

The process of designing and assembling a PCB is a critical phase in the development of electrical and electronic systems, and it plays a pivotal role in ensuring the functionality and performance of the final product. For this project, once the subsystem schematics had been carefully finalised by the respective team members, and the electrical connections and components were well defined, the focus shifted to the complexities involved in PCB layout and routing. This phase, while seemingly straightforward, represents a significant challenge in the journey towards realizing a functional prototype. For this project, the KiCad EDA tool [8] was used to produce the PCB design in its entirety.

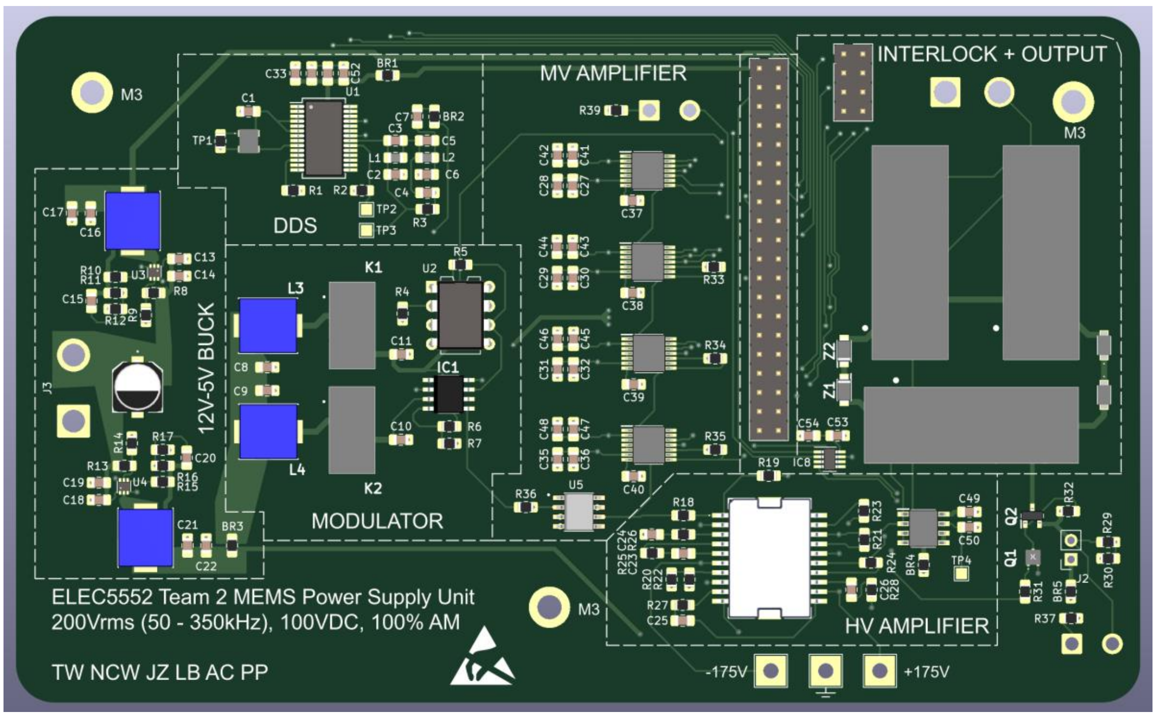

Figure 2-38: Top view of the final PCB design, rendered in KiCad

The complexities involved in PCB layout and routing arise from the need to accommodate components within a limited space, optimising for size and placement while adhering to mechanical constraints and form factors. Additionally, ensuring signal integrity and minimising electromagnetic interference (EMI) are top priorities. It requires careful planning to prevent signal loss, crosstalk, and distortion. Furthermore, the relatively high component count of this design combined with the various voltage sources meant that the task of coordinating routing was a difficult task. The PCB was chosen to be a simple 2-layer board (front & back copper layers only) to minimise cost, which also further increased the need for efficient layout and routing. The final PCB layout is shown in Figure 2-38 and Figure 2-39 as a render from the KiCad's built-in 3D viewer. This section will present the routing and layout philosophy for each subsection sequentially downstream of the $12V$ input, as well as a system-wide explanation.

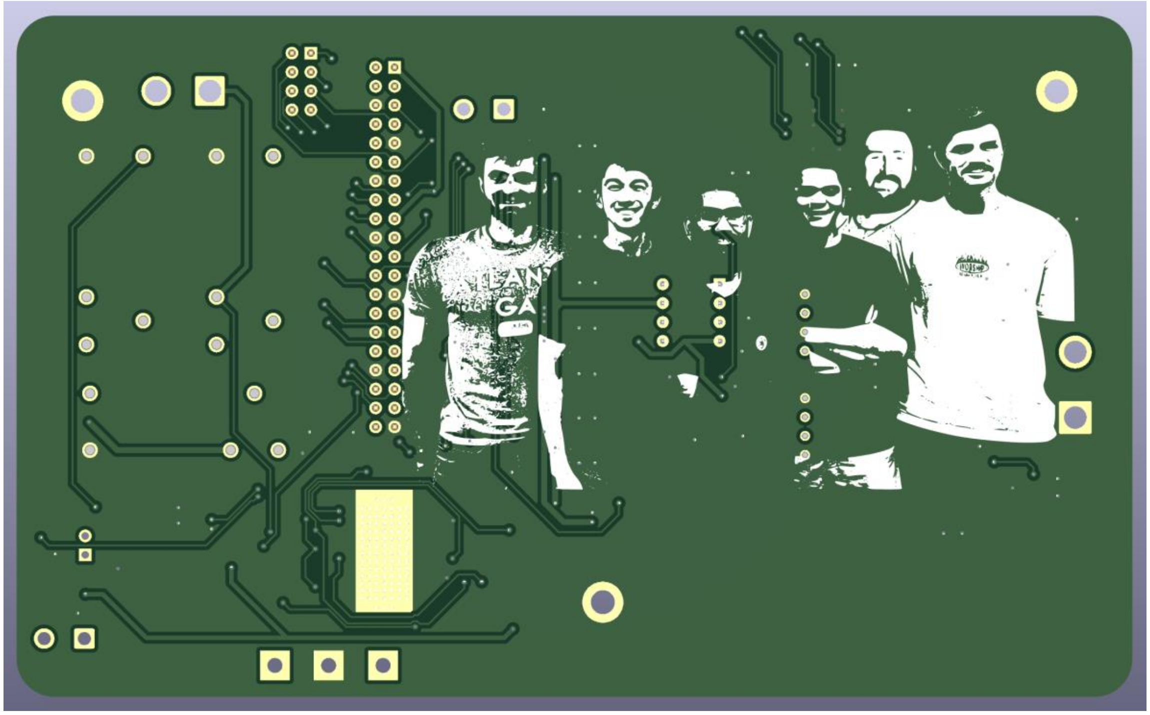

Figure 2-39: Bottom view of the final PCB design, rendered in KiCad showing the group picture on the silkscreen

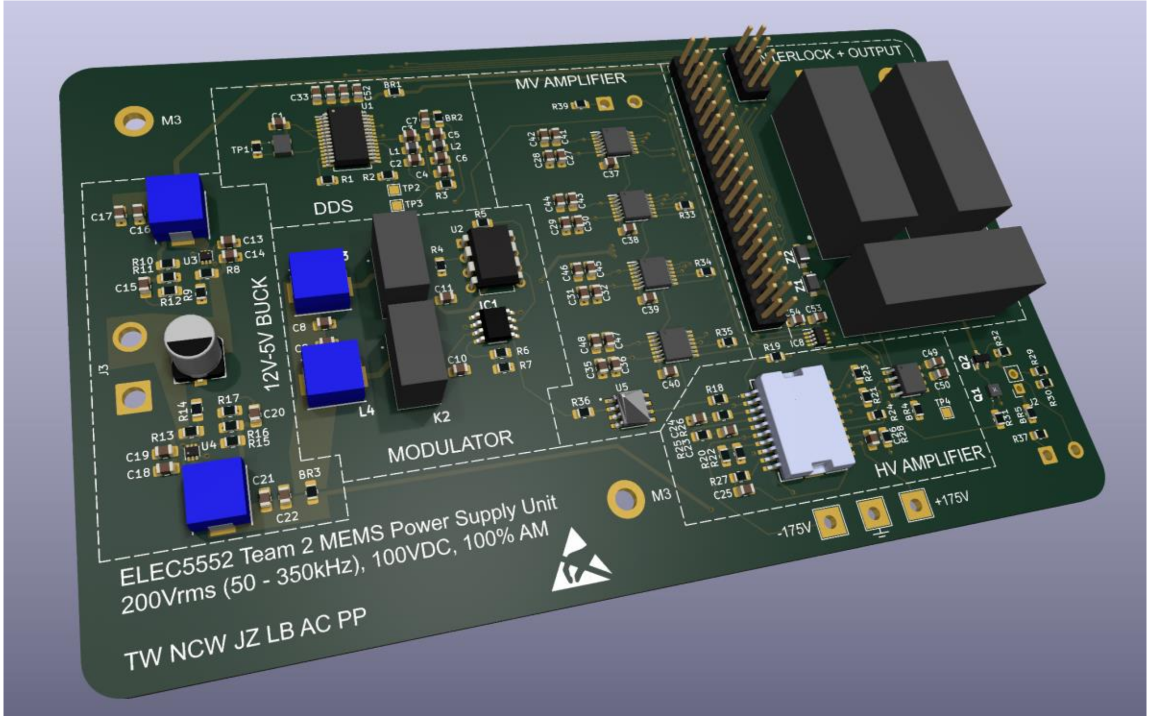

Figure 2-40: Perspective render of the top view of the PCB, showing the relative size of the components

2.4.8.2 Overall PCB Design

The overall final design of the PCB is shown in Figure 2-41 and satisfies REQ-035. The red traces and filled areas denote the top copper layer, whereas the blue traces and filled areas denote the bottom copper layer. Gold denotes through-hole pads, and the light yellow denotes items that will be printed on to the silkscreen, such as the board description on the bottom left, the Electrostatic discharge (ESD) sensitivity icon, and the subsystem dotted line borders. Utilisation of PCB was also essential for meeting the design constraint of size and weight (REQ-037), offering a compact and lightweight solution compared to a protoboard or direct wiring.

As is common practice, a large copper fill area (tied to the GND trace) covers most of the bottom copper layer. This allows easy, efficient connection from components to ground through usage of a via and reduces crosstalk/interference between components due to simpler return current paths. This is in accordance with REQ-036 to minimise EMI SFAIRP. Despite the desire to maintain as large a ground plane as possible, there were still many traces that interrupted the plane as they were required to be placed on the bottom layer due to space constraints. Each subsystem was laid out and routed, one at a time, and then placed as close as possible to each other before connecting the inter-subsystem traces.

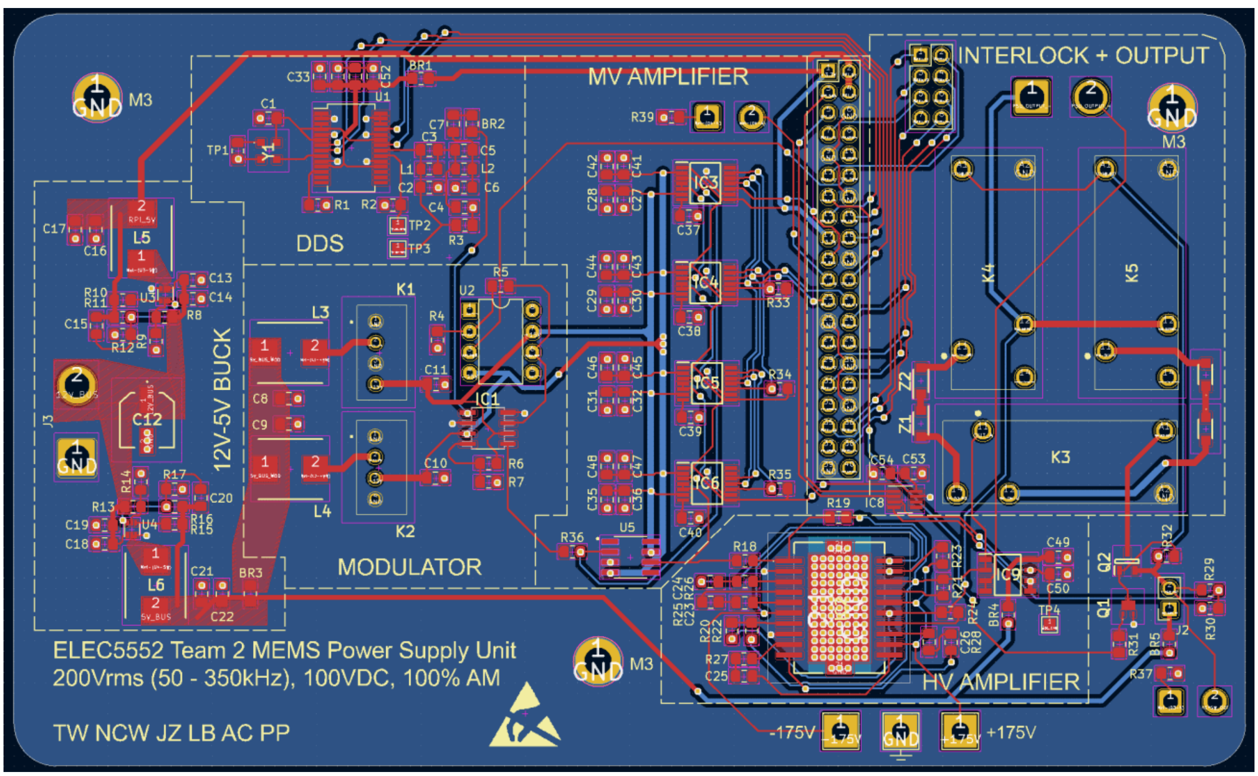

Figure 2-41: Overall PCB layout

2.4.8.3 Input & 12V to 5V Buck Converter

The first section in terms of power flow through the PCB is the $+12V$ input (including filtering capacitor) and $12V$ to $5V$ buck converter subsystem. Figure 2-42 shows the cropped and rotated subsystem layout. The large copper pours (hatched red areas) were used to maximise the effective cross-sectional area of the conducting sections for the input traces, as they supply essentially all of the current required for the entire power supply. The cluster of components to the right of the "$12V$ BUS" pad denotes the $5V$ buck converter circuit for the RPi, whereas the left-hand side cluster denotes the same buck converter circuit supplying power for the peripheral components via the BR3 solder bridge. The input filtering capacitor (C12) was placed as physically close to the input pads (J3) as feasible to ensure optimum noise decoupling.

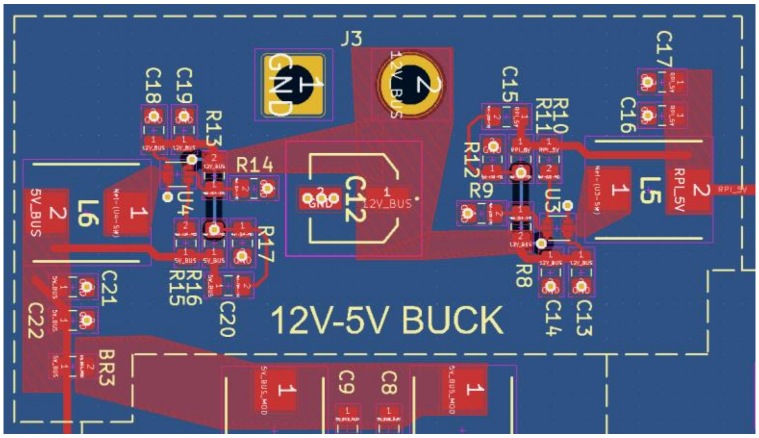

Figure 2-42: Input & $12V$ to $5V$ buck converter subsystem PCB layout and routing

2.4.8.4 Direct Digital Synthesis & Crystal Oscillator

The AD9850 DDS IC waveform generator (U1) is the heart of the design, and required careful trace routing and component selection to ensure signal distortion was minimised, as per REQ-038. The layout is shown in Figure 2-43. The $100MHz$ crystal oscillator (Y1) is placed close to the DDS to minimise trace inductance distorting the clock waveform and causing issues. A solder bridge and test points (TP2, TP3) are provided to isolate the IC's power input for testing purposes during assembly. The signal output trace does not travel above any bottom layer traces to minimise crosstalk.

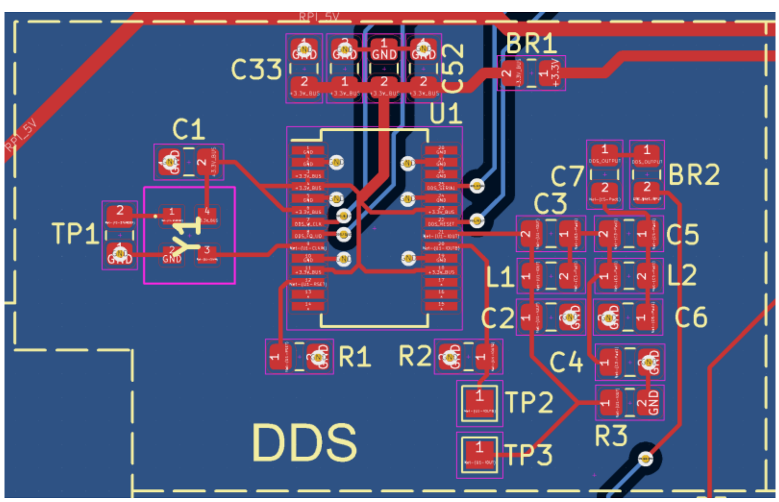

Figure 2-43: DDS & crystal oscillator subsystem PCB layout and routing

2.4.8.5 Modulator, $\pm 15\ V$ Power Supplies and Square Wave Amplifier

The $+15V$ and $-15V$ boost power supply ICs are shown in Figure 2-44 as K1 and K2, respectively. The LM741 (U2) op amp for square wave amplification, as well as the AD633 (IC1) analogue multiplier modulator, both have thick power traces routed to them from the $\pm 15\ V$ power supply pins. The 5 V power traces to the boost power supplies are brought into the subsystem via the large copper pour, on the left-hand side of the subsystem layout, to facilitate larger currents.

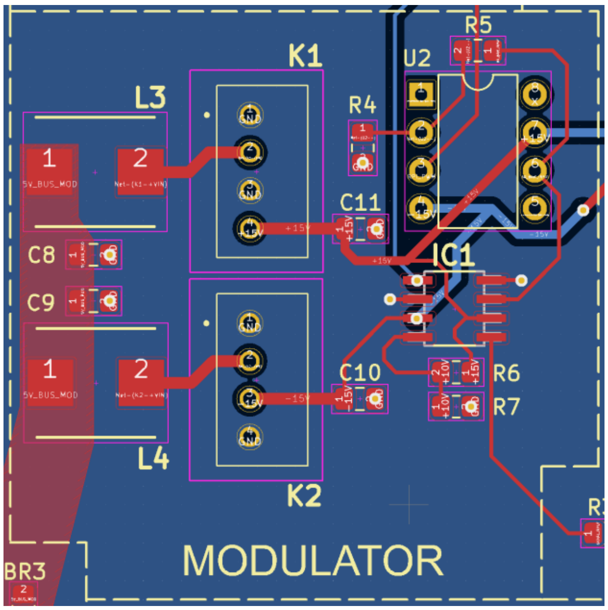

Figure 2-44: Modulator subsystem PCB layout and routing

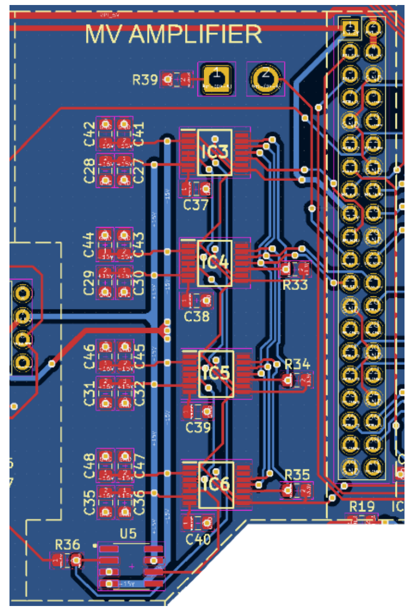

Figure 2-45: MV amplifier subsystem PCB layout and routing

2.4.8.6 MV Amplifier, Digital Potentiometers & RPi Connector

The $\pm 15V$ voltage source traces from the modulator subsystem are brought into this MV amplifier subsystem to power the 4 digital potentiometer ICs (IC3 – IC6) and the MV op-amp (U5). The layout and routing were straightforward and were mostly pre-determined by the datasheets of the components. The layout is shown in Figure 2-45 and includes the 2x20 pin header socket for the RPi-connecting ribbon cable on the right-hand side, placed in a manner to avoid physically interfering with other components

2.4.8.7 HV Amplifier & Current Sensor

As shown in Figure 2-46, the signal output from the MV amplifier is fed into the PA79 HV op amp. This component was essentially the only one with stringent thermal requirements due to the high slew rate required at $300kHz$ as well as the $\pm 175V$ power supply. For this reason, the large thermal pad in the centre has a rectangular break in the mask layer (teal) which exposes the large array of vias to the air contacting the bottom of the PCB, allowing greater thermal dissipation. Additionally, the 3 contacts are provided at the bottom for the $\pm 175V$ external power supplies to connect to. The current sensor (IC9) is oriented to provide efficient trace lengths.

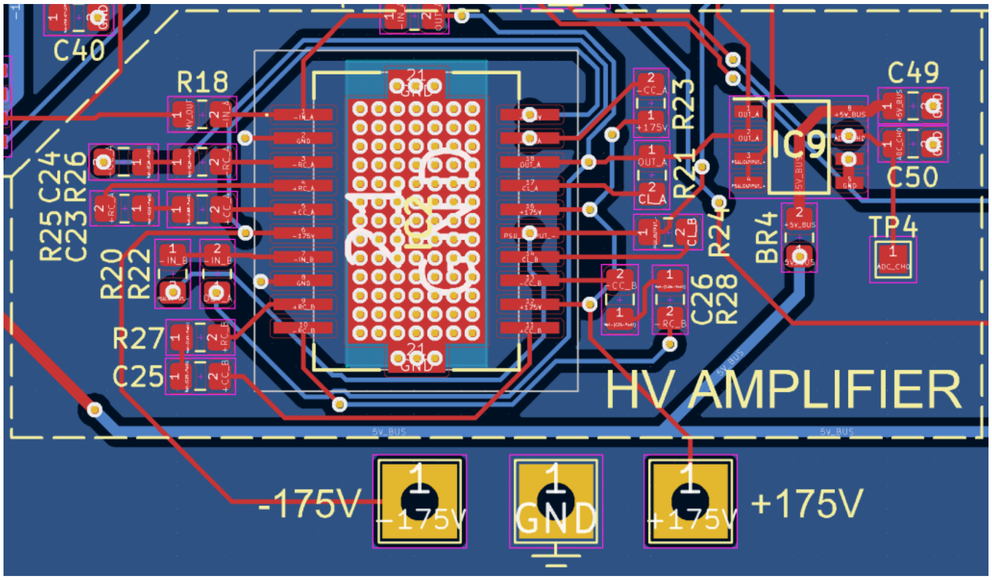

Figure 2-46: HV amplifier subsystem PCB layout and routing

2.4.8.8 Interlock, Output & Numpad Connector

The interlock & output subsystem, shown in Figure 2-47, contains the interlocking relays (K3 – K5), the 8 pin header for connecting the numpad to the RPi, the output pads to connect to the BNC connector with a pair of wires, the Zener diodes for the interlock protection mechanism, and other components. No special requirements existed for routing/layout.

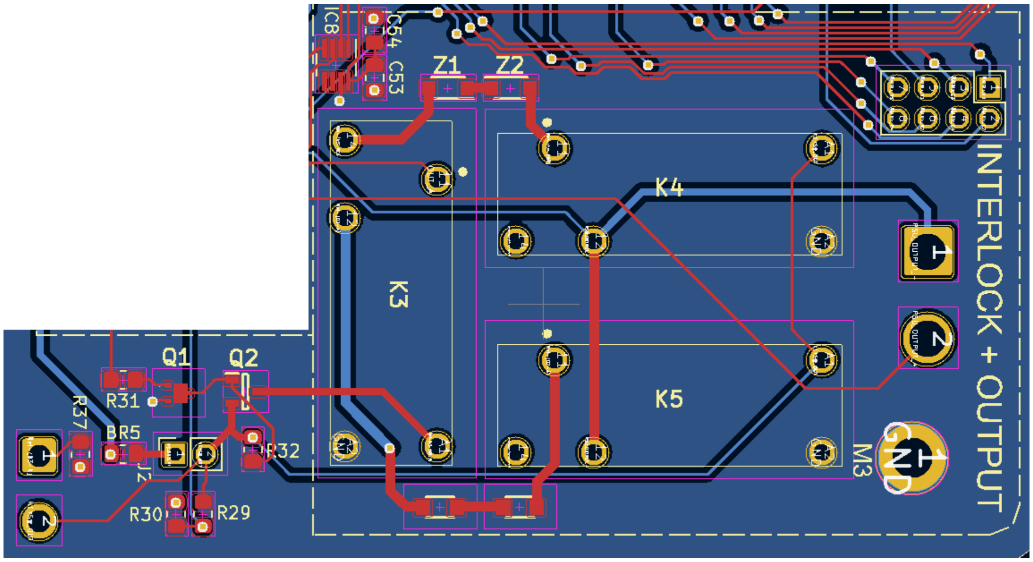

Figure 2-47: Interlock & output subsystem PCB layout and routing, rotated for ease of viewing

2.4.9 System Controller

2.4.9.1 Explanation

The RPi 3 Model B was selected as the MPU for the team's design. It should be noted that this is not a microcontroller with the main differentiator being that it works almost as similar as a desktop PC, with its own operating system called Raspbian, a standard and specialised version of Linux. The RPi was also chosen due to it having many inputs and outputs, including a DSI display port. The DSI display port allows for the simple integration of a screen to display a GUI for the device, as covered in section 2.4.10. The MPU allows for programming in Python and is what was chosen to create the GUI and control algorithms for the circuit components. This MPU also allows for future expansion. If the client prefers to be able to control and/or monitor the device externally, the RPi has Wi-Fi and Bluetooth capabilities to cater for this. The RPi 3 Model B board is shown in Figure 2-48, with its pinout diagram shown in Figure 2-49. Additionally, its specifications are shown in Table 2-5.

Figure 2-48: RPi 3 Model B board [9].

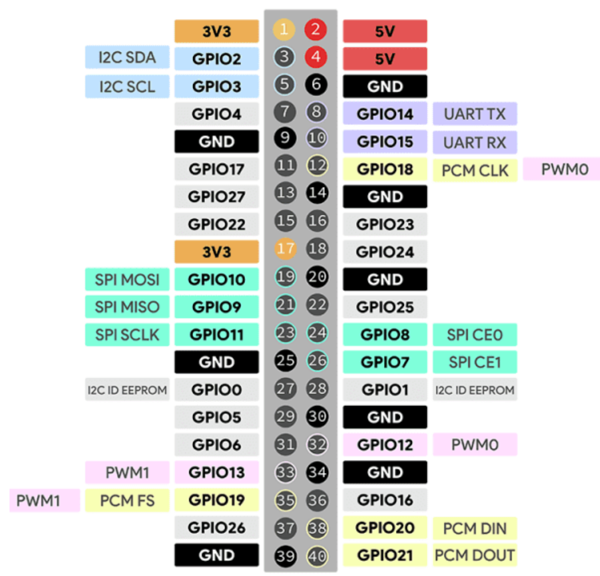

Figure 2-49: RPi 3 Model B pinout diagram [10].

Specification	Details
CPU	Quad Core 1.2GHz Broadcom BCM2837 64bit CPU
Memory	1GB RAM
Inputs and Outputs	BCM43438 wireless LAN and Bluetooth Low Energy (BLE) on board
	100 Base Ethernet
	Low-Level Peripherals: • 27 x GPIO • UART • I2C Bus • SPI Bus with Two Chip Selects
	4 USB-A ports
	4 Pole stereo output and composite video port

	Full size HDMI
	CSI camera port for connecting a RPi camera
	DSI display port for connecting a RPi touchscreen display
	Micro SD port for loading your operating system and storing data
Power Requirements	$5V$
	$2.5A$

Table 2-5: RPi 3 Model B specifications.

2.4.9.2 Requirements Met

This section of the overall design was implemented to explicitly meet REQ-013. By choosing the RPi 3 Model B, this requirement is met. Whilst this section only directly meets this single specific requirement, it is crucial that this requirement be met as without it, essential components of the design would not be able to function.

2.4.10 Display of Information

2.4.10.1 Explanation

The TFT RPi DSI touchscreen was selected as the display for the team's design. Its 5-inch size was deliberately selected to provide a user-friendly interface, ensuring system parameters can be easily viewed and updated by the user. The screen is used to display the following system parameters:

- Voltage value
- Signal frequency value
- Overcurrent protection value
- Voltage type being outputted (AC or DC)
- Whether the signal is being modulated (Yes or No)
- Modulation Frequency

The screen is shown in Figure 2-50, with its connection to the RPi shown in Figure 2-51. Additionally, its specifications are shown in Table 2-6.

Figure 2-50: 5" 800x480 TFT RPi DSI touchscreen [11].

Figure 2-51: RPi 3 Model B mounted onto the touchscreen and connected via a flat flex jumper cable [12].

Specification	Details
Power Requirements	$3.3V$
	$320mA$
Resolution	800x400
Number of Touch Points	5
Refresh Frequency	$60Hz$
Size	5 inches ($121mm \times 76\ mm$)

Table 2-6:RPi DSI touchscreen specifications.

2.4.10.2 Requirements Met

This section of the overall design was implemented to meet REQ-012 and REQ-019. The LED is connected to the input of the hardware interlock allows for REQ-012 to be achieved. REQ-019 is achieved with the device status LED and the use of the display. The advantage of the larger display becomes apparent, as it not only enhances the user experience but also reduces the necessity for numerous LEDs due to its capacity to efficiently display lots of information.

2.4.11 Physical Interface for User Inputs

2.4.11.1 Explanation

The 4x4 matrix keypad was selected as the physical interface for user inputs for the team's design. The primary reason for this is because each key on the keypad can be programmed to do what is required. The 4x4 matrix keypad shown in Figure 2-52 has been programmed to map its keys' functions as depicted in Figure 2-53. The functionality of each key is shown in Table 2-7. This functionality has been chosen so that a user is able to easily navigate through the system menu on the display and update any system parameters as required.

Figure 2-52: Original 4x4 matrix keypad [13].

Figure 2-53: Modified 4x4 matrix keypad.

Keys	Functionality
0-9	Used to enter numbers to update numeric system parameters, such as voltage and frequency
*	Used to switch between pages on the display
#	Used to enter a decimal place
A	Used to scroll up
B	Used to scroll down
C	Used as a backspace
D	Used as an enter key

Table 2-7: Description of the functionality of each key on the matrix keypad.

2.4.11.2 Requirements Met

This section of the overall design was implemented to directly meet REQ-014 and REQ-025. This is because the matrix keypad provides a physical interface for a user to change system parameters. This section also indirectly meets REQ-006, REQ-020, REQ-021 and REQ-022. This is because the matrix keypad allows users to enter in values to allow for adjustments in the required step size for voltage, frequency, and overcurrent protection.

2.4.12 Power Supply Enclosure

2.4.12.1 Explanation

In accordance with REQ-008, an enclosure for the device was modelled in SolidWorks to enable safe handling and containment. The enclosure and lid were created in a SolidWorks assembly to ensure perfect fitment of all parts, as seen in Figure 2-54 and Figure 2-55. The enclosure & lid models were 3D printed out of flame retardant (UL-94) ABS [14].

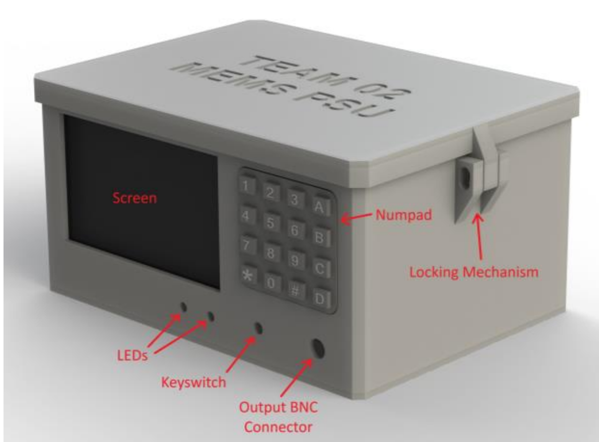

Figure 2-54: External view of rendered 3D model

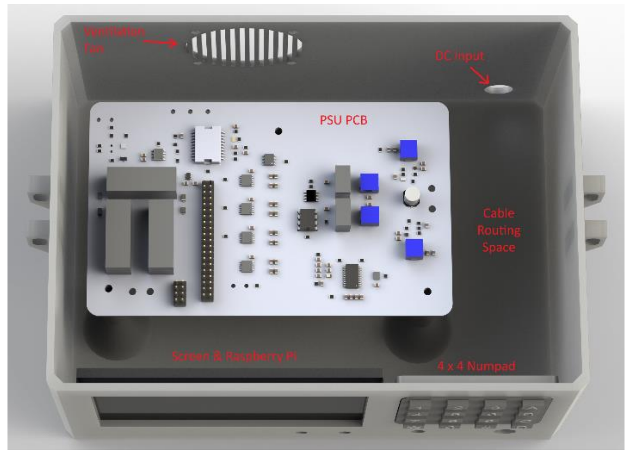

Figure 2-55: Internal view of rendered 3D model

2.4.12.2 3D Printed Enclosure

The final build of the PSU is shown in Figure 2-56, Figure 2-57, and Figure 2-58 below.

Figure 2-56: Front of the 3D printed enclosure

Figure 2-57: Back of the 3D printed enclosure

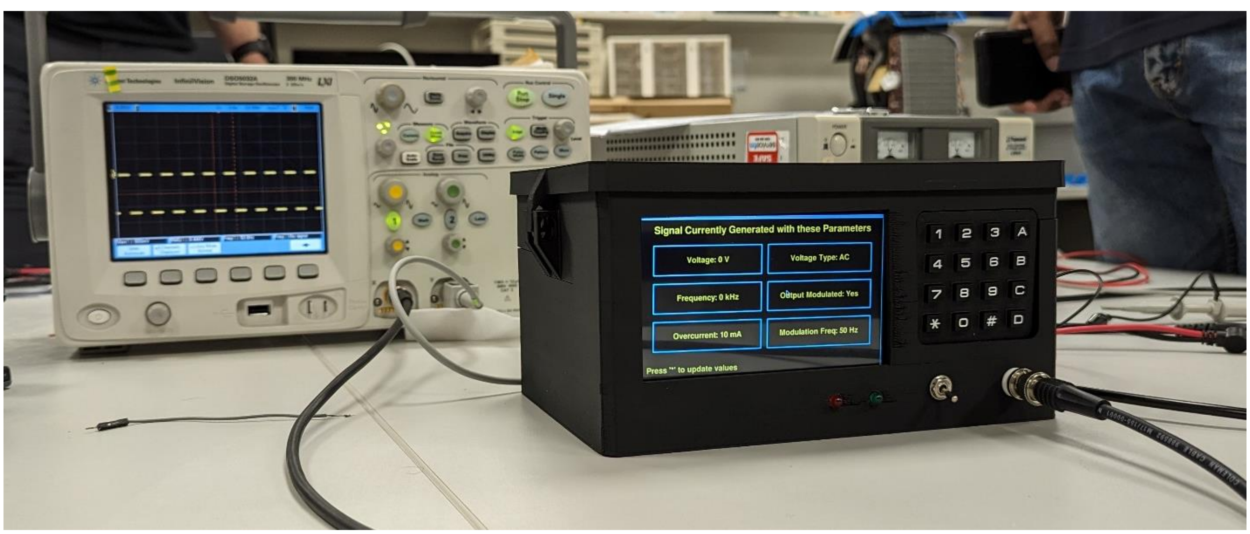

Figure 2-58: The PSU (with GUI shown) during demonstration outputting a square wave

2.4.13 Software: User Input & Display

2.4.13.1 Overview

The User Input & Display section of the software is primarily focused on the interface between the user and the system. It employs Python's Pygame library to create a graphical user interface (GUI) and the RPi.GPIO library to handle hardware interactions between the user and the matrix keypad. The overall architecture of the software system can be found in Figure 4-1. This part of the software allows users to input various parameters such as voltage, frequency, and overcurrent protection settings.

2.4.13.2 Code Functionality & Workflow

User Interface Initialisation:
The Pygame library is used to initialise the graphical user interface (GUI). The constants LENGTH_RES, WIDTH_RES, DISPLAY_BOX_WIDTH, and DISPLAY_BOX_HEIGHT define the screen resolution and dimensions of various display boxes. The GUI includes buttons and input fields that allow the user to modify settings.

Keypad Input Handling:
The matrix keypad is managed by a separate Python script that uses the RPi.GPIO library. The keypad() class contains the getKey() method, which scans the rows and columns of the keypad to detect a keypress. Once a key is pressed, the function returns the corresponding value, which is then used to modify parameters such as voltage, frequency, or overcurrent protection.

Parameter Validation:
Before any new value is set, validation functions is_valid_voltage(), is_valid_frequency(), and is_valid_overcurrent() are called. These functions check if the entered values are within the specified limits and are valid according to the requirements.

Display Updates:
The display_values() function is responsible for updating the GUI to reflect the current settings. Utility functions text_xy_centered(), text_x_centered(), and text_y_centered() are used to position the text correctly within the display boxes.

Error Handling:
If an invalid value is entered or an error occurs, the display_error_msg() function is called to display an error message on the screen.

Confirmation and Setting New Values:
Before a new value is officially set, the confirm_new_value() function displays a confirmation screen. If the user confirms, the set_new_value() function updates the parameter.

2.4.13.3 Requirements Met

The code utilises the RPi to run the software, fulfilling REQ-013. It also includes a physical interface for user inputs, meeting REQ-014. The GUI displays the status of the device through a combination of display and LEDs, in line with REQ-019.

2.4.13.4 Justification

The software's user interface was rigorously tested to ensure it meets the specified requirements. Various test cases were executed to validate the functionality of the keypad, display, and error messages.

1. Keypad Testing: The keypad was tested for all possible keypresses, including invalid inputs. The system correctly identified and processed each keypress, confirming the fulfillment of REQ-014.

2. Display Testing: The GUI was tested for clarity, responsiveness, and accuracy in displaying the device's status. The display successfully updated in real-time as parameters were changed, meeting REQ-019.

3. Error Message Testing: Error messages were triggered intentionally by entering invalid values. The system correctly displayed the error messages, providing the user with clear guidance on how to proceed.

4. MPU Utilisation: The software was successfully deployed on a RPi, confirming that it meets REQ-013.

5. Integration Testing: Finally, an integration test was conducted to ensure that the user interface worked seamlessly with other components of the system such as the matrix keypad, hardware interlock and LEDs.

Through these tests, the software has been verified to meet all the requirements related to user input and display, providing a robust and user-friendly interface.

2.4.14 Software: DDS Signal Generation

The DDS module requires software to set the frequency of the signal that is generated. This functionality is handled by the AD9850 class. Utilising the AD9850 frequency generator, the software allows for precise control of the output frequency ranging from 50kHz to 300kHz in AC mode. Overall code is designed to be both flexible and accurate, ensuring that the user can set the desired frequency easily.

2.4.14.1 Code Functionality & Workflow

The code written for the control of the DDS module is broken down into the following components, allowing for modular design and integration:

Initialisation:
The __init__ method in the AD9850 class sets up the GPIO pins and clock frequency for the AD9850 module. It also calls the initialise method to reset the AD9850 and prepare it for operation.

The PWM script sets the GPIO mode to BCM and initializes the PWM frequency and duty cycle.

Pulse Generation:
The pulse method in the AD9850 class generates a pulse on a given GPIO pin. This is essential for clocking data into the AD9850.

Setting Frequency:
The set_frequency method in the AD9850 class takes the user-defined frequency and AC mode status as inputs. It calculates the 32-bit frequency word based on the clock frequency and sends it to the AD9850. If the AC mode variable is set to False, the frequency will be set to 0Hz.

Data Sending:
The frequency and phase words in the AD9850 class are sent bit-by-bit to the AD9850 using GPIO pin toggling, controlled by the pulse method.

User Input:
The main part of the AD9850 code demonstrates how the user can input the desired frequency and whether AC mode is enabled. These values are then passed to the set_frequency method for processing.

2.4.14.2 Requirements Met

Frequency Control:
The set_frequency method in the AD9850 class allows for an AC output frequency of 50 – 300kHz sine wave, meeting REQ-015. The function also validates the frequency values, ensuring they are within the specified limits. It also validates the user input to ensure that it is a multiple of 10kHz, meeting REQ-021.

User Input and Digital Control:
The main part of the AD9850 code accepts user inputs, meeting REQ-025. These inputs control the output type.

2.4.14.3 Justification & Testing

This section of the software has undergone rigorous testing to ensure it meets the specified requirements. Here's how each requirement has been justified or tested:

REQ-015: AC Output Frequency of 50 – 300kHz:
The set_frequency method in the AD9850 class was tested across the entire range of 50 - 300kHz. Test code was written to determine if the correct values were being outputted once a frequency value was entered. It was also tested to verify that an error message occurs when a frequency value outside of the 50 – 300kHz range is entered.

REQ-021: Frequency Adjustments in Steps of 10kHz:
Test code was written to ensure that if the frequency value entered is not a multiple of 10kHz, an error message occurs.

REQ-025: Digital Input Control:
The software was tested to ensure that all controls could be manipulated via digital input. This was verified through both automated and manual testing, where the output was observed to change according to the digital input.

2.4.15 Software: Modulation Control

This section of the software is handled by a script that controls the Pulse Width Modulation (PWM) pin on the RPi. The code is designed to be both flexible and accurate, ensuring that the user can set the desired modulation parameters easily.

2.4.15.1 Code Functionality & Workflow

The frequency of the modulating signal needs to be controlled by the user. The user is able to set the frequency by entering a value between 10 and100Hz, in 10Hz steps. As mentioned in section 2.4.4, the RPi needs to produce a square wave with a magnitude of 3.3V at a set frequency. To achieve this, a duty cycle of 50% was used. When the signal modulation is turned off by the user, the duty cycle changes to 100%, producing a constant 3.3VDC.

Initialisation:
The PWM initialisation starts by setting the PWM pin to output and setting the duty cycle to 50%.

Modulation Control:
The PWM script allows the user to input a new frequency for modulation. It checks if the frequency is within a valid range and if the modulation setting has been turned on. If the setting is turned on, the frequency will update and the duty cycle will be set to 50%. Otherwise, the duty cycle will be set to 100%.

Error Handling:
The PWM script includes a check to ensure that the entered frequency is within 10-100Hz and a multiple of 10Hz, providing an error message if it's not.

2.4.15.2

Modulation Control:
The separate PWM script allows for a switchable output 100% amplitude modulated signal, fulfilling REQ-016. The script also allows for frequency adjustments in steps of 10Hz, meeting REQ-027.

2.4.15.3 Justification & Testing

This section of the software has undergone rigorous testing to ensure it meets the specified requirements. Here's how each requirement has been justified or tested:

REQ-016: Switchable Output 100% Amplitude Modulated Signal:
The PWM script was tested to ensure that it could produce a square wave.

REQ-025: Digital Input Control:
The software was tested to ensure that all controls could be manipulated via digital input. This was verified through both automated and manual testing, where the output was observed to change according to the digital input.

REQ-027: Frequency Adjustment for Square Wave in Steps of 10Hz:
Similar to REQ-021, the code was tested to confirm that the frequency of the square wave could be adjusted in steps.

Through these tests, the Modulation Control section of the software is robust, reliable, and meets all the specified requirements.

2.4.16 Software: Voltage Control

The Voltage Control section of the software is responsible for managing both DC and AC output voltages. It utilises the ADC code to measure current and set voltage limits, ensuring safe operation. This section also allows for fine-grained control over the output voltage, with adjustments possible in small steps. It is designed to be user-friendly while meeting all specified requirements for voltage control.

2.4.16.1 Code Functionality & Workflow

Initialisation:
The ADC is initialised to measure the current, which is essential for voltage control. The current_send_config() function sets the configuration byte based on the reference voltage, either "Supply Voltage" or "External."

User Input:
The user can set the desired output voltage through the main GUI. The value entered is captured and sent for validation.

Validation:
The is_valid_voltage() function checks if the entered voltage is within the specified limits (0 – 200V for DC and AC). It also checks for hardware interlock limits.

Setting Voltage:
Once validated, the voltage value is set. This is done by the sending the corresponding signals to the digital potentiometers to set their resistance.

2.4.16.2 Requirements Met

Voltage Control:
The is_valid_voltage() function in the main script validates the DC and ACoutput voltage ranges and increments, meeting REQ-001, REQ-003 and REQ-020. It also ensures that the hardware interlock limits for DC and AC voltages are adhered to, fulfilling REQ-002 and REQ-004.

2.4.16.3 Justification & Testing

The voltage control functionality was rigorously tested to ensure that it meets the specified requirements. For instance, the is_valid_voltage() function was subjected to a variety of test cases to validate its effectiveness in limiting the output voltage according to the hardware interlock settings. This ensures that the system is safe to operate and complies with requirements REQ-002 and REQ-004.

User inputs were tested for robustness and ease of use. The system was found to be user-friendly and intuitive, allowing for quick and easy adjustments to the output settings. This fulfills REQ-025, which calls for a digital input method to control various output parameters.

Through these tests, it was confirmed that the voltage control section of the software is not only functional but also robust and user-friendly, fully meeting the stipulated requirements.

The software also integrates hardware interlock control. It continuously checks the status of the interlock. If the interlock is enabled (low signal), the maximum allowable voltage is limited to 100V for DC and 50Vrms for AC. If the interlock is disabled (high signal), the voltage limits are increased to 200VDC and 200Vrms for AC. This dynamic adjustment of voltage limits based on the interlock status adds an extra layer of safety.

2.5 System Integration

2.5.1 Software: Protective Measures

This section of the software focuses on implementing safety features to protect both the hardware and the user. It includes mechanisms for overcurrent and overvoltage protection, as well as hardware interlock control. Utilising the ADC for real-time current sensing, the software can rapidly disengage the output in case of an overcurrent situation. Additionally, it monitors the hardware interlock status to ensure that the system operates within safe voltage limits.

2.5.1.1 Code Functionality & Workflow

The Protective Measures software is designed to ensure the safety of the system and the user by monitoring and controlling various parameters. It uses the ADC (Analog-to-Digital Converter) to continuously measure the current and checks for overcurrent conditions. If an overcurrent is detected, the software immediately shuts off the output within a specified time frame, thereby meeting the safety requirements.

Interlock Control:
The software also integrates hardware interlock control. It continuously checks the status of the interlock. If the interlock is enabled (low signal), the maximum allowable voltage is limited to 100VDC for DC and 50Vrms for AC. If the interlock is disabled (high signal), the voltage limits are increased to 200VDC and 200Vrms for AC. This dynamic adjustment of voltage limits based on the interlock status adds an extra layer of safety.

Error Handling:
In addition to overcurrent and overvoltage protection, the software also includes robust error handling features. If an invalid value is entered or an error occurs, an error message is displayed to the user, guiding them to take corrective action.

This workflow ensures that the software is not only user-friendly but also robust, with multiple layers of validation and error handling. It's designed to be fully compliant with the hardware it controls, thereby providing a seamless and safe user experience.

2.5.1.2 Requirements Met

Current Control and Protection:
The ADC code provides an adjustable output maximum current cutoff, fulfilling REQ-005 and REQ-006. The code also includes a mechanism to switch off the output in under 10 milliseconds in case of overcurrent, meeting REQ-007.

User Interface and Control:
The code utilizes a combination of a display and LEDs to indicate the status of the device, in line with REQ-019. It also allows for current limit adjustments with steps of 2mA, meeting REQ-022.

Interlock Control:
The software dynamically adjusts the maximum allowable voltage based on the interlock status, although this is not explicitly a requirement, it adds an extra layer of safety. The design also includes a visual indication light to show when the interlock is engaged or disengaged, fulfilling REQ-012.

2.5.1.3 Justification/Testing

This section of the software is crucial for ensuring the safety and reliability of the device. The code has been rigorously tested to confirm that it meets all the specified requirements.

Current Control and Protection:
The ADC code was tested under various conditions to ensure that it accurately measures the current and triggers the overcurrent protection mechanism within the specified time frame. The tests confirmed that the device switches off the output in under 10 milliseconds when an overcurrent condition is detected, thereby meeting REQ-007.

Hardware and Safety:
The RPi is housed in a sealed, self-extinguishing case, satisfying REQ-008 and REQ-009. The visual indication light was tested to confirm that it accurately shows the status of the interlock, fulfilling REQ-012.

User Interface and Control:
The combination of a display and LEDs was tested to ensure that they provide a clear and accurate indication of the device's status, meeting REQ-019. The current limit adjustments were tested and

confirmed to be in steps of 2mA, in line with REQ-022.

Interlock Control:
The interlock control was tested to ensure that it dynamically adjusts the maximum allowable voltage based on its status. When the interlock is enabled, the maximum voltage is limited to 100V for DC and 50Vrms for AC. When disabled, the maximum is set to 200VDC and 200Vrms for AC. This feature, although not explicitly a requirement, adds an extra layer of safety and was confirmed to work as intended during testing.

2.5.2 Data Flow Overview

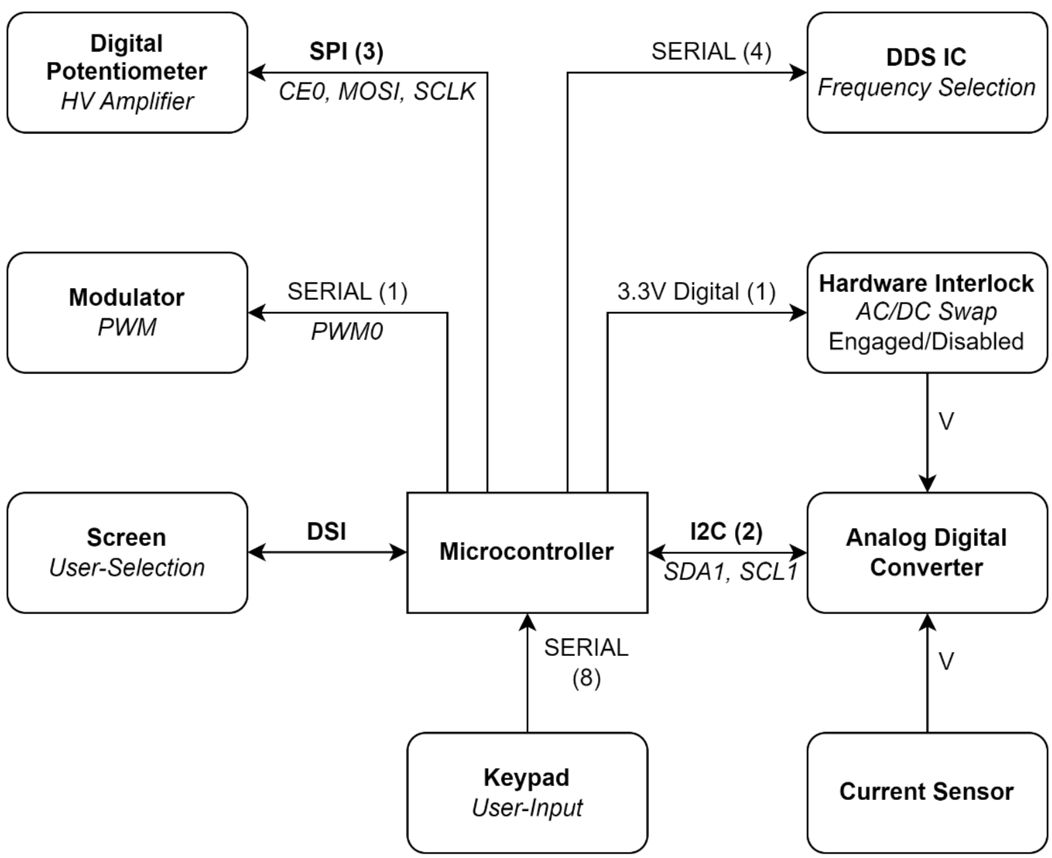

Figure 2-59: Flowchart representing data flow within the system.

2.5.3 Critical Interfaces

Physical connections within the designed power supply allows the output as the user requested. Such physical connections and direction of data flow are displayed in Figure 2-59. For modulation requirements to be met, there is one serial connection from the MPU to the modulator. This connection needs to have the Pulse Width Modulation (PWM) functionality, and that is due to the required frequency of the pulse for the square wave generation from the modulation module. The normal GPIO pins are not capable of creating pulses fast enough as required, hence the need for a

PWM pin.

For the signal generation, the DDS IC is connected via four serial pins, and these connections can be seen in Figure 2-6. The "DDS_Serial", as seen in Figure 2-6, is used to send data to the DDS IC when a change in frequency is requested by the user. The second pin called "DDS_W_CLK" is a manually created clock which is in sync with the clock of the RPi and the purpose of the pin is to send continuous pulses. On the rising edge of these continuous pulses, the DDS IC, reads one bit from the "DDS_Serial" pin, and this process is repeating forty times until the new requested frequency is acknowledged by the DDS IC. Once the data is read, a signal from the "DDS_FQ_UP", which lets the DDS IC update the outputting frequency to the requested frequency.

To output the requested voltage, communication with the digital potentiometer is critical. The communication is done through three SPI pins, as seen in Figure 2-14. The pins require special functionality which are the SCLK and MISO pins. The SCLK and pin labelled "DIG_POT_SS" are connected to all four digital potentiometers and the pin called "DIG_POT_MOSI" is connected to the first digital potentiometer. From the first potentiometer, a daisy chain connection is established, which transfers data from the first digital potentiometer to the next, in the form of chain between the four potentiometers. All the before mentioned pins and direction of communication can be better understood by viewing Figure 2-59 and Table 2-8.

2.5.4 Dependencies

- Pygame: For the graphical user interface (GUI)
- RPi.GPIO: For RPi GPIO control
- matrixKeypad_RPi_GPIO: For keypad input
- smbus2: For I2C communication with the ADC
- spidev: For SPI communication with the digital potentiometers

Some ICs depend on specific timings, one example of this is the DDS IC. The DDS pulse width requires a specific value. For example, the minimum pulse width high needs to be $3.5ns$ as well as the minimum pulse width low. This needs to be considered. If the timings are not met, the functionality of the DDS chip will fail. Furthermore, the ADC timings are important to consider, as that will determine the accuracy of current reading values.

The keypad is connected via eight physical connections, which allows the inputs from the user to be registered in the MPU and following that are specific instructions sent to the other elements shown in Figure 2-59. The transferring of data occurs when the user presses a button on keypad, causing a signal to be send via one of the eight serial pins. Following that, the screen has one physical connection which is the DSI connection, and this is ultimately dependent on the keypad and the MPU. This is because data to and from the screen are communicated through the DSI connection based on the inputs given by the user via the keypad.

2.5.5 Safety Measures

Overcurrent protection switches the output off, when the current at the output is above the limit set by the user. The way to accomplish this is by establishing a communication with the current sensing IC. This communication is done through I2C protocol. Directly communicating with the current sensing IC is not possible, hence, an ADC is used, such that the current sensing IC is able to relay sensed current in the form of analogue input, which the ADC converts it into digital format, sending it to the MPU. One of the safety measures other than the overcurrent protection is the hardware interlock. The hardware interlock is connected via a digital connection. This connection is used to indicate whether AC or DC is selected by the user. This connection is shown in Figure 2-59 and is listed in Table 2-8.

2.5.6 Pin Connections & Wiring Diagram

Table 2-8: I/O Register.

Component	**PIN**	**Direction**	**PIN2**	**Component2**	**Alternative Functions**	**Protocol**	**PURPOSE**
RPi	GPIO 2	TO	ADC_SCL	Analog Digital Converter	SDA1	I2C	Clock
RPi	GPIO 3	FROM	ADC_SDA	Analog Digital Converter	SCL1	I2C	Data Write & Read
RPi	GPIO 4	FROM	MATRIX_R1	Keypad			
RPi	GPIO 5	FROM	MATRIX_R2	Keypad			
RPi	GPIO 6	FROM	MATRIX_R3	Keypad			
RPi	GPIO 7	FROM	MATRIX_R4	Keypad	CE1	SPI	
RPi	GPIO 8	TO	SYNC	Digital Potentiometer: IC3-6	CE0	SPI	
RPi	GPIO 10	TO	MOSI	Digital Potentiometer: IC3	MOSI	SPI	
RPi	GPIO 11	TO	SCLK	Digital Potentiometer: IC3-6	SCLK	SPI	
RPi	GPIO 16	TO	MATRIX_C1	Keypad			
RPi	GPIO 17	TO	MATRIX_C2	Keypad			
RPi	GPIO 18	TO	V^+	Modulator: U2M741	PWM0		
RPi	GPIO 19	TO	MATRIX_C3	Keypad		SPI	
RPi	GPIO 20	TO	MATRIX_C4	Keypad		SPI	

RPi	GPIO 22	TO	W_CLK	DDS			Write
RPi	GPIO 23	TO	FQ_UD	DDS			Set
RPi	GPIO 24	TO	SERIAL	DDS			Read
RPi	GPIO 25	TO	RESET	DDS			Reset
RPi	GPIO 27	TO	Base	Interlock: NPN Transistor			
RPi	DSI	TO	DSI	Screen			

2.6 Stakeholder Engagement

Throughout the design process, several methods of stakeholder engagement were conducted with the client. To ensure a complete design, engagement with the client was paramount. For this project, the client contacts were Dilusha Silva and Michal Zawierta. Active communication ensured that the scope of the project did not creep as well as ensuring that the client was satisfied with any deviations from the original intended design.

2.6.1 Technical Queries Register

The Technical Query (TQ) register was predominantly used during early stages of the design development process. The register enabled the team to seek clarifications in a professional manner. This ensured the final design would align with what the client is expecting to receive.

TQ Number	Question	Answer
1	What are the clients preferred frequency step change for the carrier signal (50-$300kHz$)?	~$10kHz$ step is sufficient
2	Can the client confirm the modulation index will be fixed at 1 (i.e., 100%)?	Yes - two states: no modulation or 100% modulation with modulation frequency step ~$10Hz$
3	What is a reasonable time for the 'fast' over-current protection to kick in?	Response time in a range of single milliseconds up to tens of milliseconds to prevent device damage. If it can be faster, it would be even better.
4	Which controls would you like to control with a digital input?	Output type (DC/AC), voltage, modulation (ON/OFF), output enabled. Optionally: current limit. The digital control can be implemented as physical switches + display/LEDs or serial (USB)

		communication
5	Can we use any microcontroller? or does the client have a preferred microcontroller.	There is no preference here.
6	How distorted can the sine wave be?	As low as possible (within budget). The group should define what are limitations of particular design.
7	For the hardware interlock system, what is the preferred method?	Key, switch, or even exposed jumper should be ok
8	Can we provide buttons on the panel instead of a keyboard?	Yes
9	Does the project have to be controlled by a computer? (Aka. being plugged into a computer and it controls the power outputs?)	No, can be controlled by the buttons and state displayed using LEDs and/or display
10	For the testing above $30V$ needing to be supervised by a supervisor is this an AC limit or a peak limit?	AC_{rms}
11	How would one represent an expected 10-year life cycle without destructive testing? Can we use expected lifetimes, or do we need to perform accelerated testing.	Use of expected lifetimes should be ok. However, if you determine that it is not enough, please proceed with accelerated testing.

2.6.2 Design Review

Two design review presentations were held throughout the design process. Both reviews were presented to an independent facilitator. Whilst the facilitator was unable to provide specifics of the intended design, the feedback ensured that the design process was in fact being followed. The first design review was specifically focused on the design elements and the integration of each team members design. The second design review was primarily focused on following up actions from the first design review.

Design Element	Team Discussion / Query	Resulting Action
Interlock	Minor concern regarding the Zener diode's ability to handle the large range of frequencies.	Further modelling and investigation to confirm the diode could handle the large spectrum of frequencies.
Signal Modulation	Signal modulation output is directly related to the output of the DDS. Output of DDS needed to be	DDS team prioritised the design such that the output of the DDS could be observed

	confirmed before the modulation design could be finalised.	(theoretically). This enabled the modulation design to progress.
DDS	The DDS frequency range is limited by the input clock. Will this affect the designs capabilities?	The DDS input clock will utilise a crystal oscillator which has a frequency much greater than required for the operating conditions of the testing power supply.
Measurement and Control	The RPi has a limited ADC inbuilt. This would limit the accuracy and capabilities of the design.	An external ADC was integrated into the design to ensure the design can operate and intended.
Microcontroller and User Interface	Discussion around how the data should be presented visually was a point of contention. The LCD screen was favoured by the team however the OLED utilised less GPIO pins.	The discussion around the visual displays lead to a future discussion. This resulted in a touchscreen LCD screen being selected by the group.
High Voltage Amplification	Since the amplifiers used in this part of the design, concern was raised around thermal dissipation.	This resulted in thermal calculations to better understand the heat dissipated by the power amplifiers. The PCB was also design with redundancy for a heat sink to be added.

2.7 Safety Issues

As outlined the MEMS Testing Power Supply operates at high voltages and currents, posing various safety risks. The following section will detail key safety issues identified for the MEMS Testing Power Supply, how they were identified, and the mitigations that have been implemented. All issues were identified during team meetings and weekly design review.

2.7.1 Electrical Shock and Electrocution

The MEMS Testing Power Supply is capable of producing both DC and AC voltages up to $200V$. Incorrect handling or accidental contact with live terminals can result in electrical shock or even electrocution.

Mitigation Control:
Administrative and Engineering controls were used. Administrative control was exercised through design philosophies, focusing on minimising high-voltage exposure points. Engineering control was the implementation of a hardware interlock that limits output voltage. This was tested and verified during the prototyping phase.

2.7.2 Overcurrent and Overvoltage Protection

The device is designed to handle a maximum current of $10mA$. Exceeding this limit can result in overcurrent conditions, leading to overheating and potential fire hazards. Overvoltage conditions can also damage the device and connected equipment.

Mitigation Control:
Engineering control was the primary method. Built-in protection mechanisms were implemented and tested to automatically cut off the current and voltage if they exceed safe levels.

2.7.3 Loose Connections

While the design accounts for secure connections, there is a risk of connections coming loose due to wear and tear or improper handling. Loose connections can lead to short circuits, device malfunction, or even fires.

Mitigation Control:
Engineering control was applied through stress tests on all connections during the prototyping phase to ensure they remain secure under various conditions.

2.7.4 Damage to Safety Features

The device incorporates several safety features like hardware interlocks and overcurrent protection. Damage to these features, whether through misuse, wear and tear, or manufacturing defects, could disable these protective measures.

Mitigation Control:
Engineering control involved individual testing of each safety feature to confirm its reliability. Components showing signs of wear or potential failure were replaced.

2.7.5 User Error

Despite the device's built-in safety features, incorrect operation by the user can lead to safety hazards.

Mitigation Control:
Administrative control involved the development of a comprehensive user manual and training sessions. Warning labels were also added to the device.

2.7.6 Environmental Conditions

Operating the device in damp or wet conditions can lead to short circuits and electrical shocks.

Mitigation Control:
Engineering control was applied by designing the device casing to be water-resistant. This feature was tested under controlled conditions.

2.7.7 Regulatory Compliance

Failure to meet local and international safety standards can result in the device being unsafe for use, leading to potential legal repercussions.

Mitigation Control:
Administrative control involved a compliance review to ensure the device meets all local and international safety standards. Certificates of compliance were obtained.

2.8 Ethical Issues

Ethical issues in engineering are of paramount importance as they govern the responsible and sustainable development of technology. Engineers play a critical role in shaping society by creating innovations that can have far-reaching implications. Failing to address ethical concerns can lead to unintended consequences, safety hazards, discrimination, environmental harm, and violations of privacy. The team has ensured to the best of their ability that the design is ethical.

2.8.1 Purpose of Design

The open-source design that has been developed is intended for the sole purpose of the MEMS testing power supply. Since the design is open source, it allows academics and other researchers to access the design and adapt it as they see fit. Should the design not be used for its intended purpose, there may be potential ethical issues should it be used in systems that the team may not deem ethical.

2.8.2 Regulatory Compliance

The MEMS testing power supply is subject to regulatory compliance to ensure the design is safe to operate following protype testing. Throughout the entire design process of the testing power supply, the team has avidly tried to ensure that the design meets the required regulatory compliance requirements. An independent third-party should be consulted to ensure that the design doe in-fact meets the requirements.

2.8.3 Environmental Impacts

The greatest environmental impact from this design is from the production of the PCB. There is an abundance of toxic chemicals used in the manufacturing of the PCB. There is a chance that the waste of these chemicals is not disposed of properly. This can lead to pollutants in soil and water, resulting in the destruction of local ecosystems. There is also an amount of E-waste associated with the manufacturing of electronic components. Improper recycling methods possess a likelihood of releasing hazardous materials into the environment. The team has attempted to mitigate and limit the environmental impact as much as possible, however, the PCB production is out of the team's control. In place, the team sought a reputable PCB manufacturer.

2.8.4 Supply Chain Transparency and Human Rights

Majority of the components (including the PCB) are outsourced internationally from countries that may not enforce the same fair working conditions that are held within Australia. As such, there is a potential risk that when purchasing the electronic components, that the companies are engaged in salve labour and other human rights violations. The client is recommended to source materials and components from local (Australian) manufactures if possible. This limits the potential risk of supporting unethical working conditions.

2.9 Top 5 Risks and Mitigations

Risks in this project are ranked based on the value of the residual risk. Initially the inherent risk values were analysed, and these rankings are presented in Table 2-9.

Table 2-9: Inherent Risk analysis of the Top 5 risks.

Identifiable Hazards	Inherent Risk				Comments
	C	L	E	=	
Low voltage testing	50	1	5	250 M	According to AS/NZS 3000:2018, since we are working with voltages lower than $1000V_{AC}$ and $1500V_{DC}$, it is considered low voltage equipment. Whilst this is considered low voltage, is still has the potential to cause serious harm through electrocution.
240V equipment	50	1	5	250 M	PowerPoints and switches present, soldering equipment, and testing equipment
Flammable	25	1	3	75 L	Potential for circuitry to catch on fire.
Working Alone	50	3	1	150 M	If an injury occurs whilst working alone, the effect may be worsened due to no immediate medical attention.
Carcinogens	25	6	3	450 H	Fumes from solder flux

The hazard with the highest inherent risk is carcinogens, with a rating of 450 High, and the hazard arises from the fumes emitted from solder flux during the building phase. The Low voltage testing and $240V$ equipment are equally weighted at 250 medium and causes includes electrocution and unsafe PowerPoints, switches, and soldering equipment respectively. The hazard with the fourth highest inherent risk value is working alone and this involves when a team member gets injured whilst working alone and no immediate help can be reached. This hazard is rated at 150 medium. The last hazard is from flames, and this arises from the potential for the circuitry to catch on fire. These risks require certain mitigation/control measures to reduce the consequence, likelihood, and exposure into what is called the residual risk value. The above hazards along with their control measures and residual risk are shown in Table 2-10.

Table 2-10: Residual Risk analysis of the Top 5 risks.

Identifiable Hazards	CTRL	Control Measures	Residual Risk			
			C	**L**	**E**	**=**
Low voltage testing	TR, IN, AD	Ensure there is a trained professional supervising the testing activities. The equipment should also be thoroughly inspected before use.	50	0.5	5	125 M
240V equipment	TR, IN	Ensure students have sufficient training and are able to identify $240\ V$ equipment. The equipment should also be thoroughly inspected before use and is UWA tagged.	50	0.5	5	125 M
Flammable	TR	Have a CO2 fire extinguisher readily available during testing. Ensure students are trained to use a fire extinguisher.	15	1	3	45 L
Working Alone	AD, TR, EL	Ensure a minimum of two people from the group are working in the room at the same time. In the event that working in the lab alone is permitted, the UWA "Working Alone" policy should be followed.	15	3	1	45 M
Carcinogens	EN, PPE, AD	Fume extractor, respiratory protection (mask/respirator)	25	0.5	3	38 L

For low voltage testing, a combination of training, inspection, administrative control is recommended. This means ensuring the equipment is inspected and a trained professional is in presence during testing. For the $240V$ equipment, a combination of training and inspection are recommended, in making sure training is provided which aims to help identify the $240\ V$ equipment. The flammable hazards control is training, which entails team members having knowledge of how to use a fire extinguisher and knowing the location of the CO_2 fire extinguisher. To minimise the hazard that comes with working alone, administrative, training and elimination procedures are taken. These procedures involve having at least two people working together at the same time and to abide by the “Working Alone” policy from UWA. Lastly, with the carcinogens the appropriate controls are engineering, personal protective equipment (PPE) and administrative. These controls aim to reduce the risk value by providing a fume extractor and respiratory protection such as a mask or a respirator.

2.10 Design Outputs

The following table list the final design outputs generated during the course of this project, along with their respective formats and storage locations.

Table 2-11 Final Design Outputs

Document	Item Name	Purpose	Storage Location
Final Report	5552 – FR – Final Report	Provides a comprehensive overview of the project, including design decisions and results	Final Deliverables
System Schematics	5552 – FR – Schematic	Details the electrical connections and components used in the design.	Final Deliverables
PCB Layout & Routing	5552 – FR – PCB	Provides the physical layout of the printed circuit board, including traces and components.	Final Deliverables
Enclosure 3D Model	5552 – FR – Enclosure	Provide a 3D representation of the device's physical enclosure for manufacturing.	Final Deliverables
MPU Code	*Multiple Files*	Details the control of the hardware components and implement the device's functionality.	GitHub Link
Cost Register	5552 – FR – Cost Register	Itemises and track all costs associated with the project.	Final Deliverables
Project Risk Register	5552 – FR – Project Risk Register	Identification, assessment, and risk management throughout the project.	Final Deliverables
MPU Input/Output Register	5552 – FR – IO Register	Lists all inputs and output connections specific to the RPi MPU	Final Deliverables

Requirements Register	5552 – FR – Requirements Register	Documents the project requirements, their priori ty, and status.	Final Deliverables
Technical Queries Register	5552 – FR – Technical Query Register	Log technical queries, their resolution status, and any associated actions.	Final Deliverables
Requirements Testing	5552 – FR – Requirements Testing	List of physical system testing specific to requirements	Final Deliverables

2.11 Final Costs

The final costs of the project can be broken down into two sections for this project. The first cost breakdown includes the price to build the protype, whilst the second is the cost associated with the final build of the project.

Table 2-12 below presents a summary of the prototype construction costs. The largest associated cost with the prototype construction was the procurement of the IC chips. Since this design was completed prior to the scope amendment which excluded HV, the decision was made to still procure the HV elements. Hence, a large IC cost. A complete and detailed cost breakdown can be found in the cost register.

Table 2-12: Prototype Construction Cost

Item	Price ($AUD)
Passive Components (Inductors, capacitors, resistors, and the like)	$39.20
IC Chips	$305.98
PCB Build and Procurement	$45.69
Total	**$390.87**

The total protype build came to a total of $390.87. This was $40.87 over the allocated prototyping budget. Whilst the prototype is slightly over budget (REQ-031), the performance of the design is greatly increased with the components selected.

The protype budget overrun could potentially be mitigated by replacing the four digital potentiometers, which cost $19.23 each, with analogue potentiometers. Analogue potentiometers are generally cheaper, with prices ranging from around $6.99 to $12.95 based on current market rates. This substitution could bring the project back within the budget constraints however this would add a secondary layer of control outside of the MPU and keypad increasing design complexity.

Table 2-13: Final Design Construction Cost

Item	Price ($AUD)
Prototype Design (Items in Table)	$390.87
Controller (Assumed to be RPi 5)	$110
Display	$80
Enclosure	$10
Total	**$590.87**

Table 2-13 above presents the total design budget that is needed to build the final intended design. Assuming little adjustment is needed from the prototype design, the client needs to additionally purchase the controller, display, and the enclosure. The controller that is recommended for the final design is the RPi 5 Model B 4GB. This ensures that the design is utilising state-of-the-art microcontrollers, which may make future adaptations significantly easier and cost-effective.

3. Recommendations for Future Design

3.1 Future Design Processes & Approvals

3.1.1 Design Processes

For the next integration of the prototype, it is advisable to adopt a stage-gate model. This model would involve a series of phases separated by "gates" where decisions are made about whether to proceed, pause, or terminate a project. Each phase would involve tasks such as feasibility studies, detailed design, and prototype testing. The stage-gate model will ensure that the project is closely monitored at each stage, reducing the risk of late-stage failure.

3.1.1.1 Approvals

- **Regulatory Approvals:** Before moving to the next phase, ensure that all necessary regulatory approvals are obtained. This includes safety certifications and environmental clearances, which are crucial for marketability and legal compliance.

- **Internal Approvals:** Establish a Design Review Board comprising key stakeholders, including engineers, product managers, and legal advisors. This board will be responsible for approving the transition from one stage to the next.

- **Intellectual Property:** If the design includes proprietary technology, secure the necessary patents or copyrights before proceeding to the next stage. This will protect the design from being copied, providing a competitive edge in the market.

- **Budget Approvals:** Ensure that budget estimates are approved by the finance department at each stage. This will help in avoiding budget overruns and ensuring that adequate resources are allocated for each phase.

By following these recommended processes and obtaining the necessary approvals, the next integration of the prototype or its development into a marketable product will be more streamlined and is more likely to meet all internal and external requirements.

3.2 Future Tenders

For the next phase of this project, several tenders would need to be called to ensure the successful integration of the prototype into a market-ready product. These tenders will cover various aspects such as hardware manufacturing, software development, quality assurance, and distribution. The scope of works for each tender will be clearly defined to attract the right expertise needed for each component of the project. For instance, the hardware manufacturing tender will focus on mass-producing the device with high-quality materials and precision, while the software development tender will aim to refine the user interface and add additional features based on user feedback. Quality assurance tenders will be crucial for ensuring the device meets all safety and performance standards. Companies specialising in electrical engineering, software development, and quality testing will be invited to tender. Each tender will include specific milestones and deliverables tied to the project's overall timeline, ensuring that the development stays on track for a successful market launch.

3.3 Recommended Tests

A future iteration of the device would require a number of additional tests. These would be necessary to validate new features, improved specifications, or expanded capabilities. Here are some recommended tests for the future iteration:

1. Voltage Range Test: To validate that the enhanced device can produce a DC output voltage of $0 - 300V$ and an AC output voltage of $0 - 300\,V_{rms}$, in line with potential new requirements (beyond REQ-001 and REQ-003).

2. Frequency Range Test: To confirm that the device can operate at frequencies up to $1MHz$, exceeding the current limit of $300kHz$ (REQ-015).

3. Modulation Scheme Test: To validate the implementation of new modulation schemes like QAM or FSK, enhancing the device's versatility beyond the current 100% amplitude modulation (REQ-016).

4. Interlock Functionality Test: To ensure that the hardware interlock effectively limits the voltage to safer levels when engaged, and to test any new interlock features (REQ-002, REQ-004).

5. Current Sensing Test: To validate that the device can measure and limit output current with higher accuracy, potentially in steps of $0.5mA$, improving upon the current 1-$10mA$ range (REQ-005, REQ-006).

6. Overcurrent Protection Speed Test: To confirm that the device can switch off the output in under 5 milliseconds in case of overcurrent, improving upon the current 10 milliseconds (REQ-007).

7. User Interface Test: To evaluate the intuitiveness and user-friendliness of any new interface features, such as touch-screen controls, ensuring they meet REQ-014 and REQ-019.

8. Remote Control Test: If the new version includes remote control capabilities, tests should be conducted to confirm the reliability and security of this feature, potentially adding a new requirement for remote operation.

9. Energy Efficiency Test: To measure the power consumption of the device under various operating conditions, aiming for improved energy efficiency, which could become a new requirement.

10. Environmental Stress Test: To confirm that the device can operate under a wider range of environmental conditions, such as higher temperatures or humidity levels, potentially adding new environmental requirements.

11. Compliance Test: To ensure that the enhanced device meets any new or updated safety and regulatory standards, potentially updating REQ-008 and REQ-009 regarding the material and casing.

12. Real-world Simulation Test: To validate the device's performance in scenarios that closely mimic its intended real-world application, ensuring it meets all user and regulatory requirements, including any new requirements that may be added.

These tests are designed to validate that the enhanced device not only meets the existing requirements but also any new or expanded requirements that come with the upgraded features.

4. Design Completion & Verification

4.1 Final System Schematic

As per Table 2-11 the final system schematic can be found in document 5552 – FR – Schematic

this consists of the overarching system with numerous subsystems dedicated to each module.

4.2 Code Flow Diagram

The code flow diagram for the system can be seen in Figure 4-1. This represents the overlying architecture for the code. The software files used to construct this architecture can be found in the GitHub repository (Table 2-11).

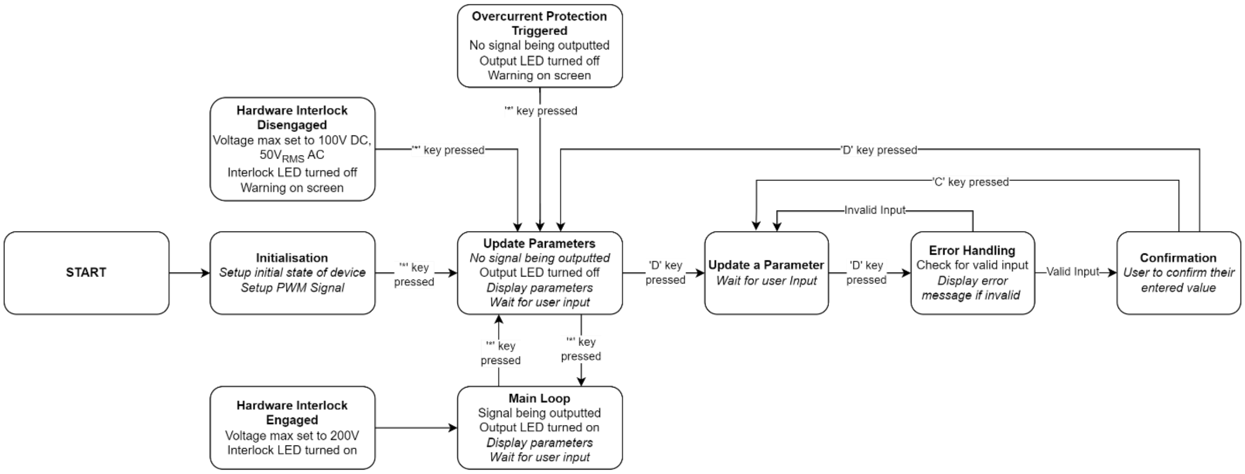

Figure 4-1: Overall code flow diagram.

4.3 PCB Design

The layout and details of the PCB can be found in the accompanying documentation (Table 2-11). The below figure is the physical board as used in the design.

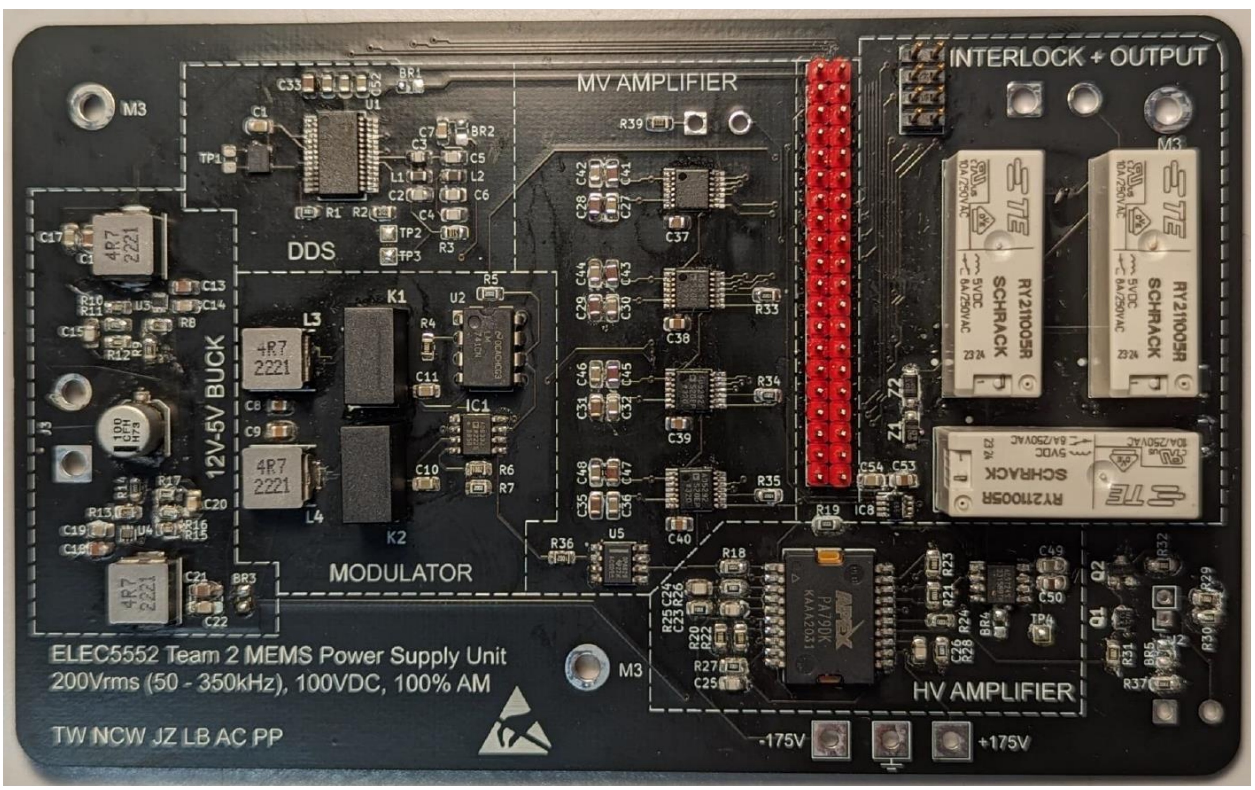

Figure 4-2 Physical PCB Board

4.4 Requirement Testing

The Requirement Testing section serves as a comprehensive evaluation framework to rigorously assess the final assembled design's compliance with the predefined set of requirements. This multi-faceted approach involves a series of targeted tests, each corresponding to a specific requirement, to ensure the design's functionality, safety, and reliability. The tests range from basic hardware checks, such as voltage and frequency outputs, to more complex evaluations like modulation control and user interface responsiveness. The table below represent an extract of the testing procedures found in document *5552 – FR – Requirements Testing*. It outlines the test specifications, descriptions, and the corresponding analyses of the test results, providing a transparent and accountable record of the design's performance metrics.

Test No.	Test specification	Test Description	Test Result Analysis
001	REQ-013	Connect the MPU onto the PCB and supply the PCB with 12V and measure the 3.3V pin from the MPU to ensure 3.3V are outputting from the pin.	All conditions passed.
002	REQ-014	Checking via python terminal to ensure the numpad inputs are received successfully.	All conditions passed.
003	REQ-019	Powered the PCB to observe the green LEDs state and activated the hardware interlock switch, with no output, to observe the interlock LEDs state.	All conditions passed.
004	REQ-018	For any 10VDC input, measure the output in ensuring the expecting output of 10VDC is returned.	All conditions passed.
005	REQ-017	For any given input, measure the output BNC connector, expecting any value.	All conditions passed.
006	REQ-001	For a maximum of 30VDC requested input, measure the output in ensuring the expecting output of up to 30VDC is returned.	Voltage above 30V output has not been tested, however all below 30V has passed.
007	REQ-003	For a maximum of 10VAC requested input, measure the output in ensuring the expecting output of up to $10VAC$ is returned.	Due to safety reasons, the team could not test up to 200Vrms, however all tests below 50Vrms have passed.
008	REQ-024	Used the power supply in Makers Lab to supply the PCB with $12V$ and measure the V_{ss} of the IC furthest away from input, indicating the IC is powered on.	All conditions passed.
009	REQ-035	A series of continuity tests were taken placed after the PCB arrived.	All conditions passed.
010	REQ-028	A 12V input was applied to the 12-5V buck converter subsystem and the output of the converter was measured. Measured $5V$ at both 12-$5V$ buck converter.	All conditions passed.
011	REQ-006	Using the numpad, an input of desired current limit is selected and check python console to print the selected current limit.	All conditions passed.
012	REQ-002	When the hardware interlock is enabled, request the power supply to output 110V. Observe the output, which should be 100V, instead of 110V.	Not tested, due to safety protocols.

013	REQ-004	When the hardware interlock is enabled, request the power supply to output 60Vrms. Observe the output, which should be 50Vrms, instead of 60Vrms.	Not tested, due to safety protocols.
014	REQ-005	After setting the current limit to 10mA in the user interface, place a load which draws more than 10mA. Observe the output using a multi meter and see if the power supply has been shut down.	The accuracy in sensing the current is not stable due to very low current.
015	REQ-007	Using a digital potentiometer at the output, apply load which draw more than 10mA. Start the timer in Python, once data has been sent to the digital potentiometer and when data is received from the ADC and the output has been shutoff, stop the timer and observe the elapsed time.	All conditions passed.
016	REQ-008	Observe the case, in ensuring its fully sealed by a lock.	All conditions passed.
017	REQ-009	Not tested.	Not tested.
018	REQ-010	A voltage of 35VDC was requested through the keypad to the MPU, and there was no potential at the output.	Condition 1: Only during testing.
019	REQ-011	During the design and testing process, ensure that all design choices and testing methods are aligned with legal and regulatory requirement.	All conditions passed.
020	REQ-012	During the modelling of the power supply case, ensure appropriate room is left to house LEDs in the front panel. The LED must be connected to the interlock module.	All conditions passed.
021	REQ-015	Run the code which initiates communication to the DDS IC, and the measure the output on an oscilloscope to ensure the correct frequency output is acquired.	All conditions passed.
022	REQ-016	Applied a sine wave from the DDS IC and measured the output of the modulator IC using an oscilloscope. Obtained a 100% modulated square wave signal.	All conditions passed.
023	REQ-020	Request the power supply to supply 10VDC, once successful, increase the requested voltage to 10.05VDC and observe the output.	Condition 1: Due to the digital potentiometers not working, analog potentiometers were used, hence step size of 0.05V or less is not stable.
024	REQ-021	First, use a MPU to set the DDS IC output frequency to 50kHz then measure the output. Secondly, set the DDS frequency to 60kHz via MPU and measure the output using an oscilloscope.	All conditions passed.
025	REQ-022	Initially the current limit is set to 10mA, meaning the output will be turned off when the MCU reads, 2.5080V from the ADC. Make an adjustment which	All conditions passed.

		changes the limit to 8mA and observe the code to see if the voltage at which the output shuts down has changed to 2.5064V.	
026	REQ-023	Whilst the output is connected to an oscilloscope, request the power supply to module a DC signal with 50Hz. Observe the oscilloscope to see if a square wave signal with 50Hz is produced.	All conditions passed.
027	REQ-025	Whilst the MPU is powered on, input commands via the keypads to change DC, AC, modulation ON and OFF. Observe the code output, to see of the requested changes have been accepted.	All conditions passed.
028	REQ-026	Ensure the design has used filtering capacitors and the power supplies (12-5V) has been well regulated.	All conditions passed.
029	REQ-027	Create a base output signal by requesting a square wave with 50Hz. Once the output has been observed using an oscilloscope, change the requested square wave frequency to 60Hz and observe the oscilloscope.	All conditions passed.
030	REQ-029	Not Tested	Design consists of easily removeable casing and accessible MPU connections for programming
031	REQ-030	Not Tested	Git Repository Created
032	REQ-031	A cost register was used to keep track of the costs of components, ensuring it is under or equal to $350.	Condition 1: Used an already owned RPi 3. Condition 2: Used an already owned 5.5 inch display.
033	REQ-032	The components were selected from Mouser and after checking the status meaning if it’s in stock, then the component could be selected.	All conditions passed.
034	REQ-033	Power the system within load and ensure all chips are functions without heating up.	Condition 1: A heatsink was added to the pre-amplifier Op-Amp.
035	REQ-034	Choose components with long expected lifetime and high operational temperatures.	Condition 1: If the power supply is not exposed to water.
036	REQ-036	Not tested.	Not tested.
037	REQ-037	Utilised SMD components to minimise weight and minimised the size of the PCB to reduce weight.	All conditions passed.
038	REQ-038	Not tested.	Not tested.
039	REQ-039	Not tested.	Not tested.

Majority of the tests have yielded positive results, confirming that the design meets the stipulated criteria for functionality, safety, and user interaction. However, it's worth noting that some tests were not conducted due to various constraints, and these areas will require further attention in future iterations of the design.

Overall, the testing phase has provided valuable insights into the design's strengths and areas for improvement, setting the stage for subsequent design refinements and enhancements.

4.5 Physical System Testing & Verification

This section delves into the final testing and verification processes carried out on the built design. These tests are crucial for ensuring that the design performs as expected under various conditions, including different modes and modulation settings. Testing was conducted under REQ-010, stating that all preliminary testing with output voltages must not exceed 30V(peak) for both DC and AC.

Figure 4-3: Physical System

4.5.1 Interlock & Overcurrent Protection

This initial subsection is dedicated to testing the interlock and overcurrent protection features of the design, including the visual indication provided by the LED. These tests are vital for ensuring the safety and reliability of the device, particularly in scenarios where it might be subjected to conditions beyond its specified limits.

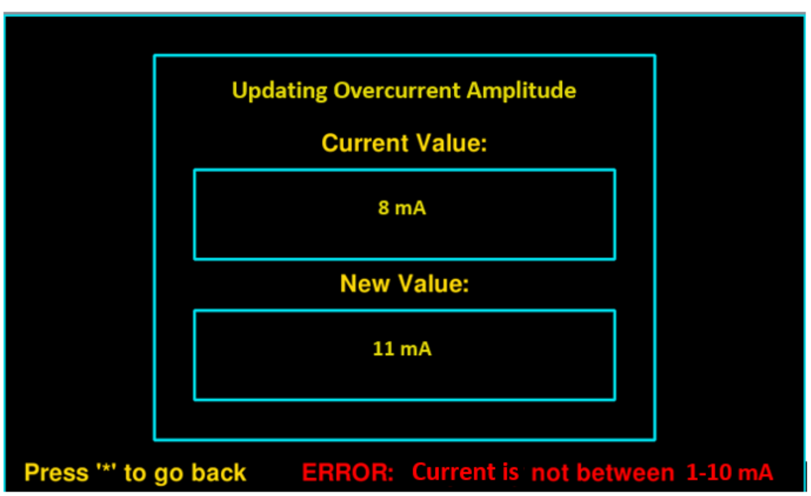

Figure 4-4 Overcurrent Protection Message

4.5.2 DDS Signal Generation

In order to test the DDS signal generation code, the output pin of the DDS module was connected to an oscilloscope so the magnitude and frequency could be measured. Figure 4-5 shows a sine wave set to 50kHz frequency. It can be observed that the oscilloscope reads 50.0kHz exactly, showing that the sine wave generates as intended, with high precision and accuracy. The DDS was then reprogrammed to output 50.2kHz. Figure 4-6 shows a sine wave with frequency 50.21kHz, as intended with a small frequency error. This demonstrates much higher accuracy than the required step size of 10kHz as stated in REQ-021. Lastly, the DDS was then programmed to output 300.5kHz, as Figure 4-7 shows.

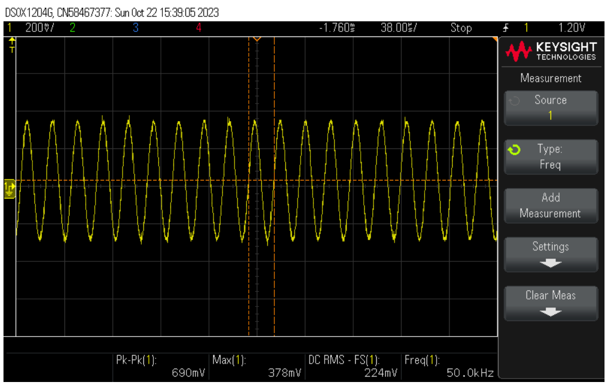

Figure 4-5: 50.0kHz signal with 224 mV pk-pk

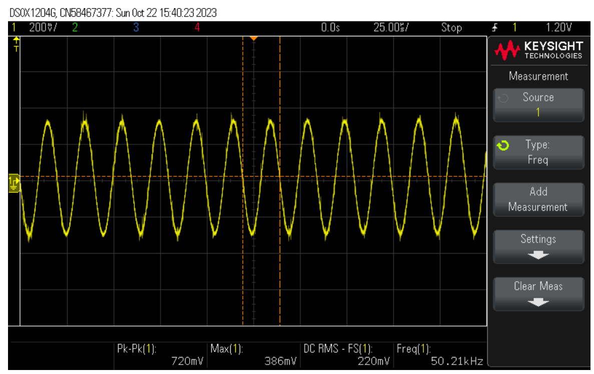

Figure 4-6: 50.21kHz signal with 220 mV pk-pk

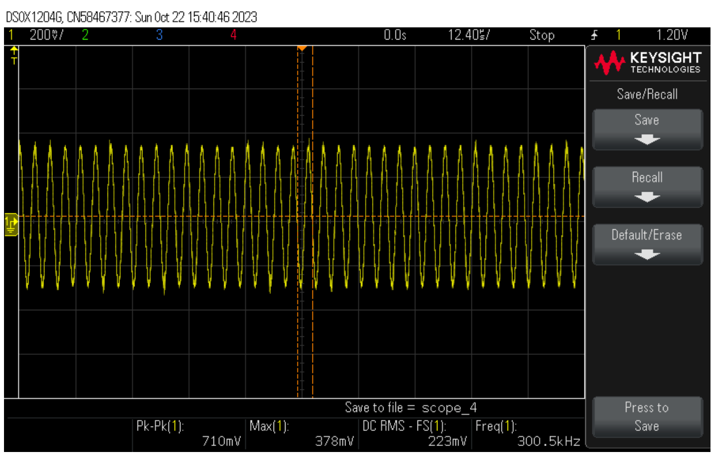

Figure 4-7: 300.5kHz signal with 223 mV pk-pk

4.5.3 PWM Signal Generation

In order to test the PWM code, pin 18 on RPi was connected to an oscilloscope so the magnitude, duty cycle and frequency could be measured. Figure 4-8 shows a square wave set to a 50% duty cycle with 50Hz frequency. It can be observed that the oscilloscope reads 49.63Hz, showing that the square wave generates as intended. This is similar to the case of Figure 4-9 which was set to 100Hz. Figure 4-10 shows a 100% duty cycle PWM signal which produces a DC signal of 3.3V magnitude, as required for when no modulation is wanted by the user.

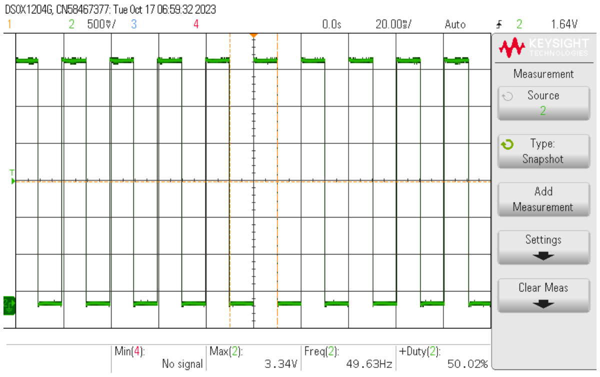

Figure 4-8: 50% duty cycle at 50 Hz square wave

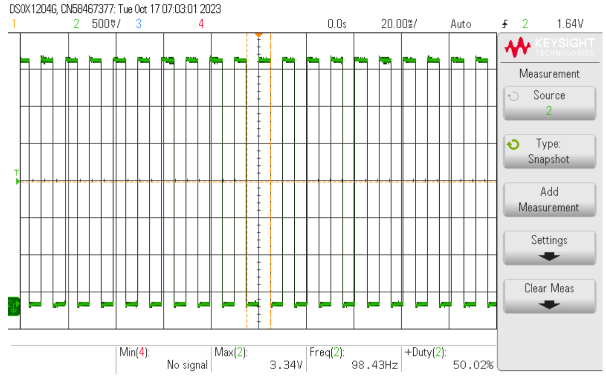

Figure 4-9: 50% duty cycle at 100 Hz square wave

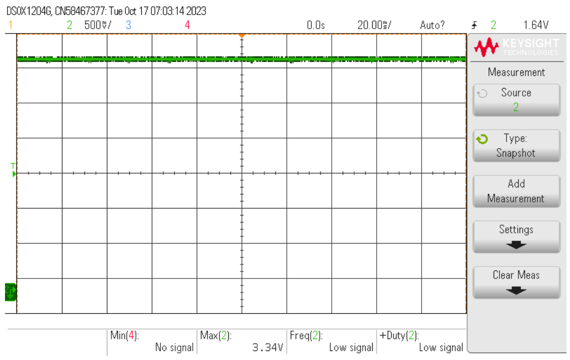

Figure 4-10: 100% duty cycle PWM generation

4.5.4 DC: Modulation

Here, the DC output is tested with modulation applied. The aim is to evaluate how well the design can modulate the square wave and the main signal generated by the DDS. Figure 4-11 shows the output of the modulation section of the PCB. The inputs are a DC generated signal from the DDS and a 50 Hz modulation signal. As expected, the output is a 100% modulated signal.

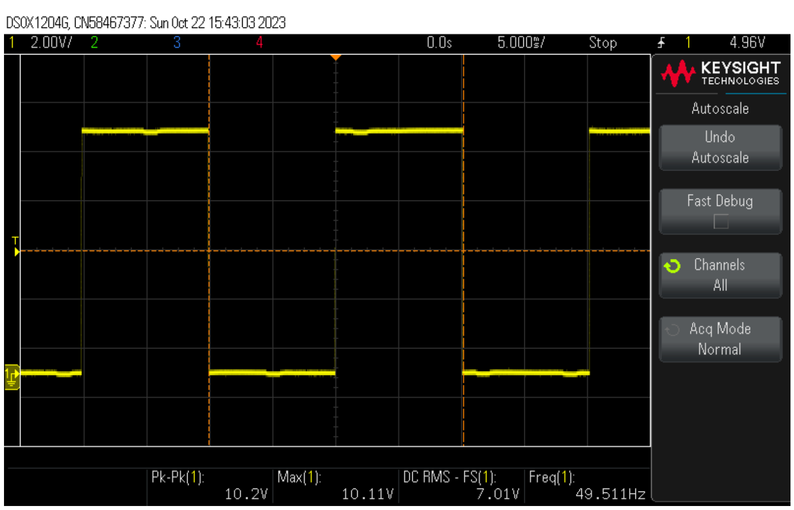

Figure 4-11: DC modulated signal with 50 Hz modulation.

4.5.5 AC: 100kHz with 50Hz Modulation and Maximum Gain

The AC output (with the 30V limit in place) was tested with 100kHz carrier frequency, modulated with a 50Hz square wave. The oscilloscope output is shown in Figure 4-12 for a maximum gain value of the potentiometers, resulting in $15V_{pk-pk}$. The output shows successful square wave modulation on the output, with only minor amounts of noise being visible.

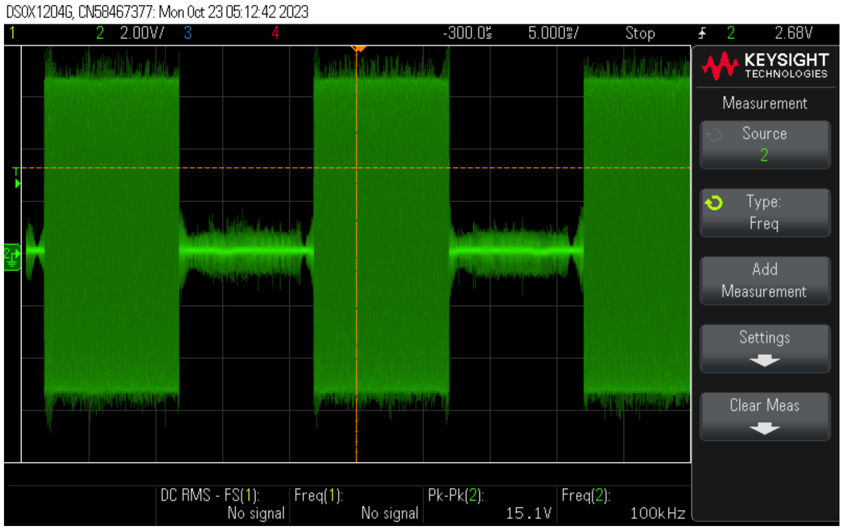

Figure 4-12: AC output for 100kHz modulated with 50Hz square wave, maximum gain

4.5.6 AC: 100kHz with 50Hz Modulation and Minimum Gain

The AC output was tested with 100kHz carrier frequency, modulated with a 50Hz square wave. The oscilloscope output is shown in for a minimum gain value with the potentiometers, resulting in $1V_{pk-pk}$. The output shows successful square wave modulation on the output, with the amplitude of the carrier wave reduced significantly, as desired.

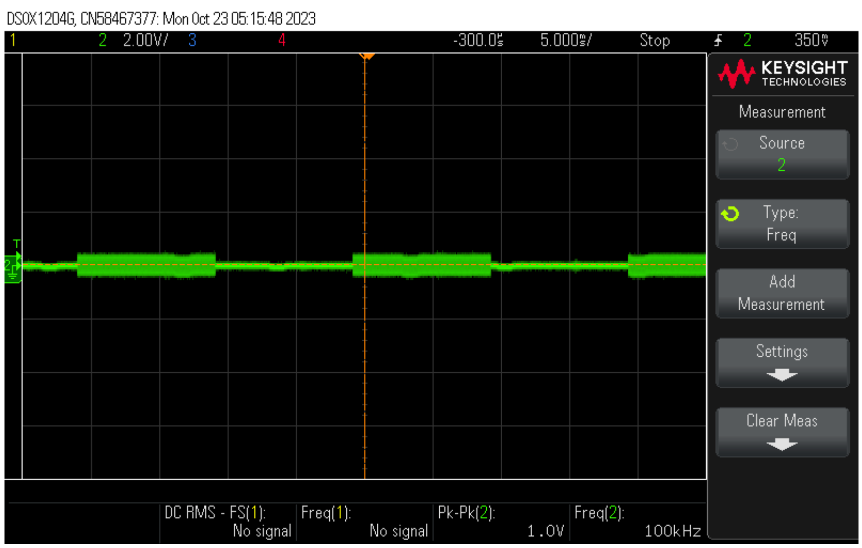

Figure 4-13: AC output for 100kHz modulated with 50Hz square wave, minimum gain

4.5.7 AC: 300kHz with 50Hz Modulation

The AC output is measured with the highest required frequency output of 300kHz inputted into the system. The oscilloscope's test result is shown in Figure 4-14. The output portrays how well the designed system can produce a 300kHz output signal, and still continue a clean square wave modulation scheme. The bandwidth of the system is estimated to be much higher than 300kHz.

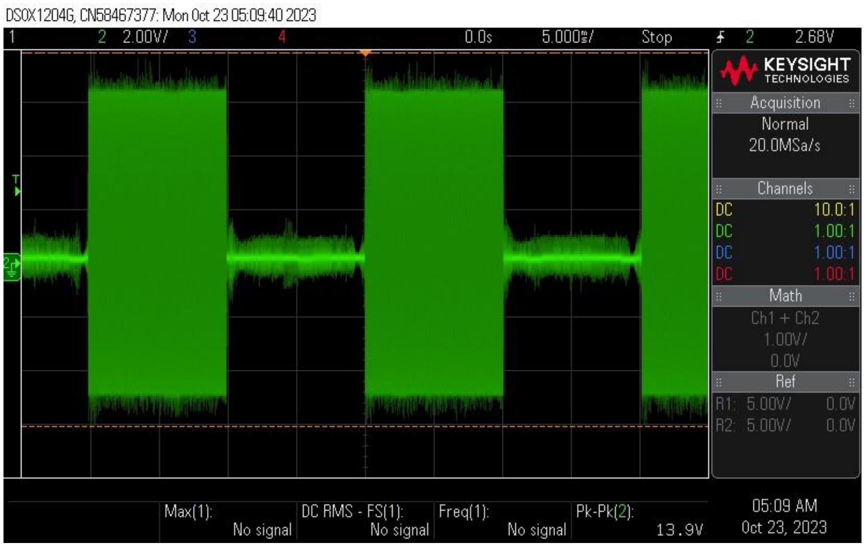

Figure 4-14: AC output for 300kHz modulated with 50Hz square wave

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6. Appendices

6.1 Appendix A – System Architecture