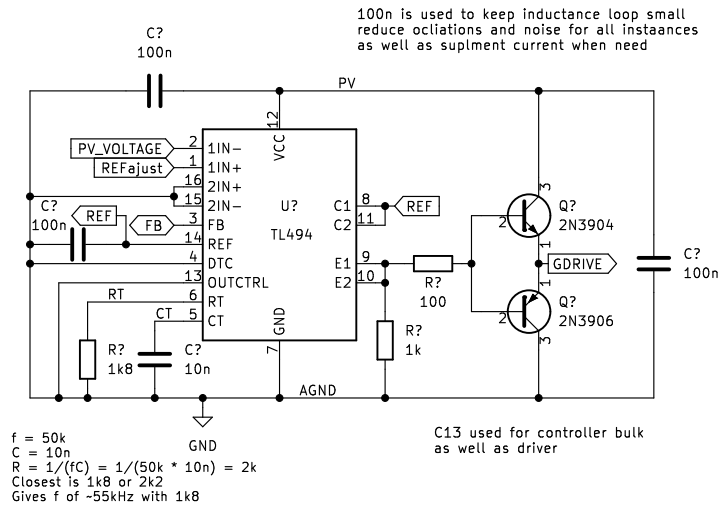


TL494 PWM @ 55kHz

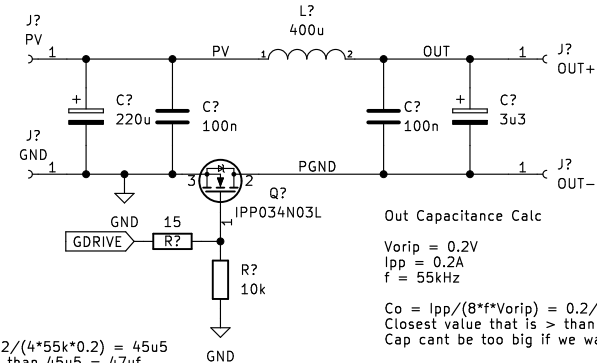


Selection of the 1k was to help reduce tf
The selection of the 100 was to help with tr
and tf by pushing the npn in to saturation hard
and to provide mimial resitance for the pnp

POWER STAGE

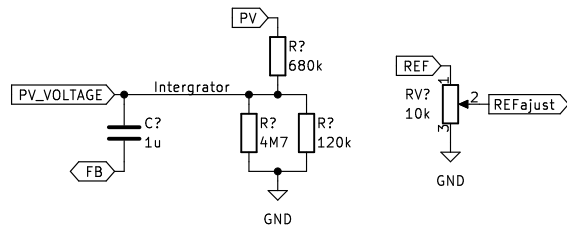
Inductor Calc

$V_s = 17V$ peak power from PV characterisation
 $I_o = 1.5A - 2A$ using largest value
 $f = 55kHz$ due to selected RT
 $I_{pp} = 0.2A$
 $L = V_s / (4 * f * I_{pp}) = 17 / (4 * 55k * 0.2) = 364uH$



10k on gate is to help make sure the gate has no charge
left when the drive goes low

Intergrator Controller



$V_{div} = 2.5V$
 $V_{mp} = 17V$
 $t = 100m$
 $C = 1u$
 $R = t/C = 100m/1u = 100k$
Thev equivalent is $R_u // R_l = 1 / (1/R_u + 1/R_l)$
voltage divider $R_l / (R_u + R_l) * 17 = 2.5$
Solving for R_l & R_u
 $R_u = 680k$ $R_l = 117.241k$
-117k Can be made with 120k//4M7