EC-252: COMPUTER ARCHITECTURE AND MICROPROCESSORS

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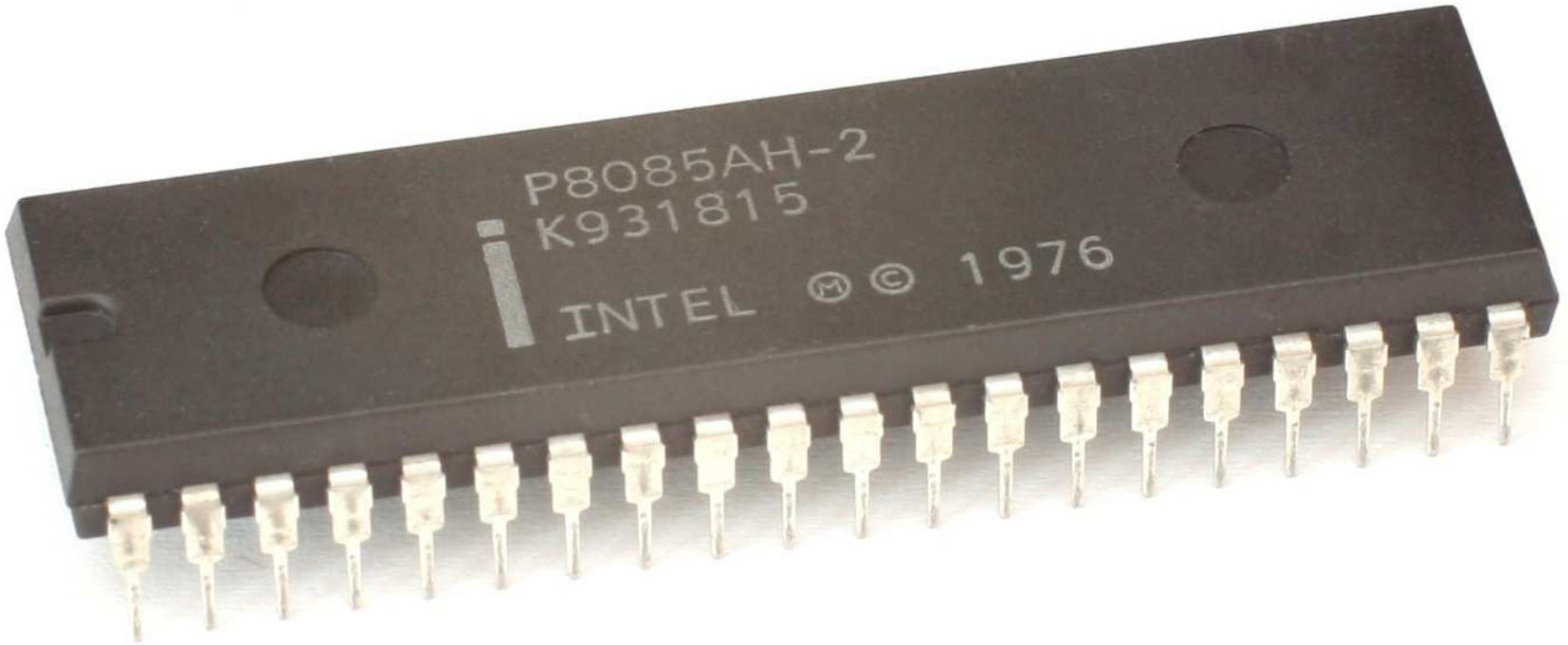
Intel 8085 MPU

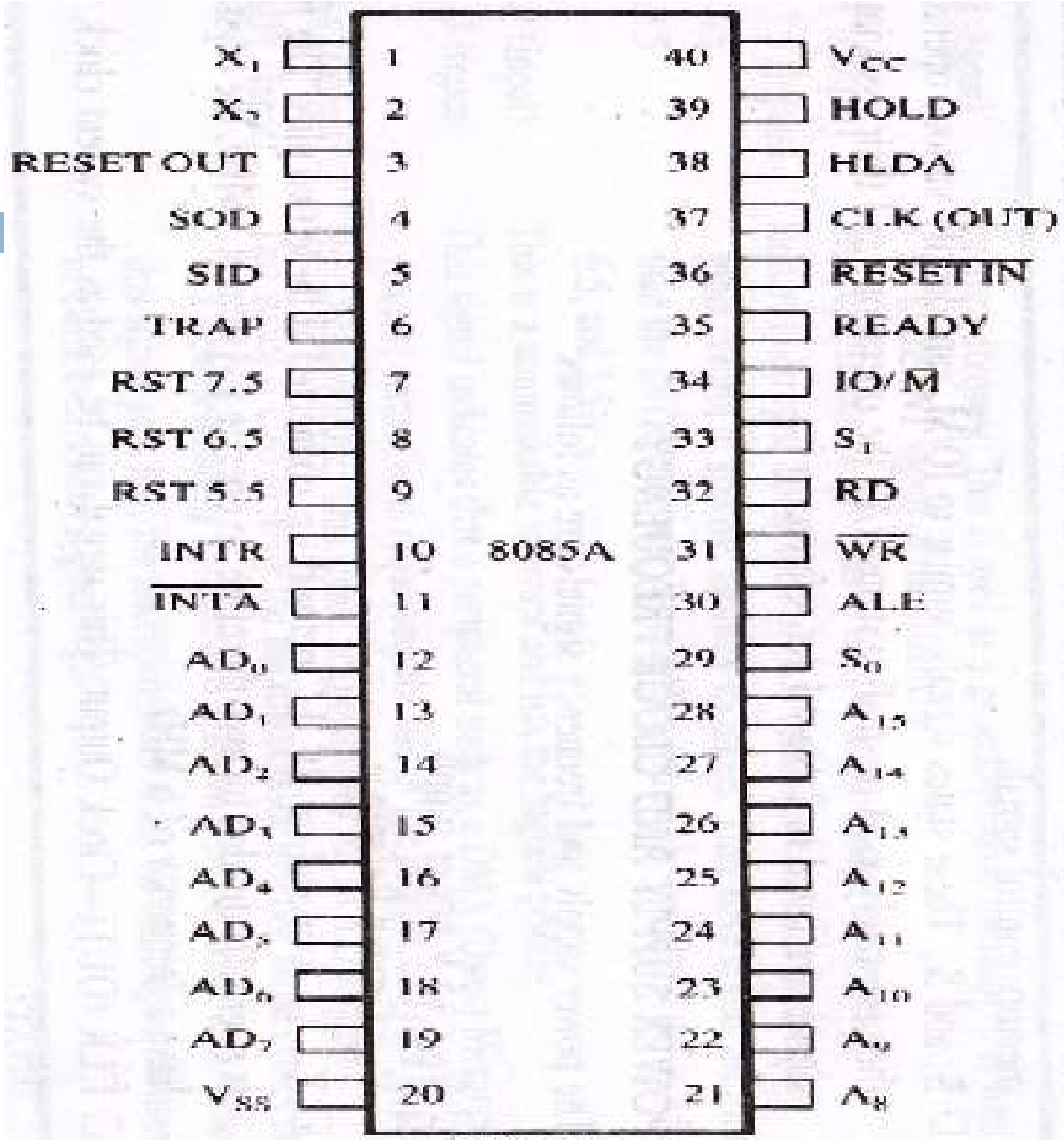


Case Study: Intel 8085 & Its Busses

- The 8085 is an 8-bit general purpose microprocessor that can address 64K Byte of memory.

- It has 40 pins and uses +5V for power. It can run at a maximum frequency of 3 MHz.

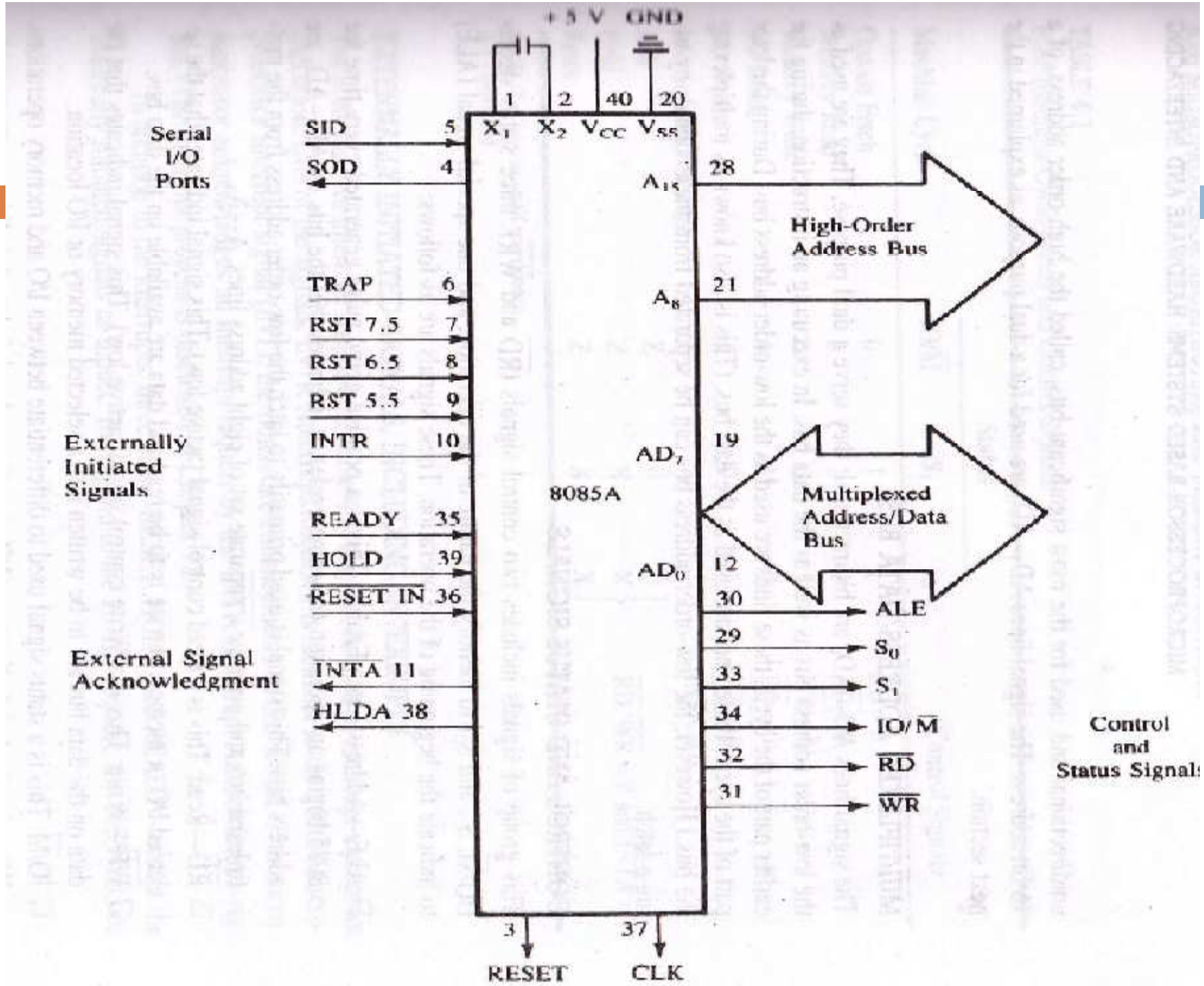
- Specifications
  - Introduced on: Mar-76
  - No. of transistors: 6,500
  - Bus speed: 2 MHz


X1 1
X2 2
RESET OUT 3
SOD 4
SID 5
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
INTA 11
AD0 12
AD1 13
AD2 14
AD3 15
AD4 16
AD5 17
AD6 18
AD7 19
VSS 20
8085A
40 VCC
39 HOLD
38 HLDA
37 CLK (OUT)
36 RESET IN
35 READY
34 IO/M
33 S1
32 RD
31 WR
30 ALE
29 S0
28 A15
27 A14
26 A13
25 A12
24 A11
23 A10
22 A9
21 A8

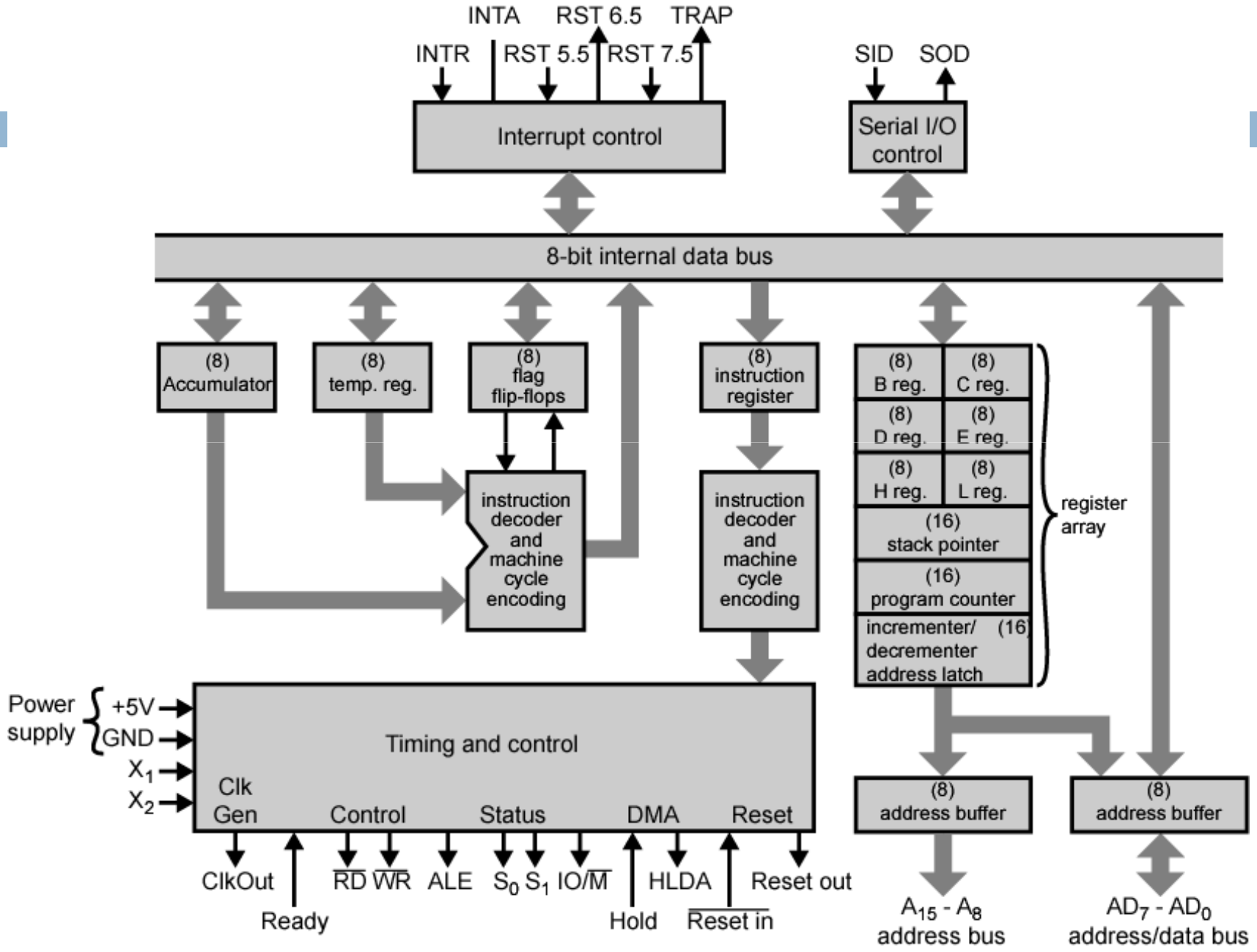
8085 Pinout

Intel 8085 Pin Configuration

- The 8085 pins can be clustered into 6 groups:
  - Address Bus & Data Bus
  - Control and Status Signals
    - ALE, RD', WR', IO/M', S0, S1
  - Power supply and clock frequency
    - V_{cc}, V_{ss}, X_1, X_2, CLK(out)
  - Externally Initiated Signals
    - INTR, INTA', RST 7.5/6.5/5.5, TRAP, HOLD, HLDA, READY, RESET-IN', RESET-OUT
  - Serial I/O ports
    - SID, SOD


+5 V
GND
1
2
40
20
X_1
X_2
V_{CC}
V_{SS}
Serial I/O Ports
SID 5
SOD 4
TRAP 6
RST 7.5 7
RST 6.5 8
RST 5.5 9
INTR 10
Externally Initiated Signals
READY 35
HOLD 39
RESET IN 36
External Signal Acknowledgment
INTA 11
HLDA 38
8085A
A_{15} 28
A_8 21
High-Order Address Bus
AD_7 19
AD_0 12
Multiplexed Address/Data Bus
ALE 30
S_0 29
S_1 33
IO/$\overline{M}$ 34
$\overline{RD}$ 32
$\overline{WR}$ 31
Control and Status Signals
3
37
RESET
CLK

Intel 8085 CPU Block Diagram



The Address and Data Buses

- The address bus has 8 signal lines A8 – A15 which are unidirectional.
- The other 8 address bits are multiplexed (time shared) with the 8 data bits.
  - So, the bits AD0 – AD7 are bi-directional and serve as A0 – A7 and D0 – D7 at the same time.
    - During the execution of the instruction, these lines carry the address bits during the early part, then during the late parts of the execution, they carry the 8 data bits.
  - In order to separate the address from the data, we can use a latch to save the value before the function of the bits changes.

Demultiplexing AD7-AD0

- From the above description, it becomes obvious that the AD7–AD0 lines are serving a dual purpose and that they need to be demultiplexed to get all the information.
- The high order bits of the address remain on the bus for three clock periods. However, the low order bits remain for only one clock period and they would be lost if they are not saved externally. Also, notice that the low order bits of the address disappear when they are needed most.
- To make sure we have the entire address for the full three clock cycles, we will use an external latch to save the value of AD7–AD0 when it is carrying the address bits. We use the ALE signal to enable this latch.

The Control and Status Signals

- There are 4 main control and status signals. These are:
  - ALE: Address Latch Enable. This signal is a pulse that become 1 when the AD0 – AD7 lines have an address on them. It becomes 0 after that. This signal can be used to enable a latch to save the address bits from the AD lines.
  - RD: Read. Active low.
  - WR: Write. Active low.
  - IO/M: This signal specifies whether the operation is a memory operation (IO/M=0) or an I/O operation (IO/M=1)
  - S1 and S0 : Status signals to specify the kind of operation being performed
    - mainly used to differentiate between various **machine cycles** (un-used in small systems)

Cycles and States

- From the above discussion, we can define terms that will become handy later on:
  - T- State: One subdivision of an operation. A T-state lasts for one clock period.
    - An instruction's execution length is usually measured in a number of T-states. (clock cycles).
  - Machine Cycle: The time required to complete one operation of accessing memory, I/O, or acknowledging an external request.
    - This cycle may consist of 3 to 6 T-states.
  - Instruction Cycle: The time required to complete the execution of an instruction.
    - In the 8085, an instruction cycle may consist of 1 to 6 machine cycles.

Machine Cycle Status & Control Signals

	Status			
Machine Cycle	**IO/M'**	**S1**	**S0**	**Control Signals**
Opcode Fetch	0	1	1	RD' = 0
Memory Read	0	1	0	RD' = 0
Memory Write	0	0	1	WR' = 0
I/O Read	1	1	0	RD' = 0
I/O Write	1	0	1	WR' = 0
Interrupt Acknowledge	1	1	1	INTA' = 0
Halt	Z	0	0	RD'=0, WR' = Z & INTA' = 1
Hold	Z	X	X	
Reset	Z	X	X	

Frequency Control Signals

- There are 3 important pins in the frequency control group.
  - X0 and X1 are the inputs from the crystal or clock generating circuit.
    - The frequency is internally divided by 2.
      - So, to run the microprocessor at 3 MHz, a clock running at 6 MHz should be connected to the X0 and X1 pins.
  - CLK (OUT): An output clock pin to drive the clock of the rest of the system.
- We will discuss the rest of the control signals as we get to them.

Mnemonic	Op	Description
ACI n	CE	Add with Carry Immediate
ADC r	8F	Add with Carry
ADC M	8E	Add with Carry to Memory
ADD r	87	Add
ADD M	86	Add to Memory
ADI n	C6	Add Immediate
ANA r	A7	AND Accumulator
ANA M	A6	AND Accumulator and Memory
ANI n	E6	AND Immediate
CALL a	CD	Call unconditional
CC a	DC	Call on Carry
CM a	FC	Call on Minus
CMA	2F	Complement Accumulator
CMC	3F	Complement Carry
CMP r	BF	Compare
CMP M	BF	Compare with Memory
CNC a	D4	Call on No Carry
CNZ a	C4	Call on No Zero
CP a	F4	Call on Plus
CPE a	EC	Call on Parity Even
CPI n	FE	Compare Immediate
CPO a	E4	Call on Parity Odd
CZ a	CC	Call on Zero
DAA	27	Decimal Adjust Accumulator
DAD B	09	Double Add BC to HL
DAD D	19	Double Add DE to HL
DAD H	29	Double Add HL to HL
DAD SP	39	Double Add SP to HL
DCR r	3D	Decrement
DCR M	35	Decrement Memory
DCX B	0B	Decrement BC
DCX D	1B	Decrement DE
DCX H	2B	Decrement HL
DCX SP	3B	Decrement Stack Pointer
DI	F3	Disable Interrupts
EI	FB	Enable Interrupts
HLT	76	Halt
IN p	DB	Input
INR r	3C	Increment
INR M	3C	Increment Memory
INX B	03	Increment BC
INX D	13	Increment DE
INX H	23	Increment HL
INX SP	33	Increment Stack Pointer
JMP a	C3	Jump unconditional
JC a	DA	Jump on Carry
JM a	FA	Jump on Minus
JNC a	D2	Jump on No Carry
JNZ a	C2	Jump on No Zero
JP a	F2	Jump on Plus
JPE a	EA	Jump on Parity Even
JPO a	E2	Jump on Parity Odd
JZ a	CA	Jump on Zero
LDA a	3A	Load Accumulator direct
LDAX B	0A	Load Accumulator indirect
LDAX D	1A	Load Accumulator indirect
LHLD a	2A	Load HL Direct
LXI B,nn	01	Load Immediate BC
LXI D,nn	11	Load Immediate DE
LXI H,nn	21	Load Immediate HL
LXI SP,nr	31	Load Immediate Stack Ptr
MOV r1,r2	7F	Move register to register
MOV M,r	77	Move register to Memory
MOV r,M	7E	Move Memory to register
MVI r,n	3E	Move Immediate
MVI M,n	36	Move Immediate to Memory
NOP	00	No Operation

8085 ISA

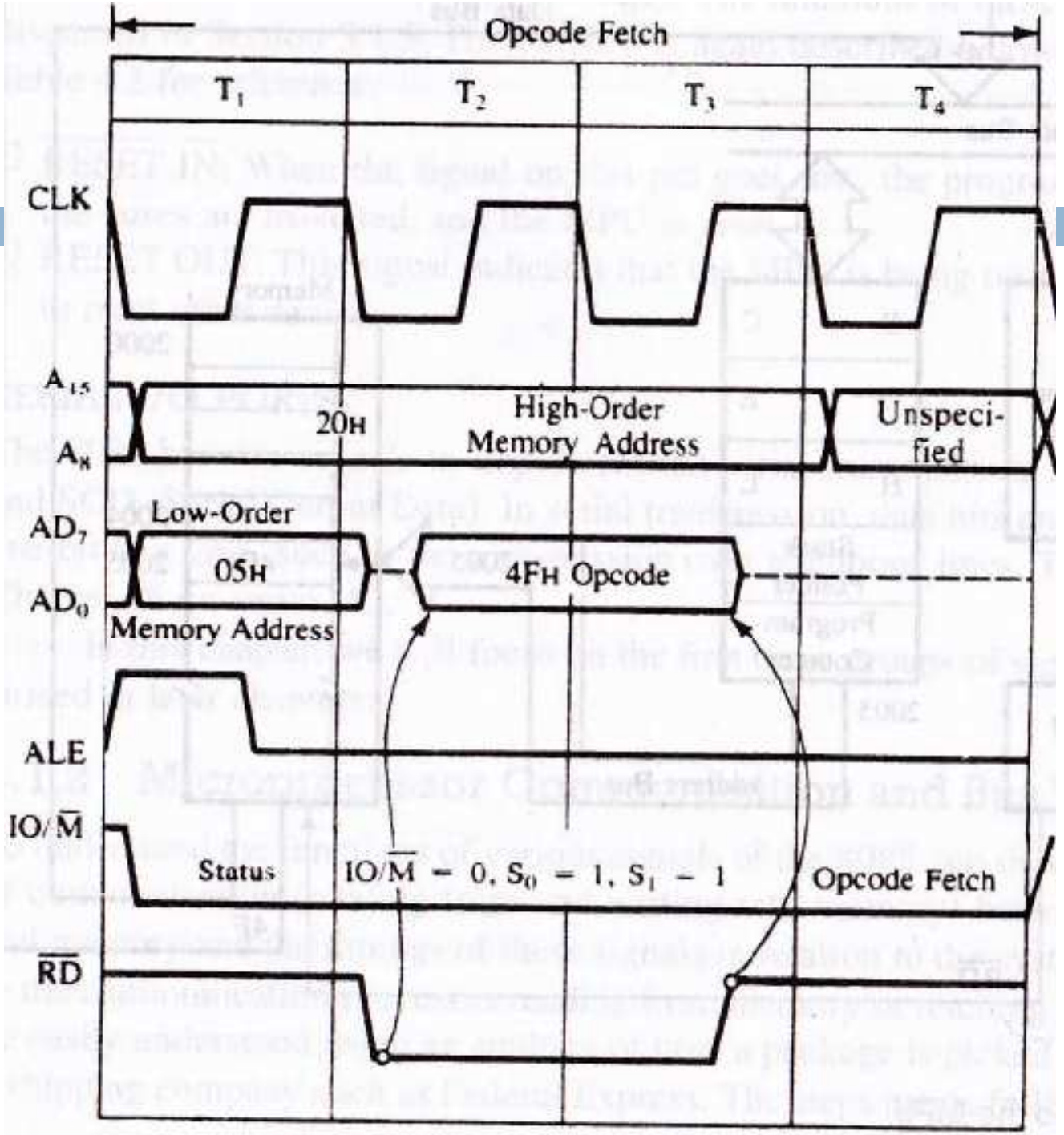
- 1-byte instruction — Hex-Codes
  - MOV C,A — (4F) => Pass the bowl
  - ADD B — (80)
- 2-byte instruction
  - MVI A,32H — (3E, 32)
- 3-byte instruction
  - LDA 2050H — (3A, 50, 20) => Order item #3
  - JMP 2085H — (C3, 85, 20)

8085 Timing Diagram(s)

- To show communication between the microprocessor and memory during a memory or I/O read or write operation
  - Memory read (opcode/instruction fetch, operand/data fetch)
  - Memory write
  - I/O read
  - I/O write

Steps For Fetching an Instruction

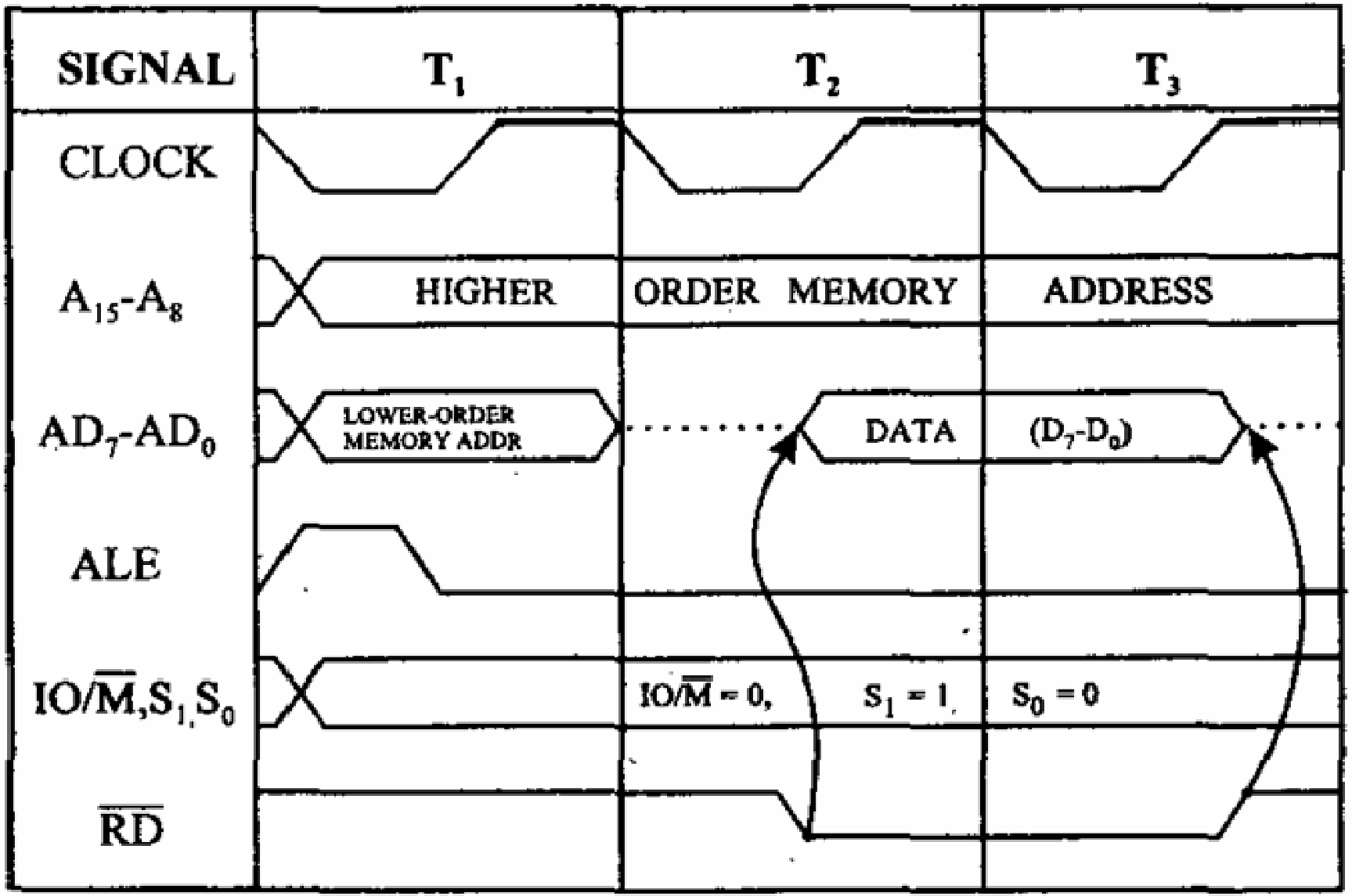
- Lets assume that we are trying to fetch the instruction at memory location 2005. That means that the program counter is now set to that value.
  - The following is the sequence of operations:
    - The program counter places the address value on the address bus and the controller issues a RD signal.
    - The memory's address decoder gets the value and determines which memory location is being accessed.
    - The value in the memory location is placed on the data bus.
    - The value on the data bus is read into the instruction decoder inside the microprocessor.
    - After decoding the instruction, the control unit issues the proper control signals to perform the operation.


Opcode Fetch
T1
T2
T3
T4
CLK
A15
A8
20H
High-Order
Memory Address
Unspeci-
fied
AD7
AD0
Low-Order
05H
Memory Address
4FH Opcode
ALE
IO/M
Status
IO/M = 0, S0 = 1, S1 = 1
Opcode Fetch
RD

Timing Signals For Fetching an Instruction

- Now, lets look at the exact timing of this sequence of events as that is extremely important
  - At T1 , the high order 8 address bits (20H) are placed on the address lines A8 – A15 and the low order bits are placed on AD7–AD0. The ALE signal goes high to indicate that AD0 – AD8 are carrying an address. At exactly the same time, the IO/M signal goes low to indicate a memory operation.
  - At the beginning of the T2 cycle, the low order 8 address bits are removed from AD7– AD0 and the controller sends the Read (RD) signal to the memory. The signal remains low (active) for two clock periods to allow for slow devices. During T2 , memory places the data from the memory location on the lines AD7– AD0 .
  - During T3 the RD signal is Disabled (goes high). This turns off the output Tri-state buffers in the memory. That makes the AD7– AD0 lines go to high impedence mode.

Memory Read Machine Cycle of 8085



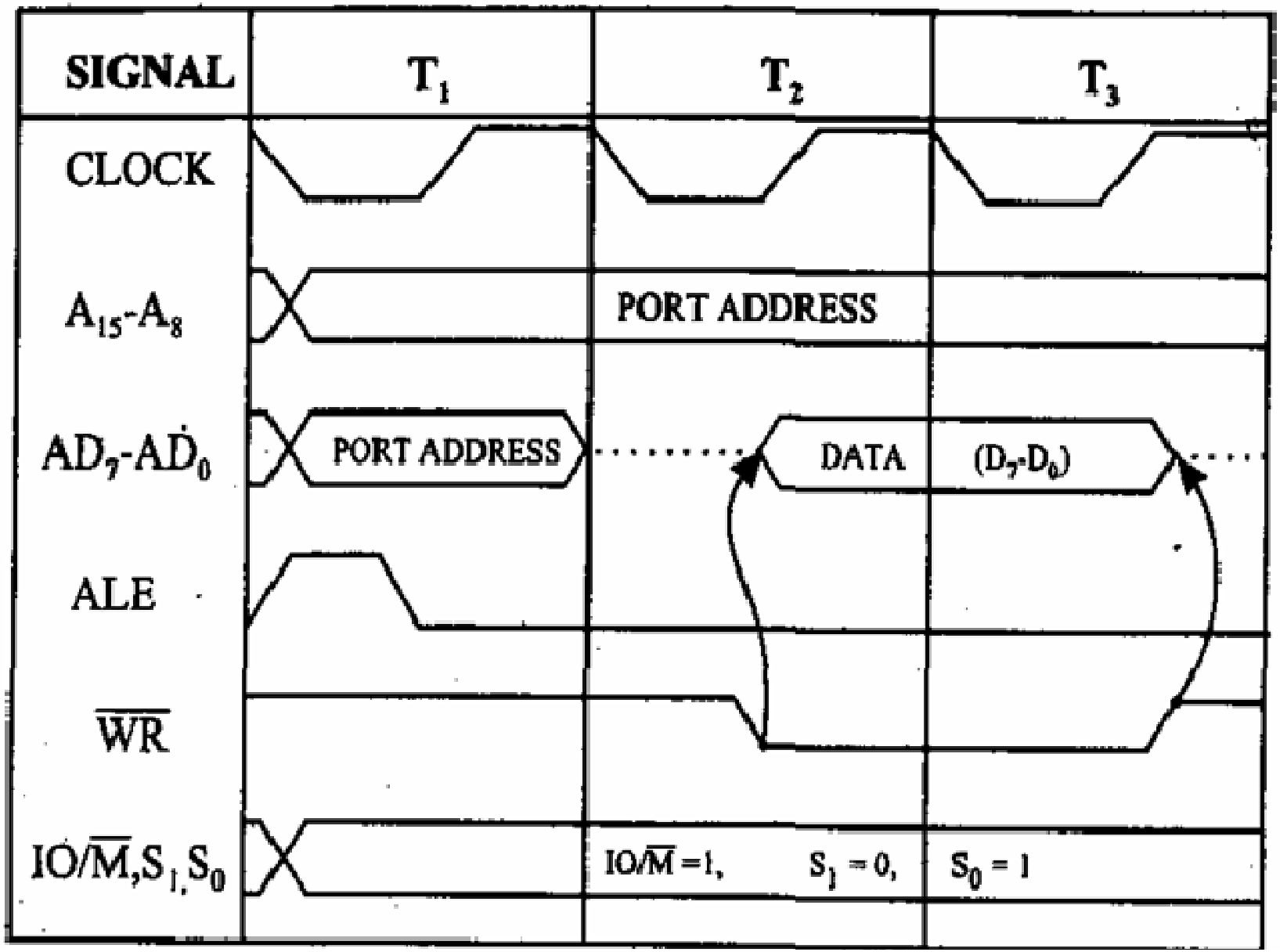
Input and Output Instructions

- OUT 01H
  - 2050 D3
  - 2051 01
- IN 84H
  - 2065 DB
  - 2066 84
- How to draw their timing diagrams?

I/O Read Cycle of 8085

- Can you draw it ??

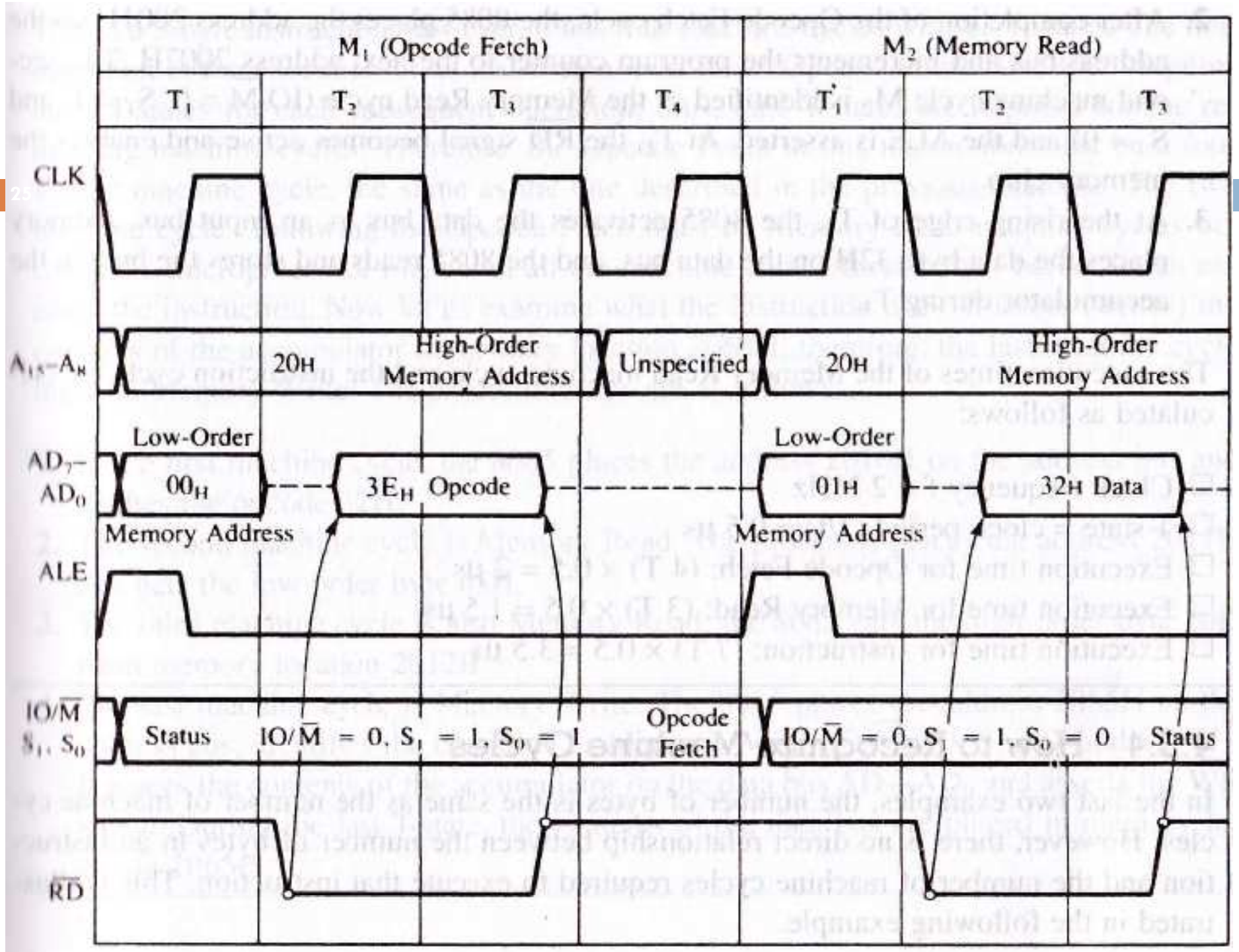
I/O Write Cycle of 8085



Opcodes for 8085

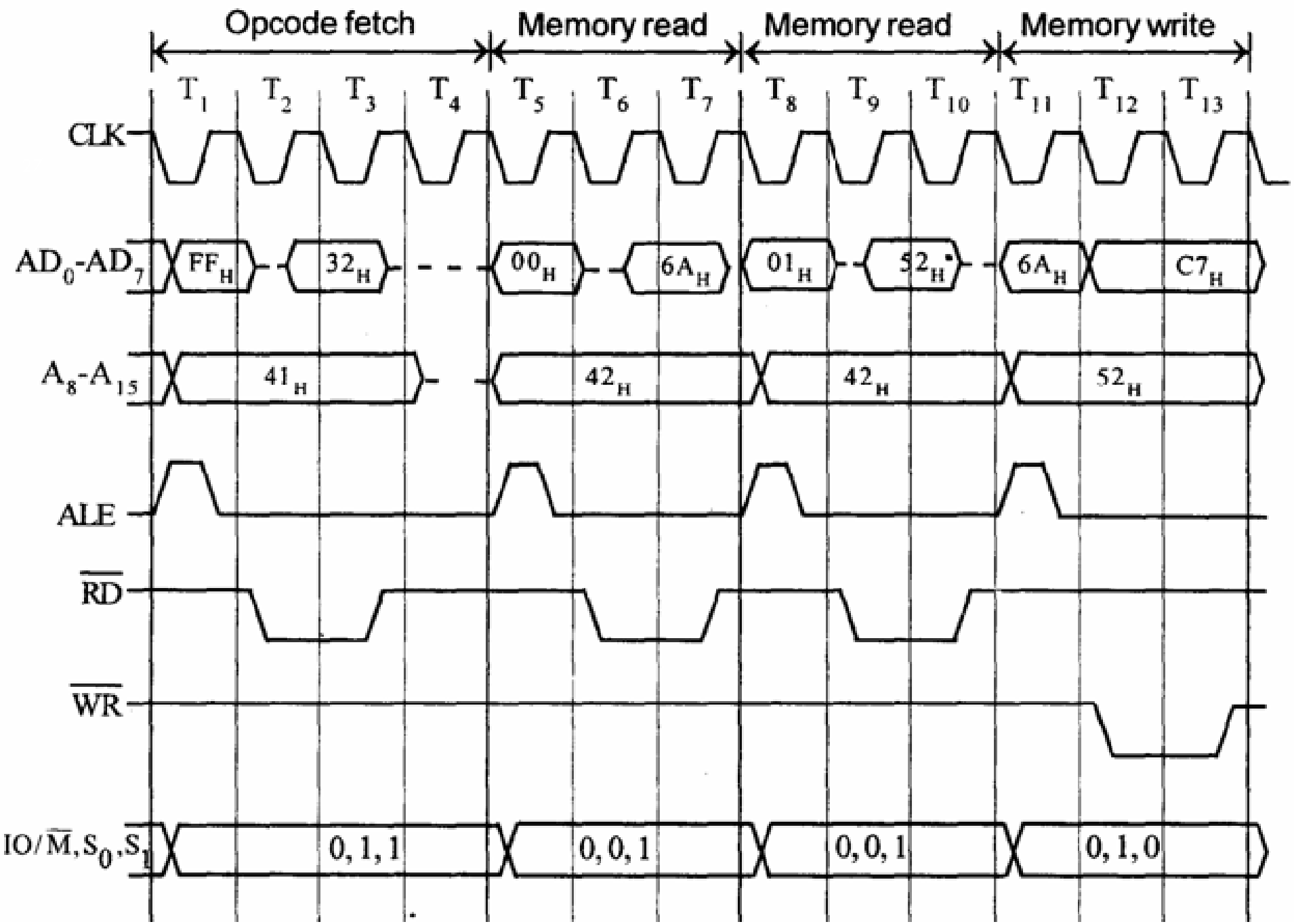
MOV r1,r2	7F	Move register to register
MOV M,r	77	Move register to Memory
MOV r,M	7E	Move Memory to register
MVI r,n	3E	Move Immediate
MVI M,n	36	Move Immediate to Memory
NOP	00	No Operation

- 2000H 3EH (hex-code for opcode MVI)
- 2001H 32H (data value)


M1 (Opcode Fetch)
M2 (Memory Read)
T1
T2
T3
T4
T1'
T2
T3
CLK
A15–A8
20H
High-Order Memory Address
Unspecified
20H
High-Order Memory Address
Low-Order
AD7–AD0
00H
3EH Opcode
Low-Order
01H
32H Data
Memory Address
Memory Address
ALE
IO/M
S1, S0
Status
IO/M = 0, S1 = 1, S0 = 1
Opcode Fetch
IO/M = 0, S1 = 1, S0 = 0
Status
RD

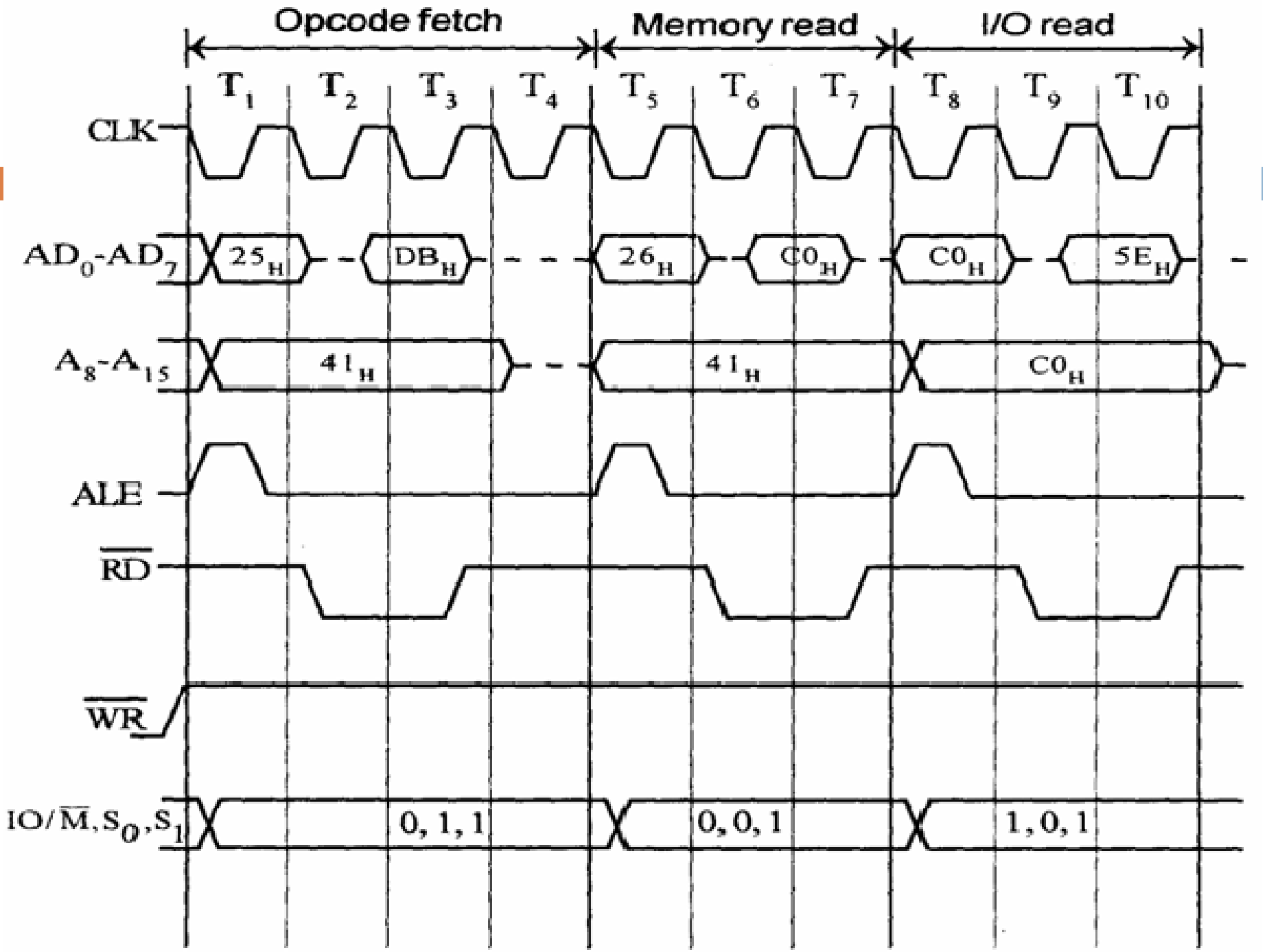
Timing Diagram for STA 526AH

Address	Mnemonics	Opcode
41FF	STA 526A$_H$	32$_H$
4200		6A$_H$
4201		52$_H$


Opcode fetch
Memory read
Memory read
Memory write
T1 T2 T3 T4 T5 T6 T7 T8 T9 T10 T11 T12 T13
CLK
AD0-AD7
FFH 32H 00H 6AH 01H 52H 6AH C7H
A8-A15
41H 42H 42H 52H
ALE
RD
WR
IO/M, S0, S1
0, 1, 1 0, 0, 1 0, 0, 1 0, 1, 0

Timing Diagram for IN C0H

Address	Mnemonics	Opcode
4125	IN $C0_H$	DB_H
4126		$C0_H$


Opcode fetch
Memory read
I/O read
T1
T2
T3
T4
T5
T6
T7
T8
T9
T10
CLK
AD0-AD7
25H
DBH
26H
C0H
C0H
5EH
A8-A15
41H
41H
C0H
ALE
RD
WR
IO/M, S0, S1
0, 1, 1
0, 0, 1
1, 0, 1