

# On Symmetric Circuits and FPC

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*Note:* dropping the uniformity condition gives us  $P/poly$ .

*Note also:* it makes no difference if the circuits are over the *Boolean basis*  $\{AND, OR, NOT\}$  or a richer basis (within  $P$ ).

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- Any symmetric circuit is invariant.
- Any formula of **FP** translates into a uniform family of polynomial-size *symmetric* Boolean circuits.
- Any formula of **FPC** translates into a uniform family of polynomial-size *symmetric* threshold (or majority) circuits.

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*No – as we shall see.*
- Are polynomial-size families of uniform symmetric *threshold circuits* more powerful than Boolean circuits? *Yes – follows from above.*
- Can every invariant circuit be translated into an equivalent symmetric threshold circuit, with only polynomial blow-up?  
*No – as we shall see.*

# Main Results

## Theorem

*A class of graphs is accepted by a  $P$ -uniform, polynomial-size, symmetric family of Boolean circuits **iff** it is definable by an  $FP$  formula interpreted in  $G \uplus ([n], <)$ .*

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*A class of graphs is accepted by a  $P$ -uniform, polynomial-size, symmetric family of threshold circuits iff it is definable in  $FPC$ .*

This gives a natural and purely circuit-based characterisation of  $FPC$  definability.

# Main Technical Tools

For a gate  $g$  in a symmetric circuit  $C_n$ , say that a partition  $\mathcal{P}$  *supports*  $g$  if every permutation that fixes each  $P \in \mathcal{P}$  also fixes  $g$ .

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Conversely, knowing that the orbit of  $g$  is at most polynomial in  $n$  gives us bounds on  $\text{Supp}(g)$ .

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## Theorem

For any  $1 > \epsilon \geq \frac{2}{3}$ , let  $C$  be a symmetric  $s$ -gate circuit over  $[n]$  with  $n \geq \frac{48}{\epsilon}$ , and  $s \leq 2^{n^{1-\epsilon}}$ . Then

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## Corollary

*Polynomial-size symmetric circuits have constant support.*



# Translating Symmetric Circuits to Formulas

Given a polynomial-time function  $n \mapsto C_n$  that generates symmetric circuits:

1. There is a formula of **FP** interpreted on  $([n], <)$  that defines a structure  $C_n$ .
2. Label gates with their support partition.
3. Transform labels into tuples by duplicating gates.
4. Determine equality test indicating edges of  $C_n$ .
5. Evaluate circuit on unordered universe (in **FP** for a Boolean circuit, in **FPC** for one with threshold gates.)

# Big Picture

<i>Logic</i>	<i>Circuits</i>
FP on structures with a disjoint number sort $([n], <)$ .	Poly-size <i>symmetric</i> Boolean circuits.
Additional predicates on number sort.	Non-uniformity (of function $n \mapsto C_n$ ).
Connections between element sort and number sort (FPC and FPrk).	Additional gates ( <i>counting</i> and <i>rank</i> ).
Choiceless polynomial time.	Breaking symmetry (how?).