Symbolic Noise Analysis of Low Voltage Amplifiers by Using Nullors

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Abstract—**We present the calculation of noise expressions of low voltage amplifiers by applying symbolic nodal analysis and using nullors. The nullor equivalents of the MOSFETs include only the dominant parasitic elements in order to generate a simplified symbolic noise expression, which provides a good insight to improve the design of low voltage amplifiers. The generated symbolic noise expressions are compared with HSPICE simulations, so that one can appreciate the good agreement with our proposed symbolic noise analysis approach.**

I. INTRODUCTION

In analog integrated circuit (IC) design, the challenges are oriented to provide high performances for analog signal processing applications. This can be possible by designing low voltage and low power ICs [1], with minimum noise and distortion, for instance.

The design of analog ICs can be improved by combining numerical simulation with symbolic approaches [2]. In fact, symbolic analysis has been applied to compute the noise of CMOS compatible analog ICs [3]. However, that symbolic approach can be enhanced by reducing the order of the system of equations when considering only dominant circuit-elements, as already shown in [2], [4], [5]. Further-more, for small matrices (up to order 12), the symbolic expression can be generated by applying Boolean logic operations [6], instead of using determinant decision diagrams [2]. In this manner, the goal of this paper is to show the application of symbolic nodal analysis (NA) [4]-[5], to generate simplified behavioral models of analog ICs using nullors [7]. In particular, we focus on low voltage amplifiers from one to three stages [1],[8]-[10].

This work is partially supported by UC-MEXUS-CONACyT under the project CN-09-310, by Promep Mexico under the project numbers UATLX-PTC-088, UATLX-CA-197, and by Consejeria de Innovacion Ciencia y Empresa, Junta de Andalucia, Spain, under the project number TIC-2532. The second author thanks to CONACyT for the sabbatical leave grant at University of California during 2009-2010. The third author thanks the support of the JAE-Doc program of CSIC, co-funded by FSE.

It can be appreciated that the use of the nullor allows us to eliminate many non-dominant parasitic elements, while the main advantage of analyzing nullor-circuits is to apply only NA, for the formulation stage [2].

In section II, we summarize the formulation by using nullors. In section III, low voltage amplifiers are analyzed using nullor equivalents. The analyses include the calculation of symbolic noise expressions for one, two and three stages amplifiers. Finally, in section IV the conclusions are shown.

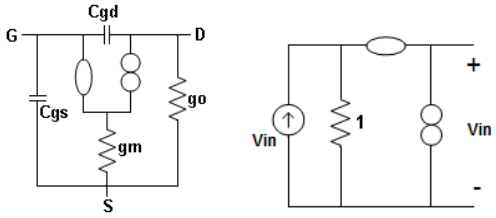

Figure 1. Nullor equivalent of the (a) MOSFET, and (b) independent voltage source.

II. FORMULATION BY USING NULLORS

The nullor equivalents of several active devices can be found in [2]-[5]. For the MOSFET, the nullor equivalent including the parasitic gate-source and gate-drain capacitors, output conductance and trans-conductance, is shown in Fig. 1(a) [2].

The nullator and the norator are quite useful to perform symbolic analysis by applying only NA, as already shown in [2]-[5]. In this manner, the independent voltage source is transformed to a current source, as shown in Fig. 1(b) [2], in order to model all circuit elements by using nullors [4]. Henceforth, the NA formulation method is summarized as follows [5]:

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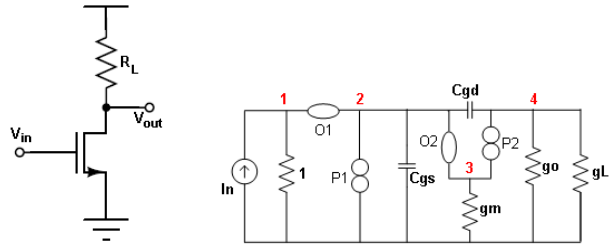
Step 1: Describe the interconnection relationships of norators P_j, nullators O_j, and admittances by generating tables including names and nodes.

Step 2: Calculate indexes associated to set row and column to group grounded and floating admittances:
(a) ROW: Contains all nodes ordered by applying the norator property whose nodes (m,n) are virtually short-circuited. These indexes are used to fill vector ***i*** and the admittance matrix ***Y***.
(b) COL: Contains all nodes ordered by applying the nullator property whose nodes (m,n) are virtually short-circuited. These indexes are used to fill vector ***v*** and the admittance matrix ***Y***.
(c) Admittances: They are grouped into two tables: Table A includes all nodes (ordered), and in each node is the sum of all admittances connected to it. Table B includes all floating admittances and its nodes (m,n).

Step 3: Use sets ROW and COL to fill vectors ***i*** and ***v***, respectively. To fill ***Y***: if in Table A a node is included in ROW and COL, introduce that admittance(s) in ***Y*** at position (ROW index, COL index). For each admittance in Table B, search the node m in ROW and n in COL (do the same but search n in ROW and m in COL), if both nodes exist the admittance is introduced in ***Y*** at position (ROW index, COL index), and it is negative.

Let's consider the common source amplifier with a resistive load shown in Fig. 2(a) [1]. By using the nullor equivalents of Fig. 1, the nullor circuit is shown in Fig. 2(b), where the input (In) is a voltage signal (v_{in}). In the formulation, the sets COL and ROW are: COL ={(1,2,3),(4)}, and ROW={(1),(3,4)}. The indexes of the admittances are given in Table A and B.

The admittance matrix is filled by performing a Cartesian product between COL and ROW sets [3], leading to the formulation given by (1). The solution for the voltage gain is given by (2). Other one stage amplifiers are the non-inverting shown in Fig. 3(a), and the differential pair shown in Fig. 3(b) [1]. For the differential pair, its nullor equivalent is shown in Fig. 4. The formulation generates an admittance matrix of order 5×5, and the exact gain is given by (3).



(a) (b)

Figure 2. (a) Common source amplifier with resistive load, and (b) its nullor equivalent.

$$\begin{bmatrix} v_{in} \\ 0 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ g_m - sC_{gd} & g_L + g_{ds} + sC_{gd} \end{bmatrix} \begin{bmatrix} v_{1,2,3} \\ v_4 \end{bmatrix} \quad (1)$$

$$A_v = \frac{(-gm + s\,Cgd)}{(gL + go + s\,Cgd)} \quad (2)$$

Table A	
Nodes	Admittances
1	1
2	sCgs+sCgd
3	gm
4	sCgd+gL+go

Table B	
Floating admittances	Nodes
sCgd	(2,4)

III. SYMBOLIC NOISE ANALYSIS APPROACH

In this section we show the calculation of the output noise expressions for low voltage amplifiers. For the input referred noise and noise figure, one can apply the expressions derived in [2], [3]. The derived noise expressions are compared with Hspice simulations using the level zero Spice 2 models.

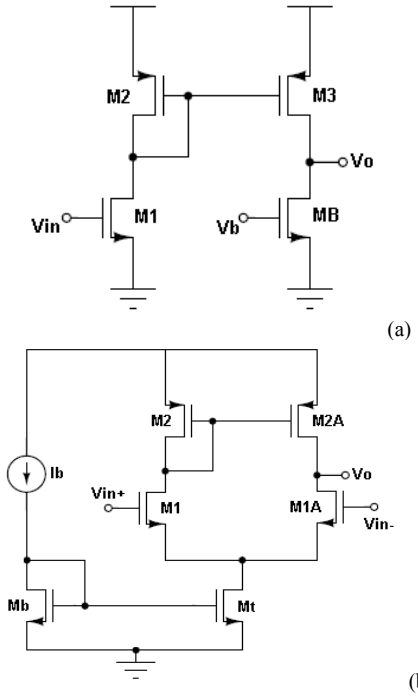


Figure 3. (a) Noninverting, and (b) differential amplifier.

$$\begin{aligned} Av = & \left(Cgd1\ Cgd3\ s^2 + (-Cgd3\ gm1 - gm3\ Cgd1)\ s + gm3\ gm1\right) / \\ & \big((Cgd1\ Cgdb + Cgs3\ Cgd3 + Cgd1\ Cgd3 + Cgd3\ Cgdb \\ & + Cgs2\ Cgd3 + Cgs2\ Cgdb + Cgs3\ Cgdb)\ s^2 + (go2\ Cgd3 \\ & + go1\ Cgdb + go1\ Cgd3 + Cgd3\ gob + Cgd3\ go3 + Cgd1\ gob \\ & + gm2\ Cgdb + Cgd3\ gm3 + go2\ Cgdb + gm2\ Cgd3 + Cgd1\ go3 \\ & + Cgs3\ gob + Cgs3\ go3 + Cgs2\ go3 + Cgs2\ gob)\ s + gm2\ go3 \\ & + gm2\ gob + go1\ go3 + go1\ gob + go2\ go3 + go2\ gob\big) \end{aligned} \quad (3)$$

The flicker and thermal noise are expressed as follows [3]:

Hspice Models	Flicker Noise	Thermal Noise
NLEV = 0	$S_{ID} = \frac{K_F I_{DS}^{AF}}{C_{ox} L_{eff}^2 f}$	$S_{channel} = \frac{8kTg_m}{3}$

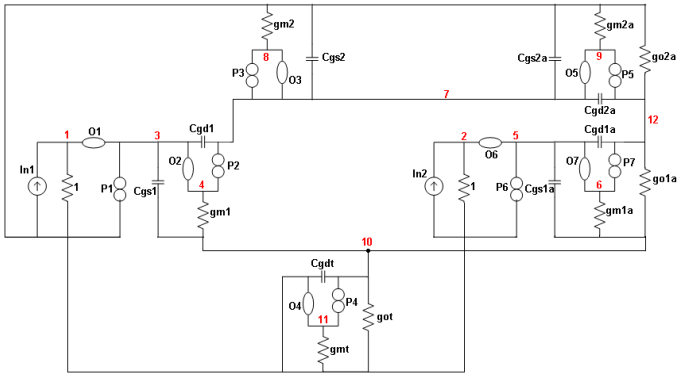


Figure 4. Nullor equivalent from Fig. 3(b).

By substituting the MOSFET from Fig. 2(a) using Fig. 1(a), eliminating capacitors and including noise sources, we get Fig. 5.

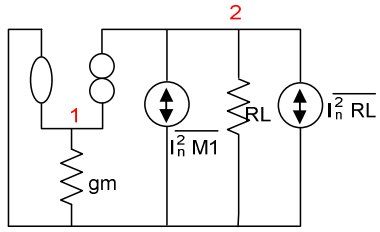


Figure 5. Equivalent circuit from Fig. 2(a) for noise analysis.

In this case, the noise source ($\overline{I_n^2 M1}$) can be represented by two components: one for thermal and the second for flicker noise. Meanwhile, the resistor includes its thermal noise source. The sets ROW and COL are: ROW={(1,2)}, COL ={(2)}. This circuit generates the equation:

$$[\mathrm{gL}]^2[\mathrm{V}_{1,2}]= [\,\overline{I_n^2 M1}+\overline{I_n^2 RL}\,]$$

Furthermore, the output noise voltage is given by (4).

$$\overline{V_{n,out}^2}=\left(4kT\frac{2}{3}gm+\frac{K}{CoxWL}\cdot\frac{1}{f}\cdot g_m^2+\frac{4kT}{R_L}\right)R_L^2 \qquad (4)$$

The output noise can be expressed by (6).

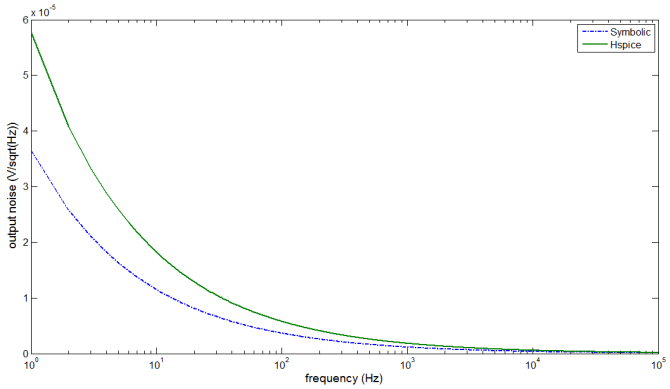


Figure 6. Noise responses for Fig. 2(a).

Comparing (4) with HSPICE simulations, we obtain the graph of Fig. 6. It can be observed the response given by the evaluation of the symbolic noise expression. The differential pair shown in Fig. 3(b), has the nullor equivalent for noise analysis shown in Fig. 7. It generates the following system of equations:

$$\begin{bmatrix} gm2^2 & gm1^2 & 0 \\ gm2a^2 & go1a^2+gm1a^2 & go1a^2+go2a^2 \\ 0 & got^2+gm1^2+gm1a^2+go1a^2 & go1a^2 \end{bmatrix}\begin{bmatrix} \overline{V^2}_{n,2,3,4} \\ \overline{V^2}_{n,6} \\ \overline{V^2}_{n,8} \end{bmatrix}=\begin{bmatrix} \overline{I^2}_{n,M1}+\overline{I^2}_{n,M2} \\ \overline{I^2}_{n,M1}+\overline{I^2}_{n,M1a}+\overline{I^2}_{n,Mt} \\ \overline{I^2}_{n,M1a}+\overline{I^2}_{n,M2a} \end{bmatrix} \qquad (5)$$

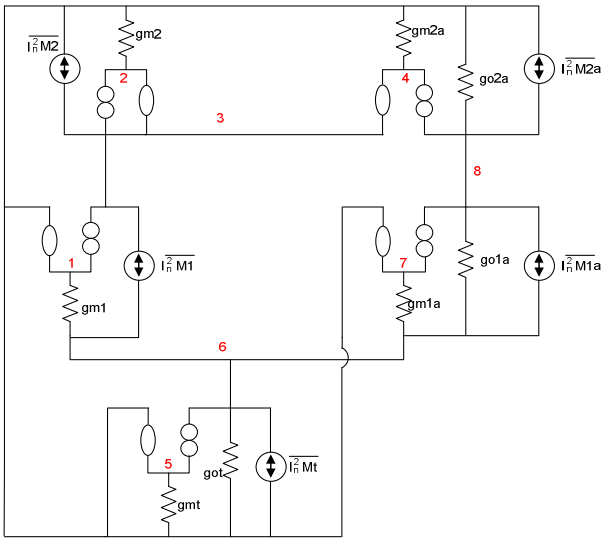


Figure 7. Equivalent circuit for Fig. 3(b).

$$\begin{aligned}\overline{V^2}_{n,out} &= (-gm2^2\,go1a^2\,\overline{I^2}_{n,M2a}-go1a^2gm2a^2\,\overline{I^2}_{n,M2}+gm1a^2gm2^2\,\overline{I^2}_{n,M1}-gm1a^2gm2a^2\,\overline{I^2}_{n,M1}-gm1a^2gm2a^2\,\overline{I^2}_{n,M2}+gm1a^2gm2^2\,\overline{I^2}_{n,Mt}\\ &+go1a^2gm2^2\,\overline{I^2}_{n,M1}+go1a^2gm2^2\,\overline{I^2}_{n,Mt}-go1a^2gm2a^2\,\overline{I^2}_{n,M1}+gm2a^2gm1^2\,\overline{I^2}_{n,M1a}+gm2^2got^2\,\overline{I^2}_{n,M1a}-gm1a^2gm2^2\,\overline{I^2}_{n,M2a}\\ &+gm2a^2gm1^2\,\overline{I^2}_{n,M2a}+gm2^2gm1^2\,\overline{I^2}_{n,M1a}+got^2gm2^2\,\overline{I^2}_{n,M1a}+got^2gm2^2\,\overline{I^2}_{n,Mt}-got^2gm2a^2\,\overline{I^2}_{n,M1}-got^2gm2a^2\,\overline{I^2}_{n,M2}+gm1^2gm2^2\,\overline{I^2}_{n,M1}\\ &-gm1^2gm2a^2\,\overline{I^2}_{n,M1}-gm1^2gm2a^2\,\overline{I^2}_{n,M2}+gm1^2gm2^2\,\overline{I^2}_{n,Mt})/(go1a^2gm2a^2gm1^2+gm2^2go1a^2got^2+gm2^2go1a^2gm1^2+gm2^2go2a^2got^2\\ &+gm2^2go2a^2gm1^2+gm2^2go2a^2gm1a^2+gm2^2go2a^2go1a^2)\end{aligned} \qquad (6)$$

Comparing the responses obtained with the evaluation of the symbolic expression and HSPICE, we obtain Fig. 8.

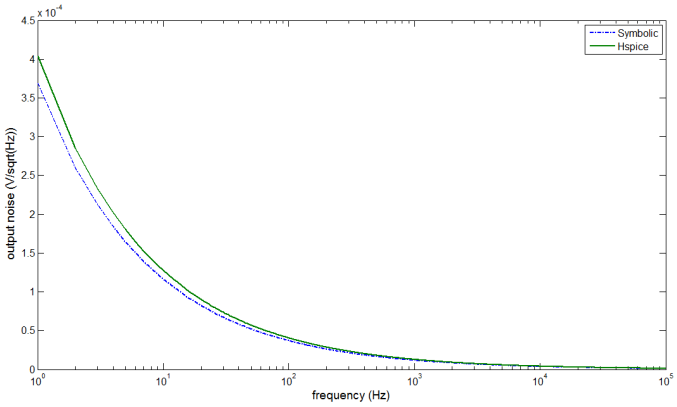


Figure 8. Responses of Hspice and the symbolic expression.

In Fig. 9 is shown a three stages amplifier. Its equivalent circuit for noise analysis is shown in Fig. 10.

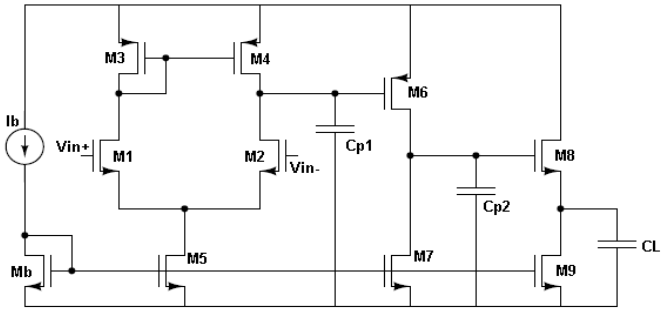


Figure 9. Uncompensated three stages amplifier.

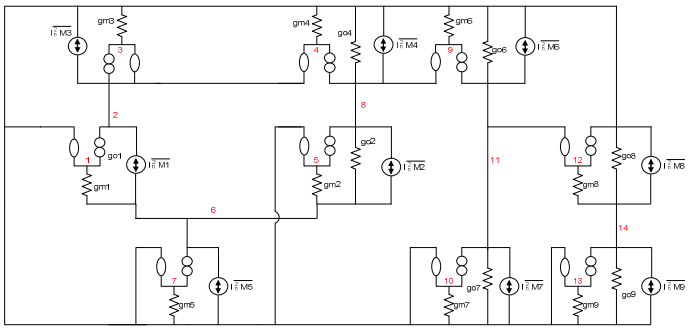


Figure 10. Equivalent circuit of the uncompensated amplifier

This circuit equivalent generates an admittance matrix of order 5×5, which can be easily solved by applying [6]. The output noise can be expressed by (7). Finally, the comparison between HSPICE and the evaluation of the symbolic expression is given in Fig. 11.

As a result, from Figs. 6, 8 and 11, we can conclude on the suitability of applying our proposed symbolic noise analysis approach for low voltage amplifiers. The main advantage is the application of only nodal analysis, while the formulation generates reduced equations which can be solved by [6].

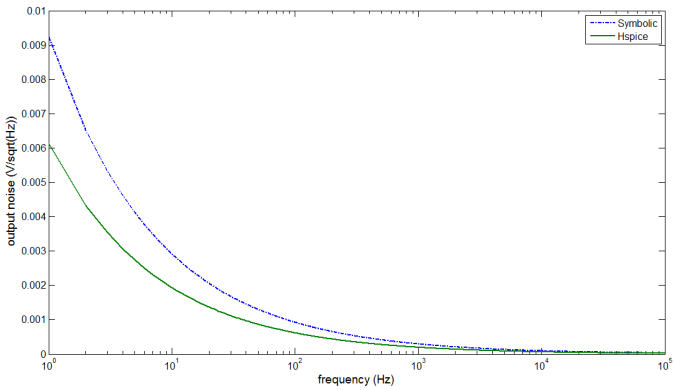


Figure 11. Response for uncompensated amplifier.

IV. SYMBOLIC NOISE ANALYSIS APPROACH

It was shown the usefulness of using nullor equivalents to generate symbolic noise expressions in low voltage amplifiers. The proposed approach can be implemented within an environment of analog IC design automation, in order to get an insight on the dominant noise sources for circuit optimization. As it can be appreciated, the order of the admittance matrices is low, so that one is able to compute other symbolic expressions and sensitivities in low computational cost. It is worthy to mention that the reduced formulation depends on the inclusion of those dominant parasitic elements, which is a future work to compute simplified behavioral models of analog integrated circuits.

Besides, the suitability of the proposed symbolic noise approach was demonstrated by comparing the generated symbolic expressions with HSPICE simulations, which are in good agreement.

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$$\overline{V^2}_{n,out} = (-gm4^2\,gm1^2\,gm8^2\,go2^2\,\overline{I^2}_{n,M7} + gm1^2\,gm8^2\,gm6^2\,gm3^2\,\overline{I^2}_{n,M1} + gm1^2\,gm3^2\,go4^2\,go6^2\,\overline{I^2}_{n,M9} - gm2^2\,gm8^2\,gm3^2\,go4^2\,\overline{I^2}_{n,M6}$$
$$+ go2^2\,gm3^2\,go4^2\,go6^2\,\overline{I^2}_{n,M9} + gm2^2\,gm3^2\,go4^2\,go7^2\,\overline{I^2}_{n,M8} - go2^2\,gm8^2\,gm6^2\,gm4^2\,\overline{I^2}_{n,M3} + go2^2\,gm8^2\,gm6^2\,gm3^2\,\overline{I^2}_{n,M1} - gm2^2\,gm8^2\,gm6^2\,gm4^2\,\overline{I^2}_{n,M1}$$
$$+ go2^2\,gm8^2\,gm6^2\,gm3^2\,\overline{I^2}_{n,M5} - go2^2\,gm8^2\,gm6^2\,gm4^2\,\overline{I^2}_{n,M1} - go2^2\,gm8^2\,gm3^2\,go4^2\,\overline{I^2}_{n,M6} - go2^2\,gm8^2\,gm3^2\,go4^2\,\overline{I^2}_{n,M7} + gm2^2\,gm8^2\,gm6^2\,gm3^2\,\overline{I^2}_{n,M5}$$
$$+ gm2^2\,gm3^2\,go4^2\,go6^2\,\overline{I^2}_{n,M9} + gm2^2\,gm3^2\,go4^2\,go6^2\,\overline{I^2}_{n,M8} + gm2^2\,gm3^2\,go4^2\,go7^2\,\overline{I^2}_{n,M8} + go2^2\,gm3^2\,go4^2\,go7^2\,\overline{I^2}_{n,M8} + go2^2\,gm3^2\,go4^2\,go7^2\,\overline{I^2}_{n,M9}$$
$$+ go2^2\,gm3^2\,go4^2\,go6^2\,\overline{I^2}_{n,M8} - gm2^2\,gm8^2\,gm3^2\,go4^2\,\overline{I^2}_{n,M7} - gm3^2\,gm2^2\,gm8^2\,gm6^2\,\overline{I^2}_{n,M4} - gm3^2\,go2^2\,gm8^2\,gm6^2\,\overline{I^2}_{n,M4} + gm4^2\,gm1^2\,go2^2\,go7^2\,\overline{I^2}_{n,M8}$$
$$- gm4^2\,gm1^2\,gm8^2\,go2^2\,\overline{I^2}_{n,M6} + gm4^2\,gm1^2\,gm8^2\,gm6^2\,\overline{I^2}_{n,M4} + gm4^2\,gm1^2\,gm8^2\,gm6^2\,\overline{I^2}_{n,M2} + gm4^2\,gm1^2\,go2^2\,go6^2\,\overline{I^2}_{n,M8} + gm4^2\,gm1^2\,go2^2\,go6^2\,\overline{I^2}_{n,M9}$$
$$+ gm1^2\,gm8^2\,gm6^2\,gm3^2\,\overline{I^2}_{n,M2} + gm4^2\,gm1^2\,go2^2\,go7^2\,\overline{I^2}_{n,M9} + gm1^2\,gm8^2\,gm6^2\,gm3^2\,\overline{I^2}_{n,M5} - gm1^2\,gm8^2\,gm6^2\,gm4^2\,\overline{I^2}_{n,M3} - gm1^2\,gm8^2\,gm6^2\,gm4^2\,\overline{I^2}_{n,M1}$$
$$- gm1^2\,gm8^2\,gm3^2\,go2^2\,\overline{I^2}_{n,M7} - gm1^2\,gm8^2\,gm3^2\,go2^2\,\overline{I^2}_{n,M6} - gm1^2\,gm8^2\,gm3^2\,go4^2\,\overline{I^2}_{n,M7} - gm1^2\,gm8^2\,gm3^2\,go4^2\,\overline{I^2}_{n,M6} + gm1^2\,gm3^2\,go2^2\,go6^2\,\overline{I^2}_{n,M9}$$
$$+ gm1^2\,gm3^2\,go2^2\,go6^2\,\overline{I^2}_{n,M8} + gm1^2\,gm3^2\,go4^2\,go7^2\,\overline{I^2}_{n,M9} + gm1^2\,gm3^2\,go4^2\,go6^2\,\overline{I^2}_{n,M8} + gm1^2\,gm3^2\,go2^2\,go7^2\,\overline{I^2}_{n,M8} + gm1^2\,gm3^2\,go2^2\,go7^2\,\overline{I^2}_{n,M9}$$
$$+ gm1^2\,gm3^2\,go4^2\,go7^2\,\overline{I^2}_{n,M8} - gm2^2\,gm8^2\,gm6^2\,gm4^2\,\overline{I^2}_{n,M3} + gm2^2\,gm8^2\,gm6^2\,gm3^2\,\overline{I^2}_{n,M1})\,/\,(gm4^2\,gm1^2\,go2^2\,go6^2\,go8^2 + gm4^2\,gm1^2\,go2^2\,go7^2\,go8^2$$
$$+ gm2^2\,gm3^2\,go4^2\,go6^2\,go9^2 + gm1^2\,gm3^2\,go2^2\,go6^2\,go8^2 + gm2^2\,gm3^2\,go4^2\,go7^2\,go8^2 + gm2^2\,gm3^2\,go4^2\,go7^2\,go9^2 + go2^2\,gm3^2\,go4^2\,go6^2\,go8^2$$
$$+ gm4^2\,gm1^2\,go2^2\,go7^2\,go9^2 + gm1^2\,gm3^2\,go4^2\,go6^2\,go9^2 + gm1^2\,gm3^2\,go4^2\,go6^2\,go8^2 + gm4^2\,gm1^2\,go2^2\,go6^2\,go9^2 + gm1^2\,gm3^2\,go4^2\,go7^2\,go8^2$$
$$+ gm1^2\,gm3^2\,go4^2\,go7^2\,go9^2 + go2^2\,gm3^2\,go4^2\,go6^2\,go9^2 + gm2^2\,gm3^2\,go4^2\,go6^2\,go8^2 + gm1^2\,gm3^2\,go2^2\,go6^2\,go9^2 + go2^2\,gm3^2\,go4^2\,go7^2\,go8^2$$
$$+ go2^2\,gm3^2\,go4^2\,go7^2\,go9^2 + gm1^2\,gm3^2\,go2^2\,go7^2\,go8^2 + gm1^2\,gm3^2\,go2^2\,go7^2\,go9^2) \qquad (7)$$

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