## On the Complexity of Path Checking in Temporal Logics

Daniel Bundala Joël Ouaknine

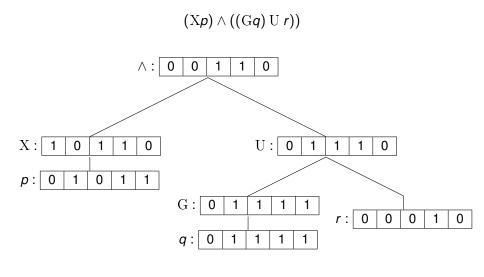
Department of Computer Science University of Oxford

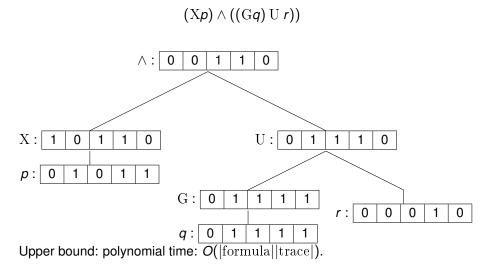
# Given LTL formula $(\mathrm{X} ho) \wedge ((\mathrm{G} q) \ \mathrm{U} \ r))$

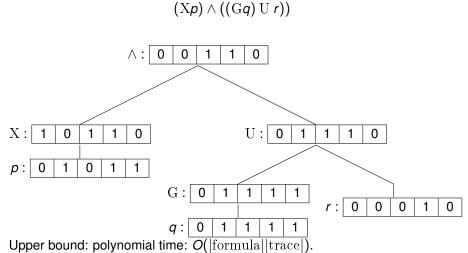
## Given LTL formula $(Xp) \wedge ((Gq) \cup r))$ and finite trace

	and finite trace							
<b>p</b> :	0	1	0	1	1			
<b>q</b> :	0	1	1	1	1			
<i>r</i> :	0	0	0	1	0			

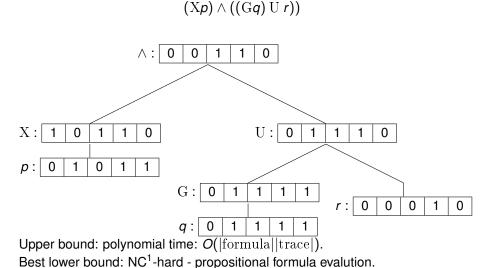
Does it satisfy the formula? What is the complexity of checking?



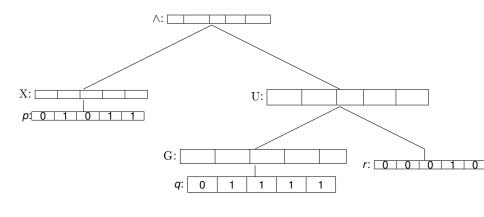


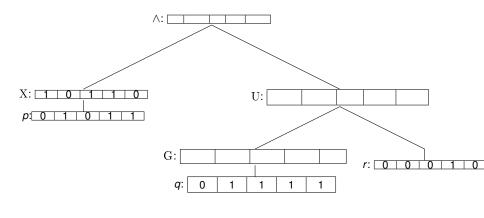


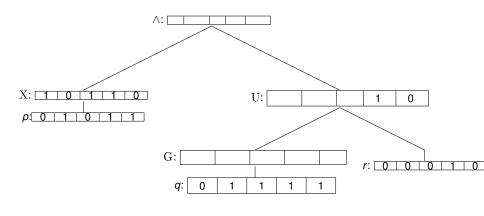
Best lower bound: NC<sup>1</sup>-hard - propositional formula evalution.

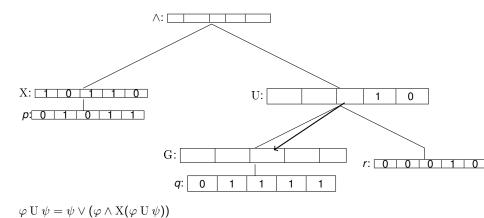


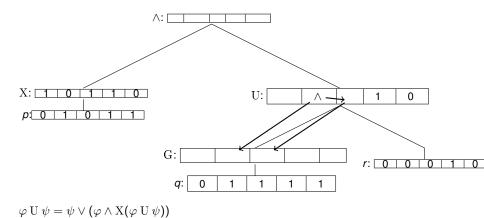
Can we do better than P?

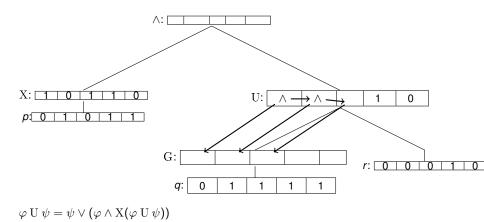


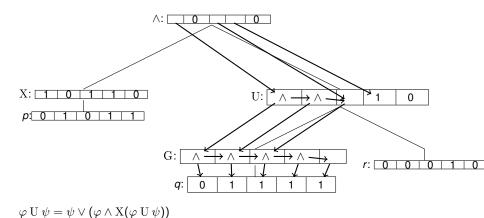


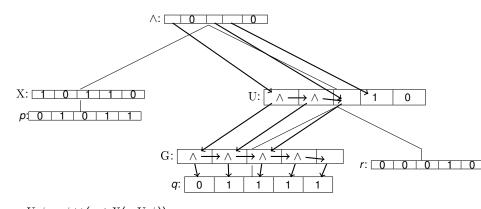




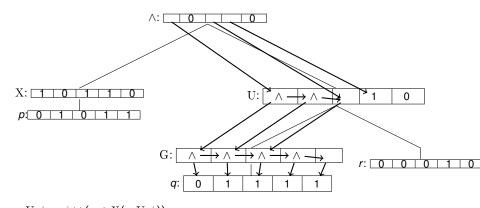








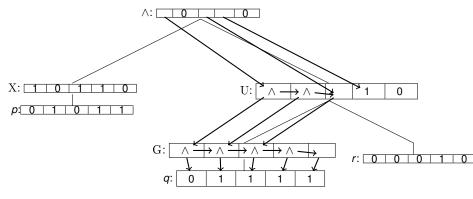
 $\varphi \ \mathrm{U} \ \psi = \psi \lor (\varphi \land \mathrm{X}(\varphi \ \mathrm{U} \ \psi))$  Build circuits for independent leaves in parallel.



$$\varphi \cup \psi = \psi \vee (\varphi \wedge X(\varphi \cup \psi))$$

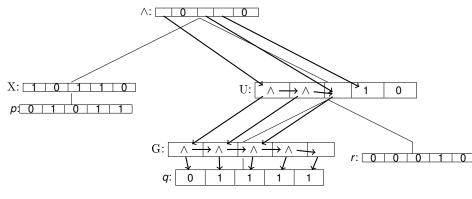
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Circuits:



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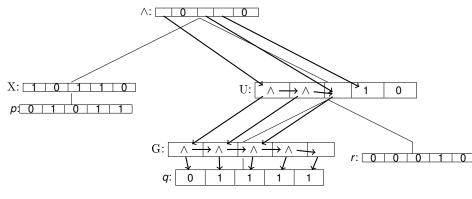
 $\varphi \ \mathrm{U} \ \psi = \psi \lor (\varphi \land \mathrm{X}(\varphi \ \mathrm{U} \ \psi))$  Build circuits for independent leaves in parallel. Circuits: planar, layered, stratified, monotone



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Circuits: planar, layered, stratified, monotone (logDCFL  $\subseteq$  AC<sup>1</sup>)

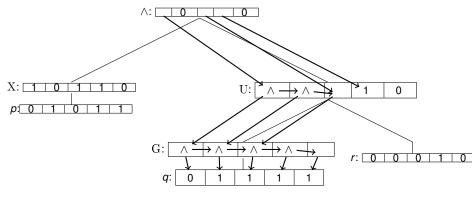


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Build circuits for independent leaves in parallel.

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log |formula| parallel stages are sufficient.

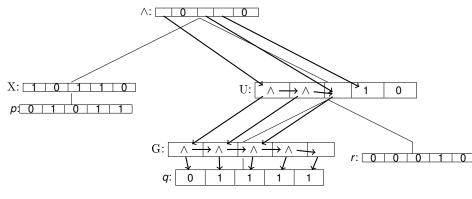


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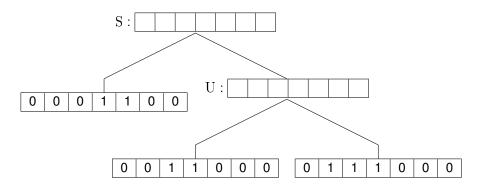
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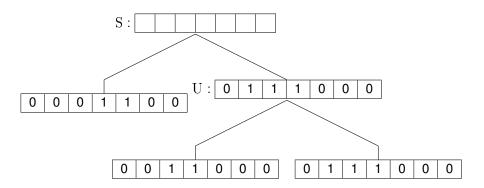
Build circuits for independent leaves in parallel.

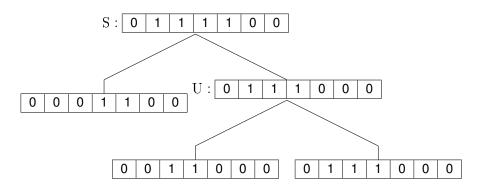
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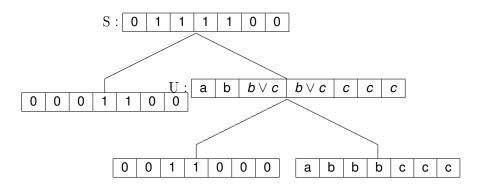
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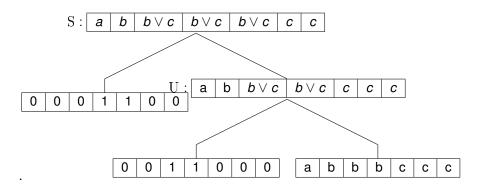
 $AC^1[logDCFL]\subseteq AC^2 \implies \text{ efficient parallel algorithm for LTL path checking. LTL path checking unlikely P-hard}$ 

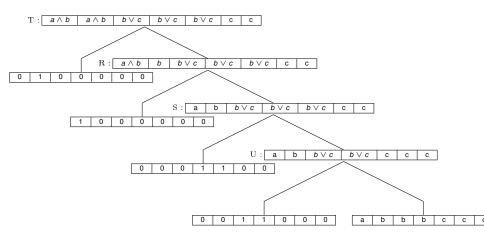


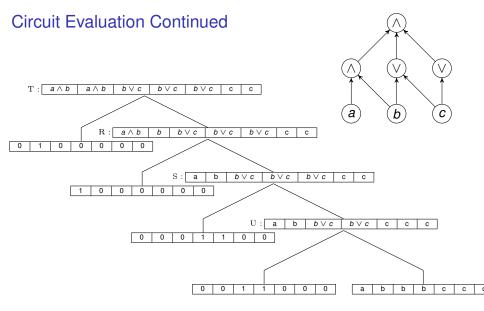




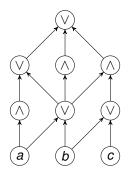




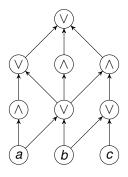




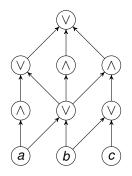
Evaluated a single layer of the circuit



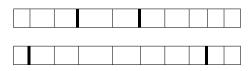
Inductively, circuit evaluation reduces to LTL path checking

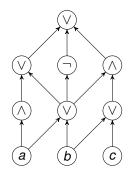


Inductively, circuit evaluation reduces to LTL path checking Matching upper bounds (AC¹[logDCFL])



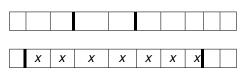
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Nonmonotone circuits: PTIME-Complete

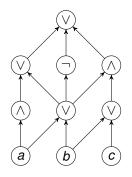




Inductively, circuit evaluation reduces to LTL path checking Matching upper bounds (AC<sup>1</sup>[logDCFL])

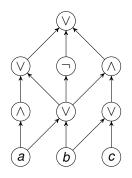
Nonmonotone circuits: PTIME-Complete





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Nonmonotone circuits: PTIME-Complete

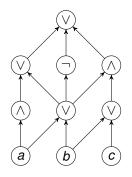
X	or		1	1				
	Х	X	Х	Х	Х	Х	X	



Inductively, circuit evaluation reduces to LTL path checking Matching upper bounds (AC<sup>1</sup>[logDCFL])

Nonmonotone circuits: PTIME-Complete

			$\neg x$	$\neg x$				
X	or		1	1				
	Χ	Х	X	Х	X	Х	X	



Inductively, circuit evaluation reduces to LTL path checking Matching upper bounds (AC<sup>1</sup>[logDCFL])

Nonmonotone circuits: PTIME-Complete

			$\neg x$	$\neg x$				
X	or		1	1				
	Χ	Х	Х	Х	Χ	Х	X	

⇒ LTL+XOR path checking is PTIME-complete





Formula  $p U_{[1,3]} q$ :

<b>p</b> :	*	*	*	*	*	*	*	*
<b>q</b> :	0	0	0	0	1	0	1	1
<i>t</i> :	1	2	3	3.5	3.8	4	4.5	5

Formula  $p U_{[1,3]} q$ :

<b>p</b> :	*	*	*	*	*	*	*	*
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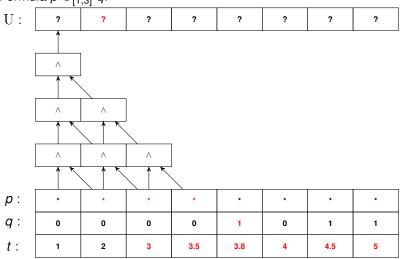
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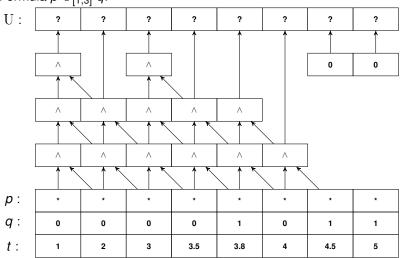
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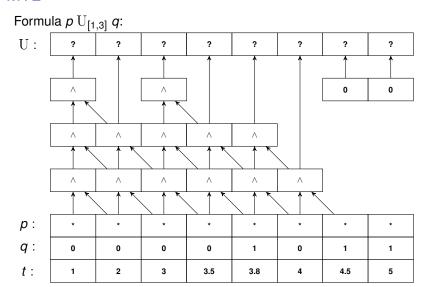
<b>p</b> :	*	*	*	*	*	*	*	*
<b>q</b> :	0	0	0	0	1	0	1	1
t:	1	2	3	3.5	3.8	4	4.5	5

# Formula $p U_{[1,3]} q$ :

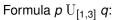


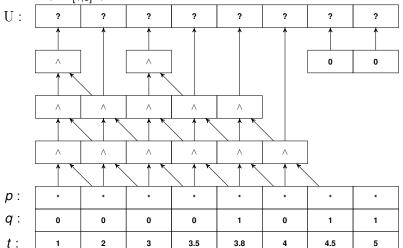
# Formula $p U_{[1,3]} q$ :





Similar circuits for other operators



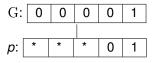


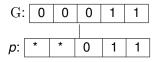
Similar circuits for other operators

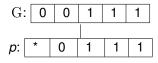
⇒ MTL path checking in AC<sup>1</sup>[logDCFL].

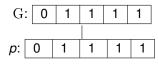














Polynomially many possibilities for  $Gp \implies$  can be stored explicitly in polynomial space

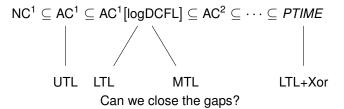


Polynomially many possibilities for  $\mathrm{G}\rho \Longrightarrow \mathrm{can}$  be stored explicitly in polynomial space Leads to  $\mathrm{AC}^1$  algorithm for UTL



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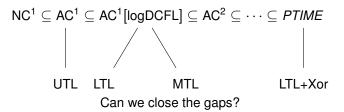
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# Questions?