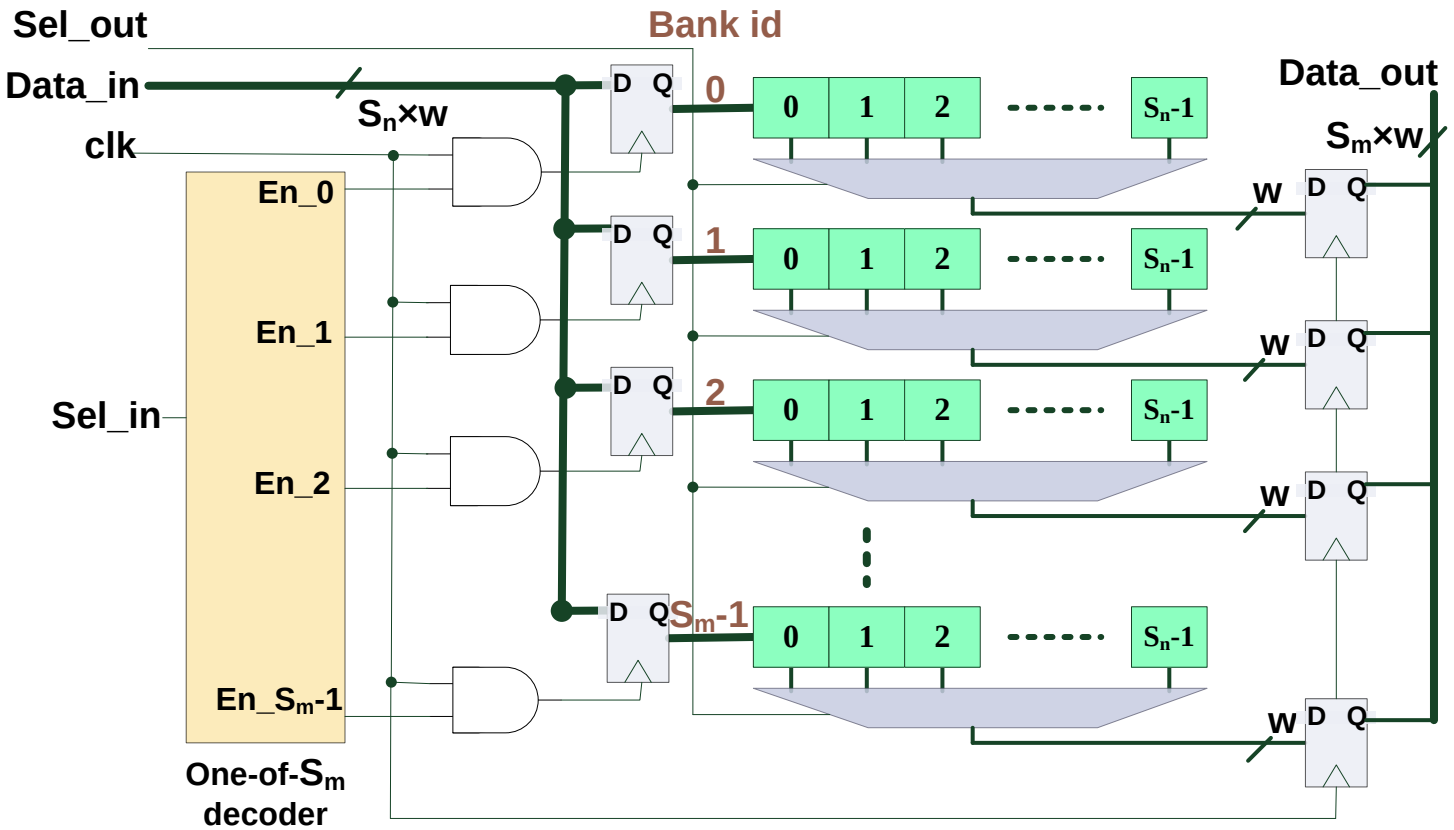
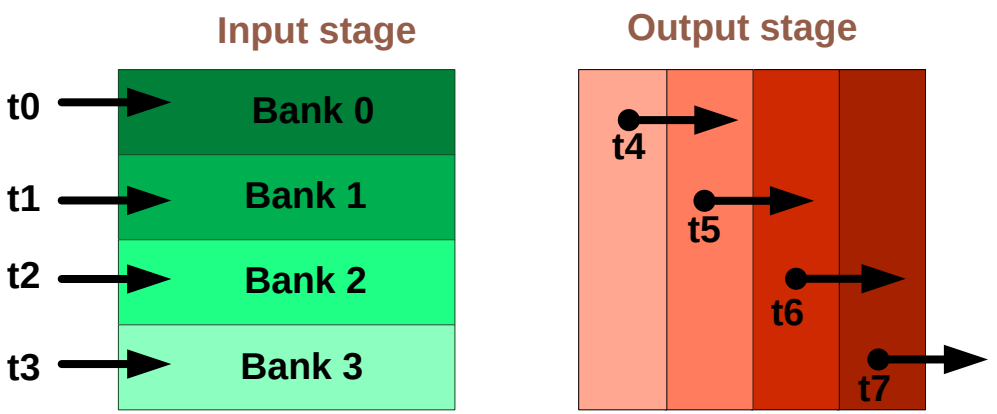

Sel_out
Bank id
Data_in
Sn×w
clk
Data_out
Sm×w
En_0
En_1
Sel_in
En_2
En_Sm-1
One-of-Sm decoder
D Q
0
1
2
Sm-1
0 1 2 Sn-1
w

(a)


Input stage
Output stage
t0
t1
t2
t3
Bank 0
Bank 1
Bank 2
Bank 3
t4
t5
t6
t7

(b)