



1. Description

1.1. Project

Project Name	AD
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	12/18/2023

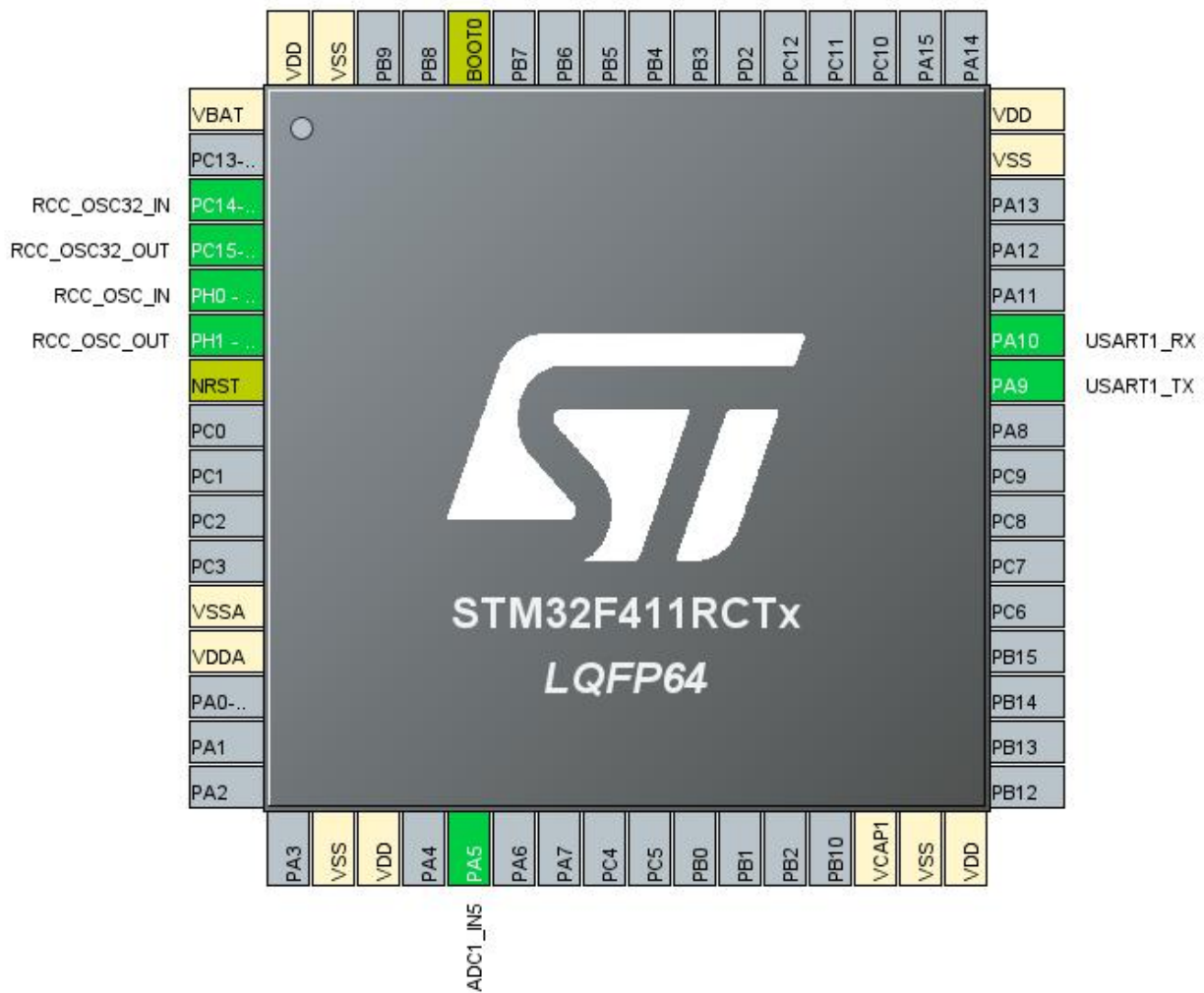
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F411
MCU name	STM32F411RCTx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4
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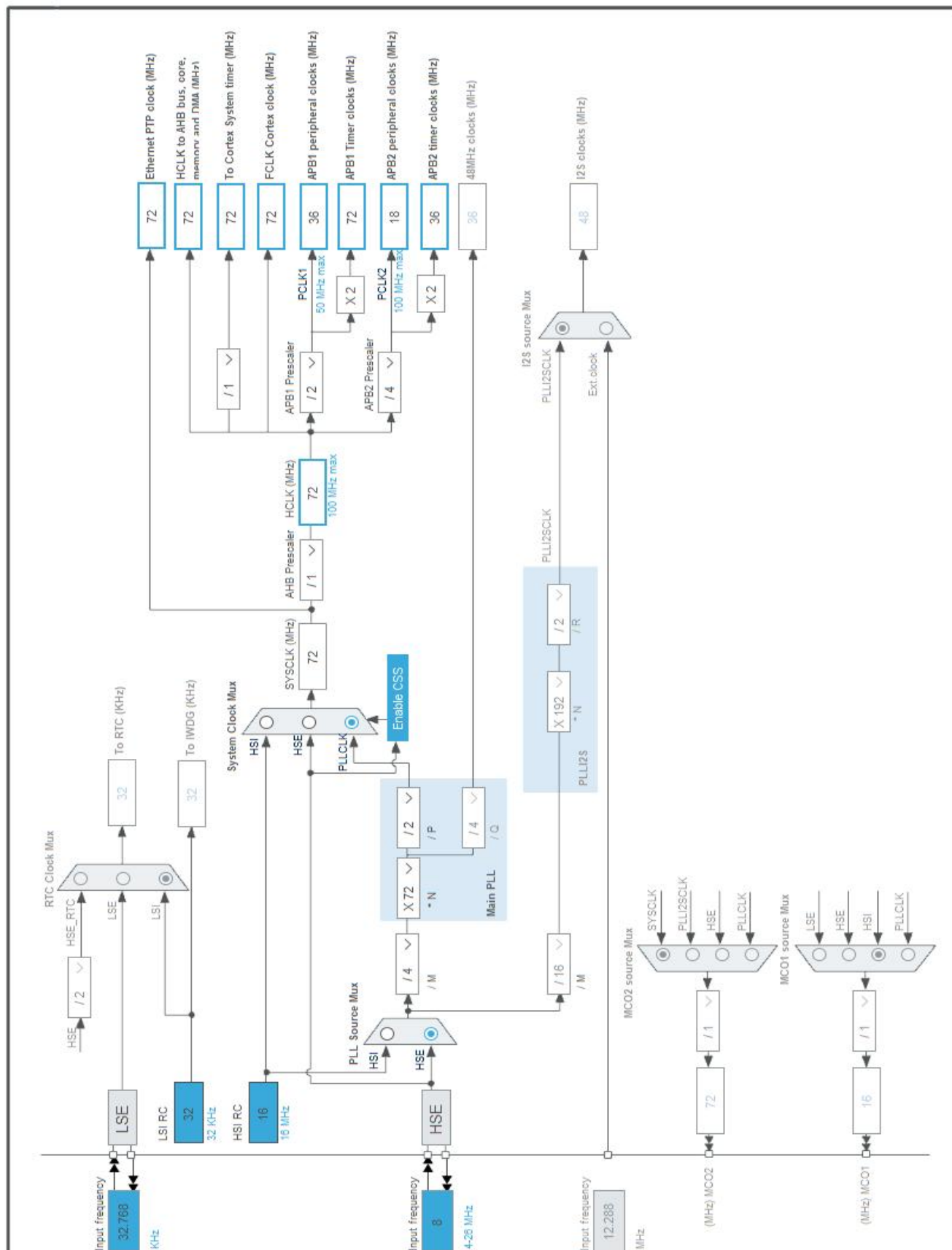
2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
3	PC14-OSC32_IN	I/O	RCC_OSC32_IN	
4	PC15-OSC32_OUT	I/O	RCC_OSC32_OUT	
5	PH0 - OSC_IN	I/O	RCC_OSC_IN	
6	PH1 - OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
18	VSS	Power		
19	VDD	Power		
21	PA5	I/O	ADC1_IN5	
30	VCAP1	Power		
31	VSS	Power		
32	VDD	Power		
42	PA9	I/O	USART1_TX	
43	PA10	I/O	USART1_RX	
47	VSS	Power		
48	VDD	Power		
60	BOOT0	Boot		
63	VSS	Power		
64	VDD	Power		

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	AD
Project Folder	C:\Users\nano\Desktop\STM32CubeMXdemo\AD
Toolchain / IDE	MDK-ARM V5
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.2
Application Structure	Advanced
Generate Under Root	No
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy all used libraries into the project folder
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	SystemClock_Config	RCC
3	MX_USART1_UART_Init	USART1
4	MX_ADC1_Init	ADC1

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F411
MCU	STM32F411RCTx
Datasheet	DS10314_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	1.7

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

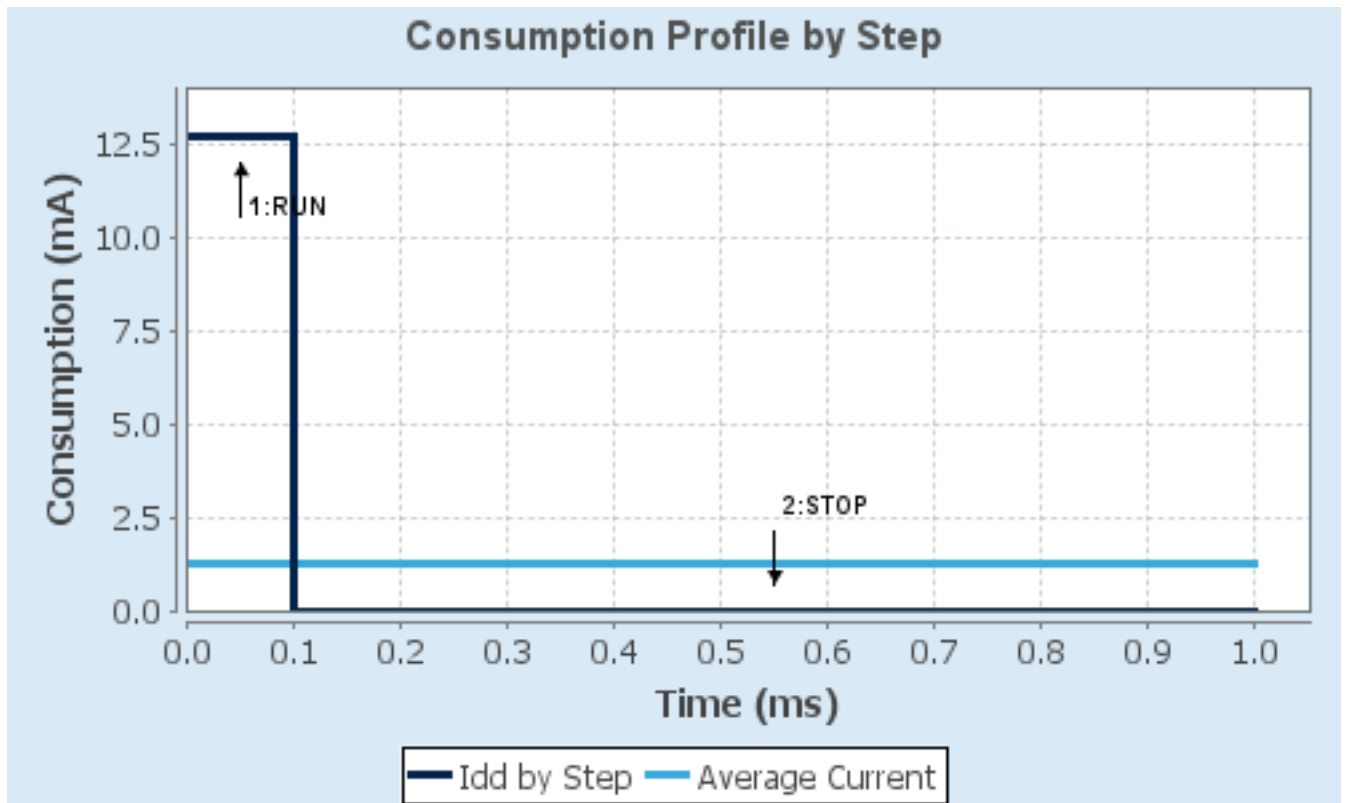
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP
Vdd	1.7	1.7
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	SRAM	n/a
CPU Frequency	100 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LPLV Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	12.7 mA	9 μ A
Duration	0.1 ms	0.9 ms
DMIPS	125.0	0.0
Ta Max	103.99	105
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	1.28 mA
Battery Life	3 months, 19 days, 6 hours	Average DMIPS	125.0 DMIPS

6.6. Chart



7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN5

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode Independent mode

ADC_Settings:

Clock Prescaler PCLK2 divided by 2

Resolution 12 bits (15 ADC Clock cycles)

Data Alignment Right alignment

Scan Conversion Mode Disabled

Continuous Conversion Mode **Enabled ***

Discontinuous Conversion Mode Disabled

DMA Continuous Requests Disabled

End Of Conversion Selection EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

External Trigger Conversion Edge None

Rank 1

Channel Channel 5

Sampling Time **15 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3

Instruction Cache Enabled

Prefetch Buffer Enabled

Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)
RCC Parameters:	
HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timeout Value (ms)	100
LSE Startup Timeout Value (ms)	5000
Power Parameters:	
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.3. SYS

Timebase Source: SysTick

7.4. USART1

Mode: Asynchronous

7.4.1. Parameter Settings:

Basic Parameters:	
Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1
Advanced Parameters:	
Data Direction	Receive and Transmit
Over Sampling	16 Samples

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA5	ADC1_IN5	Analog mode	No pull-up and no pull-down	n/a	
RCC	PC14-OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15-OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0 - OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1 - OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
USART1	PA9	USART1_TX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	
	PA10	USART1_RX	Alternate Function Push Pull	No pull-up and no pull-down	Very High *	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	15	0
ADC1 global interrupt	true	0	0
USART1 global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
ADC1 global interrupt	false	true	true
USART1 global interrupt	false	true	true

* User modified value

9. System Views

9.1. Category view

9.1.1. Current

Middleware

System Core

Analog

Timers

Connectivity

Multimedia

Computing

DMA

ADC1



USART1



GPIO



NVIC



RCC



SYS



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00115249.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00119316.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00137034.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00144612.pdf
Application note	http://www.st.com/resource/en/application_note/DM00156364.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note http://www.st.com/resource/en/application_note/DM00213525.pdf
Application note http://www.st.com/resource/en/application_note/DM00220769.pdf
Application note http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note http://www.st.com/resource/en/application_note/DM00236305.pdf
Application note http://www.st.com/resource/en/application_note/DM00257177.pdf
Application note http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note http://www.st.com/resource/en/application_note/DM00296349.pdf
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Application note http://www.st.com/resource/en/application_note/DM00325582.pdf
Application note http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note http://www.st.com/resource/en/application_note/DM00380469.pdf
Application note http://www.st.com/resource/en/application_note/DM00395696.pdf
Application note http://www.st.com/resource/en/application_note/DM00431633.pdf
Application note http://www.st.com/resource/en/application_note/DM00493651.pdf
Application note http://www.st.com/resource/en/application_note/DM00536349.pdf
Application note http://www.st.com/resource/en/application_note/DM00725181.pdf