|  |  |  |
| --- | --- | --- |
| Name | Type | Description |
| instruction\_1\_i | logic[31:0] | Input for instruction 1 |
| instruction\_2\_i | logic[31:0] | Input for instruction 2 |
| data\_out\_o | logic[31:0] | Output |
| pc\_o | Logic[4:0] | Program Counter |

Register renaming (look up table, which handles the WAW and WAR hazards)

|  |  |  |
| --- | --- | --- |
| Name | Type | Description |
| Instruction\_1\_i | Logic[31:0] | Instruction 1 for renaming |
| Instruction\_2\_i | Logic[31:0] | Instruction 2 for renaming |
| Instruction\_1\_o | Logic[31:0] | Instruction 1 after renaming |
| Instruction\_2\_o | Logic[31:0] | Instruction 2 after renaming |
| Rename\_full\_o | Wire | When there is no more register available for renaming, this signal is set to high and sent back to the previous pipeline stage to stop getting new instructions for renaming. |
|  |  |  |

Issue queue (handles RAW hazard)

|  |  |  |
| --- | --- | --- |
| Name | Type | Description |
| Instruction\_1\_i | Logic[31:0] |  |
| Instruction\_2\_i | Logic[31:0] |  |
| flush\_en | Wire | When this signal is high, flush everything stored in the issue queue. |
| Instruction\_1\_o | Logic[31:0] | Can issue at most 4 instructions every cycle. |
| Instruction\_2\_o | Logic[31:0] |  |
| Instruction\_3\_o | Logic[31:0] |  |
| Instruction\_4\_o | Logic[31:0] |  |
| Issue\_queue\_full | Wire | When full, set this signal to high. |
| issue\_queue\_empty | Wire | When empty, set this signal to high. |
|  |  |  |