# Power Estimation and Management for MachXO2 Devices

# Technical Note

FPGA-TN-02161-1.7

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# 1. Introduction

A key requirement for many of today's high volume FPGA applications is low power consumption. The MachXO2™ PLD provides many power-saving features including Power Controller, Bank Controller and Power Guard. This technical note provides detail for using the MachXO2 low power architectural features including power supply considerations and power estimations provided by the Power Calculator tool.

# 2. Power Modes

FPGA designers often minimize power consumption by turning off subsystems while configured and operational. Design modes of operation are typically categorized into the following:

**Normal operation:**
- Device is fully operational and all circuits are active
- Highest power consumption

**Low power operation:**
- Subsystems are dynamically shut down when not required
- Average to low power consumption

**Ultra low power standby:**
- All subsystems are shut down
- Lowest power consumption provides the best option for prolonged battery life

The MachXO2 offers a flexible architecture that allows many on-chip components to be dynamically turned off during the low power operation modes. These features are listed in Table 2.1.

**Table 2.1. MachXO2 Components with Low Power Features**

| Device Component | Description |
|---|---|
| Bandgap | The Bandgap can be turned off in standby mode. When the Bandgap is turned off analog circuitry such as the PLLs, on-chip oscillator, and referenced and differential I/O buffers are also turned off. |
| Power-On-Reset (POR) | The POR can be turned off in standby mode. This circuit monitors VCC levels. In the event of unsafe VCC drops, this circuit reconfigures the MachXO2 device. When the POR circuitry is turned off, limited power detection circuitry is still active. This option is only recommended for applications in which the power supply rails are reliable. |
| On-Chip Oscillator | The on-chip oscillator has two power-saving features. It may be statically switched off when not used in a design. It can also be turned off in standby mode. |
| PLL | Similar to the on-chip oscillator, the PLL also has two power-saving features. It can be statically switched off if it is not needed in a design. It can also be turned off in standby mode. |
| I/O Bank Controller | Referenced and differential I/O buffers (used to implement standards such as HSTL, SSTL and LVDS) consume more than ratioed single-ended I/Os such as LVCMOS. The I/O bank controller allows the designer to turn these I/Os off dynamically on a per-bank basis. |
| Dynamic Clock Enable for Primary Clock Nets | Each primary clock net can be dynamically disabled to save power. |
| Power Guard | Power Guard is a feature implemented in input buffers. This feature allows designers to switch off the input buffer when it is not needed. This feature can be used in both clock and data paths. Its biggest impact is in the standby mode when it can be used to switch off clock inputs that are distrib- uted using general routing resources. |

# 3. Power Controller

The MachXO2 PLD includes a Power Controller to ensure smooth transitions into and out of standby mode. The Power Controller's two primary signals, STOP and STDBY, transitions are shown in Figure 3.1.



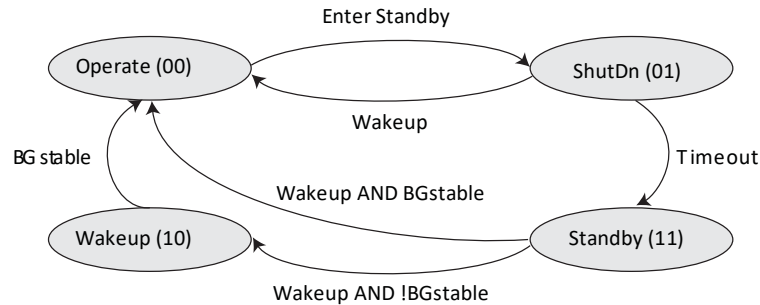**Figure 3.1. Power ControllerFigure 1 State Diagram (STDBY, STOP)**

The detailed Power Controller block diagram is shown in Figure 3.2. and its ports are defined in Table 3.1. The timeout signal is generated from an optional 8-bit Timer Counter which divides the input clock source by 28 (or 256). This injects a delay between the STOP and STDBY signals.
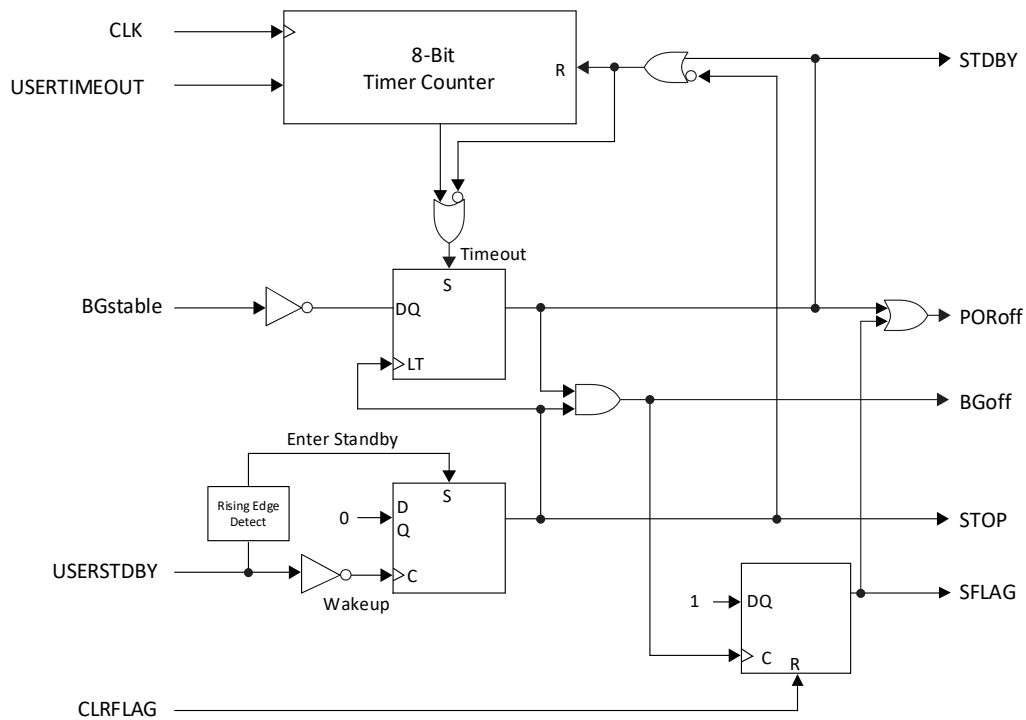


**Figure 3.2. Power Controller Block Diagram**

**Table 3.1. Power Controller Signals**

| Port | I/O | Optional | Description |
|------|-----|----------|-------------|
| CLK | Input | Yes | Clock source to the Timer Delay block. |
| USERTIMEOUT | Input | Yes | An active high enable signal for the Timer Counter block. |
| USERSTDBY | Input or Hardwired | Yes | A rising edge of this signal begins the shut-down sequence to enter standby. A falling edge of this signal begins the wake up sequence from standby. The USERSTDBY signal is from user logic or hardwire from the Configuration logic. The signals CFGSTDBY and CFGWAKE are used to provide simulation support for the Configuration I2C and SPI standby and wake commands. These ports should be connected to the matching ports on the EFB. |
| CLRFLAG | Input | Yes | Asynchronous active high reset for the standby flag. User logic should assert a high pulse on this signal once device has woken up to clear the SFLAG. |
| STOP | Output | Yes | Active high signal which is a precursor to the STDBY signal. The delay from STOP to STDBY is determined by the 8-bit Timer Counter block. The STOP signal is used to prepare logic for standby by switching off clocks, signals etc. |
| STDBY | Output | No | Active high signal through general routing to user logic, I/O pads, oscillator, and PLLs. Used to place logic in standby. |
| SFLAG | Output | Yes | This flag signal goes high to alert user logic that the device is in standby. |
| PORoff* | Hardwired | Yes | Shut-off signal to the Power Detector circuitry (POR). Power Detector circuitry is used to determine if there has been a drop in VCC. If so, the device will be reconfigured. |
| BGoff* | Hardwired | Yes | Shut-off signal to bandgap circuitry found in the MachXO2 ZE and HE versions for additional power savings. When the bandgap circuitry is turned off, POR circuitry, analog circuits (PLL, oscillator, referenced LVCMOS I/Os, SSTL I/Os, HTSTL I/Os, and differential I/Os) are turned off. |
| BGstable | Hardwired | No | The BGstable signal is a signal from the bandgap circuit. This signal will only be released after the bandgap circuitry is stable. |

**\*Note:** When POR is shuf off, limited Power Detector circuitry is still active. This option is only recommended for applications where the power supply rails are reliable. VCC must remain within the data sheet recommended range, otherwise device functionality cannot be guaranteed.

The Power Controller can be configured using IPexpress™ as shown in Figure 3.3.
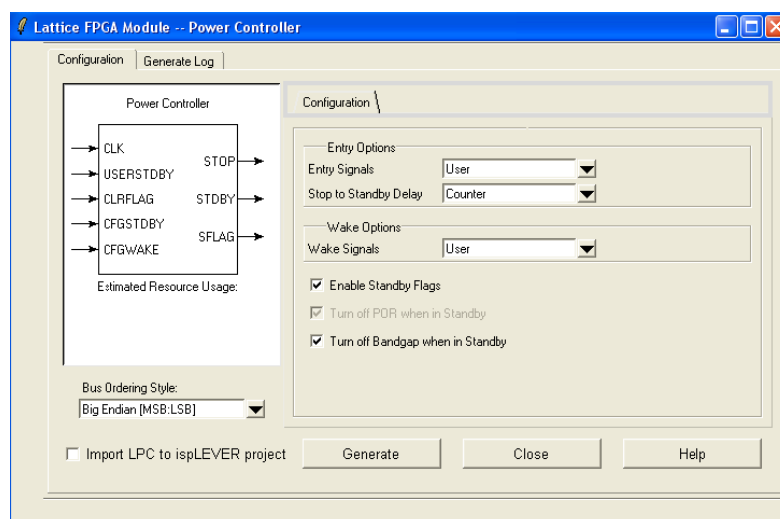


**Figure 3.3. IPexpress Power Controller**

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**Table 3.2. IPexpress Power Controller Descriptions**

| Entry | Type | Values | Default Value | Comment |
|---|---|---|---|---|
| Entry Signals | Combo Box | User, Configuration | User | Configuration includes JTAG and I$^2$C |
| Stop to Standby Delay | Combo Box | User, Counter, Bypass | Bypass | User enables the USERTIMEOUT signal for the Timer Counter. When Bypass is selected there will be no delay between the STOP and STDBY signals. |
| **Wake** | | | | |
| Wake Signals | Combo Box | User, Configuration | User | |
| **Standby** | | | | |
| Enable Standby Flags | Check Box | TRUE, FALSE | TRUE | |
| Turn off Bandgap when in Standby[1] | Check Box | TRUE, FALSE | FALSE | When the bandgap circuitry is turned off, POR circuitry, analog circuits (PLL, oscillator, refer- enced LVCMOS I/Os, SSTL I/Os, HTSTL I/Os, and differential I/Os) are turned off. |
| Turn off POR when in Standby[1] | Check Box | TRUE, FALSE | FALSE | Power Detector circuitry is used determine if there has been a drop on V$_{CC}$. If there has been, then the device will be reconfigured. |

**Note:**

1. When POR is shuf off, limited Power Detector circuitry is still active. This option is only recommended for applications where the power supply rails are reliable. VCC must remain within the data sheet recommended range, otherwise device functionality cannot be guaranteed.

The Power Controller sequence for entering and exiting standby is shown in Figure 3.4.
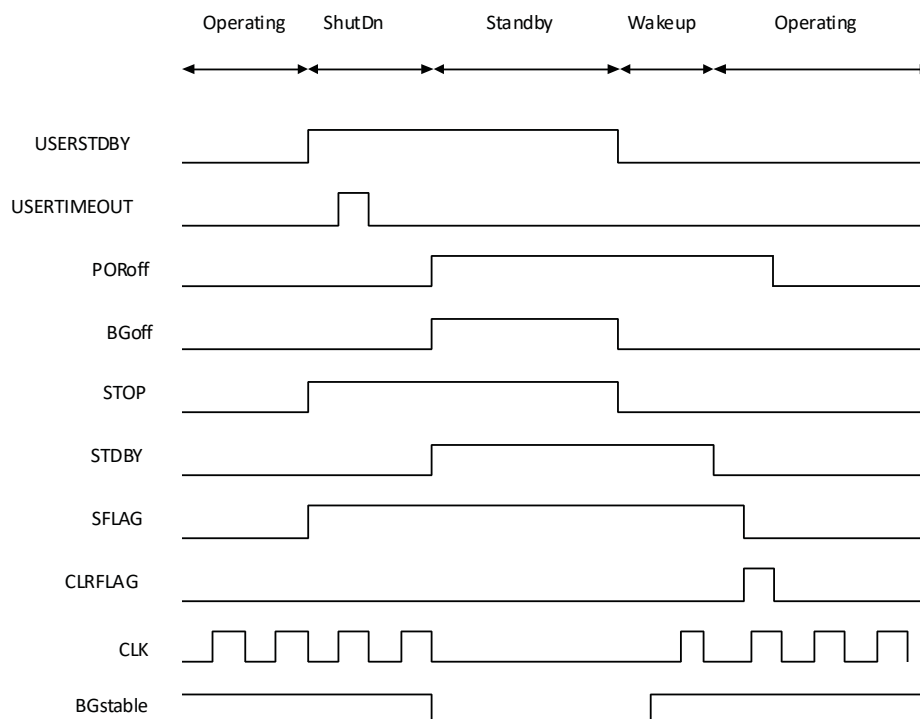


**Figure 3.4. Power Controller Waveform**

When designing with the Power Controller, users should be aware of the following:
- The software will produce an error if the Power Controller USRSTDBY signal is turned off during standby. This is to prevent a lock-up situation.
- When the Power Detector circuitry is turned off, there is still some limited circuitry within the Power Detector that is active. It is recommended to turn off the Power Detector circuitry only if the power supply rails are reliable. VCC must remain within the data sheet recommended range or functionality cannot be guaranteed.
- When the Bandgap circuitry is turned off, Power Detector circuitry, analog circuits (PLL, oscillator, referenced LVCMOS I/Os, SSTL I/Os, HTSTL I/Os, and differential I/Os) are turned off.

# 4. Bank Controller

Referenced, differential and LVDS I/O standards consume more power then other I/O standards and are not always required to be active. The active high Bank Controller allows the designer to turn these I/Os off dynamically on a per-bank selection. The Dynamic InRD (input referenced and differential I/Os) is used to turn off referenced and differential inputs. Dynamic LVDS control is used to turn off the LVDS output driver. The Bank Controller can be instantiated using the primitives shown (BCINRD for dynamic InRD, BCLVDSO for dynamic LVDS) in Figure 4.1. or using IPexpress, as shown in Figure 4.2.
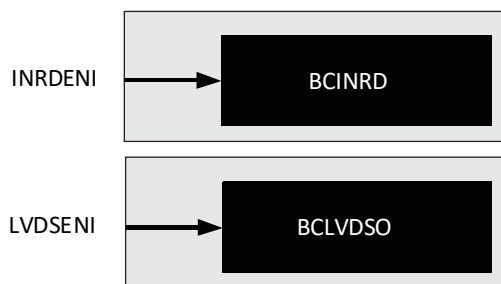


**Figure 4.1. INRDB, LVDSOB Primitive**



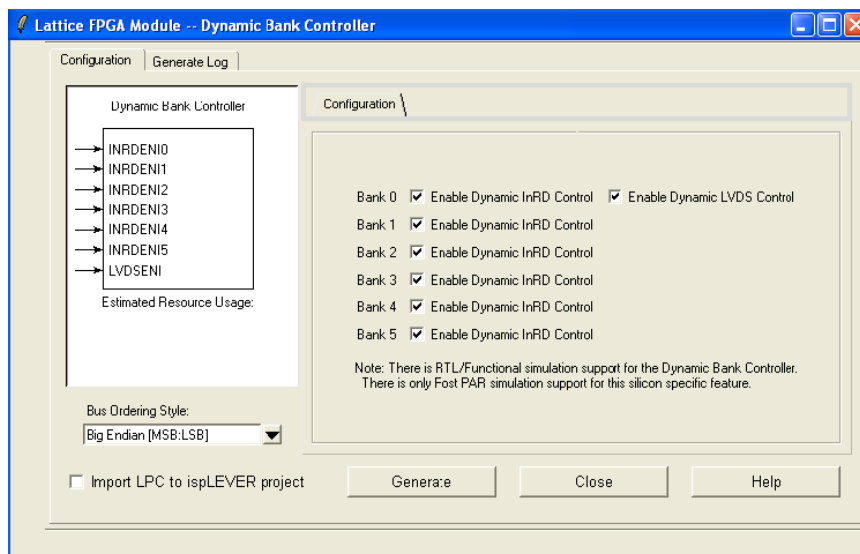**Figure 4.2. IPexpress Dynamic Bank Controller**

When designing with the Bank Controller, users should be aware of the following:
- The software will produce an error if the Bank Controller control signal is from a referenced or differential I/O in the bank which is enabled by the Bank Controller. This is in order to prevent a lock-up situation.
- Powering off the bandgap overrides the Bank Controller.

# 5.  Power Guard

The Power Guard (PG) feature minimizes dynamic power consumption on routing by gating signals at the input pin. To prevent this loss, especially on large fan-out or heavily loaded nets like clocks, inputs can be "Power Guarded". Power Guard prevents logic from getting on nets using an active high control signal. The Power Guard primitive component, as shown in Figure 5.1., can be included in your clock or data paths. For large buses, IPexpress can be used as shown in Figure 5.2.
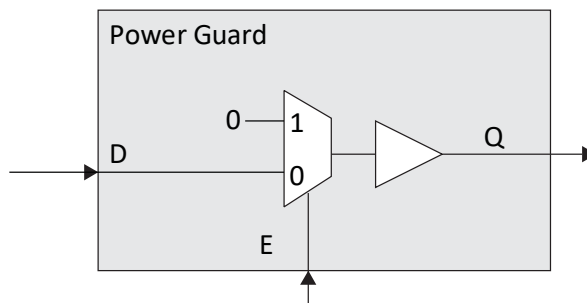


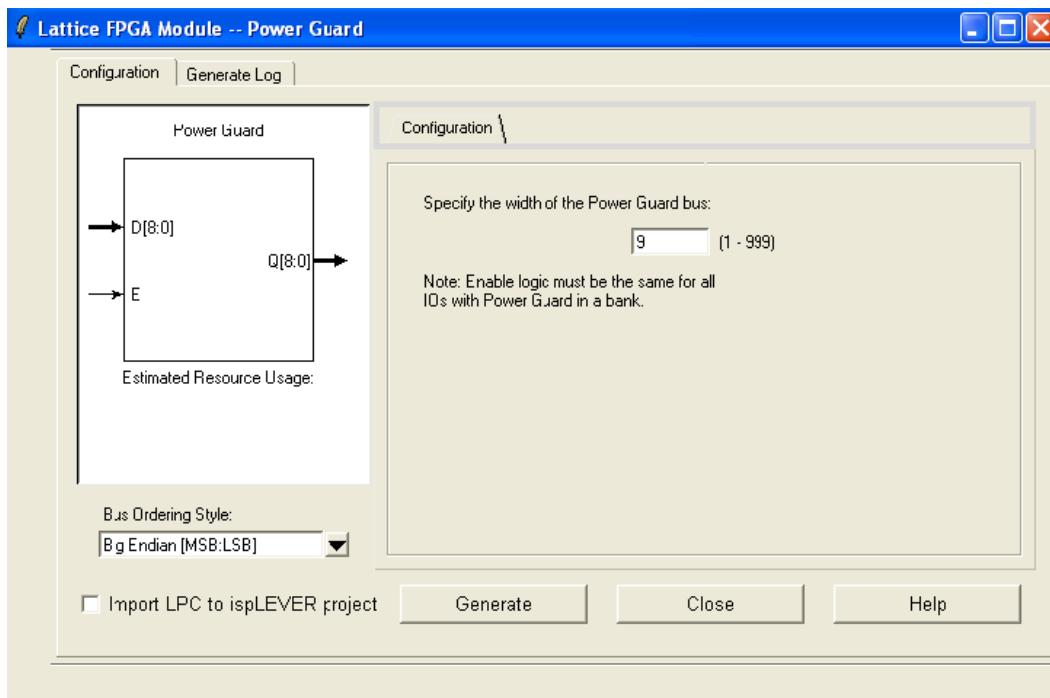**Figure 5.1. Power Guard Primitive**



**Figure 5.2. IPexpress Power Guard**

When designing with Power Guard, users should be aware of the following:
- The software will produce an error if the Power Guard control signal is from the output of the Power Guard component. This is to prevent a lock-up situation.

# 6. Low Power Design Implementation

Figure 6.1. shows an example design implementation utilizing the MachXO2 low-power architectural components.

In this design, there are four power level states:

1. Normal operation
2. Normal operation except DDR memory controller turned off
3. Preparing for standby
4. Standby

In this example design:

- White blocks are normal FPGA logic.
- Gray blocks are MachXO2 components associated with low power consumption.
- The clock CLK goes through the Power Guard component because it is a high fan-net in the design. The STDBY signal is used to block the clock signal from getting onto the routing, thus reducing dynamic power.
- The signal INRDENI is used to turn off the referenced SSTL I/Os of the DDR interface using the Bank Controller BCINRDA, reducing static and dynamic power.
- A Power State Machine is used to step through the various states of the design. The bullets below describe what happens at each state:
- Normal operation DDR Controller and I/O Expander are communicating with external memory and peripherals.
- DDR memory is not being used and the INRDENI signal is asserted high. The referenced SSTL I/Os are disabled, thereby reducing static and dynamic power.
- The device begins the low power standby sequence:
  - USERSDBY is asserted high and is used by the Power Controller to assert high STOP.
  - The DDR Controller and I/O Expander logic prepare for standby.
  - After the delay CLKX/256 from the Power Controller Timer Counter the STDBY signal is asserted high.
  - SFLAG is asserted high. Power Guard blocks the CLK signal from getting on high fan-out routing. Bank Controller turns off the referenced SSTL I/Os. DDR Controller and I/O Expander logic are in standby reaching the lowest power state.
- When in the low power standby state the device waits for the signal Wakeup before resuming normal operation.
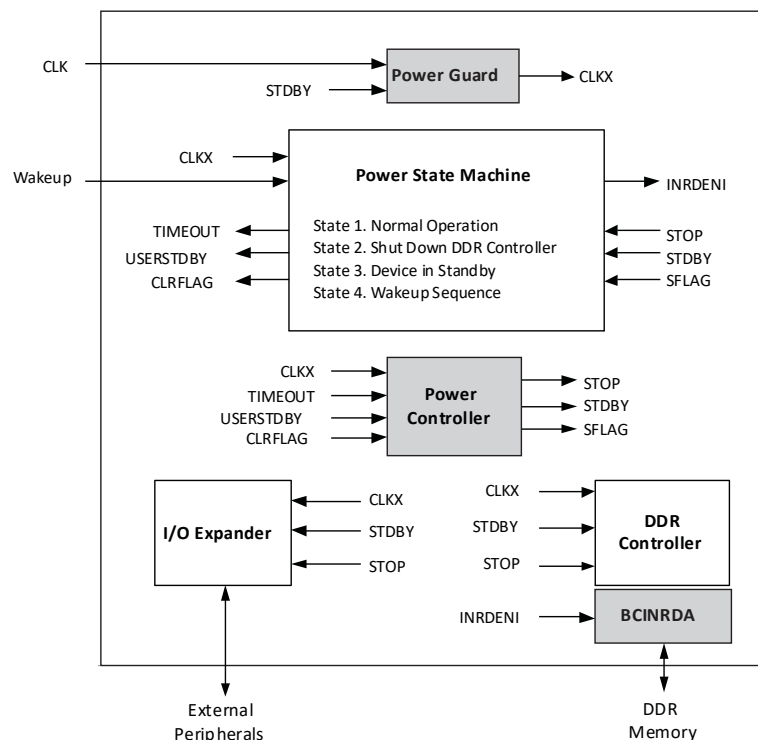
**Figure 6.1. Low Power Design Implementation**

# 7. Power Supply Sequencing and Hot Socketing

MachXO2 devices are designed to ensure predictable behavior during power-up and power-down. During powerup and power-down sequences, the I/Os remain in tri-state until the power supply voltage is high enough (VCCMIN) to ensure reliable operation. In addition, leakage into I/O pins is controlled to within the limits specified in the MachXO2 Family Data Sheet, allowing for easy integration with the rest of the system.

# 8. Recommended Power-up Sequence

Refer to the DC and Switching Characteristics section of the MachXO2 Family Data Sheet for more information on power-up sequences for the MachXO2 family.

# 9. Power Calculator

The Power Calculator is a powerful tool that allows users to estimate the power consumption of a device. This tool offers an Estimation mode for "what-if" analysis, and enables designers to import NCD design files to accurately estimate power for their designs. The background engine performs each calculation quickly and accurately.

When running the Power Calculator tool in Estimation mode, designers provide estimates of the utilization of various components and the tool provides an estimate of the power consumption. This is a good start, especially for "what-if" analysis and device selection.

Calculation mode is a more accurate approach, where the designer imports the actual device utilization by importing the post Place and Route netlist design file (or NCD file).

—

Users can also import a Trace Report (or TWR) file where the frequencies for various clocks are also imported. Note that the Trace Report only includes frequencies of the clock nets that are constrained in the Preference file.

The default Activity Factor (AF%) for dynamic power calculation is set to 10% in the Power Calculator. Users can change the default AF for the entire project or for each clock net individually. Activity Factor is discussed in more detail later in this document.

## 9.1.    Power Calculator Hardware Assumptions

The power consumption of a device can be broken down coarsely into the static (or DC) element and the dynamic (or AC) element. These elements have the following dependencies with respect to the junction temperature ($T_J$) of the die.
- Static power is a result of the leakage associated with the transistors. There are two types of static leakage.
    - Static leakage which has a strong temperature dependency
    - DC bias which is fairly constant across temperature
- Dynamic power is caused by the toggling of signals in the transistor.
    - Dynamic power is fairly constant across temperature

Each component of the device (e.g., LUT, register, EBR, I/O etc.) has its own coefficients for static and dynamic power. Certain selections in the Power Calculator tool affect some of these coefficients as discussed in the next section.

## 9.2.    Power Calculator and Power Equations

Please refer to the ispLEVER Tutorial for launching and using the Power Calculator tool under **Help > ispLEVER Help**.

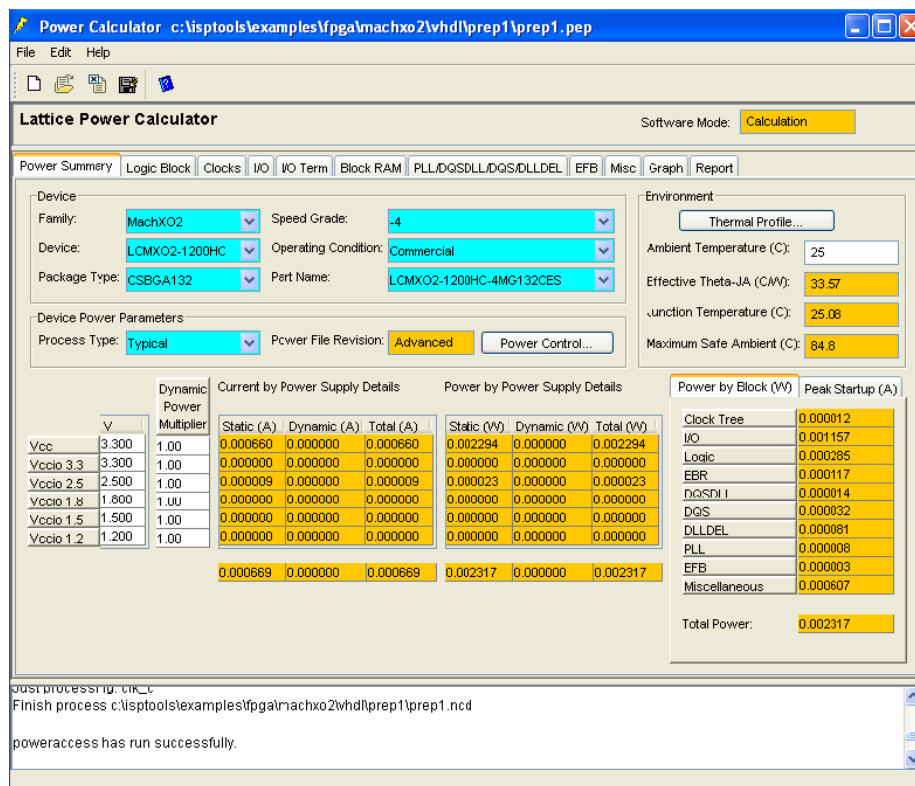Once you step through the procedure, you will see the window illustrated in Figure 9.1.



**Figure 9.1. Power Calculator Main Window**

It is important to understand how the options available with the Power Calculator affect the power consumption of a device. For example, if the ambient temperature is changed, it affects the junction temperature, according to the following equation:

$$T_J = T_A + \Theta_{JA\_EFFECTIVE} * P$$

Where $T_J$ and $T_A$ are the junction and ambient temperatures, respectively, and P is the power.

$\Theta_{JA\_EFFECTIVE}$ is the effective thermal impedance between the die and its environment.

The junction temperature is directly proportional to the ambient temperature. An increase in $T_A$ will increase $T_J$ and result in an increase of the static leakage component.

Selecting the Process Type again affects the static leakage; in particular the static leakage coefficient changes.

The DC Bias component is constant across the range.

For dynamic power, increasing the frequency of toggling will increase the dynamic component of power.

### 9.2.1. Typical and Worst Case Process Power/I$_{CC}$

Another factor that affects DC power is process variation. This variation, in turn, causes variation in quiescent power.

Power Calculator takes these factors into account and allows designers to specify either a typical process or a worst case process.

## 9.3. Junction Temperature

Junction temperature is the temperature of the die during operation. It is one of the most important factors that affect the device power. For a fixed junction temperature, voltage and device package combination, quiescent power is fixed.

Ambient temperature affects the junction temperature as shown in Equation 1. Devices operating in a high-temperature environment have higher leakage since their junction temperature will be higher. Power Calculator models this ambient-to-junction temperature dependency. When the user provides an ambient temperature, it is rolled into an algorithm that calculates the junction temperature and power through an iterative process to find the thermal equilibrium of the system (device running with the design) with respect to its environment ($T_A$, airflow etc.).

## 9.4. Maximum Safe Ambient Temperature

Maximum Safe Ambient Temperature is one of the most important numbers displayed in the Summary tab of the Power Calculator. This is the maximum ambient temperature at which the design can run without violating the junction temperature limits for commercial or industrial devices.

Power Calculator uses an algorithm to accurately predict this temperature. The algorithm adjusts itself as the user changes options such as voltage, process, frequency, AF% etc. (or any factor that may affect the power dissipation of the device).

## 9.5. Operating Temperature Range

When designing a system, users must make sure that a device operates at specified temperatures within the system environment. This is particularly important to consider before a system is designed. With Power Calculator, users can predict device thermodynamics and estimate the dynamic power budget. The ability to estimate a device's operating temperature prior to board design also allows the designer to better plan for power budgeting and airflow.

Although total power, ambient temperature, thermal resistance and airflow all contribute to device thermodynamics, the junction temperature (as specified in the MachXO2 Family Data Sheet) is the key to device operation. The allowed junction temperature range is 0 °C to 85 °C for commercial grade devices and –40 °C to 100 °C for industrial grade devices. If the junction temperature of the die is not within these temperature ranges, the performance and reliability of the device's functionality cannot be guaranteed.

## 9.6. Dynamic Power Multiplier (DPM)

The user-defined frequency of operation makes this problem even more complex. To help resolve this issue, the Dynamic Power Multiplier provides some guard bands for system and board designers.

The Dynamic Power Multiplier is defaulted to "1" which means the dynamic power is what it is. If the user wishes to add 20% additional dynamic power, the DPM can be set to 1.2 (1 + 20%) and it can be placed against the appropriate power supply. This increases the dynamic power for that supply by 20% and provides designers with some guard band (if needed).

## 9.7. Power Budgeting

The Power Calculator provides the power dissipation of a design under a given set of conditions. It also predicts the junction temperature (TJ) for the design. If the junction temperature is outside the limits specified in the MachXO2 Family Data Sheet, the viability of operating the device at this junction temperature must be re-evaluated.

A commercial grade device is likely to show speed degradation with a junction temperature above 85 °C and an industrial grade device at a junction temperature will degrade above 100 °C. It is required that the die temperature be kept below these limits to achieve the guaranteed speed operation.

Operating a device at a higher temperature also means a higher Static $I_{CC}$. The difference between the Total $I_{CC}$ and the Static $I_{CC}$ (both Static $I_{CC}$ and Dynamic $I_{CC}$) at a given temperature provides the Dynamic Icc budget available. If the device runs at a Dynamic $I_{CC}$ higher than this budget, the total $I_{CC}$ is also higher. This causes the die temperature to rise above the specified operating conditions.

The four factors of power, ambient temperature, thermal resistance and airflow, can also be varied and controlled to reduce the junction temperature of the device. The Power Calculator is a powerful tool to help system designers to properly budget the FPGA power that, in turn, helps improve the overall system reliability.

## 9.8. Dynamic Power Savings

The Power Calculator dynamically estimates the power when the Power Controller, Bank Controller and Power Guard are implemented in a design by simply enabling or disabling the components.
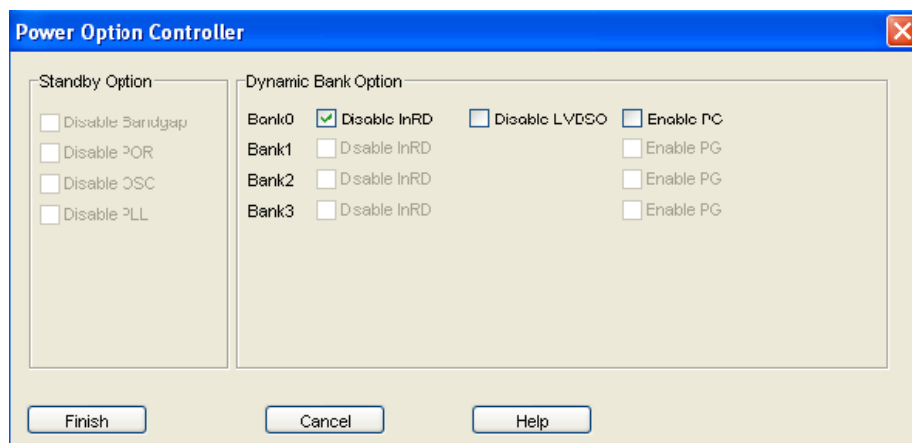


**Figure 9.2. Dynamic Power Options**

## 9.9. Activity Factor Calculation

The Activity Factor % (or AF%) is defined as the percentage of frequency (or time) that a signal is active or toggling the output. Most resources associated with a clock domain are running or toggling at some percentage of the frequency at which the clock is running. Users must provide this value as a percentage under the AF% column in the Power Calculator tool.

Another term for I/Os is the I/O Toggle Rate. The AF% is applicable to the PFU, Routing, and Memory Read Write Ports, etc. The activity of I/Os is determined by the signals provided by the user (in the case of inputs) or as an output of the design (in the case of outputs). The rates at which the I/Os toggle define their activity. The I/O Toggle Rate or the I/O Toggle Frequency is a better measure of their activity.

The Toggle Rate (or TR) in MHz of the output is defined in the following equation:

$$\text{Toggle Rate (MHz)} = 1/2 * f * AF\%$$

Users are required to provide the TR (MHz) value for the I/O instead of providing the frequency and AF% for other resources. AF can be calculated for each routing resource, output or PFU. However, this involves long calculations. The general recommendation for a design occupying roughly 30% to 70% of the device is an AF% between 15% and 25%. This is an average value. The accurate value of an AF depends upon clock frequency, stimulus to the design and the final output.

## 9.10. Thermal Impedance and Airflow

A common method for characterizing a packaged device's thermal performance is with Thermal Resistance, T. For a semiconductor device, thermal resistance indicates the steady state temperature rise of the die junction above a given reference for each watt of power (heat) dissipated at the die surface. Its units are °C/W.

The most common examples are $\Theta_{JA}$, Thermal Resistance Junction-to-Ambient (in °C/W) and $\Theta_{JC}$, Thermal Resistance Junction-to-Case (also in °C/W). Another factor is $\Theta_{JB}$, Thermal Resistance Junction-to-Board (in °C/W).

Knowing the reference (i.e. ambient, case, or board) temperature, the power, and the relevant T value, the junction temperature can be calculated per the following equations.

$$T_J = T_A + \Theta_{JA} * P$$
$$T_J = T_C + \Theta_{JC} * P$$
$$T_J = T_B + \Theta_{JB} * P$$

Where $T_J$, $T_A$, $T_C$ and $T_B$ are the junction, ambient, case (or package) and board temperatures (in °C), respectively. P is the total power dissipation of the device.

$\Theta_{JA}$ is commonly used with natural and forced convection air-cooled systems. $\Theta_{JC}$ is useful when the package has a high conductivity case mounted directly to a PCB or heatsink. And $\Theta_{JB}$ applies when the board temperature adjacent to the package is known.

Power Calculator utilizes the ambient temperature (°C) to calculate the junction temperature (°C) based on the $\Theta_{JA}$ for the targeted device. Users can also provide the airflow values (in LFM) to obtain a more accurate junction temperature value.

To improve airflow effectiveness, it is important to maximize the amount of air that flows over the device or the surface area of the heat sink. The airflow around the device can be increased by providing an additional fan or increasing the output of the existing fan. If this is not possible, baffling the airflow to direct it across the device may help. This means the addition of sheet metal or objects to provide the mechanical airflow guides to guide air to the target device. Often the addition of simple baffles can eliminate the need for an extra fan. In addition, the order in which air passes over devices can impact the amount of heat dissipated.

## 9.11. Reducing Power Consumption

One of the most critical challenges for designers today is reducing the system power consumption. A low-order reduction in power consumption goes a long way, especially in modern hand-held devices and electronics. There are several design techniques that can be used to significantly reduce overall system power consumption. Some of these include:

- Using the MachXO2 power saving architecture features like Power Controller, Bank Controller and Power Guard.
- Reducing operating voltage while staying within data sheet limits.
- Operating within the specified package temperature limitations.
- PLL jitter/power option within IPexpress
- Confirm if input-only bank saves power
- Using optimum clock frequency reduces power consumption, as the dynamic power is directly proportional to the frequency of operation. Designers must determine if some portions of the design can be clocked at a lower rate that will reduce power.
- Reducing the span of the design across the device. A more closely-placed design uses fewer routing resources and therefore less power.
- Reducing the voltage swing of the I/Os where possible.
- Ensuring input logic levels are not left floating but pulled either up or down.
- Ensuring no I/O pull-up/down conflicts with other components on the board.
- Using optimum encoding where possible. For example, a 16-bit binary counter has, on average, only 12% activity factor and a 7-bit binary counter has an average of 28% activity factor. On the other hand, a 7-bit LFSR counter will toggle at an activity factor of 50%, which causes higher power consumption. A gray code counter, where only one bit changes at each clock edge, will use the least amount of power, as the activity factor is less than 10%.
- Minimizing the operating temperature by the following methods:
  - Use packages that can better dissipate heat, such as ceramic packages.
  - Place heat sinks and thermal planes around the device on the PCB.
  - Use better airflow techniques, such as mechanical airflow guides and fans (both system fans and device mounted fans).
- To achieve the lowest standby power:
  - All clocks and combinatorial logic should be held at a steady state
  - All inputs should be held at a rail; if not possible, toggling inputs should gated using Power Guard
  - All outputs should be tri-stated and the Bank Controller should turn off referenced and LVDS outputs
  - Internal oscillator should be turned off using the STDBY port
  - PLLs should be turned off using the STDBY port
  - Bandgap and POR should be turned off using the Power Controller

## 9.12. Power Calculator Assumptions

The following are the assumptions made by the Power Calculator.

- The Power Calculator tool uses equations with constants based on a room temperature of 25 °C. The default temperature of 25 °C can be changed.
- Users can define the ambient temperature ($T_A$) for device junction temperature ($T_J$) calculation based on the power estimation. $T_J$ is calculated from the user-entered $T_A$ and the power calculation of typical room temperature.
- I/O power consumption is based on an output loading of 5 pF. Designers have the ability to change this capacitive loading.
- Users can estimate power dissipation and current for each type of power supply ($V_{CC}$, $V_{CCIO}$).
- The nominal $V_{CC}$ is used by default to calculate power consumption. A lower or higher $V_{CC}$ can be chosen from a list of available values.
- $\Theta_{JA}$ can be changed to better estimate the operating system manually or by entering Airflow in Linear Feet per Minute (LFM) along with a Heat Sink options.
- The default value of the I/O types for MachXO2 devices is LVCMOS25, 8 mA.

- The activity factor (AF) is defined as the toggle rate of the registered output. For example, assuming that the input of a flip-flop is changing at every clock cycle, 100% AF of a flip-flop running at 100 MHz is 50 MHz. The default activity factor for logic is 10%.

# References

- [MachXO2](#) web page
- [Lattice Insights](#) web page for Lattice Semiconductor training courses and learning plans

# Technical Support Assistance

Submit a technical support case through www.latticesemi.com/techsupport.

For frequently asked questions, refer to the Lattice Answer Database at
https://www.latticesemi.com/Support/AnswerDatabase.

# Revision History

**Revision 1.7, May 2024**

| Section | Change Summary |
|---|---|
| Disclaimers | Updated this section. |
| Power Controller | Updated Figure 3.2. Power Controller Block Diagram to add Rising Edge Detect block. |
| References | Added this section. |
| Technical Support Assistance | Added information about *Lattice Answer Database.* |

**Revision 1.6, November 2019**

| Section | Change Summary |
|---|---|
| All | • Changed document number from TN1198 to FPGA-TN-02161.<br>• Updated document template. |
| Disclaimers | Added this section. |

**Revision 1.5, June 2015**

| Section | Change Summary |
|---|---|
| Power Controller | Updated this section. Fixed CLRFLAG port input in Figure 3.2., Power Controller Block Diagram. |
| Operating Temperature Range | Updated this section. Changed allowed junction temperature range for industrial grade devices. |
| Technical Support Assistance | Updated this section. |

**Revision 1.4, December 2012**

| Section | Change Summary |
|---|---|
| Power Controller | Corrected formatting in the description of the Power Controller block diagram. |

**Revision 1.3, October 2012**

| Section | Change Summary |
|---|---|
| Power Controller | IPexpress Power Controller Descriptions table – updated Values and Default Values columns for the Entry Signals and Wake Signals. |

**Revision 1.2, February 2012**

| Section | Change Summary |
|---|---|
| All | • Updated document with new corporate logo<br>• Document status changed from Advance to Final. |

**Revision 1.1 April 2011**

| Section | Change Summary |
|---|---|
| Power Calculator | Updated Reducing Power Consumption list. |

**Revision 1.0 November 2010**

| Section | Change Summary |
|---|---|
| All | Initial release. |