

MachX02 Development Board

Variant: Evaluation

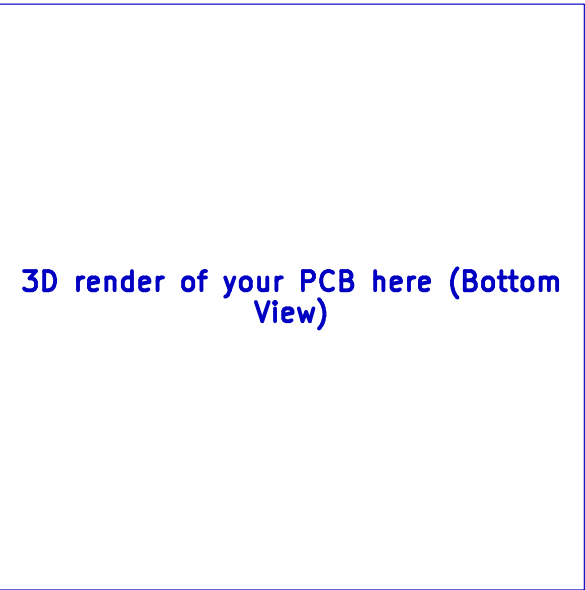
2025-05-23
Rev 1.0

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TOP VIEW



BOTTOM VIEW



NOTES

Add a comment here

Not fitted components are marked as **X**

DRAFT - Very early stage of schematic, ignore details.
PRELIMINARY - Close to final schematic.
CHECKED - There shouldn't be any mistakes. Contact the engineer if you find any.
RELEASED - A board with this schematic has been sent to production.

Evaluation 2025-06

DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

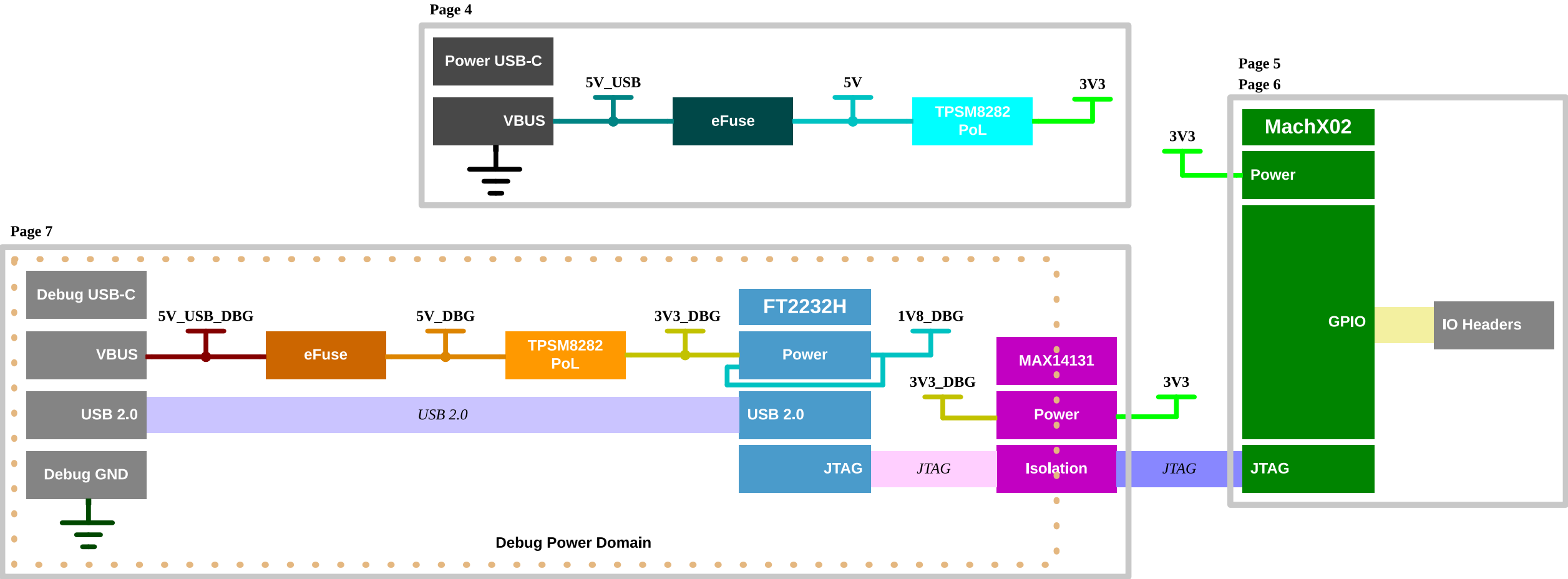
DESIGN NOTE:
Example text for debug notes.

DESIGN NOTE:
Example text for cautionary design notes.

DESIGN NOTE:
Example text for critical design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

[2] Block Diagram



| Target specifications: | |
|------------------------|-----------|
| Input voltage: | 4 - 5.5 V |
| 5V | 5V, 3A |
| 3V3 | 3.3V, 1A |
| IO Level | 3.3V |

| | | |
|---|--------------------------|----------|
| Lucas Wilch | | |
| Sheet: /Block Diagram/ File: Block Diagram.kicad_sch | | |
| Title: Block Diagram | | |
| Size: A3 | Date: Last Modified Date | Rev: 1.0 |
| KiCad E.D.A. 9.0.2 | | Id: 2/10 |

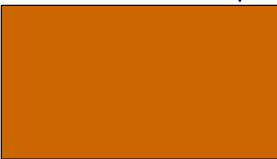
[3] Project Architecture

USB Power & PoL



File: USB Power & PoL.kicad_sch

FPGA Power & Decoupling



File: FPGA Power & Decoupling.kicad_sch

Debug



File: Debug.kicad_sch

FPGA IO

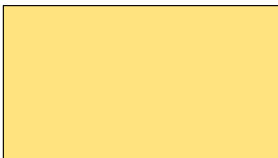


File: FPGA IO.kicad_sch

FTDI2232H USB-JTAG

Lattice MachX02 FPGA

Section Seed - Title Seed



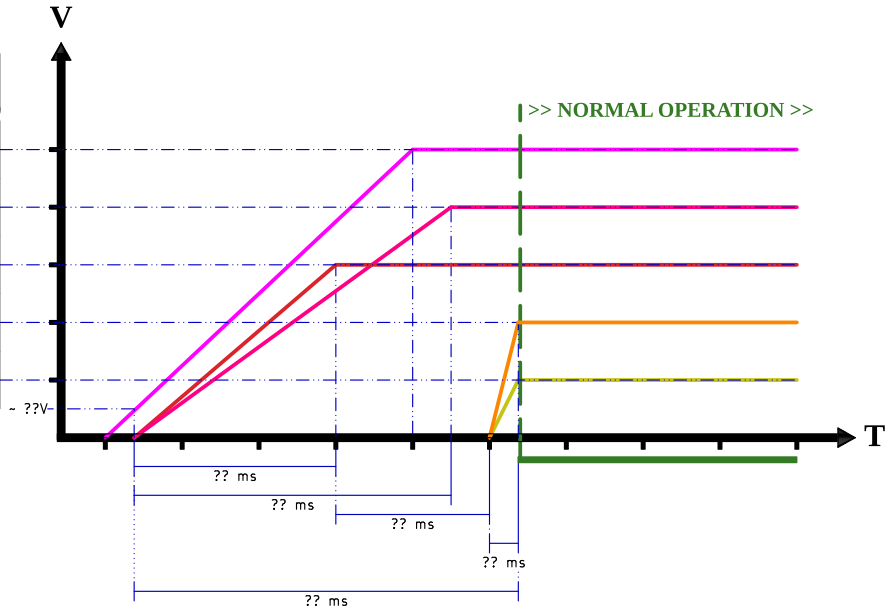
File: Section Seed - Title Seed.kicad_sch

Example

| | | |
|---|--------------------------|----------|
| Lucas Wilch | | |
| Sheet: /Project Architecture/ File: Project Architecture.kicad_sch | | |
| Title: Project Architecture | | |
| Size: A3 | Date: Last Modified Date | Rev: 1.0 |
| KiCad E.D.A. 9.0.2 | Id: 3/10 | |

[8] Power - Sequencing

| NAME | SOURCE | LEVEL |
|------|-------------|-----------|
| +??V | SOURCE NAME | ??V ± ??% |
| +??V | SOURCE NAME | ??V ± ??% |
| +??V | SOURCE NAME | ??V ± ??% |
| +??V | SOURCE NAME | ??V ± ??% |
| +??V | SOURCE NAME | ??V ± ??% |



[9] Revision History

DD.MM.YYYY - xxx Revision
Variant: xxx

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Lucas Wilch

Sheet: /Revision History/
File: Revision History.kicad_sch

Title: Revision History

Size: A4

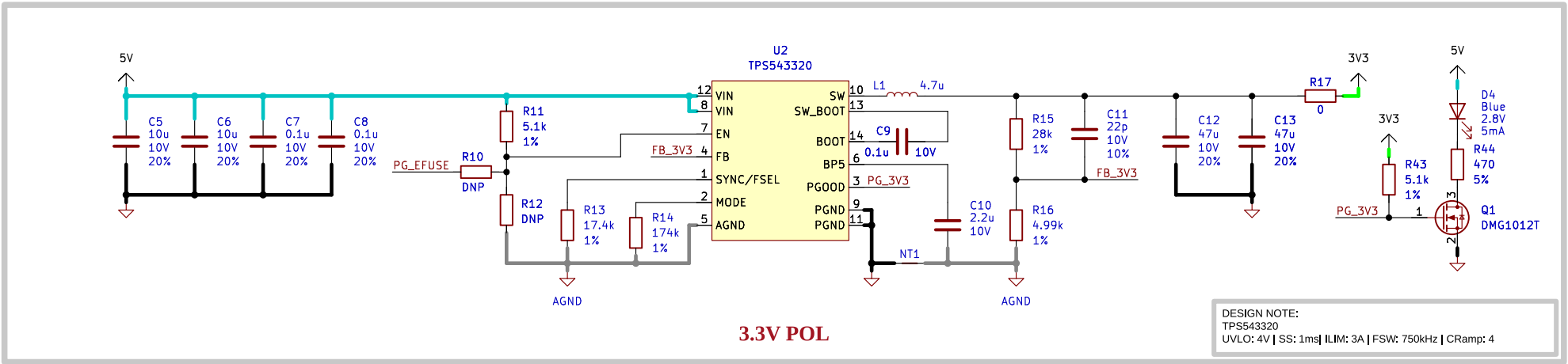
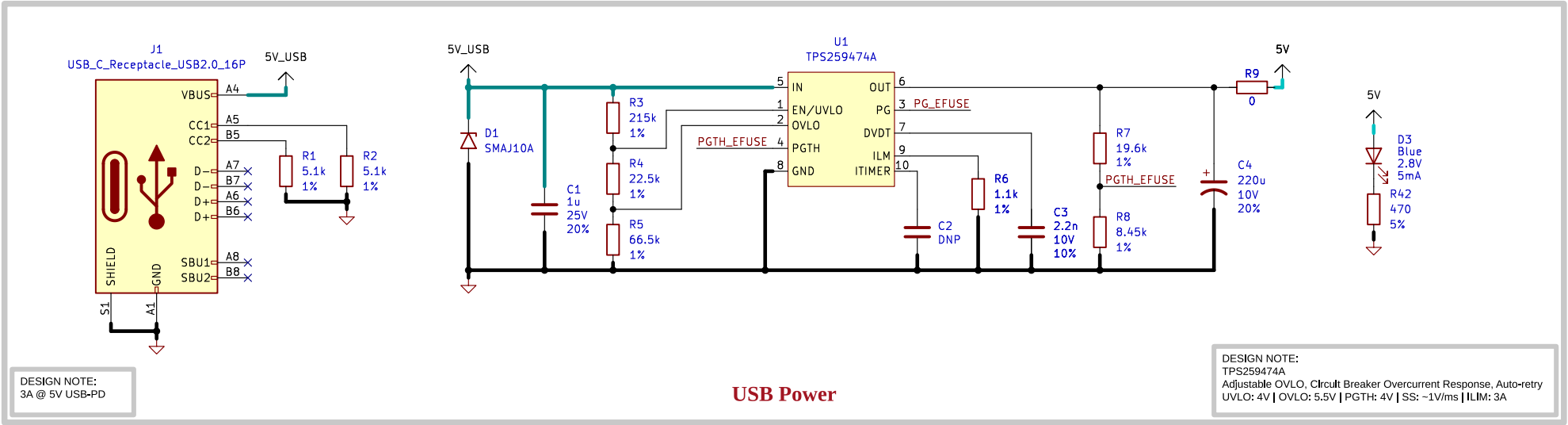
Date: Last Modified Date

Rev: 1.0

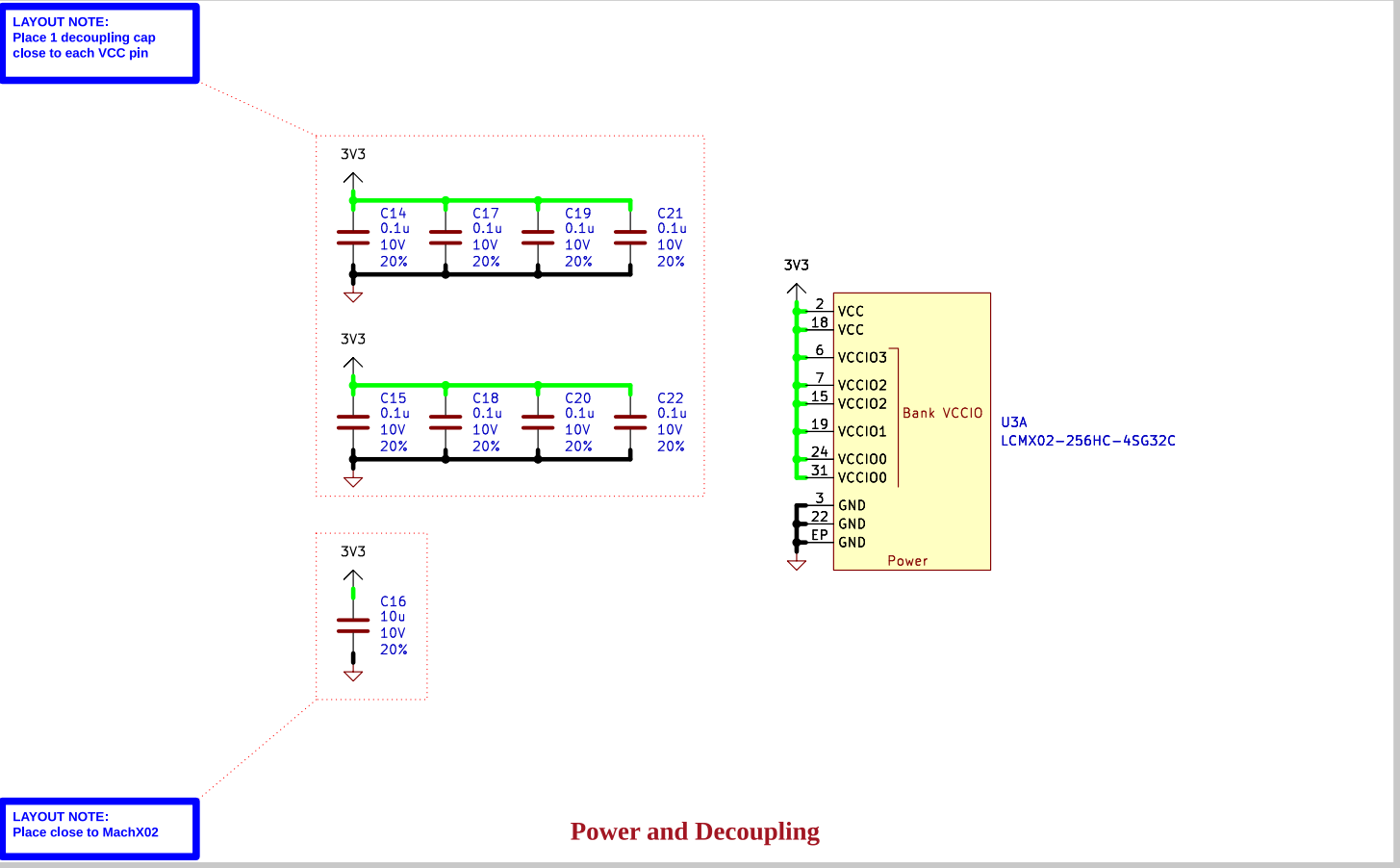
KiCad E.D.A. 9.0.2

Id: 9/10

[4] USB Power & PoL

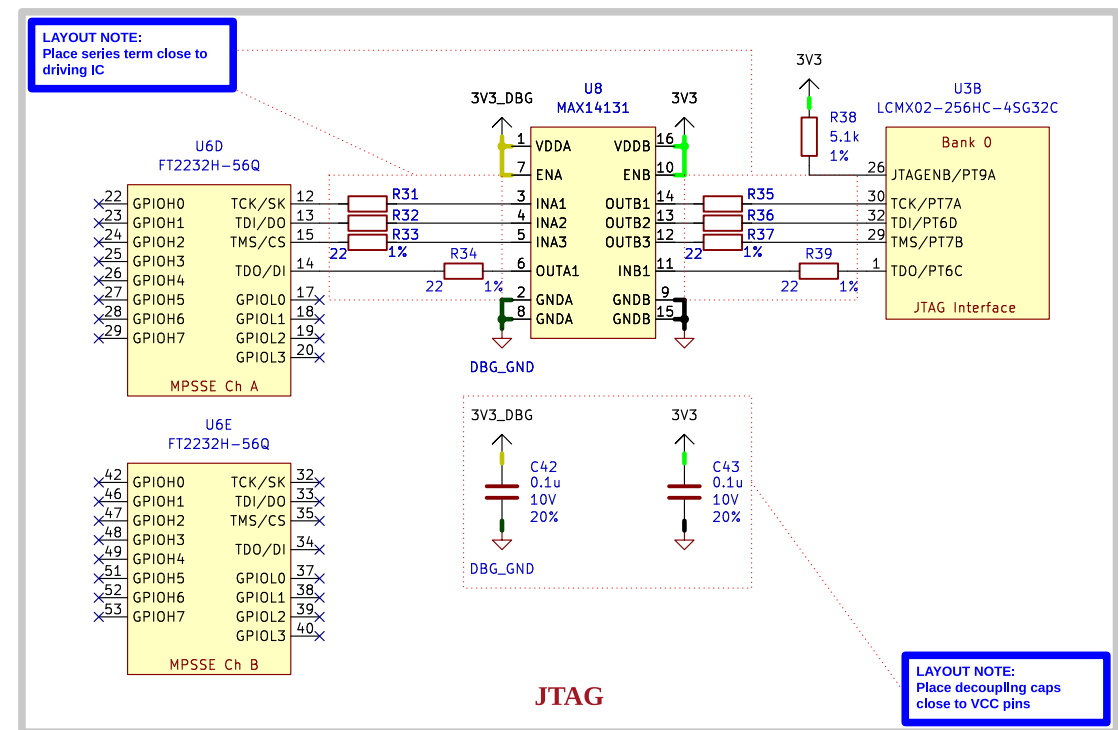
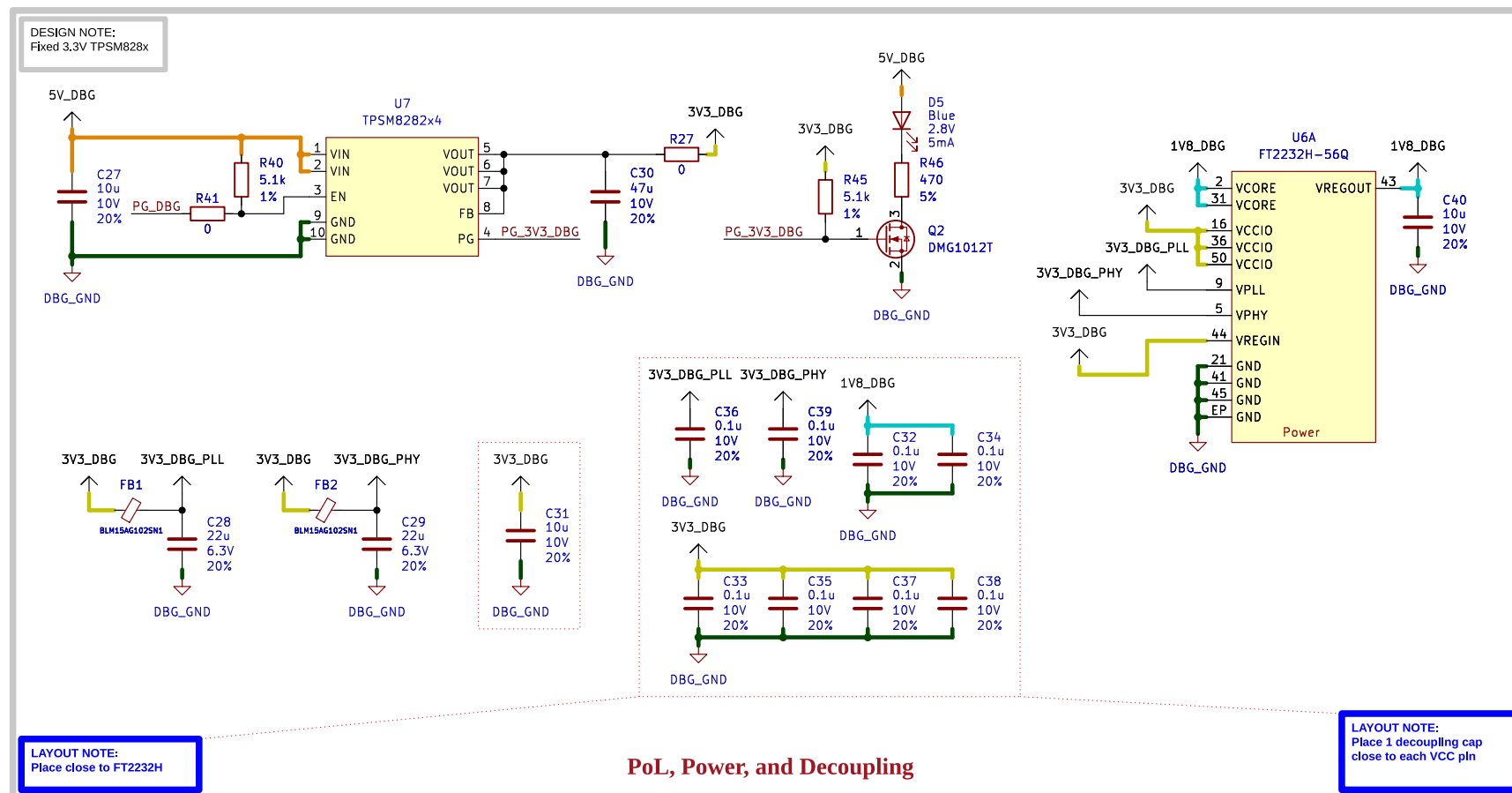
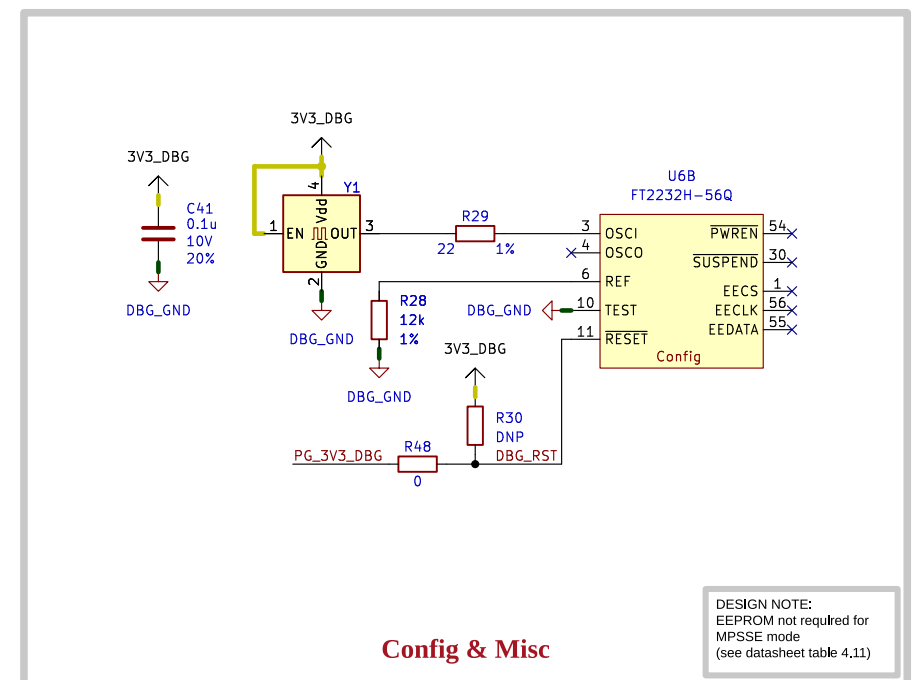
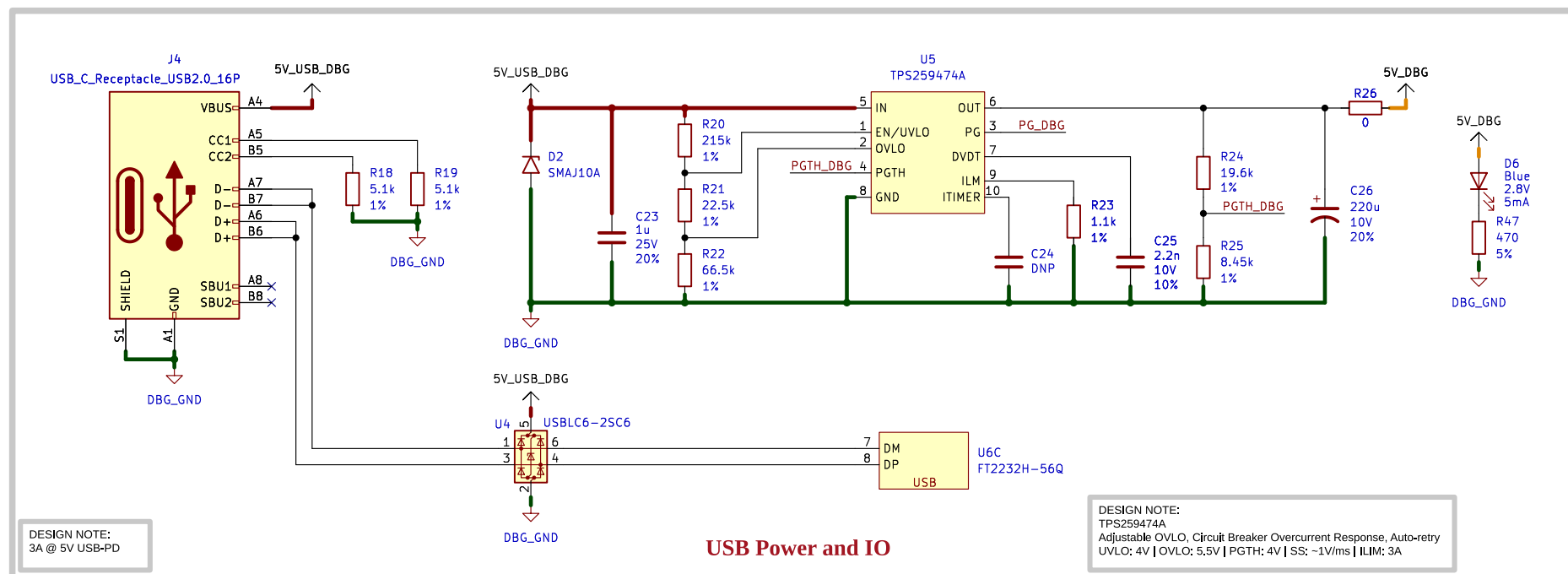


[5] FPGA Power & Decoupling



[illegible]

[7] Debug



The diagram shows a schematic layout on a grid. At the top center is a large title block: **[99] Section Seed - Title Seed**. The layout consists of several rectangular blocks, each labeled **Block Description** in dark red text. These blocks are arranged in a grid-like fashion. On the left side, there is a cluster of four notes: a yellow-bordered note with the text **DESIGN NOTE: blabla**, and three smaller notes below it (gray, orange, and blue borders) with the text **DESIGN NOTE: blabla**, **DESIGN NOTE: blabla**, and **LAYOUT NOTE: blabla** respectively. A red dotted line connects the yellow note to a small red dotted rectangle. At the bottom right, there is a **References:** section with three entries: **Flexible I/O worked examples** and **Flexible I/O source configuration**. Below the references is a metadata table with the following content:

| | | |
|---|--------------------------|-----------|
| Lucas Wilch | | |
| Sheet: /Project Architecture/Section Seed - Title Seed/ | | |
| File: Section Seed - Title Seed.kicad_sch | | |
| Title: Sheet Title B | | |
| Size: A3 | Date: Last Modified Date | Rev: 1.0 |
| KiCad E.D.A. 9.0.2 | | Id: 99/10 |