ECE 571 Final Project

Verification and Emulation of MIPS 16

*It's clear to most intellectual property (IP) creators and users today that functional verification is one of the biggest problems facing the industry. As design complexity increases, the verification effort often over shadows the design effort. Most will agree that there is no single methodology or tool that solves what many are dubbing the "verification crisis." Thus an approach of multiple methodologies is required to tackle the problem from as many angles as possible."****As our final project we will be verifying a 5-stage pipeline CPU, A MIPS16 CPU".***

Good Design: https://github.com/ECE571-winter2019/mips_16.git

Phase 1: Verification Plan Draft

- Understand the MIPS ISA, Writing Test cases, Assemble the code.
- Understand Core and co-relate with Instruction Set Architecture.
- Run the test cases on MIPS CPU.
- Write Simple Assertions to Check the Functionality of the core.
- Log the values to a file at each stage to use for unit testing

Phase 2: Final Verification Plan

- Unit Test the stages using the logged files. Multiple TB's for each stage.
- Assertions need to be in a different file and will be bind later in the top.

Phase 3: Test and Release

- Release of Broken core, find the bugs.
  - In the demo you might be asked to explain how did the assertion got the bug
- Emulation in Standalone mode with the clean design.