CELLULAR

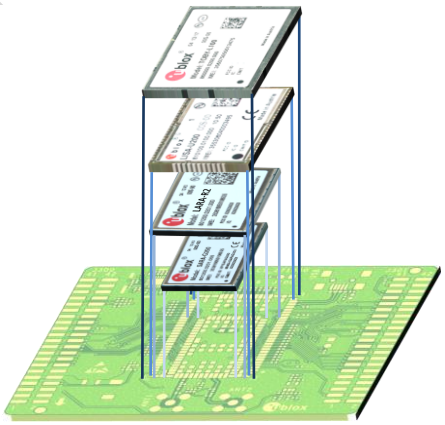
Nested Design

Reference Design for TOBY / LISA / SARA / LARA modules

Application Note

Abstract

This document describes the nested design for TOBY, LISA, SARA, and LARA cellular modules. This reference design is intended to be used as a template to assist in making application-specific products. Reference designs, including example schematics, Bill of Materials, and routing suggestions, are available to u-blox customers.



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Document Information		
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Document status explanation	
Objective Specification	Document contains target values. Revised and supplementary data will be published later.
Advance Information	Document contains data based on early testing. Revised and supplementary data will be published later.
Early Production Information	Document contains data from product verification. Revised and supplementary data may be published later.
Production Information	Document contains the final product specification.

This document applies to the following products:

Product name
TOBY-L1 series
TOBY-L2 series
TOBY-R2 series
LISA-U2 series
SARA-G3 series
SARA-U2 series
LARA-R2 series

Contents

1 Introduction

u-blox uses the term "nested design" to describe application boards on which modules of different form factors can be mounted in the same space. This document provides HW guidelines for mounting a TOBY, LISA, SARA, or LARA form factor module on the same space of a nested application board, and describes the u-blox reference design as a nested printed circuit board design for the TOBY, LISA, SARA, and LARA cellular modules.

Detailed firmware topics are not considered in this document, but TOBY, LISA, SARA, and LARA modules share most of the AT commands (for all the complete description details and differences, see the u-blox AT Commands Manual [15] or TOBY-L1 / MPCI-L1 Series AT Commands Manual [14]).

In this document, unless otherwise indicated:

- TOBY refers to TOBY-L1 series, TOBY-L2 series and TOBY-R2 series cellular modules
- LISA refers to LISA-U2 series cellular modules
- SARA refers to SARA-G3 series and SARA-U2 series cellular modules
- LARA refers to LARA-R2 series cellular modules

LISA-U1 and LISA-C2 series modules are not included as mounting options on the u-blox nested reference design in this document, because an external audio circuit for the analog audio interface of LISA-U1 and LISA-C2 modules is not implemented on this printed circuit board. However, the modules can be mounted on the reference design described here thanks to layout and pin compatibility with LISA-U2 series modules.

The following symbols are used to highlight important information within the document:

☞ An index finger points out key information pertaining to module integration and performance.

⚠ **A warning symbol indicates actions that could negatively impact or damage the module.**

This application note explains the points to consider when developing a nested application board for TOBY, LISA, SARA, or LARA modules. For further details regarding the characteristics, usage or settings of each product version of TOBY, LISA, SARA, and LARA modules, see:

- Data Sheets: TOBY-L1 [1], TOBY-L2 [2], TOBY-R2 [3], LISA-U2 [4], SARA-G3 [5], SARA-U2 [6], LARA-R2 [7]
- System Integration Manuals: TOBY-L1 [8], TOBY-L2 [9], TOBY-R2 [10], LISA-U2 [11], SARA-G3 / SARA-U2 [12], LARA-R2 [13]
- AT Commands Manuals: TOBY-L1 [14], TOBY-L2 / TOBY-R2 / LISA-U2 / SARA-G3 / SARA-U2 / LARA-R2 [15]
- the modules' pin comparisons in Table 2

2 Nested design description

2.1 Nested design concept

Migrating between TOBY, LISA, SARA, and LARA module designs is a straightforward procedure that allows customers to take maximum advantage of their hardware and software investments.

u-blox adheres to a core "nested design" philosophy. Although TOBY modules (35.6 x 24.8 mm, 152-pin LGA), LISA modules (33.2 x 22.4 mm, 76-pin LCC), SARA modules (26.0 x 16.0 mm, 96-pin LGA), and LARA modules (26.0 x 24.0 mm, 100-pin LGA) each have different form factors, the footprints for the TOBY, LISA, SARA, and LARA modules have been developed to ensure layout compatibility. This is preferred to pin compatibility, which requires every module to share the largest, most expensive package.

With the "nested design" solution, any TOBY, LISA, SARA, or LARA module can be alternatively mounted on the same nested PCB as shown in Figure 1. The eleven pins of the modules along the side where the RF pins are located (the white pins on the lower edges in Figure 1) share the same eleven pads on the nested PCB. These pins have the same pitch and nearly the same functions due to layout compatibility.

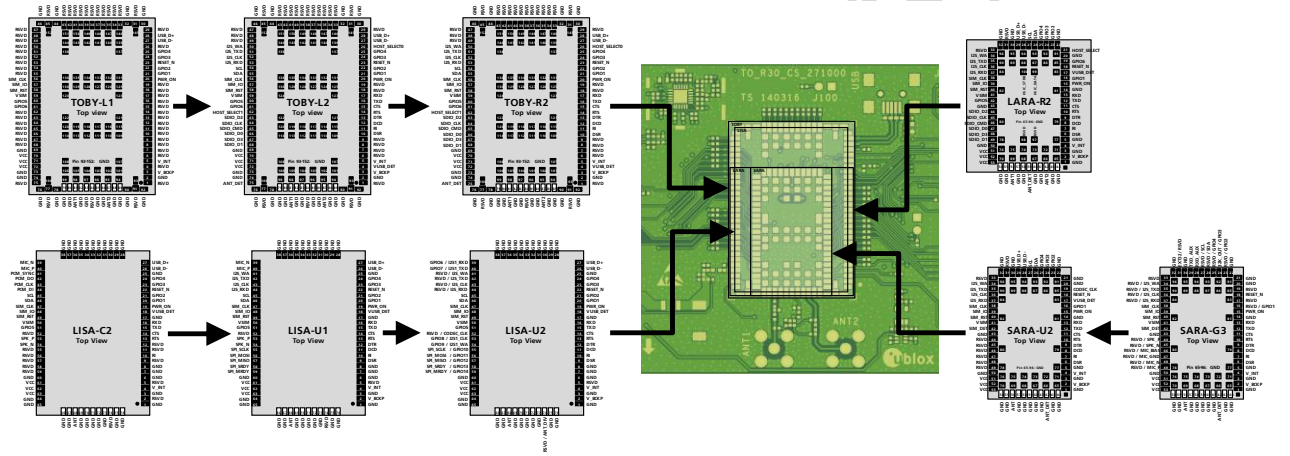
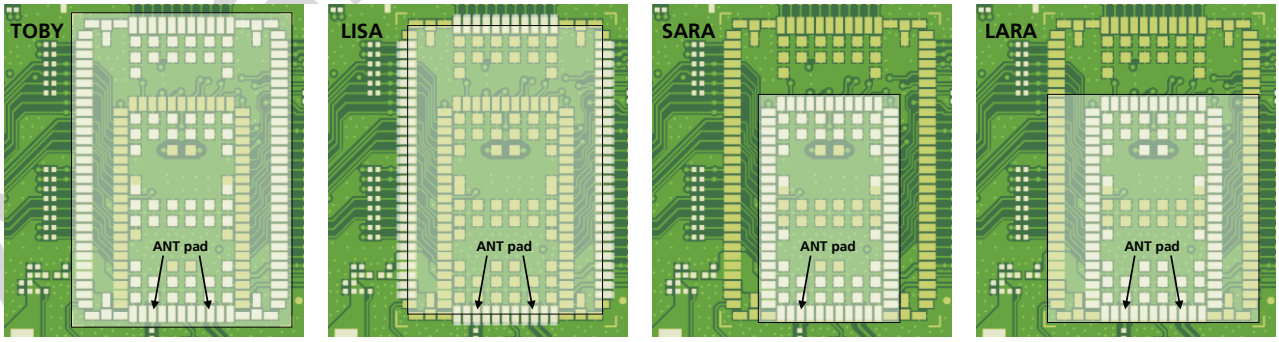


Figure 1: TOBY, LISA, SARA, LARA modules' layout compatibility: all modules are accommodated on the same nested footprint

Four different soldering paste masks are implemented in the nested design, one each for the four different form factors according to the selected mounting option (TOBY, LISA, SARA, or LARA), as shown in Figure 2.



TOBY mounting option with TOBY paste mask | LISA mounting option with LISA paste mask | SARA mounting option with SARA paste mask | LARA mounting option with LARA paste mask

Figure 2: Nested design concept description: TOBY, LISA, SARA, and LARA modules alternatively mounted on the same PCB

While the RF pin(s) of all the TOBY, LISA, SARA, and LARA modules share the same pads on the top layer of the nested application board, roughly the same concept is applicable also for all the main interfaces due to the layout compatibility between TOBY / LISA and SARA / LARA, as for example:

- The three **VCC** pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the three **VCC** pins of SARA and LARA modules to facilitate routing (see section 3.1.1, Figure 4)
- SIM pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the SIM pins of SARA and LARA (see section 3.4, Figure 16)
- UART pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the UART pins of SARA and LARA (see section 3.5.1, Figure 17)
- USB pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the USB pins of SARA and LARA (see section 3.5.3, Figure 20)
- I2S pins of TOBY and LISA share the same pads on the top layer of the nested board, and these pads are positioned very close to the pads shared by the I2S pins of SARA and LARA (see section 3.6.2.1, Figure 22)

This concept can be extended to all the interfaces shared between the modules, as described in section 3 of this application note, allowing fast and easy development of the application circuit for all modules.

2.2 Nested design bill of materials variants

The printed circuit board of the nested reference design for mounting TOBY, LISA, SARA, or LARA modules is identified by the "TO_R30_CS_271000" code (shown on the top side of the board).

Table 1 lists the different bill of materials (BoM) variants, also referred to as hardware release (HR) variants, available as mounting options on the same nested PCB[1], so that any TOBY-L1, TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, SARA-G3, or LARA-R2 module can be alternatively mounted on the same nested board with all the suitable components provided in the mounting options.

Table 1 also lists the four top-side paste masks implemented in the nested design for the four form factors (TOBY, LISA, SARA, and LARA) as described in Figure 2.

☞ Only one schematic (the TO_R30_HS_271001.pdf file) is provided, including all the necessary comments explaining the different Bill of Materials mounting options for the different hardware release variants of the nested design.

Variant ID	HW release ID	BoM file	Top-side paste mask file	Schematic file	Modules
A	HR_2710A1	SE_L20_BM_2710A1	07_PASTE_TOP_LARA	TO_R30_HS_271001	LARA-R2 series
B	HR_2710B1	SE_L20_BM_2710B1	07_PASTE_TOP_TOBY	TO_R30_HS_271001	TOBY-L2 series
C	HR_2710C1	SE_L20_BM_2710C1	07_PASTE_TOP_TOBY	TO_R30_HS_271001	TOBY-R2 series
D	HR_2710D1	SE_L20_BM_2710D1	07_PASTE_TOP_TOBY	TO_R30_HS_271001	TOBY-L1 series
E	HR_2710E1	SE_L20_BM_2710E1	07_PASTE_TOP_SARA	TO_R30_HS_271001	SARA-U2 series
F	HR_2710F1	SE_L20_BM_2710F1	07_PASTE_TOP_SARA	TO_R30_HS_271001	SARA-G3 series
G	HR_2710G1	SE_L20_BM_2710G1	07_PASTE_TOP_LISA	TO_R30_HS_271001	LISA-U2 series

Table 1: Nested design hardware releases (HR) / bill of materials (BoM) variants description

[1] The Nested Design Reference Design can be mounted on the EVB-WL1 or the EVB-WL3 Evaluation Boards as Adapter for cellular modules. The voltage rail of the modules' generic digital interfaces can be set to 1.8 V or 2.85 V on the EVB-WL1 board. The TOBY/LISA/SARA/LARA Nested Design sets this voltage to 1.8 V by tying to GND pin 41 of J301 and pin 42 of J303 as described in the schematic diagram TO_R30_CS_271000, because the V_INT voltage level of the generic digital interfaces of all TOBY, LISA, SARA, and LARA modules is 1.8 V.

2.3 Module pin-out comparison

Table 2 summarizes the electrical differences of pins on TOBY, LISA, SARA, and LARA cellular modules.

Pin Name	N°	TOBY-L1 series	N°	TOBY-L2 series	N°	TOBY-R2 series	N°	LISA-U2 series	N°	SARA-G3 series[2]	N°	SARA-U2 series	N°	LARA-R2 series
Power														
VCC	70 71 72	Operating range: 3.4 V … 4.5 V	70 71 72	Normal operating range: 3.4 V … 4.35 V Extended operating range: 3.2 V … 4.35 V TOBY-L200 / L210 / L280: Pulse current in 2G GSM TDMA connected mode	70 71 72	Normal operating range: 3.3 V … 4.4 V Extended operating range: 3.0 V … 4.5 V TOBY-R200: Pulse current in 2G GSM TDMA connected mode	61 62 63	Normal operating range: 3.3 V … 4.4 V Extended operating range: 3.1 V … 4.5 V Pulse current in 2G GSM TDMA connected mode	51 52 53	Normal operating range: 3.35 V … 4.5 V Extended operating range: 3.00 V … 4.5 V Pulse current in 2G GSM TDMA connected mode	51 52 53	Normal operating range: 3.3 V … 4.4 V Extended operating range: 3.1 V … 4.5 V SARA-U201 / U260 / U270: Pulse current in 2G GSM TDMA connected mode	51 52 53	Normal operating range: 3.3 V … 4.4 V Extended operating range: 3.0 V … 4.5 V LARA-R211: Pulse current in 2G GSM TDMA connected mode
V_BCKP	3	Output characteristics: 2.5 V typ, 3 mA max No input pin	3	Output characteristics: 3.0 V typ, 3 mA max Input operating range: 1.4 V … 4.2 V	3	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V	2	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V	2	Output characteristics: 2.3 V typ, 2 mA max Input operating range: 1.0 V … 2.4 V	2	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V	2	Output characteristics: 1.8 V typ, 3 mA max Input operating range: 1.0 V … 1.9 V
V_INT	5	Output characteristics: 1.8 V typ, 70 mA max	5	Output characteristics: 1.8 V typ, 70 mA max	5	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max	4	Output characteristics: 1.8 V typ, 70 mA max
Antenna														
ANT1 / ANT	81	RF input/output for Tx/Rx antenna	81	RF input/output for Tx/Rx antenna	81	RF input/output for Tx/Rx antenna	68	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna	56	RF input/output for Tx/Rx antenna
ANT2 / ANT_DIV	87	RF input for LTE Rx MIMO antenna	87	RF input for LTE Rx MIMO antenna and 3G Rx diversity antenna	87	RF input for LTE Rx diversity antenna anc 3G Rx diversity antenna	74	LISA-U230 only: RF input for 3G Rx diversity antenna		Not Available		Not Available	62	RF input for LTE Rx diversity antenna
ANT_DET		Not available	75	Input for antennas detection circuit[3]	75	Input for antennas detection circuit		Not available: Internal antenna detection circuit	62	SARA-G340 / SARA-G350: Input for antenna detection circuit	62	Input for antenna detection circuit	59	Input for antenna detection circuit

[2] Antenna detection (ANT_DET), DDC (I^2C), analog audio (MIC, SPK), digital audio (I2S) and GPIOs are not supported by SARA-G300 / SARA-G310: the related pins are reserved for future use (RSVD).
[3] Not supported by "00", "01", "60" product versions

Pin Name	N°	TOBY-L1 series	N°	TOBY-L2 series	N°	TOBY-R2 series	N°	LISA-U2 series	N°	SARA-G3 series[2]	N°	SARA-U2 series	N°	LARA-R2 series
System														
PWR_ON	20	Internal pull-up: Not present L-level: –0.10 V … 0.60 V H-level: 2.20 V … 4.70 V L-level pulse for switch-on: 5 s min L-level pulse for switch-off: Not supported	20	Internal pull-up: 50kΩ to VCC L-level: 0.0 … 0.3 x VCC H-level: 0.7 x VCC … VCC L-level pulse for switch-on: 5 ms min L-level pulse for switch-off: Not supported	20	Internal pull-up: 10kΩ to V_BCKP L-level: –0.30 V … 0.54 V H-level: 1.26 V … 2.10 V L-level pulse for switch-on: 50 µs min L-level pulse for switch-off: Not supported	19	Internal pull-up: Not present L-level: –0.30 V … 0.65 V H-level: 1.50 V … 4.40 V L-level pulse for switch-on: 50 µs min / 80 µs max L-level pulse for switch-off: 1 s min	15	Internal pull-up: Not present L-level: –0.10 V … 0.65 V H-level: 2.00 V … 4.50 V L-level pulse for switch-on: 5 ms min L-level pulse for switch-off: Not supported	15	Internal pull-up: Not present L-level: –0.30 V … 0.65 V H-level: 1.50 V … 4.40 V L-level pulse for switch-on: 50 µs min / 80 µs max L-level pulse for switch-off: 1 s min	15	Internal pull-up: 10kΩ to V_BCKP L-level: –0.30 V … 0.54 V H-level: 1.26 V … 2.10 V L-level pulse for switch-on: 50 µs min L-level pulse for switch-off: Not supported
RESET_N	23	Internal pull-up: 10kΩ to V_BCKP L-level: 0.00 V … 0.40 V H-level: 1.10 V … 2.60 V L-level pulse for switch-on: Not supported L-level pulse for reset: Not supported L-level pulse for switch-off: 1 s min	23	Internal pull-up: 50kΩ to VCC L-level: 0.0 … 0.3 x VCC H-level: 0.7 x VCC … VCC L-level pulse for switch-on: 18 ms min / 800 ms max L-level pulse for reset: 2.1 s min / 15 s max L-level pulse for switch-off: 16 s min	23	Internal pull-up: 10kΩ to V_BCKP L-level: –0.30 V … 0.54 V H-level: 1.26 V … 2.10 V L-level pulse for switch-on: 50 ms min L-level pulse for reset: 50 ms min L-level pulse for switch-off: Not supported	22	Internal pull-up: 10kΩ to V_BCKP L-level: –0.30 V … 0.51 V H-level: 1.32 V … 2.01 V L-level pulse for switch-on: 50 ms min L-level pulse for reset: 50 ms min L-level pulse for switch-off: Not supported	18	Internal pull-up: diode & 10kΩ to V_INT L-level: –0.30 V … 0.30 V H-level: 2.00 V … 4.70 V L-level pulse for switch-on: Not supported L-level pulse for reset: 50 ms min L-level pulse for switch-off: Not supported	18	Internal pull-up: 10kΩ to V_BCKP L-level: –0.30 V … 0.51 V H-level: 1.32 V … 2.01 V L-level pulse for switch-on: 50 ms min L-level pulse for reset: 50 ms min L-level pulse for switch-off: Not supported	18	Internal pull-up: 10kΩ to V_BCKP L-level: –0.30 V … 0.54 V H-level: 1.26 V … 2.10 V L-level pulse for switch-on: 50 ms min L-level pulse for reset: 50 ms min L-level pulse for switch-off: Not supported
EXT32K		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode	31	SARA-G300 / SARA-G310: 32 kHz input for RTC & low power idle mode SARA-G340 / SARA-G350: Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode		Not Available: Internal 32 kHz for RTC & low power idle mode
32K_OUT		Not Available		Not Available		Not Available		Not Available	24	SARA-G300 / SARA-G310: 32 kHz output, only to feed the EXT32K input SARA-G340 / SARA-G350: Not Available		Not Available		Not Available
HOST_SELECT0		Not Available	26	1.8 V input for selection of module setting by host[4]	26	1.8 V input for selection of module setting by host[4]		Not Available		Not Available		Not Available	21	1.8 V pin for module / host configuration selection[5]
HOST_SELECT1		Not Available	62	1.8 V input for selection of module setting by host[4]	62	1.8 V input for selection of module setting by host[4]		Not Available		Not Available		Not Available		Not Available

[4] Not supported
[5] Not supported by "02" product versions

Pin Name	N°	TOBY-L1 series	N°	TOBY-L2 series	N°	TOBY-R2 series	N°	LISA-U2 series	N°	SARA-G3 series[2]	N°	SARA-U2 series	N°	LARA-R2 series
SIM														
SIM_CLK	56	1.8 V / 3.0 V SIM clock	56	1.8 V / 3.0 V SIM clock	56	1.8 V / 3.0 V SIM clock	47	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock	38	1.8 V / 3.0 V SIM clock
SIM_IO	57	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	57	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	57	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	48	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up	39	1.8 V / 3.0 V SIM data Internal 4.7 kΩ pull-up
SIM_RST	58	1.8 V / 3.0 V SIM reset	58	1.8 V / 3.0 V SIM reset	58	1.8 V / 3.0 V SIM reset	49	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset	40	1.8 V / 3.0 V SIM reset
VSIM	59	1.8 V / 3.0 V SIM supply	59	1.8 V / 3.0 V SIM supply	59	1.8 V / 3.0 V SIM supply	50	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply	41	1.8 V / 3.0 V SIM supply
SIM_DET		Not available	60	Provided by GPIO5[6]: 1.8 V, SIM detect input	60	Provided by GPIO5: 1.8 V, SIM detect input	51	Provided by GPIO5: 1.8 V, SIM detect input	42	1.8 V, SIM detect input	42	1.8 V, SIM detect input	42	Provided by GPIO5: 1.8 V, SIM detect input
UART														
DSR		Not available	10	1.8 V, DSR output[7] / GPIO[6] Driver strength: 2 mA	10	1.8 V, DSR output Driver strength: 6 mA	9	1.8 V, DSR output Driver strength: 1 mA	6	1.8 V, DSR output Driver strength: 6 mA	6	1.8 V, DSR output Driver strength: 1 mA	6	1.8 V, DSR output Driver strength: 6 mA
RI		Not available	11	1.8 V, RI output[7] / GPIO[6] Driver strength: 2 mA	11	1.8 V, RI output Driver strength: 6 mA	10	1.8 V, RI output Driver strength: 2 mA	7	1.8 V, RI output Driver strength: 6 mA	7	1.8 V, RI output Driver strength: 2 mA	7	1.8 V, RI output Driver strength: 6 mA
DCD		Not available	12	1.8 V, DCD output[7] / GPIO[6] Driver strength: 2 mA	12	1.8 V, DCD output Driver strength: 6 mA	11	1.8 V, DCD output Driver strength: 2 mA	8	1.8 V, DCD output Driver strength: 6 mA	8	1.8 V, DCD output Driver strength: 2 mA	8	1.8 V, DCD output Driver strength: 6 mA
DTR		Not available	13	1.8 V, DTR input[7] / GPIO[6] Internal pull-up: ~80 kΩ	13	1.8 V, DTR input Internal pull-up: ~7.5 kΩ	12	1.8 V, DTR input Internal pull-up: ~14.4 kΩ	9	1.8 V, DTR input Internal pull-up: ~32.7 kΩ	9	1.8 V, DTR input Internal pull-up: ~14.4 kΩ	9	1.8 V, DTR input Internal pull-up: ~7.5 kΩ
RTS		Not available	14	1.8 V, Flow control input[7] Internal pull-up: ~80 kΩ	14	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ	13	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ	10	1.8 V, Flow control input Internal pull-up: ~58.1 kΩ	10	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ	10	1.8 V, Flow control input Internal pull-up: ~7.5 kΩ
CTS		Not available	15	1.8 V, Flow control output[7] Driver strength: 2 mA	15	1.8 V, Flow control output Driver strength: 6 mA	14	1.8 V, Flow control output Driver strength: 6 mA	11	1.8 V, Flow control output Driver strength: 6 mA	11	1.8 V, Flow control output Driver strength: 6 mA	11	1.8 V, Flow control output Driver strength: 6 mA
TXD		Not available	16	1.8 V, Data input[7] Internal pull-up: ~80 kΩ	16	1.8 V, Data input Internal pull-up: ~7.5 kΩ	15	1.8 V, Data input Internal pull-up: ~7.5 kΩ	12	1.8 V, Data input Internal pull-up: ~17.6 kΩ	12	1.8 V, Data input Internal pull-up: ~7.5 kΩ	12	1.8 V, Data input Internal pull-up: ~7.5 kΩ
RXD		Not available	17	1.8 V, Data output[7] Driver strength: 2 mA	17	1.8 V, Data output Driver strength: 6 mA	16	1.8 V, Data output Driver strength: 6 mA	13	1.8 V, Data output Driver strength: 5 mA	13	1.8 V, Data output Driver strength: 6 mA	13	1.8 V, Data output Driver strength: 6 mA
UART AUX														
TXD_AUX		Not Available		Not Available		Not Available		Not Available	29	1.8 V, Data input Internal pull-up: ~17.6 kΩ		Not Available		Not Available
RXD_AUX		Not Available		Not Available		Not Available		Not Available	28	1.8 V, Data output Driver strength: 5 mA		Not Available		Not Available

[6] Not supported by "00", "01", "60" product versions
[7] Not supported by "00" product versions

Pin Name	N°	TOBY-L1 series	N°	TOBY-L2 series	N°	TOBY-R2 series	N°	LISA-U2 series	N°	SARA-G3 series[2]	N°	SARA-U2 series	N°	LARA-R2 series
USB														
VUSB_DET		Not Available:	4	Leave unconnected The functionality of the pin is not supported by FW	4	Input for VBUS USB supply (5 V typical) detection	18	Input for VBUS USB supply (5 V typical) detection		Not Available	17	Input for VBUS USB supply (5 V typical) detection	17	Input for VBUS USB supply (5 V typical) detection
USB_D-	27	High-Speed USB 2.0	27	High-Speed USB 2.0	27	High-Speed USB 2.0	26	High-Speed USB 2.0		Not Available	28	High-Speed USB 2.0	28	High-Speed USB 2.0
USB_D+	28	High-Speed USB 2.0	28	High-Speed USB 2.0	28	High-Speed USB 2.0	27	High-Speed USB 2.0		Not Available	29	High-Speed USB 2.0	29	High-Speed USB 2.0
HSIC														
HSIC_DATA		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available	99	1.2 V, HSIC USB data[8]
HSIC_STRB		Not Available		Not Available		Not Available		Not Available		Not Available		Not Available	100	1.2 V, HSIC USB strobe[8]
DDC (I^2C)														
SCL		Not Available	54	1.8 V, open drain[9] Driver strength: 1 mA	54	1.8 V, open drain Driver strength: 1 mA	45	1.8 V, open drain Driver strength: 1 mA	27	1.8 V, open drain Driver strength: 3 mA	27	1.8 V, open drain Driver strength: 1 mA	27	1.8 V, open drain Driver strength: 1 mA
SDA		Not Available	55	1.8 V, open drain[9] Driver strength: 1 mA	55	1.8 V, open drain Driver strength: 1 mA	46	1.8 V, open drain Driver strength: 1 mA	26	1.8 V, open drain Driver strength: 3 mA	26	1.8 V, open drain Driver strength: 1 mA	26	1.8 V, open drain Driver strength: 1 mA
SPI														
SPI_SCLK		Not Available		Not Available		Not Available	55	1.8 V, SPI clock in / GPIO		Not Available		Not Available		Not Available
SPI_MOSI		Not Available		Not Available		Not Available	56	1.8 V, SPI data in / GPIO		Not Available		Not Available		Not Available
SPI_MISO		Not Available		Not Available		Not Available	57	1.8 V, SPI data out / GPIO		Not Available		Not Available		Not Available
SPI_SRDY		Not Available		Not Available		Not Available	58	1.8 V, SPI ctrl out / GPIO		Not Available		Not Available		Not Available
SPI_MRDY		Not Available		Not Available		Not Available	59	1.8 V, SPI ctrl in / GPIO		Not Available		Not Available		Not Available
SDIO														
SDIO_D2		Not Available	63	1.8 V, SDIO data [2] I/O[9] Driver strength: 2 mA	63	1.8 V, SDIO data [2] I/O[8] Driver strength: 6 mA		Not Available		Not Available		Not Available	44	1.8 V, SDIO data [2] I/O[8] Driver strength: 6 mA
SDIO_CLK		Not Available	64	1.8 V, SDIO clock output[9] Driver strength: 2 mA	64	1.8 V, SDIO clock output[8] Driver strength: 6 mA		Not Available		Not Available		Not Available	45	1.8 V, SDIO clock output[8] Driver strength: 6 mA
SDIO_CMD		Not Available	65	1.8 V, SDIO command I/O[9] Driver strength: 2 mA	65	1.8 V, SDIO command I/O[8] Driver strength: 6 mA		Not Available		Not Available		Not Available	46	1.8 V, SDIO command I/O[8] Driver strength: 6 mA
SDIO_D0		Not Available	66	1.8 V, SDIO data [0] I/O[9] Driver strength: 2 mA	66	1.8 V, SDIO data [0] I/O[8] Driver strength: 6 mA		Not Available		Not Available		Not Available	47	1.8 V, SDIO data [0] I/O[8] Driver strength: 6 mA
SDIO_D3		Not Available	67	1.8 V, SDIO data [3] I/O[9] Driver strength: 2 mA	67	1.8 V, SDIO data [3] I/O[8] Driver strength: 6 mA		Not Available		Not Available		Not Available	48	1.8 V, SDIO data [3] I/O[8] Driver strength: 6 mA
SDIO_D1		Not Available	68	1.8 V, SDIO data [1] I/O[9] Driver strength: 2 mA	68	1.8 V, SDIO data [1] I/O[8] Driver strength: 6 mA		Not Available		Not Available		Not Available	49	1.8 V, SDIO data [1] I/O[8] Driver strength: 6 mA

[8] Not supported by "02" product versions
[9] Not supported by "00", "01", "60" product versions

Pin Name	N°	TOBY-L1 series	N°	TOBY-L2 series	N°	TOBY-R2 series	N°	LISA-U2 series	N°	SARA-G3 series[2]	N°	SARA-U2 series	N°	LARA-R2 series
Audio														
Analog audio														
MIC_BIAS		Not Available		Not Available		Not Available		Not Available	46	2.2 V supply output for mic.		Not Available		Not Available
MIC_GND		Not Available		Not Available		Not Available		Not Available	47	Local ground sense for mic.		Not Available		Not Available
MIC_P		Not Available		Not Available		Not Available		Not Available	49	Differential signal in (+)		Not Available		Not Available
MIC_N		Not Available		Not Available		Not Available		Not Available	48	Differential signal in (-)		Not Available		Not Available
SPK_P		Not Available		Not Available		Not Available		Not Available	44	Differential signal out (+)		Not Available		Not Available
SPK_N		Not Available		Not Available		Not Available		Not Available	45	Differential signal out (-)		Not Available		Not Available
Digital audio														
I2S_TXD		Not Available	51	1.8 V, I2S data out[10] / GPIO[1] Driver strength: 2 mA	51	1.8 V, I2S data out / GPIO Driver strength: 6 mA	42	1.8 V, I2S data out Driver strength: 2 mA	35	1.8 V, I2S data out Driver strength: 5 mA	35	1.8 V, I2S data out / GPIO Driver strength: 2 mA	35	1.8 V, I2S data out / GPIO Driver strength: 6 mA
I2S_RXD		Not Available	53	1.8 V, I2S data in[10] / GPIO[10] Driver strength: 2 mA	53	1.8 V, I2S data in / GPIO Driver strength: 6 mA	44	1.8 V, I2S data in	37	1.8 V, I2S data in	37	1.8 V, I2S data in / GPIO Driver strength: 2 mA	37	1.8 V, I2S data in / GPIO Driver strength: 6 mA
I2S_WA		Not Available	50	1.8 V, I2S synch[10] / GPIO[10] Driver strength: 2 mA	50	1.8 V, I2S synch / GPIO Driver strength: 6 mA	41	1.8 V, I2S synch I/O Driver strength: 2 mA	34	1.8 V, I2S synch out Driver strength: 6 mA	34	1.8 V, I2S synch I/O / GPIO Driver strength: 2 mA	34	1.8 V, I2S synch / GPIO Driver strength: 6 mA
I2S_CLK		Not Available	52	1.8 V, I2S clock[10] / GPIO[10] Driver strength: 2 mA	52	1.8 V, I2S clock / GPIO Driver strength: 6 mA	43	1.8 V, I2S clock I/O Driver strength: 2 mA	36	1.8 V, I2S clock out Driver strength: 5 mA	36	1.8 V, I2S clock I/O / GPIO Driver strength: 2 mA	36	1.8 V, I2S clock / GPIO Driver strength: 6 mA
I2S1_TXD		Not Available		Not Available		Not Available	40	1.8 V, I2S1 Data In / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available
I2S1_CLK		Not Available		Not Available		Not Available	53	1.8 V, I2S1 synch I/O / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available
I2S1_WA		Not Available		Not Available		Not Available	54	1.8 V, I2S1 Data Out / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available
I2S1_RXD		Not Available		Not Available		Not Available	39	1.8 V, I2S1 clock I/O / GPIO Driver strength: 1 mA		Not Available		Not Available		Not Available
Other														
CODEC_CLK		Not Available	61	Provided by GPIO6[10]: 1.8 V, clock output Driver strength: 2 mA	61	Provided by GPIO6: 1.8 V, clock output Driver strength: 6 mA	52	1.8 V, clock output Driver strength: 4 mA		Not Available	19	1.8 V, clock output Driver strength: 4 mA	19	Provided by GPIO6: 1.8 V, clock output Driver strength: 6 mA

[10] Not supported by “00”, “01”, “60” product versions

Pin Name	N°	TOBY-L1 series	N°	TOBY-L2 series	N°	TOBY-R2 series	N°	LISA-U2 series	N°	SARA-G3 series[2]	N°	SARA-U2 series	N°	LARA-R2 series
GPIO														
GPIO1	21	1.8 V, configured as Network status signal	21	1.8 V, configurable GPIO Default: Wi-Fi enable Driver strength: 2 mA Pin permanently configured as WWAN status signal on '00', '01', '60' versions	21	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 6 mA	20	1.8 V, configurable GPIO Default: pin disabled Driver strength: 6 mA	16	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 6 mA	16	1.8 V, configurable GPIO Default: pin disabled Driver strength: 6 mA	16	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 6 mA
GPIO2	22	Not supported	22	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 2 mA Not supported by '00', '01', '60' product versions	22	1.8 V, configurable GPIO Default: GNSS supply ctrl Driver strength: 6 mA	21	1.8 V, configurable GPIO Default: GNSS supply ctrl Driver strength: 1 mA	23	1.8 V, configurable GPIO Default: GNSS supply ctrl Driver strength: 6 mA	23	1.8 V, configurable GPIO Default: GNSS supply ctrl Driver strength: 1 mA	23	1.8 V, configurable GPIO Default: GNSS supply ctrl Driver strength: 6 mA
GPIO3	24	Not supported	24	1.8 V, configurable GPIO Default: Pin disabled Driver strength: 2 mA Not supported by '00', '01', '60' product versions	24	1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 6 mA	23	1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 6 mA	24	1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 5 mA	24	1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 6 mA	24	1.8 V, configurable GPIO Default: GNSS data ready Driver strength: 6 mA
GPIO4	25	Not supported	25	1.8 V, configurable GPIO Default: Output / Low Driver strength: 2 mA Not supported by '00', '01', '60' product versions	25	1.8 V, configurable GPIO Default: GNSS RTC sharing Driver strength: 6 mA	24	1.8 V, configurable GPIO Default: GNSS RTC sharing Driver strength: 6 mA	25	1.8 V, configurable GPIO Default: GNSS RTC sharing Driver strength: 6 mA	25	1.8 V, configurable GPIO Default: GNSS RTC sharing Driver strength: 6 mA	25	1.8 V, configurable GPIO Default: GNSS RTC sharing Driver strength: 6 mA
GPIO5	60	Not supported	60	1.8 V, configurable GPIO Default: SIM detect input Driver strength: 2 mA Not supported by '00', '01', '60' product versions	60	1.8 V, configurable GPIO Default: SIM detect input Driver strength: 6 mA	51	1.8 V, configurable GPIO Default: SIM detection Driver strength: 6 mA		GPIO not available. 1.8 V SIM detect provided on pin 42 SIM_DET		GPIO not available. 1.8 V SIM detect provided on pin 42 SIM_DET	42	1.8 V, configurable GPIO Default: SIM detect input Driver strength: 6 mA
GPIO6	61	Not supported	61	1.8 V, configurable GPIO Default: clock output Driver strength: 2 mA Not supported by '00', '01', '60' product versions		GPIO not available. 1.8 V clock out provided on pin 61, named GPIO6	39	1.8 V, I2S1_RXD / GPIO Default: I2S1_RXD Driver strength: 1 mA 1.8 V clock out provided on pin 52 CODEC_CLK		Not Available		GPIO not available. 1.8 V clock out provided on pin 19 CODEC_CLK		GPIO not available. 1.8 V clock out provided on pin 19, named GPIO6
Reserved														
RSVD		All the pins reserved for future use (RSVD) have to be left floating		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 6 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 6 that must be externally tied to GND.		All the pins reserved for future use (RSVD) must be left floating except for the pin n° 5 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 33 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to b left floating except for the pin n° 33 that must be externally tied to GND.		All the pins reserved for future use (RSVD) have to be left floating except for the pin n° 33 that must be externally tied to GND.

Table 2: Summary of pin differences and compatibility level among modules

3 Interfaces

3.1 Power management

3.1.1 Module supply (VCC)

The same compatible external circuit can be implemented for all TOBY, LISA, SARA, and LARA modules, as for example the one described in Figure 3, even if there are minor differences in the **VCC** input voltage ranges and some differences in the current consumption figures.

The voltage provided must be within the normal operating range limits to allow module switch-on and must be above the minimum limit of the extended operating range to avoid module switch-off. For the detailed **VCC** input voltage range values see Table 2 or the module's data sheet.

The maximum average current consumption of cellular modules supporting only the 2G radio access technology is in general lower than that of modules supporting LTE and/or UMTS/HSPA, due to the different architecture.

Cellular modules supporting the 2G radio access technology require large current pulses in connected-mode when a 2G call is enabled, while modules supporting only LTE and/or UMTS/HSPA do not require large current pulses typical of 2G TDMA. For the detailed current consumption values, see the module's data sheet.

The module's system integration manual describes the detailed supply circuit design-in guidelines.

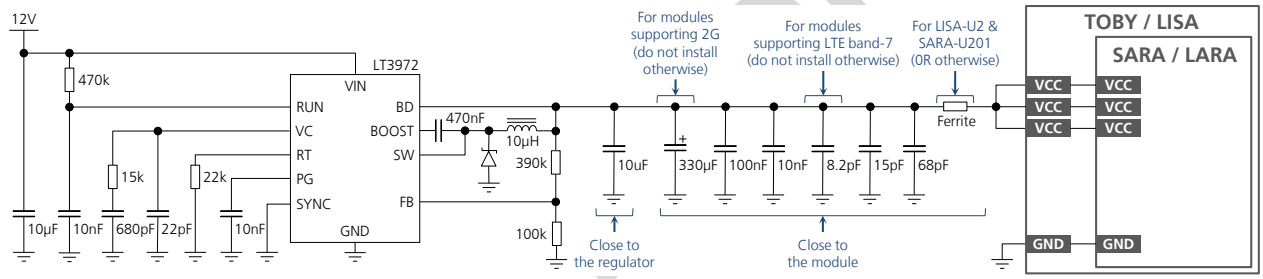


Figure 3: Example of compatible VCC supply application circuit using a high reliability step-down regulator

The three **VCC** pins of TOBY and LISA share the same pads on the top layer of the nested application board, which are positioned very close to the three **VCC** pads shared by SARA, and LARA modules to facilitate routing, as shown in the nested design top layer description shown in Figure 4.

Bypass capacitors with Self-Resonant Frequency in the supported radio frequency bands are placed very close to the **VCC** pins, at the narrowing of the **VCC** line implemented in the design, to filter EMI in the supported bands. Note that the bypass capacitors values change according to the operating bands of the module that is mounted.

In the nested design variants for LISA-U2 and SARA-U201 modules, an additional series ferrite bead for GHz band noise (Murata BLM18EG221SN1) is placed close to the **VCC** pins of the modules to filter EMI, as recommended in the module's system integration manual.

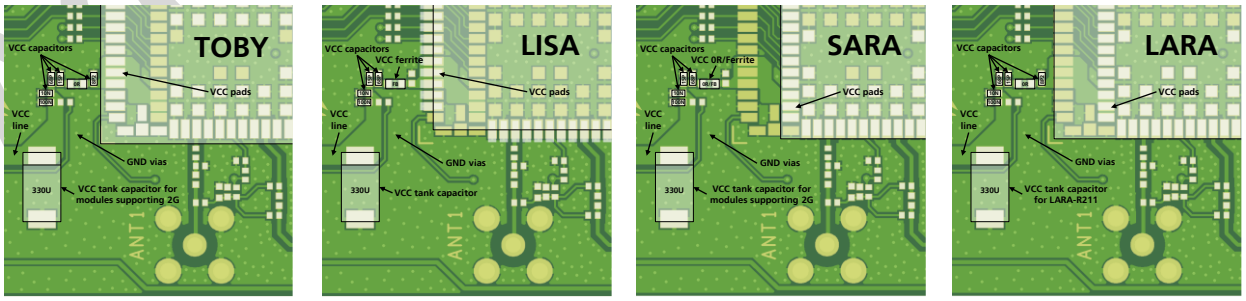


Figure 4: TOBY / LISA / SARA / LARA VCC line routing and components placement

3.1.2 RTC supply (V_BCKP)

The **V_BCKP** pin of TOBY, LISA, SARA, and LARA modules provides the output of an internal low power voltage regulator that is always enabled when the module **VCC** supply voltage is within its valid operating range.

The same compatible external circuit can be implemented using the **V_BCKP** supply output to bias the pull-up for the **PWR_ON** input pin for TOBY-L1, LISA-U2, SARA-G3 and SARA-U2 modules, even if there are minor differences in the **V_BCKP** typical output voltage, as shown in Table 2 or in the module's data sheet.

The **V_BCKP** supply output must not be used to bias an external pull-up for the **PWR_ON** input of TOBY-L2 modules because the **PWR_ON** input is equipped with an internal pull-up to **VCC** on TOBY-L2 modules.

The **V_BCKP** supply output is not required to bias an external pull-up for the **PWR_ON** input of TOBY-R2 and LARA-R2 modules because the **PWR_ON** input is equipped with an internal pull-up to **V_BCKP** on the modules.

The **V_BCKP** pin of all the modules except TOBY-L1 series can be used as input to supply the RTC when the **VCC** voltage is not present, providing RTC back-up functionality, which is not supported by TOBY-L1 modules.

The **V_BCKP** pin of TOBY and LISA share the same pad on the top layer of the nested application board, which is positioned very close to the **V_BCKP** pad shared by SARA and LARA modules in order to facilitate routing.

3.1.3 Generic Digital Interfaces supply output (V_INT)

The same compatible external circuit can be implemented for TOBY, LISA, SARA, and LARA: there are no differences in the **V_INT** output characteristics, as shown in Table 2 or in the module's data sheet.

The **V_INT** pin of TOBY and LISA share the same pad on the top layer of the nested application board, which is positioned very close to the **V_INT** pad shared by SARA and LARA modules in order to facilitate routing.

3.2 System functions

3.2.1 Module power-on

Table 3 summarizes the allowed power-on events of TOBY, LISA, SARA, and LARA modules. For more details, see the module's data sheet and system integration manual.

	TOBY-L1 series	TOBY-L2 series	TOBY-R2 series	LISA-U2 series	SARA-G3 series	SARA-U2 series	LARA-R2 series
From No-Power Mode	Applying **VCC**, with **PWR_ON** pin held low for 5 s min	Applying **VCC**	Applying **VCC**, with ramp from 2.1 V to 3.0 V within 10 ms	Applying **VCC**, with ramp from 2.5 V to 3.2 V within 1 ms	Applying **VCC**, with ramp from 2.5 V to 3.2 V within 4 ms	Applying **VCC**, with ramp from 2.5 V to 3.2 V within 1 ms	Applying **VCC**, with ramp from 2.1 V to 3.0 V within 10 ms
From Power-off Mode	Low level on the **PWR_ON** pin for 5 s min	Low level on the **PWR_ON** pin for 5 ms min	Low pulse on the **PWR_ON** pin for 50 µs min	Low pulse on the **PWR_ON** pin for 50 µs … 80 µs	Low level on the **PWR_ON** pin for 5 ms min	Low pulse on the **PWR_ON** pin for 50 µs … 80 µs	Low pulse on the **PWR_ON** pin for 50 µs min
		RTC alarm	RTC alarm	RTC alarm	RTC alarm (G340/G350 only)	RTC alarm	RTC alarm
		Low pulse on the **RESET_N** pin for 18 ms … 0.8 s	Low pulse on the **RESET_N** pin for 50 ms min	Low pulse on the **RESET_N** pin for 50 ms min		Low pulse on the **RESET_N** pin for 50 ms min	Low pulse on the **RESET_N** pin for 50 ms min

Table 3: Summary of power on events among modules

The same compatible external **PWR_ON** circuit can be implemented for TOBY, LISA, SARA, and LARA modules, as the one shown in Figure 5, even if there are minor differences in the **PWR_ON** input voltage levels ranges and in the low level time or low pulse time to switch-on the module (see Table 2 or the module's data sheet).

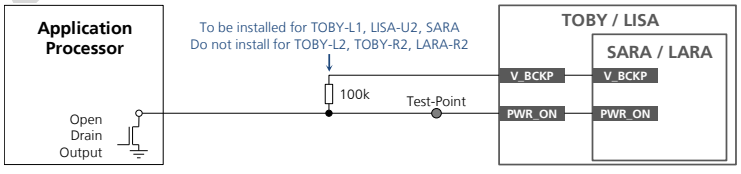


Figure 5: Example of compatible PWR_ON application circuits using an open drain output of an application processor

The line should be driven by open drain, open collector or contact switch, providing an external pull-up for the TOBY-L1, LISA-U2, and SARA modules, while an external pull-up is not needed for TOBY-L2 modules (having internal pull-up to **VCC**) and for TOBY-R2 and LARA-R2 modules (having internal pull-up to **V_BCKP**).

PWR_ON pin of TOBY and LISA share the same pad on the top layer of the nested application board, which is positioned very close to the **PWR_ON** pad shared by SARA and LARA modules in order to facilitate routing.

Figure 6 summarizes the switch-on sequence from not-powered mode in TOBY, LISA, SARA, and LARA modules.

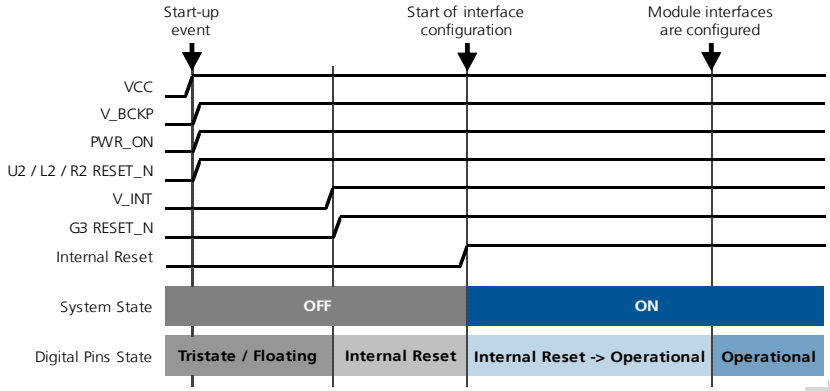


Figure 6: Description of TOBY, LISA, SARA, and LARA modules switch-on sequence from not-powered mode

1. The external supply is applied to **VCC** inputs, representing the start-up event.

   TOBY-L1: **PWR_ON** must be low while applying **VCC** to switch-on the module

   TOBY-R2, LARA-R2: if **PWR_ON** is not driven at **VCC** rising slope, then modules switch on applying **VCC**, otherwise if **PWR_ON** is driven low at **VCC** rising slope, then modules switch on when **PWR_ON** is released

   Other modules: **PWR_ON** pin status while applying **VCC** is not relevant.
2. The **V_BCKP** output is suddenly enabled by the module as **VCC** reaches valid value.
3. The **PWR_ON** line rises suddenly to the high level due to external pull-up assumed connected to **V_BCKP** on LISA and SARA, or due to internal pull-up on TOBY-L2, TOBY-R2 and LARA-R2.

   The **RESET_N** line rises suddenly to high logic level due to internal pull-up of **V_BCKP** on TOBY-R2, LISA, SARA-U2 and LARA-R2, or **VCC** on TOBY-L2.
4. All the generic digital pins are tri-stated (not powered) before the switch-on of their supply source (**V_INT**).

   Any external signal connected to the generic digital pins must be tri-stated or set low at least before the activation of the **V_INT** supply output to avoid latch-up of circuits and allow a proper boot of the module.
5. The **V_INT** generic digital interfaces supply output is enabled by the integrated power management unit.
6. The **RESET_N** line of SARA-G3 rises suddenly to high logic level due to internal pull-up to **V_INT**.
7. The internal reset signal is held low by the integrated power management unit.

   The baseband processor core and all the digital pins of the modules are held in their reset state, described in the pin-out table of the module' data sheet.
8. When the internal reset signal is released by the integrated power management unit, the processor core starts to configure the digital pins of the modules to each default operational state.

   The internal reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the start of the power-on sequence.
9. The duration of the phase of pins' configuration varies between different modules' platforms, and it varies between generic digital interfaces and the USB interface due to specific host / device enumeration timings.

   The host application processor should not send any AT command until the end of this interface's configuration phase. The greeting text can be activated by means of the AT+CSGT command to notify the external application that the module is ready to operate (i.e. ready to reply to AT commands). The first AT command can then be sent to the module, given that the UART has been configured at a fixed baud rate (the baud rate of the host application processor) to let the module send the greeting text.

Figure 7 summarizes the switch-on sequence from power-off mode of TOBY, LISA, SARA, and LARA modules.

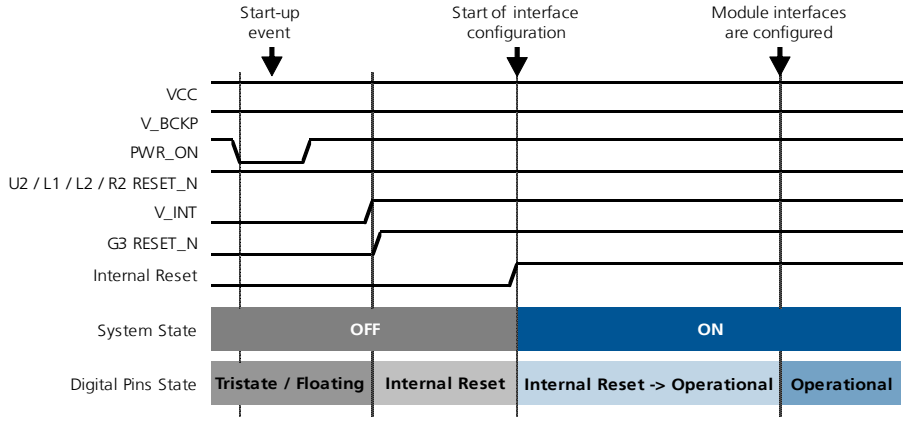


Figure 7: Description of TOBY, LISA, SARA, and LARA modules switch-on sequence from power-off mode

1. The external supply is still applied to the **VCC** inputs because it is assumed that the module has been previously switched off by the AT+CPWROFF command.

   The **V_BCKP** output is internally enabled because proper **VCC** is present.
2. The **PWR_ON** pin is set low for a valid time period, representing the start-up event.
3. All the generic digital pins of the modules are tri-stated (not powered) before the switch-on of their supply source (**V_INT**).

   Any external signal connected to the generic digital pins must be tri-stated or set low at least before the activation of the **V_INT** supply output to avoid latch-up of circuits and allow a proper boot of the module.
4. The **V_INT** generic digital interfaces supply output is enabled by the integrated power management unit.
5. The **RESET_N** line of SARA-G3 modules rises suddenly to high logic level due to internal pull-up to **V_INT**.
6. The internal reset signal is held low by the integrated power management unit.

   The baseband processor core and all the digital pins of the modules are held in their reset state, described in the pin-out table of the module's data sheet.
7. When the internal reset signal is released by the integrated power management unit, the processor core starts to configure the digital pins of the modules to each default operational state.

   The internal reset signal is not available on a module pin, but the application can monitor the **V_INT** pin to sense the start of the power-on sequence.
8. The duration of the phase of pins' configuration varies between different modules' platforms, and it varies between generic digital interfaces and the USB interface due to specific host / device enumeration timings

   The host application processor should not send any AT command until the end of this interface's configuration phase. The greeting text can be activated by means of the AT+CSGT command to notify the external application that the module is ready to operate (i.e. ready to reply to AT commands). The first AT command can then be sent to the module, given that the UART has been configured at a fixed baud rate (the baud rate of the host application processor) to let the module send the greeting text.

3.2.2 Module power-off

TOBY, LISA, SARA, and LARA modules can be all properly switched off in this way:

- AT+CPWROFF command (for more details see the module's AT commands manual). The current parameters are saved in the module's non-volatile-memory and a proper network detach is performed

LISA-U2 modules and SARA-U2 modules can also be properly switched off in this way:

- Low pulse on **PWR_ON** pin, as shown in Table 2 or in the module's data sheet.

TOBY-L1 and TOBY-L2 series modules can also be switched off in this way:

- Low level on **RESET_N** pin for a valid period of time (see the Table 2 or the module's data sheet). In this case, the current parameters are not saved in the module's non-volatile-memory and a proper network detach is not performed.

Figure 8 summarizes the switch-off sequence of TOBY, LISA, SARA, and LARA by AT+CPWROFF command.

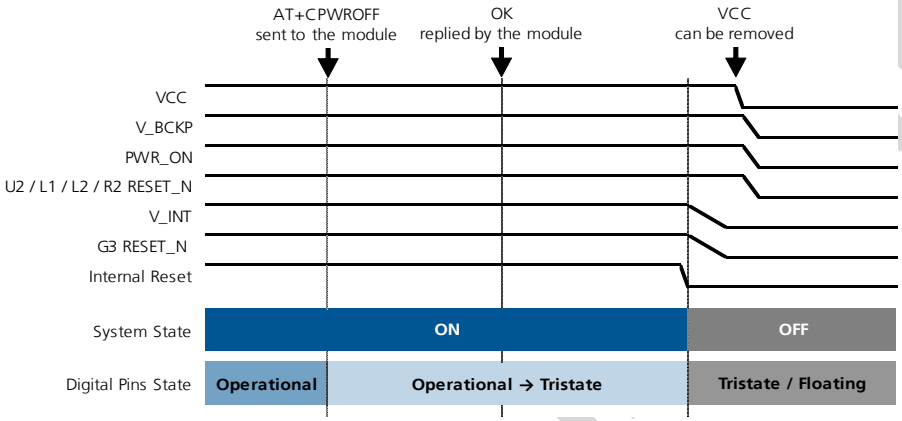


Figure 8: Description of TOBY, LISA, SARA, and LARA modules switch-off sequence by AT+CPWROFF command

1. When the AT+CPWROFF command is sent, the module starts the switch-off routine.
2. The module replies OK on the AT interface: the switch-off routine is in progress.
3. At the end of the switch-off routine, the internal reset signal is set low by the PMU
   The generic digital interfaces supply output (**V_INT**) is turned off by the module
   All the digital pins are tri-stated (not powered) because their supply is turned off
   The application can monitor **V_INT** to sense the end of the switch-off routine.
4. After the end of the switch-off routine, the module is in power-off mode as long as a valid supply is held: **V_BCKP** output is still turned on during this phase.
5. The module supply can be removed entering not-powered mode.

3.2.3 Module reset

TOBY, LISA, SARA, and LARA modules can all be properly reset (re-booted) in this "software" way:

- AT+CFUN command (see the module's AT commands manual). The current parameter settings are saved in the module's non-volatile memory and a proper network detach is performed.

An abrupt hardware reset (re-boot) is performed on TOBY-L1 series modules in this "hardware" way:

- Low level on the **RESET_N** pin, normally high by internal pull-up, for a valid time period (see Table 2) and then forcing the low level on the **PWR_ON** pin, normally high with external pull-up, for a valid time period (see Table 2). The current parameter settings are not saved in the module's non-volatile memory and a proper network detach is not performed.

An abrupt hardware reset (re-boot) is performed on TOBY-L2, TOBY-R2, LISA, SARA, and LARA-R2 in this way:

- Low level on the **RESET_N** pin, normally high by internal pull-up, for a valid time period (see Table 2 or the module's data sheet). The current parameter settings are not saved in module's non-volatile memory and a proper network detach is not performed.

The same compatible external reset circuit can be implemented for TOBY, LISA, SARA, and LARA modules even if there are minor differences in the **RESET_N** input voltage level ranges and in the low level time, as shown in Table 2 or in the module's data sheet. The line should be driven by open drain, open collector or contact switch, because all the modules are equipped with an internal pull-up.

The **RESET_N** pin of TOBY and LISA share the same pad on the top layer of the nested application board, which is positioned very close to the **RESET_N** pad shared by SARA and LARA modules to facilitate routing.

On the **RESET_N** line of the nested application board, there are spaces to mount proper bypass capacitors and a series ferrite bead / EMI suppression filter as additional circuit precautions for LISA-U2 series modules to satisfy ESD immunity test requirements, as suggested in LISA-U series System Integration Manual [11].

These additional components are not required for the other modules.

3.2.4 External 32 kHz input (EXT32K)

SARA-G300 and SARA-G310 modules provide the **EXT32K** input pin, which must be fed by a proper 32 kHz signal (e.g. the one provided by the **32K_OUT** output of the same modules), to furnish the reference clock for the RTC, allowing low power idle-mode and RTC functions support (see Table 2 or SARA-G3 Data Sheet [5]).

TOBY, LISA, LARA and the other SARA modules do not provide the **EXT32K** input pin.

The SARA-G300 / SARA-G310 **EXT32K** pin shares a pad on the top layer of the nested PCB with the **RSVD** (reserved) pin of the other SARA modules, while the same pad is not used for any TOBY or LISA pins.

The 0 Ω series resistor R228 can be mounted to connect the **EXT32K** pin with the **32K_OUT** pin of SARA-G300 / SARA-G310 modules. Otherwise, a 32 kHz signal can be provided mounting the Y200 oscillator circuit.

3.2.5 Internal 32 kHz output (32K_OUT)

SARA-G300 and SARA-G310 modules provide the **32K_OUT** output pin, which gives a 32 kHz reference signal suitable only to feed the **EXT32K** input pin of the same modules. (which in turn furnishes the reference clock for the RTC, allowing low power idle-mode and RTC functions support with modules switched on.)

TOBY, LISA, LARA and the other SARA modules do not provide the **32K_OUT** output.

32K_OUT pad for SARA-G300 / SARA-G310 is shared on the top layer of the nested PCB with the **GPIO3** pad for the other SARA modules, while the same pad is not shared with any pad for TOBY and LISA.

3.2.6 Module / host configuration selection

LARA-R2 modules include one pin (**HOST_SELECT**) for the selection of module / host processor configuration: the pin is available to select, enable, connect, disconnect and subsequently re-connect the HSIC interface.

TOBY-L2 and TOBY-R2 modules include two **HOST_SELECTx** pins, but the functionality is not supported, while TOBY-L1, LISA, and SARA modules do not provide host select input pins.

Host select pins of TOBY-L2 and TOBY-R2 share the pads on the top layer of the nested PCB with **RSVD** pins of TOBY-L1 and LISA, while the host select pin of LARA-R2 shares the pad with a **GND** pin of SARA.

3.3 RF connection

3.3.1 RF interface for Tx/Rx main antenna

The same compatible external circuit can be implemented for all the TOBY, LISA, SARA, and LARA modules on the RF input/output for the main Tx/Rx antenna (**ANT1** pin of TOBY and LARA, **ANT** pin of LISA and SARA), even if there are some differences in the operating bands frequency ranges, as summarized in Figure 9.

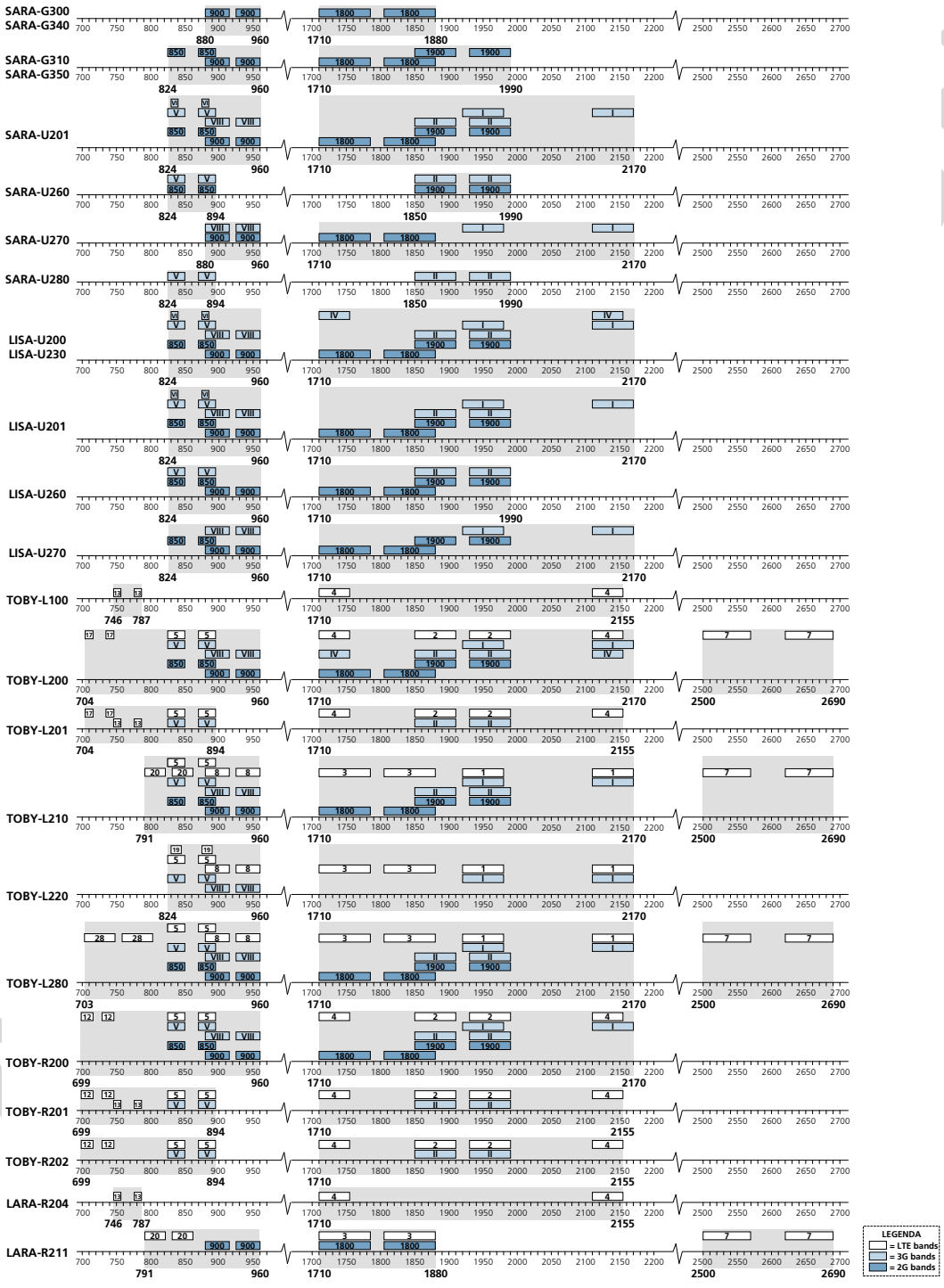


Figure 9: Summary of operating bands frequency ranges among TOBY, LISA, SARA, and LARA modules

The **ANT1** / **ANT** pin of TOBY, LISA, SARA, and LARA share the same pad on the top layer of the nested application board, so that a unique 50 Ω transmission line can be implemented on the application board for the main RF input/output. This is shown in the nested design top layer description reported in Figure 10 to Figure 14.

On the main RF line of the nested application board there are spaces to mount a high-pass filter (series capacitor and shunt inductor) as additional circuit precaution for LISA-U2 and SARA-U2 modules to satisfy ESD immunity test requirements, as suggested in the module's system integration manual. These additional components are not required for TOBY and SARA-G3 modules, which provide ESD immunity up to ±4 kV / ±8 kV for Contact / Air Discharge according to IEC 61000-4-2.

On the main RF line of the nested application board there are spaces to mount a high-pass filter (series capacitor) as part of the main antenna detection circuit connected to the **ANT_DET** pin of TOBY-L2, TOBY-R2, LARA-R2, SARA-U2, SARA-G340, and SARA-G350 modules, as suggested in the module's system integration manual. These additional parts are not required for LISA-U2 modules, which are equipped with internal circuit for antenna detection support, and for the TOBY-L1 and SARA-G300 / SARA-G310 modules, which do not support antenna detection.

3.3.2 RF interface for Rx MIMO / diversity antenna

The same compatible external circuit can be implemented for TOBY, LARA, and LISA-U230 on the RF input for the Rx MIMO antenna or for the Rx diversity antenna (**ANT2** pin of TOBY or LARA, **ANT_DIV** pin of LISA-U230), even if there are some differences in the operating bands frequency ranges, as summarized in Figure 9.

The **ANT2** / **ANT_DIV** pin of TOBY, LARA, and LISA-U230 share the same pad on the top layer of the nested application board, so that a unique 50 Ω transmission line can be implemented on the application board, as shown in the nested design top layer described from Figure 10 to Figure 14.

The SARA modules and the other LISA-U2 series modules do not support Rx diversity nor MIMO communication.

On the secondary RF line of the nested application board there are spaces to mount a high-pass filter (series capacitor) as part of the secondary antenna detection circuit connected to the **ANT_DET** pin of TOBY-L2, TOBY-R2, and LARA modules, as suggested in the module's system integration manual.

ANT2 / **ANT_DIV** pin of TOBY, LARA, and LISA-U230 shares a pad on the top layer of the nested application board with the antenna detection input (**ANT_DET** pin) of SARA-G340 / SARA-G350 and SARA-U2 modules, and with a **RSVD** (reserved) pin of the other LISA-U2 series modules and SARA-G300 / SARA-G310 modules.

3.3.3 Antenna detection interface (ANT_DET)

An external application circuit, connecting the **ANT_DET** and the **ANT** or **ANT1** / **ANT2** pins, is implemented when SARA-G340 / SARA-G350, TOBY-L2, TOBY-R2 or LARA-R2 modules are mounted, to provide antenna detection functionality as described in the modules' system integration manual and in Figure 10 to Figure 14.

The **ANT_DET** pin of SARA-G340 / SARA-G350 and SARA-U2 modules shares a pad on the top layer of the nested application board with the **ANT2** / **ANT_DIV** / **RSVD** pin of TOBY, LARA and LISA modules.

The **ANT_DET** pin of TOBY modules does not share a pad on the top layer of the nested application board with the other LISA, SARA, and LARA modules.

The **ANT_DET** pin of LARA modules shares a pad on the top layer of the nested application board with a **RSVD** pin of TOBY and with a **GND** pin of SARA and LISA modules.

LISA-U2 modules are equipped with an internal circuit for antenna detection support. Thus external antenna detection components are not mounted for these modules. Anyway, in the LISA-U2 nested design hardware release variant (HR_2710G1), a high-pass filter (series capacitor and shunt inductor) is provided on the main RF line as additional circuit precaution to satisfy ESD immunity test requirements, as suggested in LISA-U series System Integration Manual [11]. These additional components prevent support of antenna detection functionality by LISA-U2 modules on the HR_2710G1 nested design hardware release variant.

TOBY-L1 and SARA-G300 / SARA-G310 modules do not support the antenna detection. Thus external antenna detection components are not mounted for these modules.

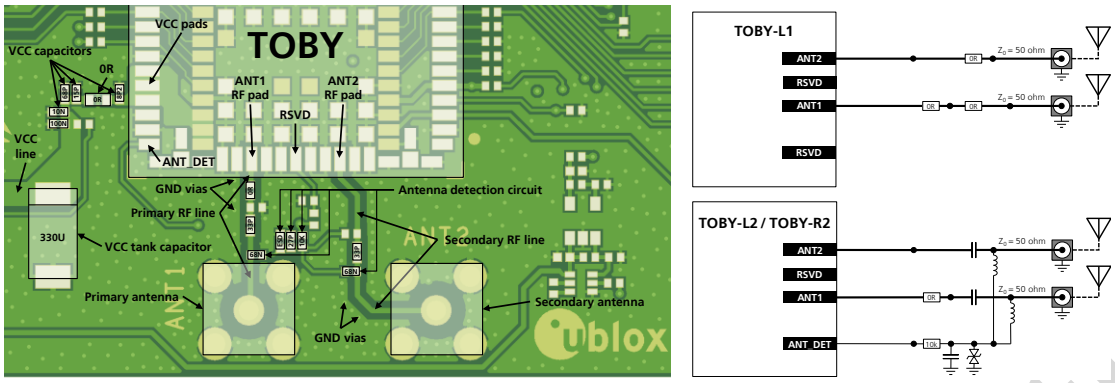


Figure 10: TOBY RF and VCC lines routing and components placement

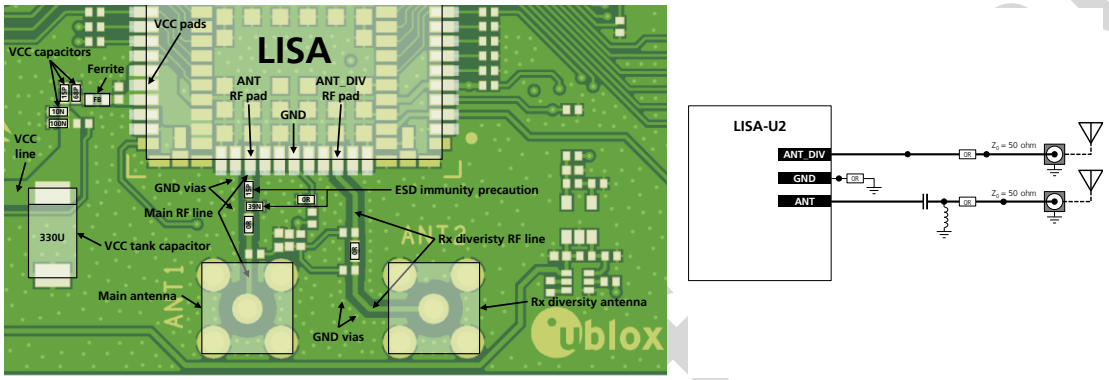


Figure 11: LISA RF and VCC lines routing and components placement

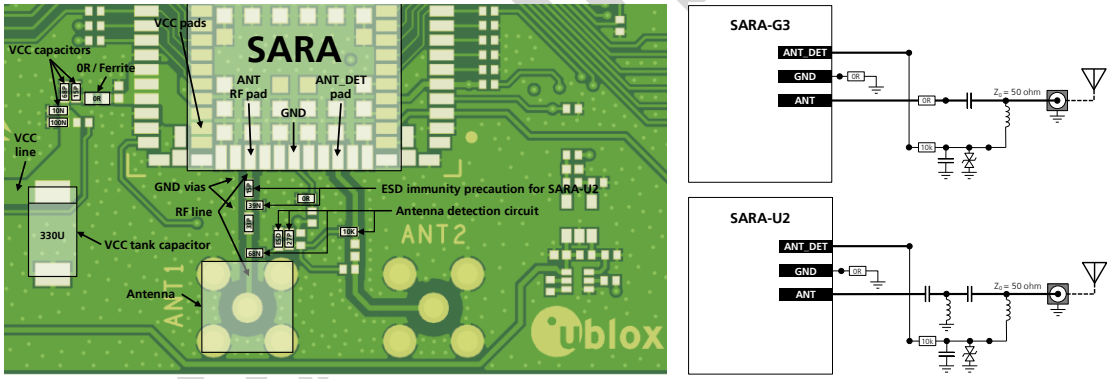


Figure 12: SARA RF and VCC lines routing and components placement

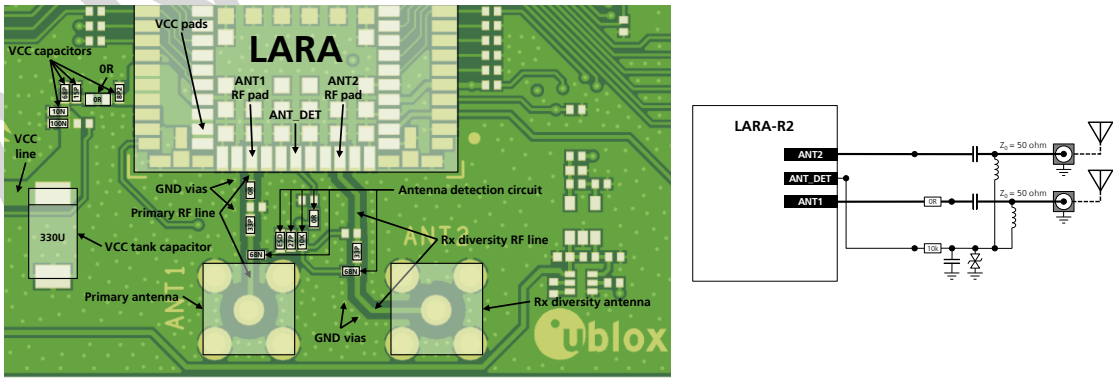


Figure 13: LARA RF and VCC lines routing and components placement

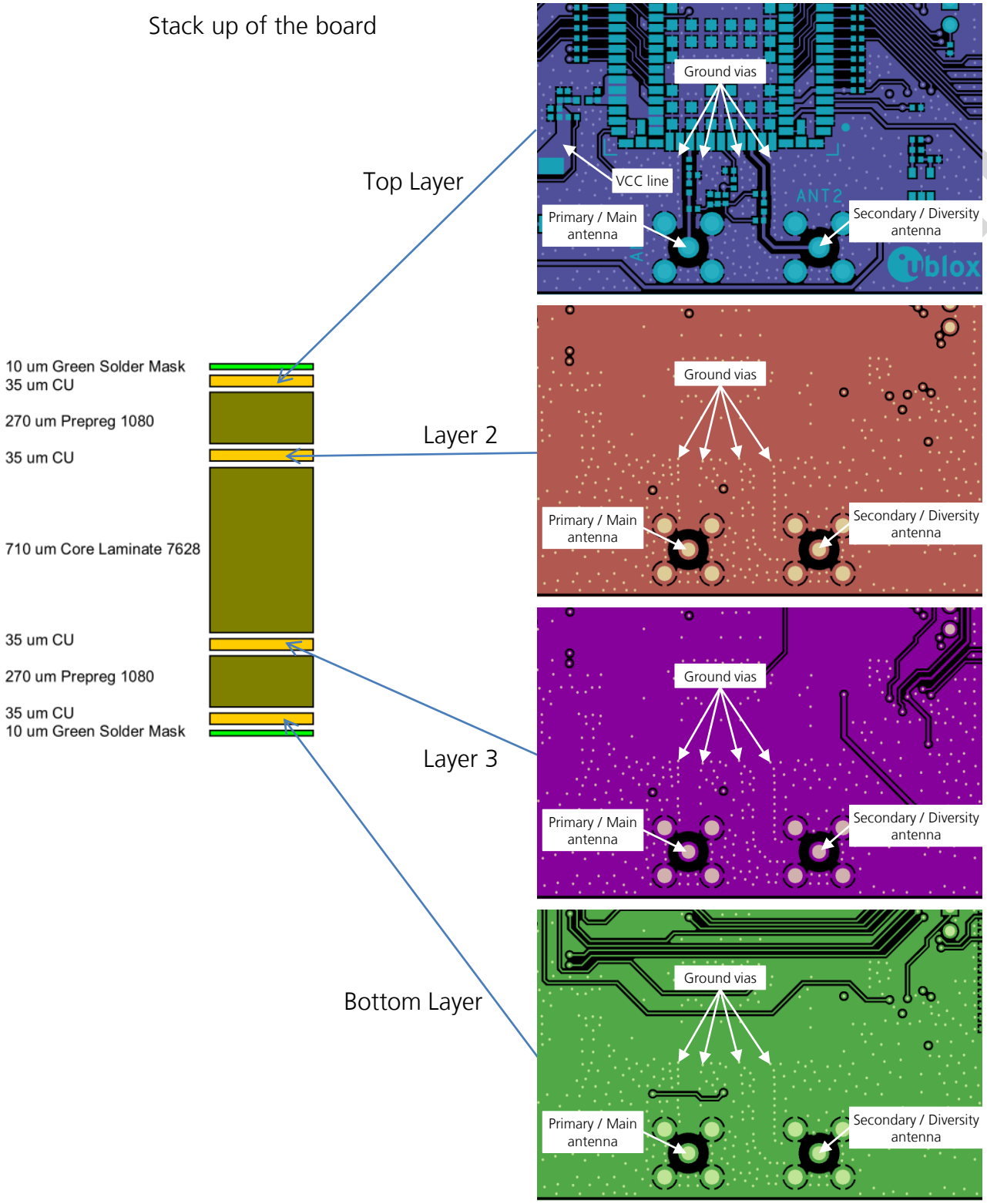


Figure 14: Stack up of the nested design board and view of the different layers close to RF and VCC circuits

3.4 SIM interface

The same compatible external circuit can be implemented for TOBY, LISA, SARA, and LARA modules: 1.8 V and 3.0 V SIM card / IC are supported over the available SIM interface.

SIM card detection function is available on the **GPIO5** pin of TOBY-L2, TOBY-R2, and LISA-U2 modules, and the pin shares the same pad on the top layer of the nested application board. The pad is positioned very close to the pad shared by SARA / LARA modules for the SIM card detection pin (**SIM_DET** pin on SARA, **GPIO5** on LARA). TOBY-L1 modules do not support the SIM card detection function, while SIM card hot insertion/removal function is additionally configurable on the same pin of TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, and LARA-R2 modules.

Figure 15 shows an example of compatible application circuit for the connection of a removable SIM card placed in a SIM card connector equipped with a normally-open mechanical switch for the optional implementation of the SIM card detection function.

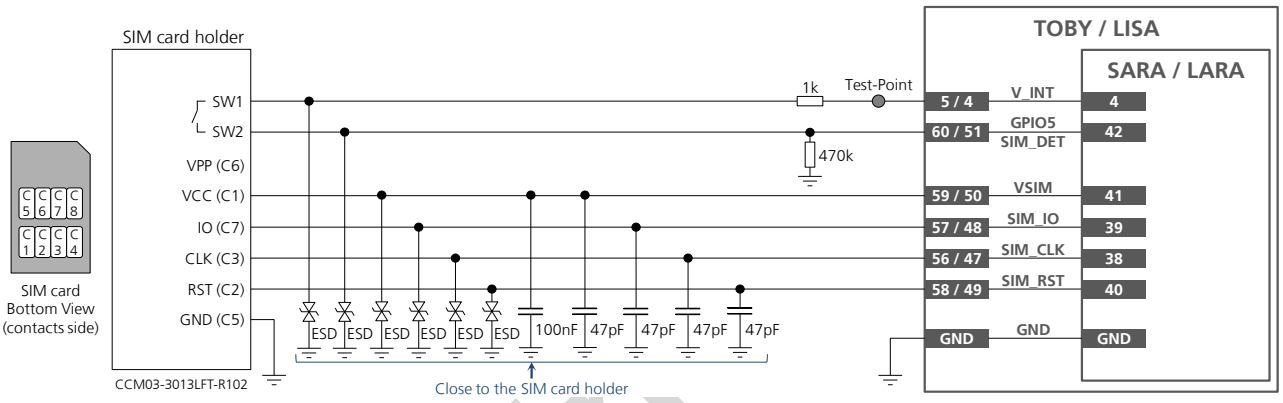


Figure 15: Example of compatible application circuit connecting a removable SIM card, with SIM card detection implemented

SIM interface pins of TOBY / LISA, including the pin providing the SIM card detection function, share the same pads on the top layer of the nested application board. These pads are positioned very close to the SIM pads shared by SARA / LARA modules to facilitate routing; see Figure 16.

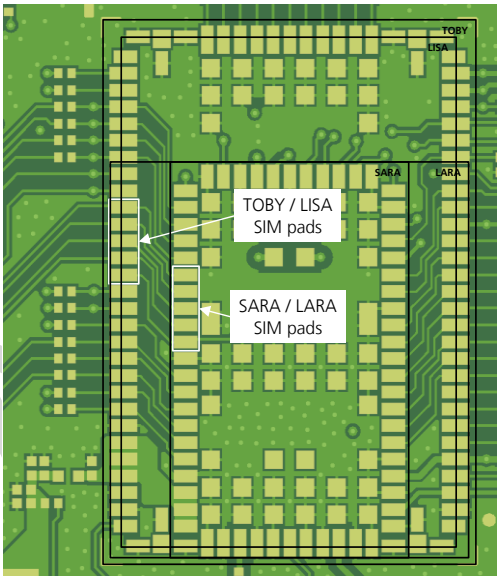


Figure 16: SIM interface pads for TOBY / LISA and SARA / LARA modules' SIM pins are positioned to facilitate routing

3.5 Serial interfaces

3.5.1 UART interface

The same compatible external circuit for a 1.8 V UART interface can be implemented for TOBY, LISA, SARA, and LARA modules, as shown in Figure 17. The communication with a 3.0 V Application Processor (DTE) is implemented by means of appropriate unidirectional voltage translators. This provides a partial power down feature so that either the DTE 3.0 V supply or the **V_INT** 1.8 V supply of the module can be ramped up first.

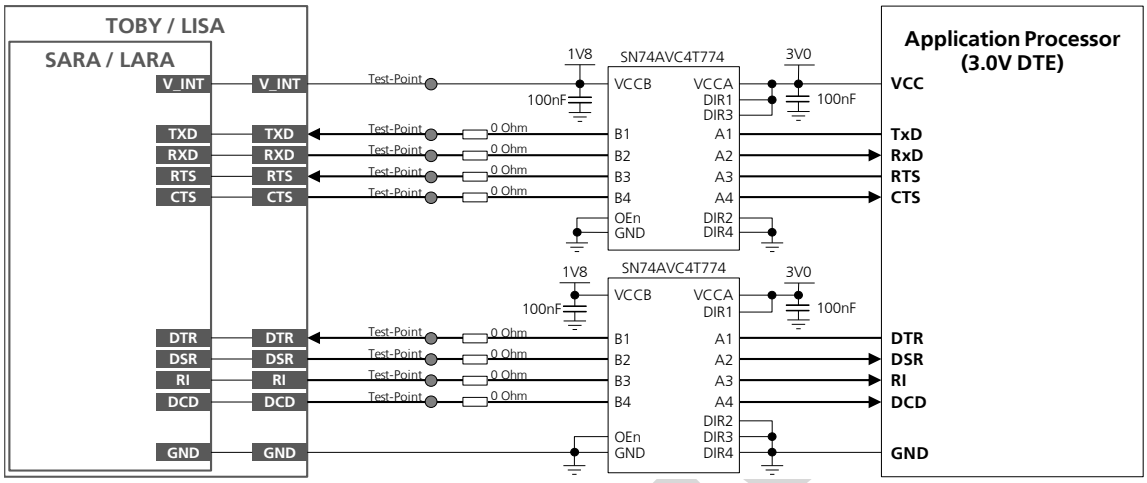


Figure 17: Compatible UART interface application circuit with complete V.24 serial communication with 3.0 V DTE

All the modules support a UART interface except TOBY-L1 and the product version "00" of TOBY-L2 modules.

Table 2 and the module's data sheet report minor differences for internal pull-ups and drivers strengths.

UART interface pins of TOBY / LISA share the same pads on the top layer of the nested application board, while SARA / LARA pins do not share the same pads, but they are positioned very close each other facilitating routing, as shown in Figure 18.

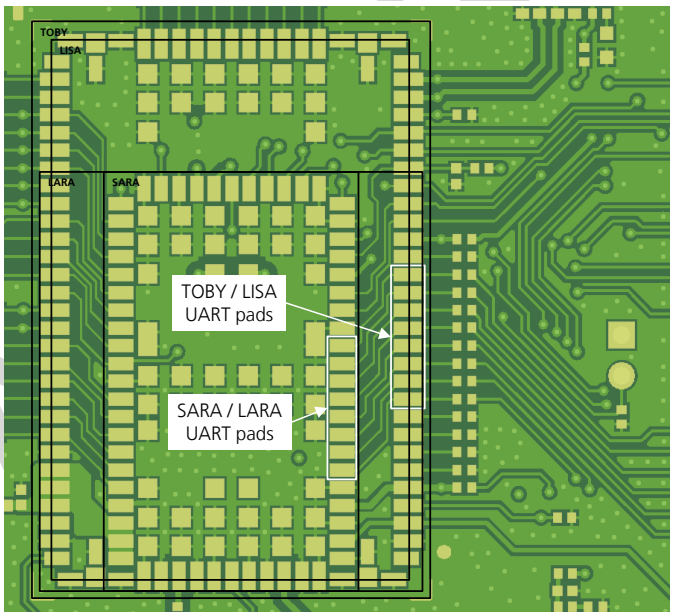


Figure 18: UART interface pads for TOBY / LISA and SARA / LARA modules' UART pins are positioned to facilitate routing

3.5.2 UART AUX interface

Only the SARA-G3 modules provide an auxiliary UART interface, which is not provided by the other modules.

The auxiliary UART interface pins (**RXD_AUX** / **TXD_AUX**) of SARA-G3 modules share the same pads on the top layer of the nested application board with the USB data interface pins (**USB_D-** / **USB_D+**) of SARA-U2 and LARA-U2 modules: 0 Ω series resistors are provided to detach the auxiliary UART signals and avoid stubs on the impedance-controlled USB lines (see Figure 19 and Figure 20).

The pads for auxiliary UART on the nested application board are not shared with any TOBY and LISA pins.

3.5.3 USB interface

All the modules except SARA-G3 series provide a USB High-Speed 2.0 compliant interface.

USB_D- / **USB_D+** pins of TOBY and LISA share the same pads on the top layer of the nested application board: the impedance-controlled USB data lines (differential characteristic impedance Z_0 = 90 Ω and common mode characteristic impedance Z_{CM} = 30 Ω as per USB 2.0 specifications) are routed on the top layer of the nested application board providing direct connection between TOBY / LISA pins and the USB connector.

USB_D- / **USB_D+** pins of SARA-U2 and LARA-R2 do not share the same pads with the **USB_D-** / **USB_D+** pins of TOBY and LISA: 0 Ω series resistors are provided on the bottom layer, close to TOBY / LISA pads, to detach the signals when TOBY / LISA modules are mounted, avoiding stubs on the USB lines (see Figure 19 and Figure 20).

USB_D- / **USB_D+** pins of SARA-U2 auxiliary UART share the same pads with the **RXD_AUX** / **TXD_AUX** pins of SARA-G3 modules: 0 Ω series resistors are provided on the bottom layer, close to SARA / LARA pads, to detach the signals and avoid stubs on the impedance-controlled USB lines (see Figure 19 and Figure 20).

In the nested design variants for TOBY-R2, LISA, SARA-U2, and LARA-R2 modules there are two 0 Ω series resistors to route the VBUS supply (+5V) from the USB connector to the **VUSB_DET** pin of TOBY-R2 (pin 4), LISA (pin 18), or SARA-U2 / LARA-R2 (pin 17) respectively (see Figure 19).

TOBY-L2 modules do not support the **VUSB_DET** functionality: the pin (pin 4) must be left unconnected and it is accordingly left unconnected in the nested design variants for TOBY-L2 modules. TOBY-L1 modules do not require an additional pin for VBUS USB supply, so they have no **VUSB_DET** pin.

The LISA **VUSB_DET** pin 18 shares the pad on the top layer of the nested application board with the TOBY **RSVD** pin 19, while the LISA **GND** pin 3 shares the pad with the TOBY pin 4, which is **RSVD** on TOBY-L1, not supported on TOBY-L2, **VUSB_DET** on TOBY-R2. A 0 Ω series resistor is provided to connect the pad to GND only if LISA is mounted. The pad for SARA-U2 / LARA-R2 **VUSB_DET** pin is not shared with any TOBY and LISA pin; the signal is routed from the pad designed for LISA **VUSB_DET** pin to the pad designed for SARA-U2 / LARA-R2 **VUSB_DET** pin (see Figure 19).

See the module's data sheet and system integration manual for detailed USB features description and guidelines for **USB_D-** and **USB_D+** High-Speed data lines routing rules.

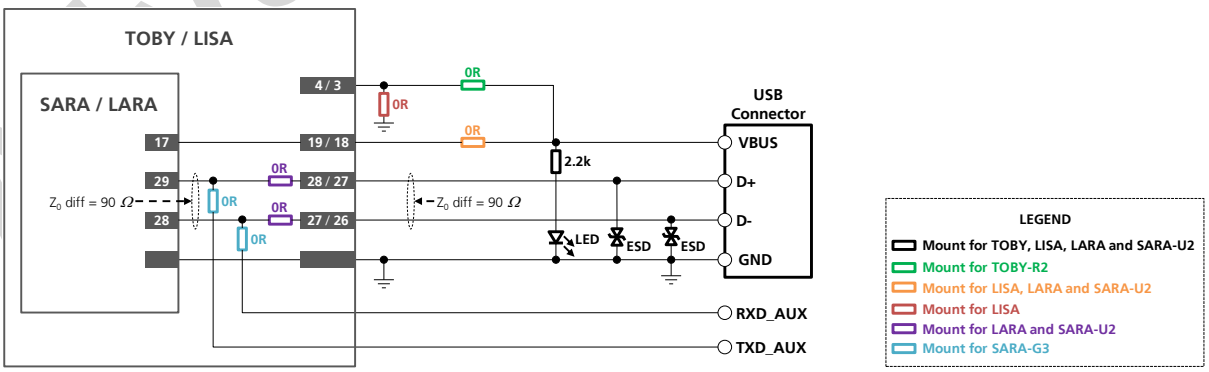


Figure 19: TOBY / LISA / LARA / SARA-U2 USB and SARA-G3 UART AUX signals schematic diagram

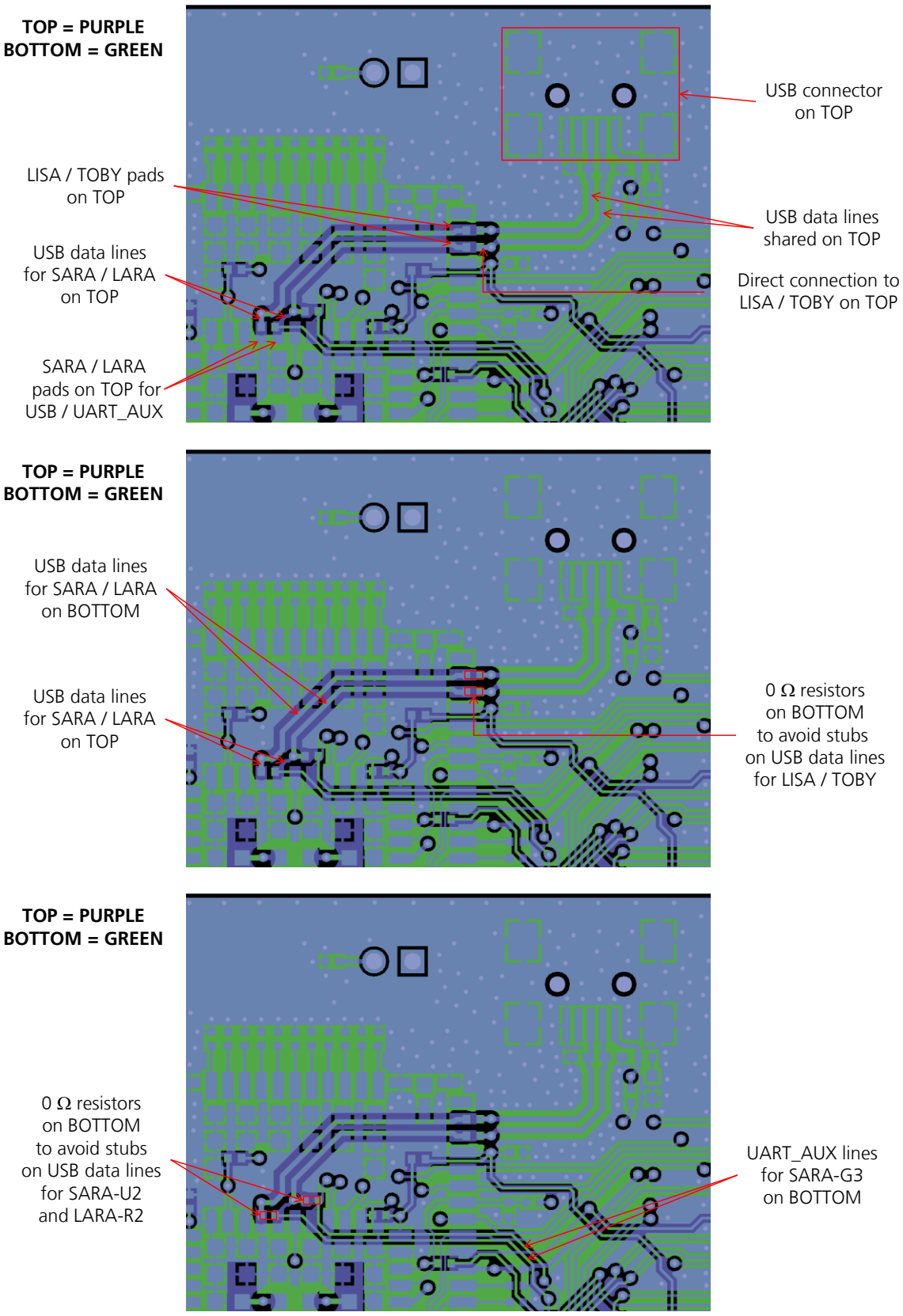


Figure 20: TOBY / LISA / SARA-U2 / LARA USB and SARA-G3 UART AUX signals layout description

3.5.4 HSIC interface

LARA-R2 modules provide a USB High-Speed Inter-Chip compliant interface (**HSIC_DATA**, **HSIC_STRB**), which is not available on the other modules. The HSIC interface pins of LARA-R2 modules do not share pads on the top layer of the nested application board with pins of the other modules.

3.5.5 SPI interface

LISA-U2 modules provide an SPI interface (5-wire IPC interface), which is not available on the other modules.

SPI interface pins of LISA-U2 modules share pads on the top layer of the nested application board with **RSVD** (reserved) pins of TOBY-L1 modules and with SDIO interface pins of TOBY-L2 and TOBY-R2 modules, while the same pads are not shared with any SARA / LARA pins.

See the LISA-U series System Integration Manual [11] for application circuits and further details.

3.5.6 DDC (I^2C) interface

All the modules except SARA-G300, SARA-G310, TOBY-L1 and the product versions "00", "01" and "60" of TOBY-L2 modules provide a 1.8 V DDC (I^2C bus compatible) interface.

The same compatible external circuit can be implemented: all the modules except TOBY-L1 and TOBY-L2 support communication with u-blox GNSS receivers over the DDC (I^2C) interface, and all the modules except TOBY-L1 and SARA-G3 support communication with any I^2C slave over the DDC (I^2C) interface.

DDC (I^2C) pins of TOBY-L2, TOBY-R2 and LISA-U2 modules share pads on the top layer of the nested application board. The same pads are used by TOBY-L1 **RSVD** (reserved) pins and are positioned very close to the DDC (I^2C) pads shared by SARA / LARA modules to facilitate routing.

Table 4 summarizes additional GNSS functionalities provided over GPIOs, where supported by module FW (more details in the module's data sheet, system integration manual and AT commands manual).

Function	SARA / LARA	LISA-U2	TOBY-R2	Comments
GNSS data ready	**GPIO3** / pin 24	**GPIO3** / pin 23	**GPIO3** / pin 24	The GNSS receiver sends this interrupt to the cellular module to claim data available on DDC (I^2C) interface
GNSS RTC sharing	**GPIO4** / pin 25	**GPIO4** / pin 24	**GPIO4** / pin 25	The cellular module sends this interrupt to the GNSS receiver to provide timing information
GNSS supply enable	**GPIO2** / pin 23	**GPIO2** / pin 21	**GPIO2** / pin 22	This is an output of the cellular module used to enable/disable the supply of the GNSS receiver

Table 4: GNSS custom function overview over GPIOs

3.5.7 SDIO interface

TOBY-L2, TOBY-R2, and LARA-R2 modules include a 4-bit SDIO (Secure Digital Input Output) high speed serial interface for communicating with an external u-blox short range radio communication Wi-Fi module.

The SDIO interface is not provided by TOBY-L1, LISA, and SARA modules.

SDIO interface pins of TOBY-L2 and TOBY-R2 modules share pads on the top layer of the nested application board with **RSVD** (reserved) pins of TOBY-L1 and with SPI / I2S1 pins of LISA-U2 modules.

SDIO interface pins of LARA-R2 modules share pads on the top layer of the nested application board with analog audio pins of SARA-G350 and SARA-G340 modules, and with **RSVD** (reserved) pins of SARA-U2, SARA-G300, and SARA-G310 modules.

The pads for the SDIO pins of TOBY-L2 and TOBY-R2 modules are positioned very close to the pads for the SDIO pins of LARA-R2 in order to facilitate routing.

See the modules' system integration manuals and data sheets for application circuits and further details.

3.6 Audio interface

3.6.1 Analog audio

TOBY, LISA-U2, LARA-R2, SARA-U2, SARA-G300 and SARA-G310 modules do not provide an analog audio interface, but SARA-G340 and SARA-G350 modules do.

All the modules, except SARA-G300, SARA-G310, TOBY-L1 and the product versions "00", "01" and "60" of TOBY-L2 modules, provide digital audio interface: analog audio capability can be provided by converting the digital signal with an external audio codec. This is implemented on the nested application board for all the modules supporting digital audio, except SARA-G340 and SARA-G350. The external audio codec has DAC and ADC integrated, converting an incoming digital data stream to analog audio output and converting the microphone signal to the digital bit stream over the digital audio interface.

The analog audio interface pins of SARA-G340 / SARA-G350 modules and the digital audio interface pins of TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, and LARA-R2 modules are positioned to facilitate the routing.

The same compatible external audio circuit can be implemented, as the one shown in Figure 21:

- TOBY-L2, TOBY-R2, LISA-U2, SARA-U2 and LARA-R2 modules:
  - **I2S_TXD**, **I2S_RXD**, **I2S_WA**, **I2S_CLK** digital audio interface is routed by 0 Ω series resistors to the audio codec, which provides the digital / analog audio conversion
  - **SDA**, **SCL** I^2C interface is routed to the audio codec configurable by AT commands over I^2C
  - **GPIO6** / **CODEC_CLK** digital clock output is routed to the audio codec providing the master clock
  - Codec analog audio input lines are routed as differential pair to an external microphone, providing also the bias for the external microphone by means of a two 2.2 kΩ resistors circuit
  - Codec analog audio output lines are routed as differential pair to an external speaker
- SARA-G340 / SARA-G350 modules:
  - **MIC_BIAS** supply output is routed to bias an external microphone by means of a bridge structure created by two 2.2 kΩ and one 4.7 kΩ resistors circuit, plus an additional 1.5 kΩ series resistor
  - **MIC_GND** is routed as sense line providing the star connection to ground for microphone lines
  - **MIC_P**, **MIC_N** analog audio input lines are routed as differential pair to the microphone bias circuit with two 100 nF DC-blocking series capacitors
  - **SPK_P**, **SPK_N** analog audio output lines are routed as differential pair to an external speaker

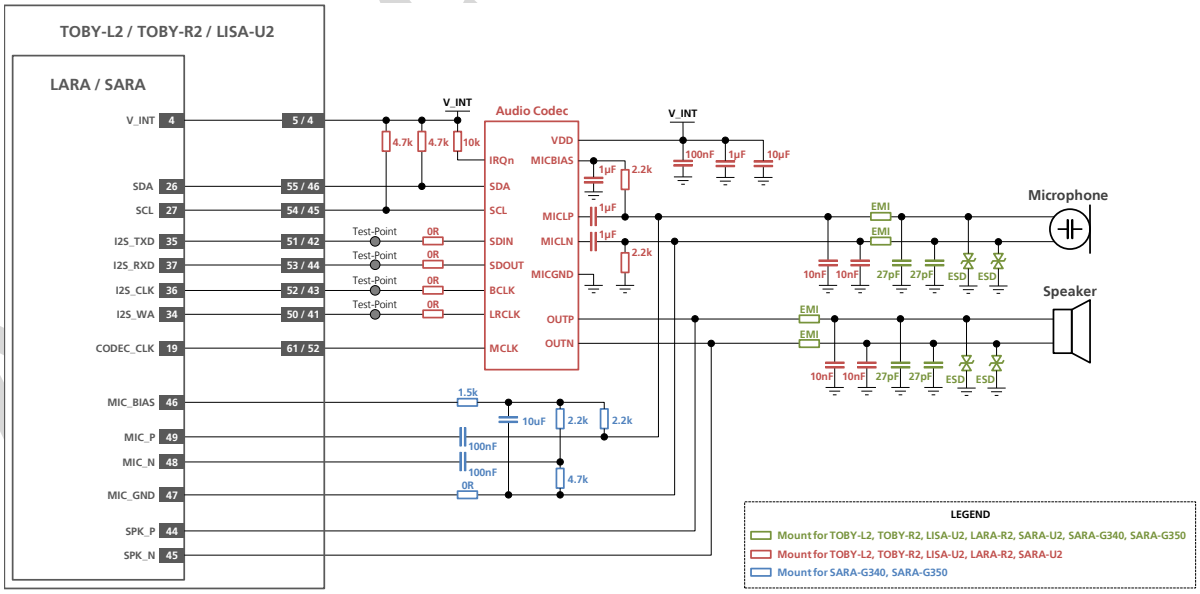


Figure 21: Compatible TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, LARA-R2, and SARA-G340 / SARA-G350 audio circuit example

3.6.2 Digital audio

3.6.2.1 First digital audio interface

All the modules, except SARA-G300, SARA-G310, TOBY-L1, and the product versions "00", "01" and "60" of TOBY-L2 modules, support digital audio.

A digital audio interface is provided on the **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA** pins of TOBY, LISA, SARA, and LARA modules, where supported by the module firmware. The same compatible external circuit can be implemented according to external digital audio device capabilities. For more details, see the module's data sheet, system integration manual and AT commands manual.

The digital audio interface pins of TOBY / LISA share the same pads on the top layer of the nested application board, which are positioned very close to the SIM pads shared by SARA / LARA modules to facilitate routing, as shown in Figure 22.

Optionally, compatibility for digital audio interface is also provided for LISA-U1 and LISA-C2 series modules.

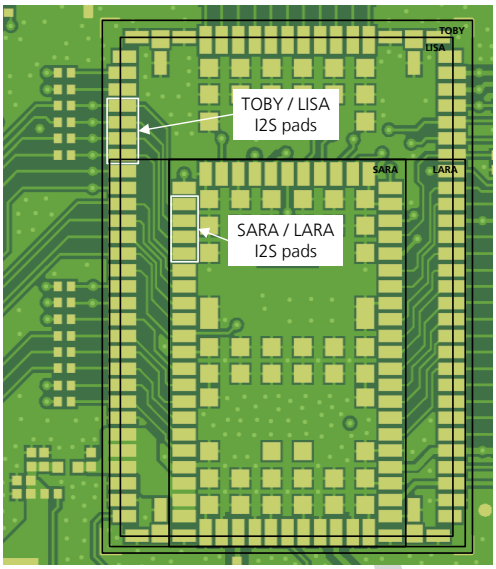


Figure 22: I²S interface pads for TOBY / LISA and SARA / LARA modules' I²S pins are positioned to facilitate routing

For further details regarding digital audio interface settings and application circuits, see the module's data sheet, system integration manual and AT commands manual.

3.6.2.2 Second digital audio interface

LISA-U2 modules provide a second I²S interface on the **I2S1_TXD**, **I2S1_RXD**, **I2S1_CLK**, **I2S1_WA** pins. On TOBY, SARA, and LARA modules the second I²S interface (I2S1) is not available.

3.6.2.3 Enabling analog audio feature on TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, LARA-R2 modules

Analog audio capability can be made available by using an external audio codec connected to the digital audio interface of TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, and LARA-R2 modules, providing digital / analog conversion and vice versa, as shown in Figure 21.

The DDC (I²C bus compatible) interface of the module can control the external audio codec. A digital clock output is provided for the external audio codec master clock. For more details on external codec integration, see the module's system integration manual, I²S interface application circuits section.

3.7 General Purpose Input/Output (GPIO)

TOBY, LISA and SARA modules provide different numbers of GPIO pins:

- TOBY-L1 modules provide 6 GPIOs (**GPIO1**-**GPIO6**), not supported by FW except for the "Wireless Wide Area Network status" indication configured on the **GPIO1**
- TOBY-L2 modules provide 14 GPIOs (**GPIO1**-**GPIO6**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**, **DTR**, **DSR**, **DCD**, **RI**), not supported by product versions "00", "01" and "60" except for the "Wireless Wide Area Network status" indication configured on the **GPIO1**
- TOBY-R2 modules provide 9 GPIOs (**GPIO1**-**GPIO5**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**)
- LISA-U2 modules provide 14 GPIOs (**GPIO1**-**GPIO14**)
- SARA-G3 modules provide 4 GPIOs (**GPIO1**-**GPIO4**), not supported by SARA-G300 / SARA-G310
- SARA-U2 modules provide 9 GPIOs (**GPIO1**-**4**, **SIM_DET**, **I2S_RXD**, **I2S_TXD**, **I2S_CLK**, **I2S_WA**)
- LARA-R2 modules provide 9 GPIOs (**GPIO1**-**GPIO5**, **I2S_TXD**, **I2S_RXD**, **I2S_CLK**, **I2S_WA**)

The same compatible external circuit can be implemented using the same function on the 1.8 V GPIOs provided by the modules.

For further details regarding the available GPIO functions / settings and application circuits, see the module's data sheet, system integration manual, and the AT commands manual.

The GPIO pins of TOBY / LISA share pads on the nested design application board, and the SARA / LARA pins are positioned to facilitate routing.

3.8 Reserved pins (RSVD)

All the modules have pins reserved for future use, marked as **RSVD**:

- TOBY-L2: **RSVD** pin **6** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- TOBY-L1: **RSVD** pins **16**, **17** and **49** should be connected to test points for direct accessibility (diagnostic),
  All the other **RSVD** pins should be left unconnected.
- TOBY-R2: **RSVD** pin **6** must be connected to GND,
  RSVD pins **18** and **19** should be connected to test points for direct accessibility (diagnostic),
  All the other **RSVD** pins should be left unconnected.
- LISA-U2: **RSVD** pin **5** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- SARA-G3: **RSVD** pin **33** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- SARA-U2: **RSVD** pin **33** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.
- LARA-R2: **RSVD** pin **33** must be connected to GND,
  All the other **RSVD** pins should be left unconnected.

4 Production guidelines

As described in Figure 2, a different stencil is needed for the production of TOBY, LISA, SARA, and LARA variants because the paste mask Gerber files are different for TOBY, LISA, SARA, and LARA (see section 4.1 to identify the different Gerber files within the delivered package).

Note that on this reference design a step stencil has been used, with the following different thicknesses:

- 150 µm stencil thickness for the USB connector and the TOBY / LISA / SARA / LARA modules
- 120 µm stencil thickness for any other component on the PCB

For more details on TOBY, LISA, SARA, and LARA handling and soldering on the nested design board, see the specific module's system integration manual.

4.1 Description of the delivered package

The delivered TOBY / LISA / SARA / LARA Nested Design Reference Design package contains three folders:

- **HS_Schematic** contains the hardware schematic (TO_R30_HS_271001 file), which has all the necessary text comments explaining the different BoM mounting options for the different hardware release variants of the nested design.
- **BM_Bom** contains the seven Bill of Materials variants (TO_R30_BM_2710x1 files, where "x" denotes the variant), available as mounting options on the same nested PCB, so that any TOBY-L1, TOBY-L2, TOBY-R2, LISA-U2, SARA-U2, SARA-G3 or LARA-R2 module can be alternatively mounted on the same nested board with all the suitable components provided in the mounting options:.
  - TO_R30_BM_2710A1 LARA-R2 series BoM mounting variant
  - TO_R30_BM_2710B1 TOBY-L2 series BoM mounting variant
  - TO_R30_BM_2710C1 TOBY-R2 series BoM mounting variant
  - TO_R30_BM_2710D1 TOBY-L1 series BoM mounting variant
  - TO_R30_BM_2710E1 SARA-U2 series BoM mounting variant
  - TO_R30_BM_2710F1 SARA-G3 series BoM mounting variant
  - TO_R30_BM_2710G1 LISA-U2 series BoM mounting variant
- **CS_Gerber** contains the Gerber files for the PCB production. Gerber files are the same for each variant, as the PCB is the same for all the hardware releases, but a different top-side stencil is needed for production because top-side soldering paste masks are different for TOBY, LISA, SARA, and LARA variants, as described in Figure 2. Paste mask Gerber files are the following:
  - 07_PASTEMASK_TOP_TOBY Top-side paste mask for variants with TOBY
  - 07_PASTEMASK_TOP_LISA Top-side paste mask for variants with LISA
  - 07_PASTEMASK_TOP_SARA Top-side paste mask for variants with SARA
  - 07_PASTEMASK_TOP_LARA Top-side paste mask for variants with LARA
  - 08_PASTEMASK_BOT Bottom-side paste mask for all the variants

☞ It is possible to mount different modules with the same BOM, intended as any other part populated on the board except the module, due to the hardware / pin compatibility within TOBY-L2 series modules (BoM variant 'B'), LISA-U2 series modules (BoM variant 'G'), SARA-G3 series modules (BoM variant 'F'), SARA-U2 series modules (BoM variant 'E') and LARA-R2 series modules (BoM variant 'A'). The provided Bill of Materials files remark any further optimization reducing the number of components required for specific modules within each series.

On this reference design a step stencil has been used, with a thickness of 150 µm for the USB connector and the TOBY / LISA / SARA / LARA modules and a thickness of 120 µm for any other component.

5 Design checklist

5.1 Schematic checklist

The following are the most important points for a check of a nested design schematic:

☑ DC supply must provide a nominal voltage at **VCC** pins within the operating range limits:
- TOBY-L1: 3.40 V min / 4.50 V max
- TOBY-L2: 3.40 V min / 4.35 V max
- TOBY-R2: 3.30 V min / 4.40 V max
- LISA-U2: 3.30 V min / 4.40 V max
- SARA-G3: 3.35 V min / 4.50 V max
- SARA-U2: 3.30 V min / 4.40 V max
- LARA-R2: 3.30 V min / 4.40 V max

☑ DC supply must be capable of supporting both the highest peak and the highest averaged **VCC** current consumption values in connected-mode, as specified in the module's data sheet:
- Considerable max average current for modules supporting LTE and/or 3G radio access technology
- Considerable max current pulses for modules supporting 2G radio access technology

☑ **VCC** voltage profile must be clean, with very low ripple/noise, providing the suggested parts to filter EMI, in particular if the application device integrates an internal antenna:
- 100 nF bypass capacitor, for any module
- 10 nF bypass capacitor for any module
- 68 pF or 56 pF bypass capacitor, with Self-Resonant Frequency ~800/900 MHz, for any module
- 15 pF bypass capacitor with SRF ~1800/1900 MHz, for any module
- 8.2 pF bypass capacitor, with SRF ~2600 MHz, for modules supporting LTE band 7 range
- 330 µF bypass capacitor, with very low ESR, for modules supporting 2G radio access technology
- Series ferrite bead for GHz band noise, for LISA-U2 and SARA-U201 modules

☑ The **VCC** and/or the **PWR_ON** and/or the **RESET_N** circuits must be capable to generate appropriate module's power-on events as summarized in Table 3

☑ The **PWR_ON** line should be driven by an open-drain/collector, with pull-up necessity as following:
- TOBY-L1: Provide external 100k pull-up to **V_BCKP** or **VCC**
- TOBY-L2: Do not provide external pull-up, as there is an internal 50k pull-up to **VCC**
- TOBY-R2: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**
- LISA-U2: Provide external 100k pull-up to **V_BCKP** or **VCC**
- SARA-G3: Provide external 100k pull-up to **V_BCKP** or **VCC**
- SARA-U2: Provide external 100k pull-up to **V_BCKP** or **VCC**
- LARA-R2: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**

☑ The **RESET_N** line should be driven by an open-drain/collector, without external pull-up necessity:

- TOBY-L1: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**
- TOBY-L2: Do not provide external pull-up, as there is an internal 50k pull-up to **VCC**
- TOBY-R2: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**
- LISA-U2: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**
- SARA-G3: Do not provide external pull-up, as there is an internal 10k pull-up to **V_INT**
- SARA-U2: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**
- LARA-R2: Do not provide external pull-up, as there is an internal 10k pull-up to **V_BCKP**

☑ The **PWR_ON** and **RESET_N** lines must be accessible (e.g. by means of test-point for LGA modules), for diagnostic purposes

☑ The **HOST_SELECT** pin of LARA-R2 modules has to be accessible (e.g. by means of test-point), for diagnostic purposes

☑ The **V_INT** output should be monitored by the application to sense the end of the switch-off routine of the module, for a safe **VCC** supply removal (see section 3.2.2 and Figure 8)

☑ The **V_INT** has to be accessible (e.g. by means of test-point for LGA modules) for diagnostic purposes

☑ The selected antennas have to provide optimal return loss (or V.S.W.R.) figure and optimal efficiency figure over all the required operating frequencies, considering that there are some differences in the operating bands frequency ranges of the modules as summarized in Figure 9

☑ Consider antenna ESD immunity precautions, as an external high pass filter, consisting of a series 15 pF capacitor and a shunt 39 nH coil (see section 3.3, and in particular the circuits illustrated in Figure 10, Figure 11 and Figure 12), may be necessary according to application requirements:

- TOBY-L1: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- TOBY-L2: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- LISA-U2: Add an external high pass filter (series 15 pF and shunt 39 nH), if the application requires reaching 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2, but mind that this will prevent the usage of the antenna detection functionally
- SARA-G3: No further precaution to ESD immunity testing is needed, as the module already provide 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2
- SARA-U2: Add an external high pass filter (series 15 pF and shunt 39 nH), if the application requires reaching 4 kV contact / 8 kV air ESD immunity rating as per IEC 61000-4-2, and note that this will not prevent the usage of the antenna detection functionally

☑ Consider antenna detection function, as an appropriate external antenna circuit (see section 3.3, and in particular the circuits illustrated in Figure 10, Figure 11 and Figure 12), may be necessary if the antenna detection functionality is required by the application:

- TOBY-L1: Antenna detection is not supported
- TOBY-L2: Implement the external antenna circuit illustrated in Figure 10 if the antenna detection functionality (not supported by '00', '01', '60' versions) is required by the application
- TOBY-R2: Implement the external antenna circuit illustrated in Figure 10 if the antenna detection functionality is required by the application
- LISA-U2: The modules are equipped with an internal circuit for antenna detection support: external components on the board are not necessary to provide the functionality
- SARA-G3: Implement the external antenna circuit illustrated in Figure 12 if the antenna detection functionality (not supported by SARA-G300 / G310) is required by the application
- SARA-U2: Implement the external antenna circuit illustrated in Figure 12 if the antenna detection functionality is required by the application
- LARA-R2: Implement the external antenna circuit illustrated in Figure 13 if the antenna detection functionality is required by the application

☑ The UART has to be accessible (e.g. by means of test-point for LGA modules) for diagnostic purposes

- TOBY-L1: Provide accessible test-points directly connected to **RSVD** pin 16 and **RSVD** pin 17 for diagnostic purposes, even if the UART is not supported
- TOBY-L2: Provide accessible test-points directly connected to all the UART pins (**TXD**, **RXD**, **RTS**, **CTS**, **DTR**, **DSR**, **DCD**, **RI**) for diagnostic purposes, in particular providing a 0 Ω series jumpers to detach each line from the DTE application processor, even if the UART is not supported by "00" modules' product versions
- TOBY-R2: Provide accessible test-points directly connected to the **TXD** and **RXD** pins and to the **DTR** and **DCD** pins for diagnostic purposes, in particular providing 0 Ω series jumpers to detach each line from the DTE application processor
- LISA-U2: Provide accessible test-points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, in particular providing a 0 Ω series jumpers to detach each line from the DTE application processor
- SARA-G3: Provide accessible test-points directly connected to the **TXD_AUX** and **RXD_AUX** pins for diagnostic purposes, in particular providing a 0 Ω series jumpers to detach each line from the DTE application processor
- SARA-U2: Provide accessible test-points directly connected to the **TXD**, **RXD**, **RTS** and **CTS** pins for diagnostic purposes, in particular providing a 0 Ω series jumpers to detach each line from the DTE application processor
- LARA-R2: Provide accessible test-points directly connected to the **TXD** and **RXD** pins and to the **DTR** and **DCD** pins for diagnostic purposes, in particular providing 0 Ω series jumpers to detach each line from the DTE application processor

☑ The UART interface of all the modules is not tolerant up to 3.0 V, so that the following topics have to be considered for the connection to a 3.0 V DTE application processor:

- it is recommended to use appropriate unidirectional voltage translators (e.g. the TI SN74AVC4T774 providing partial power-down feature so that the DTE 3.0 V supply can be also ramped up before **V_INT** 1.8 V supply), using **V_INT** as supply source for the translators on the module side
- alternatively, the voltage scaling from 3.0 V to 1.8 V can be implemented by means of a voltage divider, but consider the different values of the pull-ups integrated at each UART input of the modules (see Table 2) for the correct selection of the voltage divider resistance values
- mind that any DTE signal connected to the module must be tri-stated or set low when the module is in power-down mode and during the module power-on sequence (at least until the activation of the **V_INT** supply output of the module), to avoid latch-up of circuits and allow a proper boot

☑ The USB interface has to be designed with controlled impedance on the **USB_D+** / **USB_D-** signal lines, and the USB interface lines have to be connected on the nested board as in Figure 19 and Figure 20

☑ The USB has to be accessible (e.g. by means of test-point for LGA modules) for diagnostic purposes, if the interface is not connected to the host application processor

☑ The HSIC has to be designed with controlled impedance on the **HSIC_DATA** / **HSIC_STRB** lines

☑ The HSIC has to be accessible (e.g. by means of test-point for LGA modules) for diagnostic purposes, if the interface is not connected to the host application processor

☑ The DDC (I^2C) interface of all the modules except SARA-G3 series is not tolerant up to 3.0 V: the connection to the related I^2C pins of a u-blox 3.0 V GNSS receiver must be implemented using a proper I^2C-bus Bidirectional Voltage Translator with proper pull-up resistors (e.g. the TI TCA9406 providing the partial power down feature, so that the GNSS 3.0 V supply can be ramped up before the **V_INT** supply which has to be used as supply source for the translator on the module side)

☑ The SIM interface has to be designed providing bypass capacitor of about 22 pF to 47 pF, very close to each pad of the SIM connector, to prevent RF coupling especially in case of internal antenna

☑ ESD protections with low capacitance and series resistance have to be added on SIM lines if accessible

☑ Analog audio interface has to be designed providing the suggested passive EMI / EMC filtering parts, and the analog audio functionality should be provided on the nested board as shown in Figure 21

☑ The I^2S and GPIO3 pins of SARA-G3 modules "02" product versions onwards have to be accessible (e.g. by means of test-point for LGA modules) for diagnostic purposes, providing 0 Ω series jumpers to detach each line if connected to the application circuit

☑ All the pins reserved for future use (**RSVD**) has to be left unconnected, except:

- TOBY-L1: **RSVD** pins 16, 17 and 49 should be connected to a test point for direct accessibility
- TOBY-L2: **RSVD** pin 6 must be connected to GND
- TOBY-R2: **RSVD** pin 6 must be connected to GND
  RSVD pins 18 and 19 should be connected to a test point for direct accessibility
- LISA-U2: **RSVD** pin 5 must be connected to GND
- SARA-G3: **RSVD** pin 33 must be connected to GND
- SARA-U2: **RSVD** pin 33 must be connected to GND
- LARA-R2: **RSVD** pin 33 must be connected to GND

5.2 Layout checklist

The following are the most important points for a check of a nested design layout:

☑ The modules' footprint on the top layer of the nested board has to be designed as implemented in the available 01_TOP.art gerber file, with Non Solder Mask Defined (NSMD) pad type as implemented in the available 05_SOLDERMASK_TOP.art gerber file

☑ Four different paste masks have to be used for the top layer according to the module mounted on the top layer of the nested board, and have to be designed as implemented in the available gerber files:

- 07_PASTE_TOP_TOBY.art top-side paste mask for variants with TOBY
- 07_PASTE_TOP_LISA.art top-side paste mask for variants with LISA
- 07_PASTE_TOP_SARA.art top-side paste mask for variants with SARA
- 07_PASTE_TOP_LARA.art top-side paste mask for variants with LARA

☑ The **VCC** lines have to be designed with bypass capacitors in the picoFarad range and the additional series ferrite bead placed as close as possible to the modules' **VCC** pins, in particular if the application device integrates an internal antenna (see Figure 4)

☑ The antennas RF transmission lines have to be designed with nominal characteristic impedance as close as possible to 50 Ω (see Figure 10, Figure 11 and Figure 12)

☑ The RF and analog parts / circuits must be clearly separated from any possible source of radiated energy (primarily USB signals, high-speed digital lines and SIM signals), and must be clearly separated from any sensitive part / circuit which may be affected by EMI.

☑ The antennas terminations have to provide optimal return loss (or V.S.W.R.) figure and optimal efficiency figure over all the required operating frequencies, considering that there are some differences in the operating bands frequency ranges of the modules as summarized in Figure 9

☑ The recommendations of the antenna producer for correct antenna installation and deployment have to be strictly followed (PCB layout and matching circuitry)

☑ High and similar efficiency has to be provided for both the primary and the secondary antenna

☑ High isolation between the primary and the secondary antenna has to be provided

☑ Low Envelope Correlation Coefficient between primary and secondary antennas has to be provided: the 3D antenna radiation patterns should have radiation lobes in different directions

☑ The maximum gain of the transmitting antenna for products marked with the FCC logo (United States Federal Communications Commission) and/or the IC logo (Industry Canada) must not exceed the following limits for mobile and fixed or mobile operating configurations, according to regulatory radiofrequency radiation exposure rules:

Module	700 MHz band		750 MHz band		850 MHz band		1700 MHz band		1900 MHz band		2600 MHz band		Unit
	FCC	IC	FCC	IC	FCC	IC	FCC	IC	FCC	IC	FCC	IC	
TOBY-L100	-	-	10.7	10.7	-	-	6.57	6.57	-	-	-	-	dBi
TOBY-L200	9.8	9.8	-	-	4.3	4.3	5.5	5.5	2.8	2.8	6.0	6.0	dBi
TOBY-L201	9.8	6.7	10.2	6.9	10.0	6.7	6.8	6.8	8.5	8.5	-	-	dBi
TOBY-L210	9.8	9.8	-	-	4.3	4.3	5.5	5.5	2.8	2.8	6.0	6.0	dBi
TOBY-L280	-	-	-	-	4.3	1.0	-	-	3.4	3.4	10.8	7.8	dBi
TOBY-R202	9.7	6.7	-	-	10.0	6.7	7.9	9.3	8.5	9.1	-	-	dBi
LISA-U200	-	-	-	-	4.25	4.25	7.3	7.3	2.74	2.74	-	-	dBi
LISA-U201	-	-	-	-	4.0	0.7	-	-	3.5	3.5	-	-	dBi
LISA-U230	-	-	-	-	4.78	4.78	7.55	7.55	3.95	3.95	-	-	dBi
LISA-U260	-	-	-	-	4.88	4.88	-	-	4.08	4.08	-	-	dBi
LISA-U270	-	-	-	-	4.88	4.88	-	-	4.08	4.08	-	-	dBi
SARA-U201	-	-	-	-	3.42	0.61	-	-	1.51	1.51	-	-	dBi
SARA-U260	-	-	-	-	3.5	3.5	-	-	3.1	3.1	-	-	dBi
SARA-U280	-	-	-	-	10.0	10.0	-	-	10.3	10.3	-	-	dBi
SARA-G310	-	-	-	-	8.39	8.39	-	-	3.11	3.11	-	-	dBi
SARA-G350	-	-	-	-	8.39	8.39	-	-	3.11	3.11	-	-	dBi

☑ **USB_D+** / **USB_D-** traces should meet the characteristic impedance requirement (90 Ω differential and 30 Ω common mode) and should not be routed close to any RF line / part (see Figure 20)

☑ **HSIC_DATA** / **HSIC_STRB** traces should meet the characteristic impedance requirement (50 Ω nominal)

☑ Optimal ground connection has to be provided using as many vias as possible to connect the ground planes on multilayer PCB, adding additional vias along the RF lines, the high speed data lines and in general at the edges of the each ground area

☑ One layer of the application board should be implemented as ground plane, and all the layers should be filled with ground plane as much as possible, connecting each ground area with complete via stack down to the main ground layer of the board

Related documents

[1] u-blox TOBY-L1 series Data Sheet, Docu No UBX-13000868
[2] u-blox TOBY-L2 series Data Sheet, Docu No UBX-13004573
[3] u-blox TOBY-R2 series Data Sheet, Docu No UBX-16005785
[4] u-blox LISA-U2 series Data Sheet, Docu No UBX-13001734
[5] u-blox SARA-G3 series Data Sheet, Docu No UBX-13000993
[6] u-blox SARA-U2 series Data Sheet, Docu No UBX-13005287
[7] u-blox LARA-R2 series Data Sheet, Docu No UBX-16005783
[8] u-blox TOBY-L1 / MPCI-L1 series System Integration Manual, Docu No UBX-13001482
[9] u-blox TOBY-L2 / MPCI-L2 series System Integration Manual, Docu No UBX-13004618
[10] u-blox TOBY-R2 series System Integration Manual, Docu No UBX-16010572
[11] u-blox LISA-U series System Integration Manual, Docu No UBX-13001118
[12] u-blox SARA-G3 / SARA-U2 series System Integration Manual Docu No UBX-13000995
[13] u-blox LARA-R2 series System Integration Manual, Docu No UBX-16010573
[14] u-blox TOBY-L1 / MPCI-L1 series AT Commands Manual, Docu No UBX-13002211
[15] u-blox AT Commands Manual, Docu No UBX-13002752

All these documents are available on our homepage (www.u-blox.com).

☞ For regular updates to u-blox documentation and to receive product change notifications, register on our homepage (www.u-blox.com).

Revision history

Revision	Date	Name	Status / Comments
R01	13-Apr-2016	sses	Initial release
R02	11-Jul-2016	sses	Document applicability updated to TOBY-R200, TOBY-R201, TOBY-R202, LARA-R204 and LARA-R211 as TOBY-R2 series and LARA-R2 series modules
R03	23-Sep-2016	sses	Document status updated to Advance Information Updated Power on, GPIO and Clock Output interface description

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