A simple test for ideal memristors

Y. V. Pershin

E-mail: pershin@physics.sc.edu
Department of Physics and Astronomy, University of South Carolina, Columbia,
South Carolina 29208, USA

M. Di Ventra

E-mail: diventra@physics.ucsd.edu Department of Physics, University of California San Diego, La Jolla, California 92093, USA

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Abstract. An ideal memristor is defined as a resistor with memory that, when subject to a time-dependent current, I(t), its resistance $R_M(q)$ depends only on the charge q that has flowed through it, so that its voltage response is $V(t) = R_M(q)I(t)$. It has been argued that a clear fingerprint of these ideal memristors is a pinched hysteresis loop in their I-V curves. However, a pinched I-V hysteresis loop is not a definitive test of whether a resistor with memory is truly an ideal memristor because such a property is shared also by other resistors whose memory depends on additional internal state variables, other than the charge. Here, we introduce a very simple and unambiguous test that can be utilized to check experimentally if a resistor with memory is indeed an ideal memristor. Our test is based on the duality property of a capacitor-memristor circuit whereby, for any initial resistance states of the memristor and any form of the applied voltage, the final state of an ideal memristor must be identical to its initial state, if the capacitor charge finally returns to its initial value. In actual experiments, a sufficiently wide range of voltage amplitudes and initial states are enough to perform the test. The proposed test can help resolve some long-standing controversies still existing in the literature about whether an ideal memristor does actually exist or it is a purely mathematical concept.

Although materials and systems that show a resistive response with memory or, in other words, time non-local resistance (see Ref. [1] for a thorough review) have been known for about two centuries [2], in 1971 a particular class of two-terminal resistive devices with memory has been suggested [3]. These devices have been postulated to satisfy the following equation [3]

$$V_M(t) = R_M(q)I(t), (1)$$

where V_M and I are the voltage across and current through the particular device, and $R_M(q)$ is its resistance which depends *only* on the charge q that has flowed through the device from an initial moment of time. These devices have been given the name of "memristors" ‡.

Note that, although the name "memristor" is nowadays used liberally to indicate any resistive device with memory, the mathematical definition (1) is quite strict. In fact, it can be shown, using the theory of response functions [4], that *any* resistive element subject to a time-dependent voltage (or current) can be described by the set of equations [5]

$$I(t) = R^{-1}(x, V_M, t) V_M(t)$$
(2)

$$\dot{x} = f(x, V_M, t) \tag{3}$$

where f is some vector function of internal state variables, x, other than the charge. These are the variables that provide memory to the system, and come in various physical realizations, such as spin polarization, atomic position of defects, etc. [1].

Devices that satisfy Eqs. (2) and (3) are more aptly called "memristive" [6] to distinguish them from *ideal memristors* as those represented by Eq. (1). Of course, from a purely mathematical point of view, the devices that are described by Eq. (1) can be viewed as a subset of those described by Eqs. (2) and (3), by simply stating that the *only* state variable is the charge that flows through the device: x = q and f is then simply the current I(t) = dq/dt.

However, this seemingly innocuous mathematical reduction hides a very important *physical* question: do devices that are represented by Eq. (1) (ideal memristors) actually exist in Nature?

Researchers claiming that ideal memristors actually do exist point to the well-known consequence of Eq. (1) that the corresponding I-V curves are pinched hysteresis loops, and this has been claimed to serve as the fingerprint of ideal memristors [7, 8] (see the ideal memristor curve in Fig. 1). This argument, however, is very weak and not definitive since also other resistive devices whose memory depends on internal state variables other than the charge, do show pinched hysteresis loops (see, e.g., Ref. [1] and the memristive system curve in Fig. 1).

This fact has contributed to debates in the literature [9, 10] concerning the memristor "discovery" [11]. In addition, from the physical point of view, the present

‡ The definition of flux-controlled memristors is equivalent to Eq. (1).

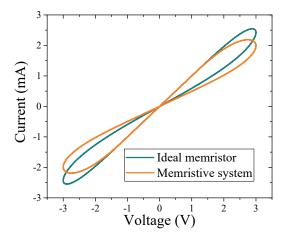


Figure 1. Current-voltage characteristics of the ideal memristor (Eq. (4) as a model for Eq. (1)) and a threshold-type memristive system (Eqs. (5) and (6) as models for Eqs. (2) and (3), respectively) driven by a sinusoidal voltage source $V(t) = V_0 \sin(2\pi\nu t)$. The plot has been obtained by using $V_0 = 3$ V, $\nu = 0.5$ kHz, $R_M(t=0) = R_{on} = R_0 = 1$ k Ω , $R_{off} = 10R_{on}$, $\alpha = 3 \cdot 10^{11}$ k Ω /C², $\beta = 10^3$ k Ω /V·s, $V_t = 1$ V.

authors [5] and others [12, 13] have identified several drawbacks of the definition (1) as a possible physically realizable device. These drawbacks include incompatibility with the symmetries of Maxwell's equations [5], violation of Landauer's principle of minimal heat generation [12, 5], and stochastic catastrophe [5].

Since the above physical flaws of a possible device represented by Eq. (1) do not seem to have settled the question posed above, in this letter we introduce a very simple test that can be done in any laboratory to *unambiguously* distinguish ideal memristors (Eq. (1)) from all other resistive switching devices (memristive systems, Eqs. (2) and (3)). For this purpose, we suggest to use a capacitor-memristor circuit as sketched in Fig. 2(a). The circuit is driven, in the simplest case, by a rectangular voltage pulse followed by zero bias (Fig. 2(b)). We emphasize that any other waveform followed by zero bias, that would cause the tested device to switch, would provide similar results.

Our main idea is based on the following duality property of the capacitor-memristor circuit: For any initial state of the memristor and any form of the applied voltage V(t), the final state of the memristor (its resistance) must be identical to its initial state, if the capacitor charge finally returns to its initial value. In practice, for any particular device subject to this test, the return into the initial state should be verified in a reasonably wide range of applied voltage amplitudes and for various representative initial states of the tested device. The test is passed if the initial and final states (the memristor resistances) are within the limits of experimental accuracy.

We also stress that the presence of an additional parasitic capacitance (typically originating from the parallel-plate geometry of the device electrodes [1]), would *not* invalidate the test we suggest. The reason is that also this capacitance will discharge by the end of the circuit evolution and, thus, the charge flowed through the memristor will

be zero, when the final state of the memristor is read. Therefore, for an ideal memristor, its final resistance (which corresponds to the state with q=0) must coincide with its initial one *irrespective* of the presence of additional parasitic capacitances (if their final charges are the same as the initial ones). Likewise, our test is valid *irrespective* of the physical mechanism that gives rise to memory.

The duality property of the capacitor-memristor circuit we discussed above is self-evident. Indeed, since the current can not flow across the capacitor, the capacitor in the circuit of Fig. 2(a) serves as a *charge-tracking* device so that the charge across the capacitor defines the instantaneous value of the memristance. In what follows we first exemplify the test by considering an ideal memristor and a threshold-type memristive system [14]. We will numerically model the test applied to the above mentioned devices and compare the test outcomes.

For the sake of definiteness, we assume that the ideal memristor is described by

$$R_M(q) = R_0 + \alpha (q - q_0)^2,$$
 (4)

where R_0 is the minimal value of R_M , α is a constant, and q_0 is used to define the initial value of R_M . Note that any other model of ideal memristor would provide similar test results.

For a typical memristive system, we instead choose the model of threshold-type memristive elements (describing physically sound, experimentally realized systems) as formulated in Ref. [14]:

$$I(t) = R_M^{-1} V_M(t) \tag{5}$$

$$\frac{\mathrm{d}R_M}{\mathrm{d}t} = \begin{cases}
\beta(V_M - V_t) & \text{if } V_t < V_M \\
\beta(V_M + V_t) & \text{if } V_M < -V_t \\
0 & \text{otherwise}
\end{cases} , \tag{6}$$

where the memristance R_M is used as the internal state variable [6], β is the switching rate, V_t is the (positive) threshold voltage. Moreover, it is assumed that the memristance is limited to the interval $[R_{on}, R_{off}]$, where R_{on} and R_{off} are the low and high resistance states of the memristive system, respectively [14].

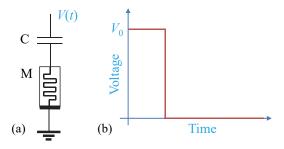


Figure 2. (a) Capacitor-memristor circuit used for the suggested memristor test. (b) The simplest form of the testing voltage V(t).

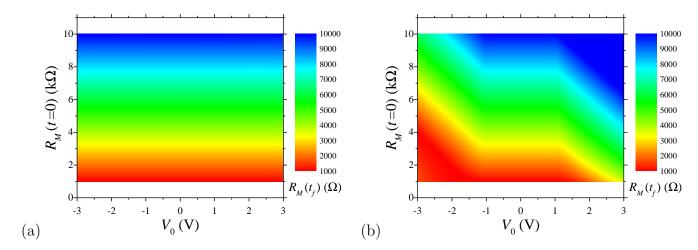


Figure 3. Map of the final states of (a) an ideal memristor and (b) a threshold-type memristive system as a function of their initial state, $R_M(t=0)$, and voltage pulse amplitude, V_0 . Parameters used in these simulations are $R_0=R_{on}=1$ k Ω , $R_{off}=10R_{on},\ V_t=1$ V, C=2 $\mu\mathrm{F},\ t_f=100$ ms and the voltage pulse width of 2 ms. The initial memristances, $R_M(t=0)$, range from 1 k Ω to 10 k Ω , and the pulse amplitudes, V_0 , range from -3 V to 3 V. Colors range from high values of final resistance (blue) to low values of final resistance (red). An ideal memristor shows the same value of final resistance as the initial one for the entire range of initial states and voltage amplitudes. Instead, a memristive element clearly shows a structure in the corresponding map.

In our numerical simulations, the circuit in Fig. 2(a) was modeled for different values of the initial memristance, $R_M(t=0)$, and pulse amplitude, V_0 . To reach (at the final moment of time) the initially uncharged state of the capacitor, a sufficiently long circuit evolution time was selected. Fig. 3 presents the maps of the final states, $R_M(t_f)$, of an ideal memristor (Fig. 3(a)) and a threshold-type memristive system (Fig. 3(b)) as a function of their initial state, $R_M(t=0)$, ranging from 1 k Ω to 10 k Ω , and voltage pulse amplitude, V_0 , ranging from -3 V to 3 V.

Figure 3(a) clearly shows that, as expected, in the case of an ideal memristor, the final and initial states of the resistance must always be the same. Therefore, an ideal memristor would pass the test we propose. On the other hand, the final states of the threshold-type memristive system strongly depend on the initial state and pulse amplitude, V_0 , and coincide with the initial states only when $-V_t < V < V_t$, namely, when the applied voltage is not sufficiently strong to switch the device resistance. Hence, the memristive system does not pass the test.

We emphasize that the plot in Fig. 3(b) depends on the capacitance C, which must be properly selected as follows. Since our test evaluates the resistance switching characteristics of tested devices, the resistance switching must occur in wide regions of the parameter space. Therefore, with regard to the choice of C, the latter should be sufficiently large to provide a suitable voltage fall across the tested device for a sufficient interval of time to induce its switching. In other words, the R_MC time must be sufficiently larger than (or on the same order of) the time it takes the device to

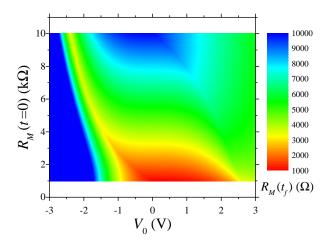


Figure 4. Map of the final states of a sinh-type memristive system. Model and calculation details are given in the text.

switch.

To further illustrate our test, we plot the map of final states found for memristive systems described by a sinh-type model of switching [15]. Here, all the calculations have been performed similarly to the above with the difference that Eq. (6) is replaced with

$$\frac{\mathrm{d}R_M}{\mathrm{d}t} = \gamma \sinh\left(\frac{V_M}{V_t}\right),\tag{7}$$

where γ is a constant and V_t is the threshold voltage. The map of final states obtained for $\gamma = 10^3 \text{ k}\Omega/\text{s}$ and $V_t = 1 \text{ V}$ is presented in Fig. 4. Similarly to Fig. 3 (b), the map contains a structure showing that Eq. (7) device is *not* an ideal memristor. This emphasizes again that only the devices described by R(q) will pass the test introduced in this work.

In summary, since a pinched hysteresis loop is not a definitive test to determine whether any resistive switching device exists that can be represented by Eq. (1) (ideal memristor), we propose a simple and yet unequivocal test that would accomplish this. Our test is based on the duality property of a capacitor-memristor circuit. This duality requires that for any initial state of the memristor (its inital resistance) and any form of the applied voltage V(t), the final state of the memristor (its final resistance) must be identical to its initial state, if the capacitor charge finally returns to its initial value. In practice, a wide enough range of initial states of the memristor and forms of the applied voltage would suffice to render this test valid.

At the moment, we are not aware of any experimental resistance switching device that can pass our test. We thus hope the test we propose will be used in all those devices that are currently classified as ideal memristors to check if that classification is indeed correct or simply serves as a rough mathematical approximation to physical systems that are actually more complex than Eq. (1) would suggest.

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