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Characterization Methods for Ultrathin Wafer and Die Quality: A Review

Michael Raj Marks, Zainuriah Hassan, *Member, IEEE*, and Kuan Yew Cheong, *Member, IEEE*

***Abstract*— Ultrathin silicon die is a key enabler for high-performance semiconductor devices and ultrathin packaging. The quality of ultrathin wafers and dies has a significant influence on packaging assembly yield and device reliability. The key quality characteristics of ultrathin wafers and dies are bow/warpage, total thickness variation (TTV), subsurface damage (SSD), surface roughness, and mechanical strength. Wafer and die bow/warpage cause handling and processing problems in manufacturing processes, and induce defects during various packaging assembly processes that eventually lead to device reliability issues. The wafer TTV requirement is becoming more stringent for new generations of thin and 3-D packages. SSD, surface roughness, and dicing defects have adverse effects on die mechanical strength and reliability. Therefore, characterization methods are needed for these quality characteristics to control the manufacturing processes for ultrathin wafers and dies to ensure good device performance and reliability. The following ultrathin wafer and die characterization techniques are discussed in this paper: noncontact bow/warp/TTV measurement, materialographic analysis with optical and electron microscopy, high-resolution X-ray diffraction, micro-Raman spectroscopy, scanning infrared depolarization, optical profilometry, atomic force microscopy, and uniaxial/biaxial bending tests.**

***Index Terms*— Bow, die mechanical strength, subsurface damage (SSD), surface roughness, total thickness variation (TTV), ultrathin die, ultrathin wafer, warpage.**

I. Introduction

SILICON die thickness plays an important role on the performance of many semiconductor devices owing to the relatively low thermal conductivity and influence on parasitic effects [1]. In semiconductor devices, die thickness limits the thermal performance because of junction heating [2]. Ultrathin dies, defined as dies having thicknesses <100 μm, operate at a substantially reduced junction temperature, and lower the junction-to-case thermal resistance significantly [3], [4]. A large fraction of the junction-to-case thermal resistance of packaged devices originate from the temperature gradient across the die thickness itself. Electrically, this reduced junction temperature leads to higher output power and efficiency. In cases where contact to ground is made through the die backside, a lower die thickness can reduce the device resistance, parasitic effects, and increase RF efficiency [3], [4].

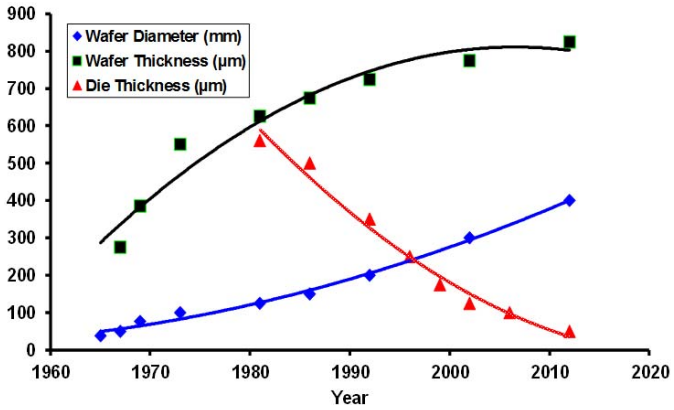

Fig. 1. Trends for wafer thickness, wafer diameter, and die thickness [10].

As electronics applications shrink in size, semiconductor packages must be reduced both in footprint and thickness. Thin silicon devices are a key-enabling factor for many advanced and emerging semiconductor packaging technology. Some advanced packages and applications requiring ultrathin dies are ultrathin packages, electronic labels, smart cards, 3-D stack packaging, and flexible electronics [5]. In 3-D stack packaging, using through-silicon-via (TSV) technology, it is possible to put more devices on the same footprint without the need to shrink the size of transistor [6], [7]. In smart card and flexible electronics, the silicon die must be able to withstand consistent mechanical stress mainly from bending. To prevent the silicon die from breaking, it needs to be flexible enough during thickness reduction [8], [9]. Fig. 1 shows the trend of decreasing die thickness in electronic packages [10].

A simplified ultrathin wafer preassembly process flow on the basis of a wafer carrier system is as shown in Fig. 2. A brief description of the process steps is as follows. Bonding to carrier: the thick wafer is temporarily bonded to a rigid carrier plate by using an adhesive. The carrier mechanically supports the wafer throughout the thinning process and maintains the flatness. The active frontside of the wafer is protected by the adhesive from mechanical and chemical damage during backgrinding and postgrinding treatment. Mounting to dicing tape: the thin wafer and carrier stack is mounted on a dicing tape. Debonding from carrier: the thin wafer is detached

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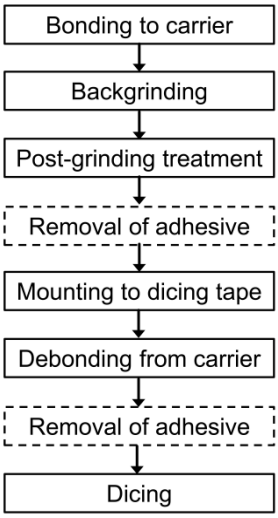

Fig. 2. Simplified ultrathin wafer preassembly process flow.

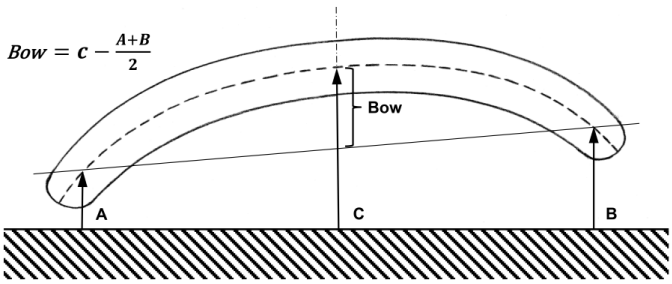

Fig. 3. Definition of bow.

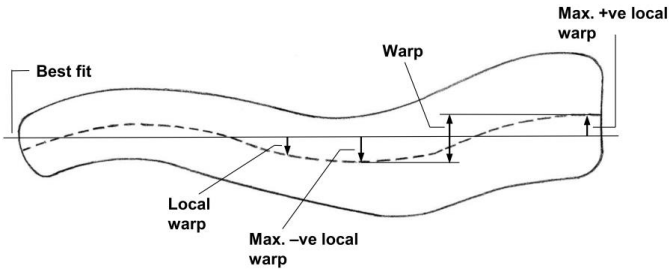

Fig. 4. Definition of warp.

from the carrier by melting the adhesive, or by separating a release layer on the carrier surface through laser heating or mechanical means. The thin wafer remains constantly supported by the dicing tape on a vacuum chuck. Removal of adhesive: residual adhesive on the wafer surface is removed. The adhesive removal could be carried out by solvent cleaning before dicing tape mounting, or by mechanical peeling after carrier debonding, depending on the type of carrier/adhesive system.

There are three commercialized temporary wafer bonding/debonding and adhesive systems for ultrathin wafer handling in the market: 3M's Wafer Support System (WSS) [11], Brewer Science, Inc.'s WaferBOND HT10.10 [12], and Thin Materials AG's T-MAT [13].

The key quality characteristics of ultrathin wafers and dies are bow/warpage, total thickness variation (TTV), subsurface damage (SSD), surface roughness, and mechanical strength. Ultrathin wafers with high bow/warpage cause wafer handling and processing difficulties in manufacturing processes [21], [22]. High bow/warpage also causes packaging assembly process defects during wafer dicing, flip-chip bonding, die attach, and wire bonding which subsequently lead to reliability issues [6], [8], [19], [23]–[26]. The TTV requirement for wafers is becoming more stringent for new generations of thin and 3-D packages [6], [80]. SSD and surface roughness induced by the wafer-backgrinding process lower the die fracture strength and reliability [14], [15]–[18], [47]–[54]. Die sidewall defects induced by the dicing process also reduce the die fracture strength and reliability [5], [79]–[91]. Therefore, characterization methods are needed for all these quality characteristics to optimize and control the manufacturing processes for ultrathin wafers and dies. With these characterization methods, good process quality, device performance, and reliability can be assured.

This paper presents a review of ultrathin wafer and die quality characterization methods for bow/warpage, TTV, SSD, surface roughness, and mechanical strength. Such a comprehensive review is needed to appreciate the interdependencies between the various characteristics of ultrathin wafers and dies along the manufacturing process chain. To our knowledge, there is no similar comprehensive review being reported. The principles and applications of these characterization methods on ultrathin silicon wafers and dies will be discussed.

II. Characterization of Ultrathin Wafer and Die Quality

A. Bow, Warp, and TTV

The abrasive removal of silicon during backgrinding leads to a layer of damaged silicon crystal structure which has high compressive stress [15]–[18]. Metallization deposition on the wafer backside induces large tensile stresses. On the other hand, the active layers on the frontside of the wafer are mainly under tensile stress. The combined effect of these residual stresses acting on the backside and frontside of the wafer results in wafer bow or warp.

Bow and warp have different definitions [27], [28]. Bow is how concave or convex the deformation of the median surface of a free, unclamped wafer/die is at its center point (Fig. 3). Warp is the difference between the maximum positive and maximum negative distances of the median surface of a free, unclamped wafer/die from the least squares fit plane of the median surface (Fig. 4). A Japanese variant of warp, sori, is the difference between the maximum positive and maximum negative distances of the front surface of a free, unclamped wafer/die from the least squares fit plane of the front surface. There is a very small difference between warp and sori, depending on TTV [29].

TTV of the silicon wafer, is defined as the difference between maximum thickness and minimum thickness within the area of the wafer. TTV is an important indication of system performance of the wafer temporary bonding/debonding system because silicon wafers are ground with reference to the

TABLE I
SUMMARY OF SILICON WAFER BOW/WARP/SORI/TTV MEASUREMENT METHODS FROM VARIOUS SEMI STANDARDS

Wafer shape test type	Test method reference	Applicable wafer diameter & thickness	Wafer support method	Measurement probe type/Location of measurement	Gravity cancellation method
Bow	SEMI MF534-0707 [27]	Diameter ≥ 25 mm Thickness ≥ 180 µm Diameter/Thickness ratio ≤ 250	Three-point support	Contact probe/Center of wafer surface	-
Warp, TTV	SEMI MF657-0707 [28]	Diameter 50-200 mm Thickness ≥ 100 µm	Three-point support	Opposed pair of non-contact probes/Selected points along a scan pattern	Three methods proposed
Sori	SEMI MF1451-0707 [29]	Diameter ≥ 50 mm Thickness ≥ 100 µm	Small-area chuck	Opposed pair of non-contact probes/Selected points along a scan pattern	Three methods proposed
Warp	SEMI MF1390-0707 [30]	Diameter ≥ 50 mm Thickness ≥ 100 µm	Small-area chuck	Opposed pair of non-contact probes/Selected points along a scan pattern	Three methods proposed
Flatness, Thickness, TTV	SEMI MF1530-0707 [31]	Diameter ≥ 50 mm Thickness ≥ 100 µm	Small-area chuck	Opposed pair of non-contact probes/Selected points along a scan pattern	-

carrier surface on the opposite side of the bonded silicon wafer. The industry requires even better TTV as packaging technologies for 3-D stacking advances and TTV of below 1–2 μm, is being sought [6], [80].

Apart from the contribution of wafer residual stresses to wafer bow/warp, another aspect is the gravitational force on unsupported thin wafers in wafer cassettes. As final thickness is decreased, the wafer becomes progressively less able to support its own weight. A thin wafer supported along the edges in a wafer cassette has a different shape and form compared with one that is laying on a flat surface due to gravity-induced deflection [9].

Wafer bow/warp needs to be minimized in thin wafer production because manual and automatic handling of deformed wafers during processing is difficult or even impossible. Wafer bow/warp and the wafer mechanical strength directly affect handling of thin wafers. Wafer bow/warp increases significantly while its mechanical strength decreases significantly with the reduction of wafer thickness [8], [15], [19], [21]. As wafer thickness is reduced to $<$100 μm, the gravity-induced wafer deflection becomes very high and handling of these ultrathin wafers by using conventional wafer handling methods becomes very challenging. Therefore, a rigid wafer support system is required to handle ultrathin wafers in the wafer fabrication and packaging assembly processes [21], [22]. High wafer bow/warp due to residual stresses also increases the risk of die chippage and cracks during the wafer dicing process, thus, weakening the mechanical and electrical properties of the singulated die [40].

Any stress-induced bow/warp at wafer level will translate to bow/warp at die level after the wafer dicing process (Fig. 5). The amount of the die bow/warp depends on the product, its active layers, and the die size. Major challenges are faced in the packaging assembly processes of ultrathin dies associated with bow/warp. The attachment of ultrathin dies onto substrates by flip-chip bonding can result in uneven gaps between the solder bumps and pads on the substrate due to bow/warp, which would cause nonuniform solder joint

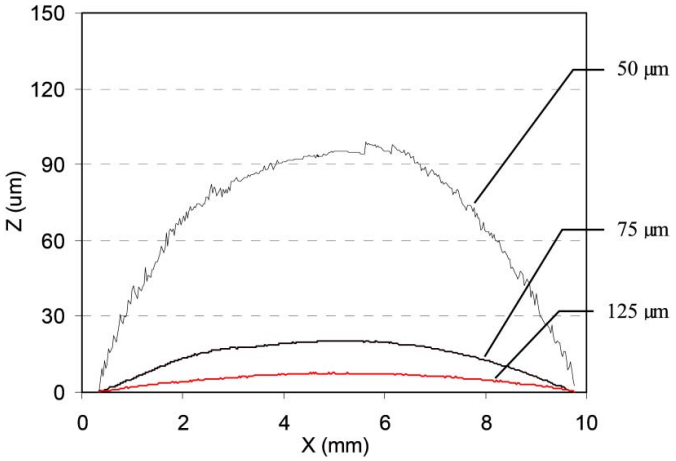

Fig. 5. Optical surface profile of 10 × 10 mm silicon dies with various thicknesses [8].

connections and open failures [6], [8], [19], [23]. In conventional die attachment using solder or epoxy adhesive, die bow/warp will lead to nonuniform bond-line thickness and die attach voids, which can result in die cracks owing to high stress concentrations in the silicon at the edges of the voids [24], [25]. In severe bow/warp cases, this can cause an overhanging of the die edges making wire bonding at peripheral bond pads impossible owing to lack of support at the bottom of the ultrathin die [26].

1) Wafer Bow, Warp, and TTV Measurement: Table I shows a summary of silicon wafer bow/warp/sori/TTV measurement methods from various Semiconductor Equipment and Materials International (SEMI) standards. The wafer thickness requirement is 100 μm and above and therefore these methods are not applicable for ultrathin wafers. In the ultrathin wafer manufacturing flow, the SEMI methods are recommended for monitoring bow/warp/sori/TTV of wafers in process steps before the wafers are bonded on rigid carriers for thinning. Once a wafer is bonded on a rigid carrier, the

wafer cannot be measured as a free and unclamped body, and measurement of wafer bow/warp/sori is not possible. However, monitoring of residual stress induced in a wafer because of the backgrinding and postgrinding treatment processes on rigid carrier could be done indirectly by measuring the bow/warp of ultrathin dies. Measurement methods for ultrathin die bow/warp will be discussed in the next section.

The TTV of ultrathin wafers that are thinned on rigid carriers depends significantly on how parallel the bonded wafer surface is related to the carrier surface. If the wafer has an excessive bow/warp before bonding on a carrier, the wafer surface may not be bonded completely parallel to the carrier surface due to the limitation of the carrier bonding process and tool. This will result in a higher TTV after backgrinding. Wafer bow/warp, owing to residual stresses from the active layers on the wafer frontside, should be minimized not only to improve the TTV of ultrathin wafers, but also to improve the bow/warp of ultrathin dies. Therefore, it is important to monitor and control the bow/warp of wafers before bonding to carriers.

Because of the low stiffness of silicon wafers, bow/warp/sori/TTV measurement accuracy is affected by the method of supporting the wafer and gravity [32], [33]. SEMI has recommended bow/warp/sori/TTV measurement methods using a three-point support or a small-area chuck support to minimize the contact area of the support system to the wafer [27]–[32]. The disadvantage of these types of support is that gravity strongly influences the results. SEMI has proposed three gravity cancellation methods [28]–[30] based on the principles of reference wafer inversion, sample wafer inversion, and theoretical modeling. New wafer support methods to minimize gravity-induced deflection during bow/warp/sori measurement have been developed by other workers. Kuroda Precision developed a vertical support system to minimize gravity effects [34]. The wafer is supported at three positions at the periphery and rotated during the measurement. However, wafer position shift during measurement and wafer distortion due to clamping force cause inaccuracies in warp/sori measurements. Natsu *et al.* [34] proposed a new warp/sori measurement method using a horizontal three-point support on the vertices of a equilateral triangle at the wafer edge. Gravity cancellation by wafer inversion method was applied. It was found that the three-point support method has better repeatability and antivibration ability than that of a one-point support method. The precise positioning of the supports is crucial to obtain accurate sori results. Moreover, Natsu *et al.* [34] reported a dependency of the maximum gravity-induced deflection on the crystal orientation of the wafer. Dunn *et al.* [33] developed a wire support methodology consisting of a series of very thin wires. It was reported that the wire support substantially reduced bow and warp induced by gravity, and was able to significantly reduce the wafer-to-wafer variance in bow and warp measurements compared with a three-point support.

Noncontact measuring methods for bow and warp are recommended for silicon wafers, because methods requiring physical contact will cause deflection of the wafer because of its low stiffness. A noncontact probe measures the distance between probe and wafer surface by using capacitance, optical, or other noncontact sensors [28]–[30]. Noncontact probes based on capacitance sensors are mostly used owing to its high measurement resolution of 0.1 μm at a fraction of the cost of other high-performance sensors [36], [37]. In the SEMI methods for measuring warp/sori, both wafer surfaces are simultaneously scanned along a prescribed pattern by an opposed pair of probes [28]–[30]. The distances between each probe and the nearest surface of the wafer are determined in pairs at intervals along the scan pattern. This data is then used in the calculations for warp/sori and gravity cancellation. Most instruments used for bow and warp measurements will also provide measurements of the wafer flatness, thickness, and TTV, which are bulk properties of the wafer not influenced by wafer deflection [31], [36], [37]. The accuracy of bow/warp/TTV measurement systems are constrained by the resolution of the noncontact sensor and the limited number of data points on the wafer with extensive interpolation. Commercial measurement systems using capacitive sensors typically have a ± 2 μm bow/warp accuracy and a ± 0.25 μm TTV accuracy [36], [37].

Optical interferometry technology can improve the accuracy of the bow/warp/TTV measurements to ± 0.05 μm, because it enables full wafer characterization with a measurement resolution of 0.015 μm at a spatial resolution <1 mm [33]. Phase-measuring infrared interferometers operating at a wavelength of 1550 nm are typically used for measuring thickness and TTV of low-doped silicon wafers [38], [39]. The Fizeau or Haidinger interferometer configurations are used for wafers which are polished on both sides, but the Twyman-Green configuration is used for nonpolished wafers [38], [39]. As thickness and TTV measurements of silicon wafer with infrared interferometry require light to be transmitted through the silicon and reflected from both the front and back surfaces, this method has the disadvantage that it cannot be applied for high-doped silicon, and for wafers with reflective layers on both sides.

Computer-aided reflection moiré has gained popularity for wafer bow/warp measurements because of its relatively fast full-field measurement, compared with current optical point-by-point measurement methods [40], [41]. Another advantage of this method is the simple equipment setup and easy implementation. The main disadvantage of this method is the requirement for a specular reflection of the wafer surface. In reflection moiré, a sinusoidal pattern of horizontal and vertical gratings is generated and displayed on a liquid crystal display. A beam-splitter is used to project the grating onto the wafer surface. The image of the grating reflected from the wafer surface is captured using a charge-coupled device camera. The reflected grating images from the specular wafer surface in deformed and reference states are superimposed to create a moiré pattern which is analyzed with a phase-measuring algorithm. This pattern provides the information on the out-of-plane slope. Reflection moiré has an out-of-plane resolution of <0.15 μm but the spatial resolution (0.25 mm for 8-in wafer) is low because the entire wafer is imaged in a single shot [41].

2) Die Bow/Warp Measurement: Ultrathin wafers need to be supported on rigid carriers during thinning and mounted on tape during dicing. As the wafer is mechanically constrained on the carrier or tape, wafer bow/warp measurement is not applicable anymore. However, once the ultrathin wafer has been diced, it will be possible to detach individual dies from the dicing tape for bow/warp measurements. Monitoring of combined residual stresses induced in ultrathin wafers due to active layers on the wafer frontside, and due to backgrinding and postgrinding treatment on the wafer backside, is possible indirectly through bow/warp measurement of ultrathin dies. Bow/warp control for ultrathin dies is necessary to ensure the manufacturability and reliability of the dies as discussed in Section II-A.

Noncontact optical profilometry methods by confocal imaging and interferometry can be used to measure the bow/warp of ultrathin dies [42]. A confocal microscope has a spatial resolution of <0.15 μm while the out-of-plane resolution is <1 nm with a $150\times$ objective lens. Phase-measuring and white-light interferometry can achieve a spatial resolution of <0.25 μm and an out-of-plane resolution of <1 nm with an objective lens of $100\times$. Confocal imaging and interferometry require vertical and in-plane scanning of the sample.

Temperature-dependent warpage is an important issue for the manufacturing yield and reliability of ultrathin dies. For example, ultrathin dies will warp during flip-chip bonding, die attach soldering, or die attach adhesive curing due to mismatch in the coefficients of thermal expansion (CTE) of the different materials in the die. The die warpage will result in quality and reliability issues as discussed in Section II-A. There is a need to characterize variations in the die warpage during a temperature excursion, and to find solutions for minimizing the warpage. Confocal and interferometry methods are not suitable for dynamic temperature-dependent measurements because the time delay caused by sample scanning cannot cope with the rapid temperature ramp rate.

Noncontact, full-field optical methods, that is, shadow moiré, fringe projection, and digital image correlation (DIC), have been used for real-time temperature-dependent warpage measurements of electronic components [43]–[46]. In temperature-dependent measurements, samples are uniformly heated in an enclosed chamber with a transparent quartz window [43], [44]. The temperature range can be set from room temperature up to 300 °C with a programmable ramp rate. These methods could be explored for ultrathin dies. Shadow moiré uses geometric interference between a reference grating and its shadow on a sample to measure out-of-plane displacement at each pixel position in the resulting interference pattern image. In fringe projection, a fringe pattern is projected onto a sample surface through a set of projection lenses. A camera above the sample acquires the distorted fringe patterns, which are then used to calculate the out-of-plane displacement at each pixel position from its reference plane. In DIC, the sample surface is viewed through two cameras at different angles. A software identifies the same random pattern on the sample surface from both camera perspectives using pattern recognition within a small pixel window. Using stereo triangulation, the spatial position of the pixel window can be determined and is used to calculate the in-plane and out-of-plane displacements. Pan *et al.* [43] found that shadow moiré has better out-of-plane resolution for large samples (>10 mm), whereas fringe projection is better for small samples (<10 mm), and DIC is recommended where in-plane strain is important. Ding *et al.* [45] similarly concluded that fringe projection has better out-of-plane resolution when used to measure small samples.

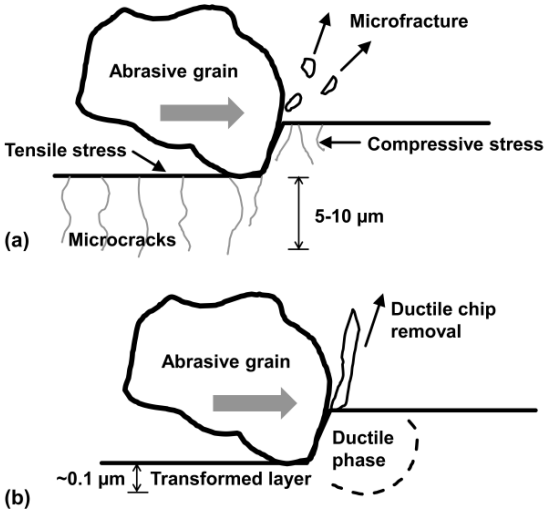

Fig. 6. Silicon removal mechanisms. (a) Brittle mode. (b) Ductile mode [18].

One potential issue in using shadow moiré, fringe projection, and DIC for warpage measurement of ultrathin dies is the need to coat the sample surface with a thin layer of high-temperature white paint to increase the signal-to-noise ratio. The thickness, stiffness, and CTE of this coating could have an influence on the warpage behavior of ultrathin dies. Therefore, thermomechanical properties of various types of coating material need to be evaluated, as well as the methods of application to minimize the coating thickness.

B. Subsurface Damage

Backgrinding is the standard method for wafer thinning and today's production limit for grinding reduces wafers from an average starting thickness of 725 μm to less than 10 μm. One of the biggest issues for ultrathin dies is die fracture during packaging assembly, reliability testing, or field application. Many studies of die mechanical strength have attributed low fracture strength to SSD in silicon induced by the backgrinding process [15]–[18], [47]–[54]. Ductile and brittle modes of grinding can happen in single crystal silicon and the transition between them can be controlled by changing the machining conditions [18]. Fig. 6 shows the brittle and ductile silicon removal mechanisms using an abrasive grain. The preferred regime in which silicon removal and deformation takes place is the ductile mode.

From investigations by Hadamovsky [50] and Gert *et al.* [51], two models to characterize the surface integrity of machined single crystals have been proposed (Fig. 7). The subsurface regions shown in Fig. 7 consist of polycrystalline layer, a region of microcracks, dislocations,

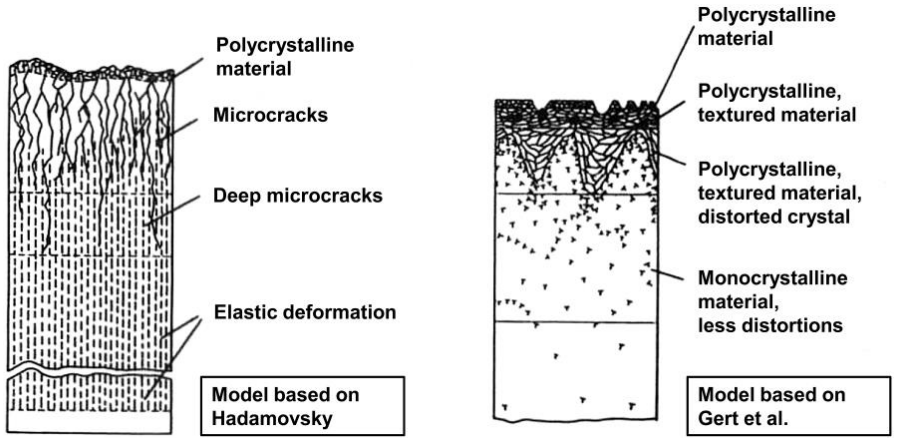

Fig. 7. Models of SSD [50], [51].

and residual stresses. Different types of damaged surface layers occur depending on the mechanical treatment, size of abrasive, and other factors. The depth of damaged surface varies approximately from 1 to 50 μm [48]. The Hadamovsky model has a better agreement with observed SSD in single crystal silicon induced by the backgrinding process [15]–[18], [47]–[54]. Microcrack configurations caused by indentation and grinding of silicon have been studied and documented by various workers [18], [52]–[54].

Many techniques have been developed to observe and measure SSD in silicon wafers. These techniques can be classified into destructive evaluation and nondestructive evaluation methods.

1) Destructive Evaluation Methods: Destructive techniques require the localized area of the specimen or the entire specimen to be mechanically and/or chemically prepared using appropriate procedures before the actual SSD observation or measurement.

Many of the techniques used by SSD investigators [18], [53], [54] are based on the principles of materialography [59], which is the science and art of preparing a material surface for analysis by grinding and polishing, and chemical etching to reveal the structure of the specimen. Materialographic techniques generally involve precision polishing of the specimen to the plane of interest, either at a perpendicular angle or at a low angle (Fig. 8) to geometrically enlarge the depth dimension of the SSD. Once the plane of interest has been reached, a chemical polishing or chemical etching step is required to reveal the SSD structure. Young *et al.* [18] and Gao *et al.* [54] employed low-angle cross sections to study the effects of various wafer grinding parameters on the structure and depth of subsurface cracks. Planar polishing and etching of the wafer surface could be done using similar to the materialographic procedures that used for cross-sectional specimens to study the lateral SSD morphology and distribution on the wafer surface [18]. The observation and size measurement of the SSD are normally done with a high-power optical microscope or a scanning electron microscope (SEM) when higher imaging resolution is needed.

The resolutions of high-power optical microscopy and the SEM are limited to observing microcracks in the SSD layer.

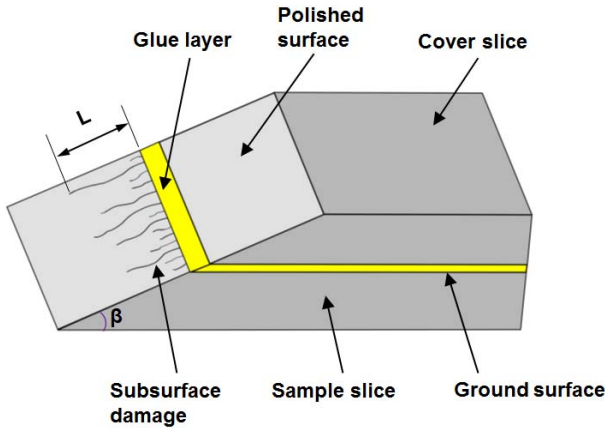

Fig. 8. Principle of low-angle materialography [54].

To observe crystalline defects in the SSD layer such as lattice disorders and dislocation defects, transmission electron microscopy (TEM) is required. Fig. 9 shows an SSD layer with polycrystalline structure and dislocation defects. Reiche and Wagner [16], Draney *et al.* [20], and Halahan *et al.* [47] showed using TEM analysis that even after fine grinding of silicon wafers, crystal damage from the previous course grinding could not be completely removed. Chen *et al.* [68] used TEM to confirm the presence of dislocations and stacking faults in the SSD layer after fine grinding of silicon wafers. Sandireddy and Jiang [100] compared various silicon wafer-thinning techniques and found by TEM measurements that the SSD depths after backgrinding, backgrinding + poligrind, and backgrinding + chemical–mechanical polishing (CMP) were 0.2, 0.1, and 0 μm, respectively.

TEM sample preparation by using focused ion beam (FIB) significantly simplifies and shortens the time for the sample preparation procedure compared to conventional TEM sample preparation techniques [60]. Another advantage of using FIB is the ability to precisely select a sample location for TEM analysis. Li *et al.* [88] used FIB extensively for TEM sample preparation to analyze the sidewall damage of ultrathin dies after blade dicing and laser dicing, and subsequent XeF_2 dry etching to remove the sidewall damage.

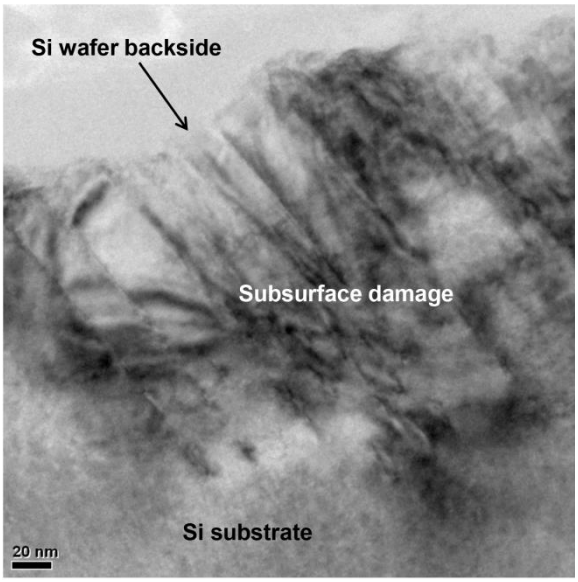

Fig. 9. SSD layer after fine grinding as shown by cross-sectional TEM.

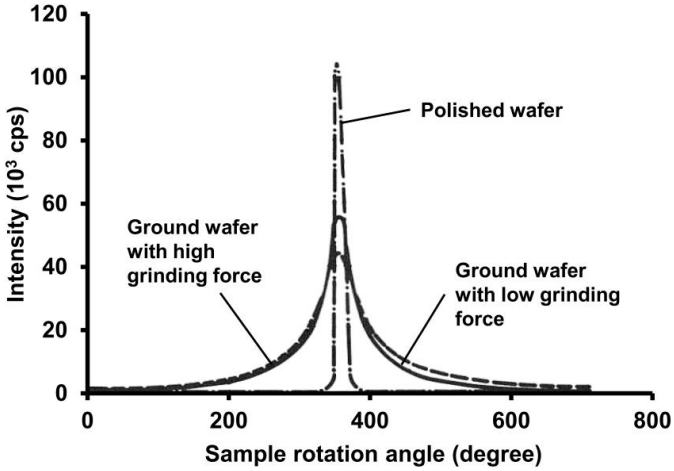

Fig. 10. High-resolution XRD patterns of polished and ground silicon wafers [48].

2) Nondestructive Evaluation Methods: It is advantageous to have nondestructive evaluation methods to characterize SSD as there is none or little sample preparation required and the specimen remains intact for other types of analysis.

a) X-ray diffraction: X-ray diffraction (XRD) is a nondestructive method to determine residual stress from lattice deformation of a crystal. A crystal lattice is a regular 3-D distribution of atoms in space. When incident X-rays approach at a particular angle, they are reflected specularly from different planes of crystal atoms. For a particular set of planes with interplanar spacing d, the reflected waves is only observed if Bragg's condition is met for constructive interference [61]. Plastic deformation occurs in the SSD layer because of cracking and local elastic expansion or contraction of the crystal lattice [48]. As such, elastic strain is produced in the crystal lattice. Using elasticity theory, these strain components can be converted into stress values. The lattice constant change in a silicon SSD layer is detectable by a high-resolution X-ray diffractometer [48]. This type of diffractometer consists of a four-crystal monochromator that produces a highly parallel and monochromatic incident beam so that a high resolution of XRD can be achieved. Micro-XRD technology is capable of small analysis in areas up to 10 μm in diameter, owing to improvements made in the measurements by optical systems, detectors, and high-intensity X-ray sources [62], [63].

Bismayer *et al.* [48] found that the penetration depth of X-ray into silicon is 30–60 μm for conventional Bragg diffraction. Different peak positions and full-width at half-maximum (FWHM) values occur owing to residual stresses and damage of the silicon lattice [48]. The XRD peak of ground silicon wafers measured with CuK_α radiation showed an increased FWHM compared with that of polished silicon wafers (Fig. 10).

b) Raman spectroscopy: Raman spectroscopy is a nondestructive technique for analyzing residual stress and phase transformation in a crystal. When photons are scattered from a molecule, most photons are elastically scattered, that is, most of the scattered photons have the same frequency and wavelength as the incident photons. However, few photons are scattered at optical frequencies different from, and usually lower than, the frequency of the incident photons, ω_i. This inelastic scattering of photons is called the Raman effect [64]. Inelastic scattering by the lattice vibrations, the phonons of the crystal with frequency $\omega_{\rm ph}$, leads to a shift of the excitation line according to $\omega_s = \omega_i \pm \omega_{\rm ph}$, where ω_s is the scattered beam frequency. The signs $-$ and $+$ represent Stokes and anti-Stokes processes, respectively. Microscopic changes (long- and short-range disorders), impurities and residual strains strongly influence the Raman spectrum of a material.

Micro-Raman spectroscopy can achieve a spatial resolution of 1 μm by focusing a monochromatic laser beam through an optical microscope [48], [65]–[68]. The scattered photons are then focused with a lens on the entrance slit of a spectrometer. Sparks and Paesler [70] found that the light penetration deep into silicon changes with different excitation wavelengths. Verhey *et al.* [65] reported an analysis depth range of 1–40 μm in silicon depending on the wavelength. Thus, it is possible to probe different depths of the silicon sample by varying the wavelength.

Bismayer *et al.* [48] studied the stress-depth profiles of ground silicon wafers with micro-Raman spectroscopy. Compared with polished silicon, different Raman peak positions and FWHM were observed for ground silicon attributed to SSD (Fig. 11). The peak shift to higher frequencies is caused by compressive stresses in the wafer surface related to the Gruneisen effect [48]. The broadened line shape with FWHM $= 16.5$ cm^{-1} can be explained by the density of states effect of a polycrystalline layer with grain size of 6–10 nm, according to the calculations by Fauchet and Campbell [71].

Sparks and Paesler [70] found that a Raman peak shift of 1 cm^{-1} in crystalline silicon corresponds to a stress of 250 MPa. The ability of micro-Raman spectroscopy to measure residual stresses in silicon was further demonstrated by Srikar *et al.* [72] and Jeon *et al.* [106], where the relationship between uniaxial (σ_{xx}) or biaxial stress ($\sigma_{xx} + \sigma_{yy}$) in the

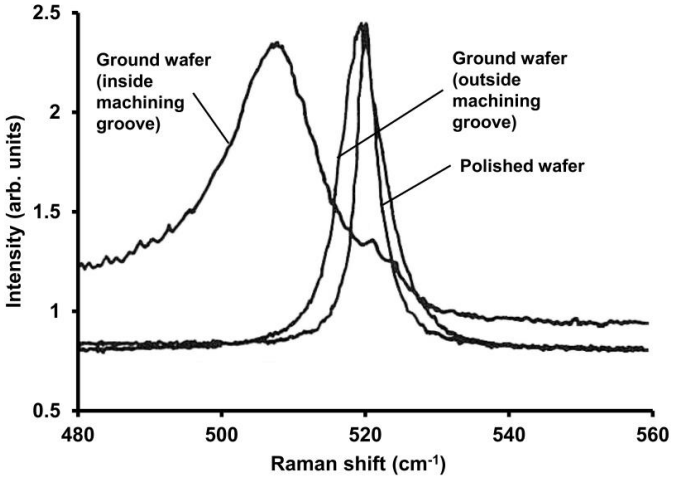

Fig. 11. Raman peaks of polished and ground silicon wafers [48].

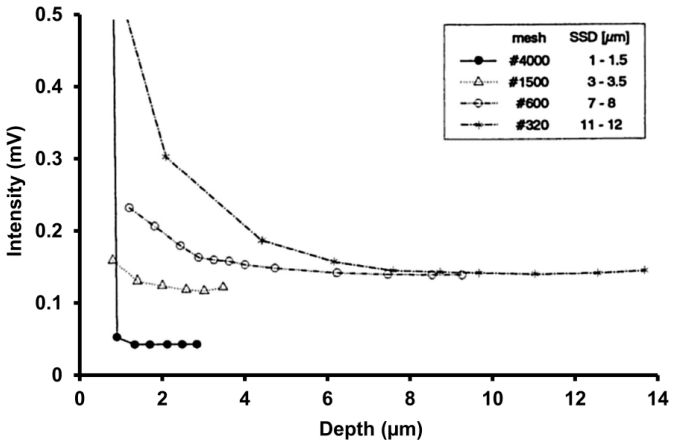

Fig. 12. Depolarization decay curves for ground silicon wafers [49].

(100) plane and the Raman scattering frequency was found to be as follows:

$$\sigma_{xx} \cong -434\Delta\omega \tag{1}$$

$$\sigma_{xx} + \sigma_{yy} \cong -434\Delta\omega \tag{2}$$

$$\Delta\omega = \omega_s - \omega_o \tag{3}$$

where σ_{xx} is the residual stress and expressed in unit of MPa, $\Delta\omega$ is the Raman shift as expressed in (3), ω_s is the measured Raman frequency from the experiment, and ω_o is the silicon's Raman peak. Compressive stress will result in an increase of the measured Raman frequency, whereas tensile stress will result in a decrease.

Micro-Raman spectroscopy has been widely used for nondestructive SSD studies in silicon wafers. Verhey *et al.* [65] and Chen *et al.* [68] observed that the peak shifts and line broadening in ground silicon wafers were reduced or eliminated by chemical etching of the SSD layer. Chen *et al.* [68] found that Raman spectroscopy is very sensitive to residual stresses rather than to microcracks induced by wafer grinding. Yan [69] detected the presence of amorphous silicon and residual stresses in silicon wafers machined by single-point diamond. Takyu *et al.* [90], [97] compared the stress-depth profiles in ultrathin silicon wafers subjected to various wafer-thinning methods.

c) Scanning infrared depolarization: Scanning infrared depolarization (SIRD) can be applied to measure SSD qualitatively. The stress due to the damaged surface layer of the silicon induces birefringence in the silicon crystal [49]. This stress can be visualized by examining silicon wafers between cross polarizers by using infrared laser beam. A helium–neon laser beam with a wavelength of 1152 nm is transmitted through the wafer to measure the depolarization due to SSD. The wafer is located between a pair of crossed polarizers and a pair of quarter wave plates. The quarter wave plates were employed to obtain circularly polarized light to determine the depolarization without depending on the angle between the plane of polarization of the incident beam and the wafer orientation. From the measured light intensities, the depolarization $DP = L_c/L_p$ can be calculated, where L_c is the light intensity with crossed polarizers, and L_p is the light intensity with parallel polarizers. The amount of depolarization of the laser beam is a qualitative measure of the SSD. A damage map can be generated by scanning the wafer with the laser beam at a spatial resolution of 1 mm.

As the infrared beam needs to be transmitted through the silicon sample, the application of SIRD is limited to low-doped silicon and samples without reflective layers on the front and back surfaces. The depth of the SSD cannot be determined directly by SIRD. To investigate a depth profile of the SSD, the sample has to be chemically etched is steps, with depolarization measurement taken after each etching step. Unfortunately, this becomes a destructive evaluation. Lundt *et al.* [49] investigated the effects of diamond abrasive mesh size on grinding wheels on the SSD depth in silicon wafers by using SIRD (Fig. 12). It was found that the SSD depth decreases with smaller abrasive size, and that it is possible to minimize the SSD depth below 1 μm.

d) Other nondestructive methods: There are other nondestructive evaluation techniques for SSD that are still at experimental and development stages. These are briefly discussed here.

Zhang *et al.* [55] developed a laser scattering system to measure subsurface cracks in grounded silicon wafers. When a laser beam is focused on the surface of a silicon wafer, it can penetrate beneath the surface for a certain depth. Zhang and Sun [56] found that the depth of penetration in silicon was increased from 9 to 120 μm by increasing the laser wavelength from 630 to 900 nm. The basic principle of laser scattering technology is that subsurface cracks cause a random polarization of the scattered/reflected light, and this is detected using polarizing beam-splitters. Laser scattering has the potential to be a high-resolution and full-wafer method for measuring the spatial and depth distributions of subsurface cracks in silicon wafers.

Karabutov and Podymova [57] studied the depth of SSD in silicon by using laser-induced ultrasonic signal. This method is based on the different mechanisms of laser generation of ultrasonic signal in undamaged and damaged layers in silicon wafers. A pulsed laser at a wavelength of 1064 nm and pulse

width of 10^{-8} s was used. The minimum reliably detected depth of SSD was estimated at the level of 0.15–0.2 μm. Laser-induced ultrasonic signal has the potential of being a full-wafer and economical SSD depth measurement method due to its simple setup.

Ishikawa *et al.* [58] used a reflection acoustic microscope to estimate the thickness of SSD layers in silicon wafers. In this method, acoustic waves are generated by applying high-voltage pulses (300–600 MHz) to a piezoelectric film mounted on an acoustic lens. The acoustic lens focuses the acoustic waves on a sample via water as the coupling medium. The reflected acoustic waves from the sample return to the piezoelectric film by the same route, and converted to voltage signal. By analyzing the voltage signal, it is possible to determine the velocity of surface acoustic waves (SAWs) in the sample surface layer which is influenced by the SSD level. It was found that surface roughness also has an influence to the SAW velocity and this is a problem that needs to be resolved.

C. Surface Roughness

Any surface when suitably magnified will reveal itself as a series of peaks and valleys which may vary both in height and spacing. The wafer's back surface as produced by grinding is of no exception. It is by these irregularities that the surface finishing is determined. Thus, to control the grinding process it is useful to employ surface quality parameters such as R_a, $R_{\max}$, and R_t as a measure of its roughness. The definition of these parameters and measurement methods will be discussed later in this section.

Surface roughness causes microscopic stress concentrations that lower the mechanical strength of a wafer and singulated die [73]. Lim [14] has conducted die strength experiments by using a simply supported beam test on singulated dies and impact test on packaged dies. An inversely proportional relationship was seen between the fracture strength and the surface finish parameters—the die weakens as the degree of surface roughness is increased. However, the experiments by Lim [14] did not take into account the combined effect of both roughness and the underlying SSD on mechanical strength.

Higher roughness can be an indication of deeper SSD, because the wafer surface roughness can sometimes be correlated with SSD and is more amenable to routine measurement [74]. Therefore, it is desirable that the surface roughness on ground wafers is low.

In the context of ultrathin wafers and dies, this means that it is critical for the postgrinding treatment of wafers to significantly lower the surface roughness and SSD to a level where the ultrathin wafers and dies are robust enough for subsequent processing and to withstand packaging stresses.

The most commonly quoted surface roughness parameters in case of silicon are R_a, $R_{\max}$, and R_t (Fig. 13) [14], [75]. The R_a value is the arithmetic mean surface roughness measured along a sampling length and is commonly used as a general purpose surface finish parameter. These are mean values and do not fully reflect the extent of local surface defects. The root-mean-square (rms) roughness value, or R_q, is generally 11% higher than the R_a value for the same surface roughness.

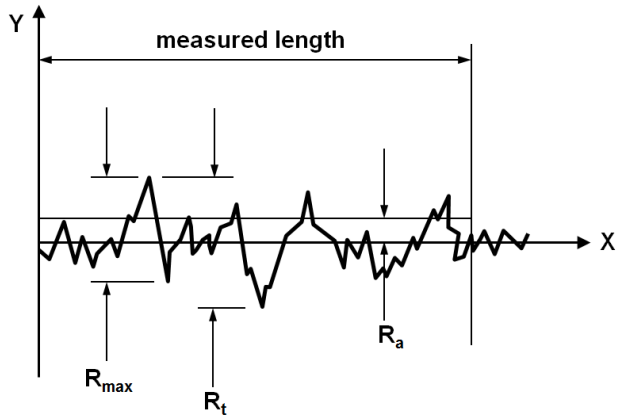

Fig. 13. Definitions of surface roughness parameters.

The $R_{\max}$ value gives the maximum individual peak-to-valley height along the measured length and thus measure the largest surface defect. The distance between the highest peak and the lowest valley along the measured length is represented by the R_t value. The $R_{\max}$ parameter is recommended as a wafer grinding roughness control parameter as it is a measure of the maximum surface defect [14].

Typical roughness measurements are performed using stylus profilers, noncontact optical profilers, or atomic force microscopes (AFMs) [75], [76]. Stylus measurements are widely used for surface roughness, but they lack lateral resolution due to the tip geometry. They also may cause surface damage owing to high forces exerted on the surface and is therefore not recommended for ultrathin wafers and dies.

White-light interferometry and confocal scanning microscopy are well-established methods in optical profilometry [77]. Optical profilers offer quick measurement of surface features without surface contact, but they are limited in resolution owing to the wavelength of light used. AFM extends the resolution to atomic dimensions and is nondamaging in the noncontact and tapping modes [75]–[78]. Typical vertical and lateral resolutions of an optical profiler are 0.1 nm and <1 μm (depending on lens type) respectively, whereas that of an AFM are 30 pm and <20 nm (depending on probe tip radius), respectively [78]. Information about the principles and operation of optical profilometry and AFM can be found elsewhere [75], [78]. If the surface topography does not have features smaller than the nominal resolution of the optical profilers, measurements obtained with the optical profilers are indicative of the true surface roughness. Having microfeatures, an AFM should be used to provide accurate roughness data [76].

Sudani *et al.* [87] used an optical profiler to measure the sidewall roughness of ultrathin dies in comparing the quality of ultrashort-pulse laser dicing with different parameters and assist gases. They found that the best die sidewall R_a value of 0.35 μm was obtained at a pulse width of 214 fs and a repetition rate of 4.33 MHz by using an average laser power of 15.5 W with nitrogen gas assist. Wu *et al.* [104] evaluated the backside surface roughness of ultrathin wafers with different postgrinding treatments using optical profilometry. Their experimental work showed that the R_a values of backgrinding and plasma etching were, respectively, three and

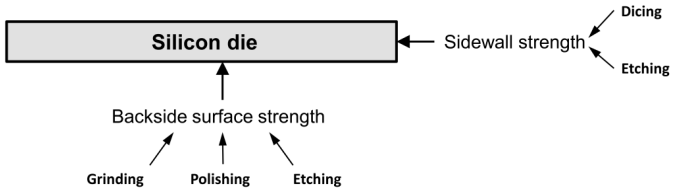

Fig. 14. Influence of processing methods on the mechanical strength of a silicon die.

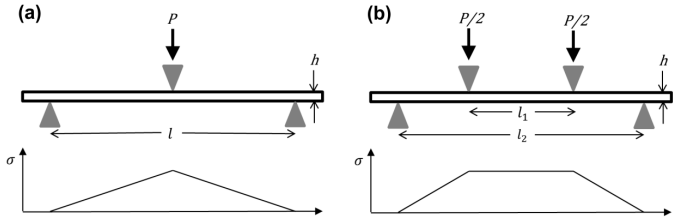

Fig. 15. Setup of (a) three-point bend test and (b) four-point bend test with tensile stress distribution along the sample backside surface.

six times higher than wet chemical etching. AFM has been widely used for roughness measurement of ultrathin wafers and dies because of its higher resolution. AFM has been extensively employed in studies on backgrinding and post-grinding damage removal by Sun *et al.* [99], Sheng *et al.* [9], Sandireddy and Jiang [100], and Chong *et al.* [79]. In laser dicing experiments proposed by Haupt *et al.* [101], the effects of laser wavelength and pulse width on the sidewall roughness of ultrathin dies were investigated using AFM. Their study revealed that continuous wave laser produced a much lower die sidewall R_a value than μs, ns, and ps laser pulse widths.

D. Mechanical Strength

With the reduction of die thickness to less than 100 μm, the requirement for die strength is becoming more stringent. Studies have shown that as die thickness becomes lower, the value of fracture load also reduces [79]. Die strength is not only dependent on die thickness and size, but it could be affected by backside and sidewall defects induced by the thinning and dicing processes respectively [5], [80]–[91]. There are two major factors affecting the die strength, namely backside surface strength and sidewall fracture strength (Fig. 14). The backside surface fracture strength is generally improved by postgrinding and stress-relief processes such as CMP, wet chemical etching, and plasma etching. These processes reduce the wafer backside surface roughness and residual stress, hence improves the die strength. The sidewall fracture strength can be improved if the die sidewalls are smooth and free of crystalline damage and residual stress after wafer dicing. For ultrathin dies, maximizing the die strength is important as it improves the ability of the dies to withstand the mechanical and thermomechanical stresses in the assembly process and packaging.

Uniaxial and biaxial bending tests in various configurations are used to evaluate the mechanical strength of silicon dies. The standard testing system typically utilizes a screw-driven crosshead and load cell assembly to apply a load to the die sample at a fixed loading rate and displacement rate until the die is fractured. The maximum load at the point of fracture is then used to calculate the die mechanical strength.

1) Uniaxial Bending Tests: The three-point bend test setup is shown in Fig 15(a). In this setup, the die sample is placed on parallel support rods with the die backside facing down. The distance between the support rods is variable depending on the length of the die sample. A third rod places a load from the frontside of the die along the die centerline. This will result in a uniaxial stress state with compressive stress on the die frontside and a tensile stress on the die backside. The tensile stress on the die backside varies linearly with its peak at the die centerline. The region of highest tensile stress is mainly on the die backside surface, which includes a minimal portion of the die sidewall. Therefore, three-point bend testing is highly sensitive to die backside defects closest to the centerline, namely damage caused by wafer-thinning processes. The maximum three-point bending stress can be calculated from the following equation [92]–[94]:

$$\sigma_{3\mathrm{PB}} = \frac{3Pl}{2bh^2} \tag{4}$$

where l is the load span, b and h are the sample width and thickness respectively, and P is the applied load.

The four-point bend test setup is similar to that of the three-point bend test as shown in Fig. 15(b). The load is applied to the die frontside at two points which are equidistant from the die centerline. The maximum tensile stress on the die backside is constant in the region between the two loading rods. This region includes the backside surface of the die, and a significant portion of the die sidewall. Thus, four-point bend testing is more sensitive to die sidewall defects coming from the wafer dicing process, compared to three-point bend testing. The maximum four-point bending stress can be calculated from the following equation [95]:

$$\sigma_{4\mathrm{PB}} = \frac{3P}{2bh^2}(l_2 - l_1) \tag{5}$$

where l_2 is the load span, l_1 is the inner load span, b and h are the sample width and thickness respectively, and P is the applied load.

A limitation of analytical stress analysis based on (4) and (5) is that the sample deflection should be small to avoid nonlinear behavior between the applied load and stress [103]. However, the deflection of ultrathin dies in uniaxial bend tests can be large due to the flexibility of the die. ASTM C674-13 [92], ASTM D790 [94], and ASTM D6272-00 [95] recommend that the sample deflection should not exceed 10% of the support span. SEMI G86-0303 [93] recommends to use a support span $\leq$2 mm for samples with thickness $<$100 μm to prevent excessive deflection. Finite element analysis (FEA) is a useful tool to verify whether the calculated stress from (4) and (5) is still valid for larger deflection. For example, Wasmer *et al.* [108] used FEA to verify the validity of calculated four-point bend stresses due to excessive sample deflection.

Three-point and four-point bend tests have been widely used for evaluating wafer dicing and wafer-thinning technologies for thin wafers (Table II). Although four-point bend test is theoretically more sensitive to wafer dicing damage,

TABLE II
APPLICATIONS OF THREE-POINT BENDING (3PB), FOUR-POINT BENDING (4PB), BALL-ON-RING (BOR), AND RING-ON-RING (ROR) TESTING ON THIN SILICON DIES FOUND IN THE LITERATURE

Bending test type	Die size (mm)	Die thickness (μm)	Areas of study	Reference
4PB	14.3 x 6.7	10-50	Backgrinding parameters, dicing-by-grinding, and post-grinding treatments.	Takyu et al. [82,90,97]
3PB	10 x 10	125	Waterjet-guided laser dicing and blade dicing.	Richerzhagen et al. [102]
3PB	-	100	Backgrinding parameters, dicing-by-grinding, and post-grinding treatments.	Sandireddy et al. [100]
3PB BOR	14 x 6 14 x 14	50	Backgrinding and post-grinding treatments, dicing-by-grinding, blade dicing, and laser dicing.	Chen et al. [83]
3PB	-	10-30	Blade dicing, dicing-by-grinding, stealth laser dicing, laser dicing with different pulse width.	Miyazaki et al. [80]
3PB 4PB BOR	15 x 15 15 x 15 15 x 15	125-300	Die thickness, dicing-by-grinding, post-grinding treatments, blade dicing, waterjet-guided laser dicing, and laser dicing.	Kroninger et al. [81]
3PB	8.8 x 6.7	50	Blade dicing, laser dicing, and post-dicing chemical etch.	Li et al. [88]
3PB	10 x 2.5	80	Femtosecond laser dicing parameters and assist gas.	Sudani et al. [87]
3PB	12 x 3	220	Laser dicing pulse width and continuous wave laser.	Haupt et al. [101]
3PB	11.2 x 5.45	283	Backgrinding parameters and post-grinding treatments.	Chen et al. [98]
3PB 4PB ROR	18 x 6 18 x 6 18 x 18	60-80	Backgrinding parameters and post-grinding treatments.	Sheng et al. [9]
3PB 4PB BOR	9 x 5 20 x 5.5 20 x 20	50-75	Die thickness, backside surface roughness, backgrinding parameters, polishing parameters, die edge defects.	Sun et al. [99]
BOR	10 x 10	102	Backgrinding parameters and post-grinding treatments.	Wu et al. [104]
3PB	-	100-300	Backgrinding scratch line orientation, die size, die thickness, and wafer type.	Chong et al. [79]
3PB 4PB	-	100	Backgrinding parameters and chemical etch	Yeung et al. [105]
BOR	13 x 9.1	22-40	Backgrinding parameters	Jeon et al. [106]
BOR	-	100-400	Backgrinding parameters	Liu et al. [107]

it can be seen that three-point bend test is still widely used for such evaluations because of the simpler setup. Schoenfelder *et al.* [96] found that for large sample deflections, the stress distribution in the inner load span of the four-point bend test becomes nonlinear and peaks at the centerline of the sample. Hence, there is no strong benefit in using the four-point bend test over the three-point bend test for samples with large deflection. In summary, the three-point bend test seems to be more robust for uniaxial stress measurements of ultrathin dies.

2) Biaxial Bending Tests: The ball-on-ring test setup is shown in Fig. 16(a). A square die sample with the backside surface facing down is placed on a support ring. A concentric ball is used to apply load from the frontside of the die. This will result in a biaxial stress state with compressive stress on the die frontside and tensile stress on the die backside.

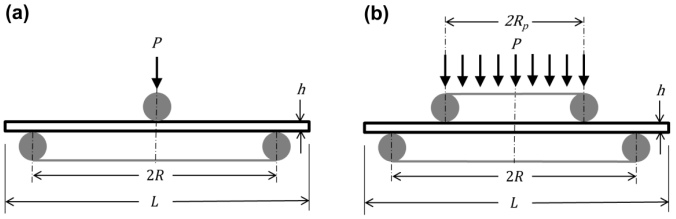

Fig. 16. Setup of (a) ball-on-ring test and (b) ring-on-ring test.

There is negligible stress on the die sidewalls. The maximum ball-on-ring stress can be calculated from the following equation [109], [110]:

$$\sigma_{\mathrm{BOR}} = \frac{3P}{4\pi h^2}(1+\upsilon) \times \left(1 + 2\ln\frac{R}{z} + \frac{1-\upsilon}{1+\upsilon}\left(1 - \frac{z^2}{2R^2}\right)\frac{R^2}{r_{\mathrm{eq}}^2}\right) \quad (6)$$

where P is the applied load, h is the sample thickness, υ is the Poisson's ratio, R is the support radius, and z is the contact radius. Shetty *et al.* [110] estimated the contact radius z to be $h/3r_{\mathrm{eq}}$ is the equivalent sample radius based on the sample length L defined as follows:

$$r_{\mathrm{eq}} = \frac{L(1+\sqrt{2})}{4}. \quad (7)$$

The ring-on-ring test setup is similar to that of ball-on-ring as shown in Fig. 16(b). A concentric ring is used to apply load from the frontside of the die. This will result in a biaxial stress state with compressive stress on the die frontside and tensile stress on the die backside. The maximum tensile stress on the die backside is constant in the region within the loading ring. There is negligible stress on the die sidewalls. The maximum ring-on-ring stress can be calculated from the following equation [109]–[111]:

$$\sigma_{\mathrm{ROR}} = \frac{3(1+\upsilon)P}{4\pi h^2}\left(2\ln\frac{R}{R_p} + \frac{1-\upsilon}{1+\upsilon}\frac{R^2 - R_p^2}{r_{\mathrm{eq}}^2}\right) \quad (8)$$

where P is the applied load, h is the sample thickness, υ is the Poisson's ratio, R is the support radius, R_p is the loading radius, and r_{eq} is the equivalent sample radius according to the sample length L with the same definition as in (7).

Similar to uniaxial bend tests on thin dies, problems with large sample deflections in biaxial bend tests have to be dealt with to minimize nonlinearity. According to Schoenfelder *et al.* [96], biaxial bending is much more sensitive to large deflection than uniaxial bending, and that (6) and (8) are valid if the deflection does not exceed $h/2$. Jeon *et al.* [106], Liu *et al.* [107], Wasmer *et al.* [108], and Barredo *et al.* [109] have used FEA to verify the validity of analytical calculations for biaxial bend experiments with large deflection. In ball-on-ring tests, Jeon *et al.* [106] found that the analytical solution for die strength correlates well with FEA solution for die thicknesses between 22 and 31 μm.

Ball-on-ring test and ring-on-ring test are widely used to evaluate wafer thinning and postthinning treatment processes where any influence of the sample edges is unwanted (Table II). The ball-on-ring test is more popular than ring-on-ring test due to the simpler setup. Additionally, the ring-on-ring test loses its advantage of a constant biaxial stress field in the case of large deflections in ultrathin dies [96]. The ball-on-ring test seems to be more robust for biaxial bending test of ultrathin dies.

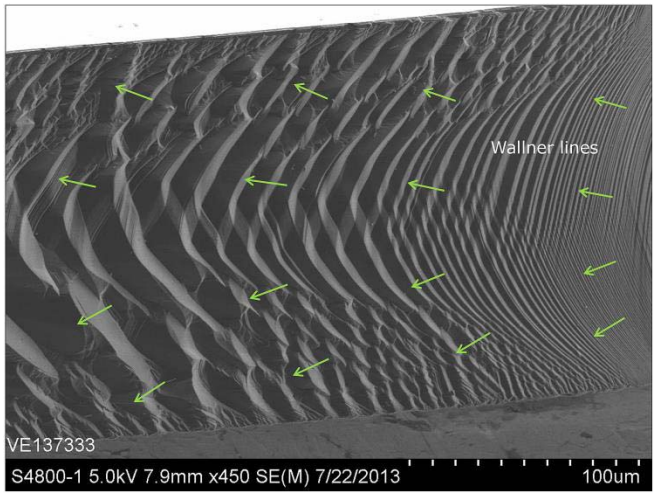

Fig. 17. Example of fractographic features on a die fracture surface indicating the direction of fracture propagation (arrows) and the fracture origin.

3) Fractographic Analysis: Fracture propagation path is determined by the physical properties, microstructure, stress configuration, and environment of the material. The combination of these conditions can vary in such a manner to create a significant range of fracture propagation path types. The resultant fracture topography is a record of the integration of the material, stress, and environmental factors. Fractography is the study of fracture topography and its relation to fracture propagation. It is basically an attempt to deconvolute topographical information on the fracture surface into information about the fracture propagation direction.

Marks [112] described the technique of silicon fractography and the interpretation of macroscopic and microscopic fracture surface markings in monocrystalline silicon (Fig. 17). The careful application of fractographic analysis enables the determination of the fracture propagation direction, the stress pattern, and the fracture initiation site. The defect at the fracture origin can be identified and subsequently the root cause can be determined.

Chong *et al.* [79], Bohm *et al.* [113], and Yeung and Lee [105] have applied fractographic analysis to determine the fracture origins and types of surface defect in silicon die bending test samples. The application of fractography in bend test samples is important to validate whether the test result is related to the objective of the test. For example, in a bend test to evaluate wafer dicing quality, the fracture origin should be at a die sidewall defect. Likewise, in a bend test to evaluate wafer-thinning quality, the fracture origin should be at a die backside surface defect. If the die fracture in a bend test is not originating from the region of interest, then the configuration and setup of the bend test is incorrect and need to be changed.

I. Summary

Ultrathin die is a key enabler for higher electrical and thermal performance in semiconductor devices, as well as

for ultrathin and flexible semiconductor packaging. The key quality characteristics of ultrathin wafers and dies are bow/warpage, TTV, SSD, surface roughness, and mechanical strength. As the quality of ultrathin wafers and dies have a significant impact on packaging assembly yield and device reliability, it is essential to have characterization methods to control these quality characteristics in the manufacturing processes.

The bow/warp of silicon wafers should be monitored before bonding to rigid carriers because this has an influence to the final wafer TTV after backgrinding, as well as to the final bow/warp of ultrathin dies. Noncontact measuring methods for bow/warp/TTV are recommended for silicon wafers, using a support system that minimizes wafer contact area and gravity-induced deflection. Noncontact probe technologies for bow/warp/TTV measurements utilize capacitance, optical, or other noncontact sensors. Optical interferometry technology enables full-wafer bow/warp/TTV characterization with improved measurement accuracy and spatial resolution. Computer-aided reflection moiré has gained popularity for wafer bow/warp measurements because of its relatively fast full-field measurement and simple setup.

Monitoring of combined residual stresses induced in ultrathin wafers due to active layers on the wafer frontside, and due to backgrinding and postgrinding treatment on the wafer backside, is possible indirectly through bow/warp measurement of ultrathin dies. Noncontact optical profilometry methods such as confocal microscopy and interferometry are recommended for measuring bow/warp of ultrathin dies. One area that is gaining importance is temperature-dependent die warpage behavior during high-temperature assembly processes. The fringe projection method has the potential to be developed for this application. However, a white coating needs to be applied on the sample surface to enhance the signal-to-noise ratio. The effect of the white coating on the thermomechanical behavior of the ultrathin die needs to be investigated.

SSD induced by backgrinding reduces the mechanical strength of the wafer and die. Destructive methods for characterizing SSD include materialographic and FIB cross-sectioning, and high-magnification observation with optical microscopy, SEM, or TEM. Nondestructive evaluation methods for SSD can be performed by high-resolution XRD, micro-Raman spectroscopy, and SIRD. The ability of micro-Raman spectroscopy to quantify the residual stresses in the silicon at high spatial resolution is an advantage.

Higher roughness can be an indication of deeper SSD, and is more amenable to routine measurement in production. Typical roughness measurements are performed using noncontact optical profilers or AFM to prevent any physical damage on ultrathin wafer and die samples.

The mechanical strength of the die is affected by backside and sidewall defects due to thinning and dicing processes, respectively. For ultrathin dies with high flexibility, the three-point bend test is a robust method for evaluating die sidewall strength, and the ball-on-ring test is a robust method for evaluating die backside surface strength. As the thickness of silicon dies goes below 20 μm, excessive deflection during standard uniaxial and biaxial bend tests will become a more significant problem for nonlinear analytical solutions. Hence, new techniques for measuring the die strength for such extremely low die thickness need to be developed.

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