A CMOS Integrated Three-Axis Accelerometer Fabricated With Commercial Submicrometer CMOS Technology and Bulk-Micromachining

Hidekuni Takao, Hirofumi Fukumoto, and Makoto Ishida

***Abstract*—In this paper, a bulk-micromachined three-axis accelerometer fabricated with commercial submicrometer CMOS wafers has been developed for low-cost realization of smart accelerometers and improvement of device performance. The signal processing circuits for three-axis detection were formed using a commercial 0.8-μm CMOS technology. After that, micromachining processes were performed to the complete CMOS wafers to form accelerometer structures. The important technologies to separate micromachining processes from the CMOS process are wafer thickness control after CMOS fabrication and backside polishing with chemical spin etching. Accelerometers with 3×3 mm^2 and 6×6 mm^2 die size were fabricated with the developed fabrication technology. As a result of device evaluation, 2.0 mg$_{\rm rms}$ resolution of Z-axis acceleration, and 10.8 mg$_{\rm rms}$ resolution of X and Y-axis acceleration were obtained by the accelerometers with 6×6 mm^2 die size. Comparing for the same die area, the 6×6 mm^2 size accelerometer showed about 21.3 times higher resolution of Z-axis acceleration and 37.8 times higher resolution of X, Y-axis acceleration as compared to our previous three-axis accelerometer fabricated with 5.0-μm CMOS technology. Temperature dependence and reliability for repetitive vibration loads were also evaluated. Through these evaluations, basic performance of the CMOS integrated three-axis accelerometer has been confirmed.**

***Index Terms*—Acceleration measurement, CMOS integrated circuits, intelligent sensors, micromachining, MOSFETs, piezoresistive devices.**

I. Introduction

SILICON micromachined accelerometers are well known for their ability to integrate peripheral circuits in the same die. For example, there is a commercial product of surface-micromachined CMOS integrated accelerometer which can detect two-axis acceleration (Analog Devices ADXL-202). Such accelerometers are fabricated by combining surface-micromachined structures and CMOS circuits [1]. On the other hand, it is necessary for bulk-micromachined accelerometers to establish fabrication technology for integration of CMOS circuits. Although we have reported a CMOS integrated three-axis accelerometer fabricated with 5.0-μm CMOS technology and bulk-micromachining [2], some procedures in the CMOS fabrication steps were modified and optimized for following bulk-micromachining steps. The modification of standard procedure of CMOS fabrication is not acceptable to the most of commercial CMOS factory. Utilization of commercial (i.e., standard) CMOS technologies is attractive to produce bulk-micromachined smart sensors in a reasonable cost, since they always provide smaller MOS devices and higher performance with lower cost as compared to previous CMOS technologies. However, some problems based on difference of specification among commercial CMOS technologies have been remained for CMOS post bulk-micromachining as follows:

1) accommodation to various wafer thickness of each commercial CMOS technology;
2) existence of unnecessary layers on the initial backside of CMOS wafers;
3) difficulty in achieving a smooth mirror finish on the wafer backside for following anisotropic etching process and glass bonding;
4) selection of proper masking material for post-CMOS anisotropic etching.

Anisotropic wet etching using TMAH is necessary for low-cost formation of microstructure *without contamination of harmful ions*, because it has higher throughput and can use much simpler apparatuses than deep-dry etching process [3].

Due to the above problems, it has been difficult to fabricate smart bulk-micromachined sensors using commercial CMOS technologies. In the present study, a bulk-micromachined three-axis accelerometer fabricated with a commercial submicrometer CMOS technology has been developed for low cost realization and improvement of device performance. The above problems, i.e., difference of specification among CMOS technologies are no longer major problems in the developed device fabrication process. So, CMOS integrated three-axis accelerometers with bulk-micromachining can be manufactured with reasonable costs using a commercial CMOS technology. The circuitry in the three-axis accelerometer was fabricated with a commercial 0.8-μm CMOS technology. The operation principle, details of the developed fabrication process, and evaluation results of the three-axis accelerometer are explained and discussed in the later sections. In addition, the effect of shrinking of CMOS design rule in the three-axis accelerometer is also discussed.

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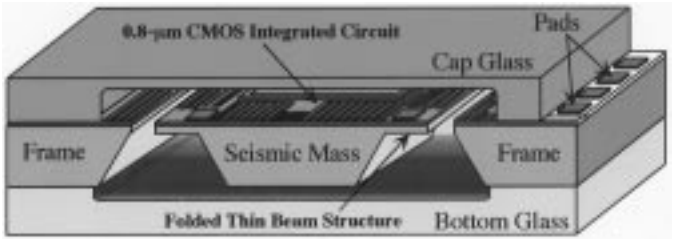

Fig. 1. Cut-away simplified drawing of the 0.8-μm CMOS integrated three-axis accelerometer.

II. Device Configuration

A. Structure of the Three-Axis Accelerometer

Fig. 1 shows a cut-away simplified drawing of the 0.8-μm CMOS integrated three-axis accelerometer. The device has a three-layer structure formed by cap glass, micromachined silicon and bottom glass. On the silicon surface, signal processing circuits are formed by a commercial 0.8-μm CMOS technology. Detection of three-axis acceleration, and signal processing to extract each component of acceleration are performed by the on-chip CMOS circuitry. For detection of acceleration, p-MOSFETs are used as stress sensitive elements to transform the deflection of the beam structures caused by input acceleration into electrical signal [2]. The sensing principle is based on piezoresistive effect of p-type inversion layer in p-MOSFETs [4], [5]. Since p-MOSFETs are standard elements in CMOS circuits, it is convenient to use them in CMOS integrated sensors as sensing elements [6]–[8]. Furthermore, piezoresistive coefficient of p-MOSFETs does not strongly depend on the CMOS technology used, while that of conventional piezoresistors is quite sensitive to their impurity concentration.

B. Detection of Mechanical Strain Generated by Acceleration

Fig. 2 shows the top view of the three-axis accelerometer showing the structure of four sets of folded beams with a silicon thickness of 10 μm. The folded beam was designed to have the maximum sensitivity in a die size. Optimization of the beam length [9] is not necessary in this accelerometer design because the maximum beam length is determined by the size of structure area, the minimum width of each beam structure (50 μm) and separation area (50 μm). For example, the designed beam length in 3×3 mm^2 die size accelerometer is 1550 μm. The size of seismic mass is determined to minimize dead space (volume). Four sensing p-MOSFETs are formed on the folded edges of each beam where the largest strain is generated by beam deflection. In most of piezoresistive accelerometers, piezoresistors are put near boundary between bulk structure and thin beam structure. So, sensitivity of them varies considerably with the distance from the boundary. The sensing piezoresistive p-MOSFETs in this accelerometer are put on the points at a distance from the boundary. The maximum stress is generated near the folded edge of beams. Thus, it can be considered that the device performance of this accelerometer is not so sensitive to device fabrication error. The sensing p-MOSFETs in this accelerometer are standard p-MOS devices formed in the commercial CMOS

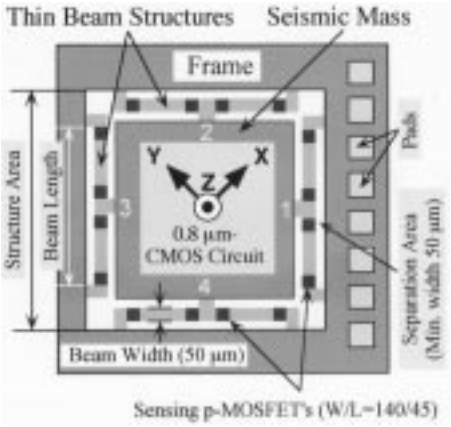

Fig. 2. Top view of the surface of three-axis accelerometer showing the configuration of four sets of folded beam structures.

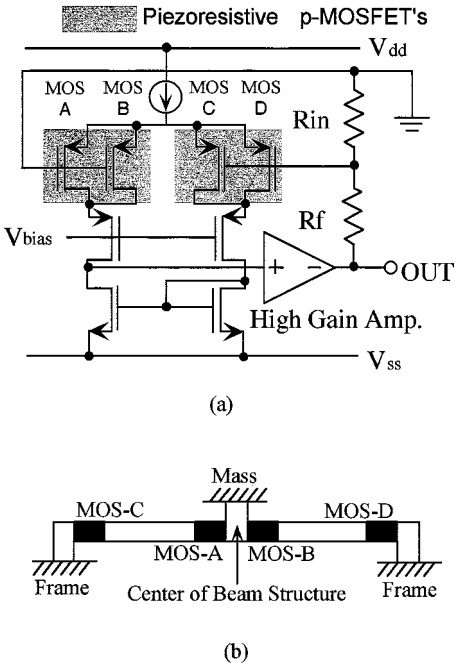

Fig. 3. The stress detection circuit using four sensing p-MOSFETs on each beam structure: (a) circuit configuration and (b) positions of four sensing p-MOSFETs on each beam structure.

fabrication process used. The gate size of them is 45 μm in length and 140 μm in width, respectively. The area of gate was designed to be relatively large so as to reduce $1/f$ noise from them.

The stress detection circuit using the four sensing p-MOSFETs on each beam [8] is shown in Fig. 3(a). In this accelerometer, four sets of the detection circuit are integrated for each folded beam structure (1–4 shown in Fig. 2). By putting the input p-MOSFETs as shown in Fig. 3(b), each detection circuit can detect the direction (polarity) and amplitude of deflection at the center of each beam structure. Furthermore, the detected strain signal is amplified by the detection circuit at the same time. If the center of the beam (connection point with the mass) is moved upwards from the chip surface, generated stress becomes tensile on MOS-A and MOS-B, while it becomes compressive on MOS-C and MOS-D. So, differential mobility change occurs

between the two MOSFET pairs in the input stage of the differential amplifier due to piezoresistive effect in p-MOS inversion layer. Thus, an input offset voltage due to the differential mobility change is generated in proportion to acceleration, and it is amplified by the total voltage gain of the amplifier with negative feedback configuration. The output voltage of the detection circuit for each beam Vn ($n = 1$–4) is expressed by the following expression:

$$\begin{aligned} Vn &= A \cdot V_{\text{offset}} = A \cdot C \cdot \pi_{\text{pMOS}}(\sigma_{AB} - \sigma_{CD}) \\ &= A \cdot C \cdot \pi_{\text{pMOS}}(T_{Xn} \cdot \alpha_X + T_{Yn} \cdot \alpha_Y + T_{Zn} \cdot \alpha_Z) \end{aligned} \quad (1)$$

where

A	total voltage gain of the amplifier;
V_{offset}	input offset voltage of the amplifier induced by stress;
C	constant which depends on circuit design;
π_{pMOS}	piezoresistive coefficient of the p-MOSFET;
σ_{AB}	induced stress on MOS-A and MOS-B;
σ_{CD}	on MOS-C and MOS-D;

and T_{Xn}, T_{Yn}, and T_{Zn} are the translation constants between induced differential stress on each beam ($n = 1$–4) and each component of input acceleration vector (α_X, α_Y, α_Z), respectively. The total voltage gain, A, almost becomes the ratio of $-R_f/R_{\text{in}}$, if the product of voltage gains of the first stage and the second stage amplifier is much higher than the ratio. In this study, A was set to -100 by setting the resistor ratio (100 kΩ/1 kΩ).

C. Detection of Three-Axis Acceleration

Three-axis components of acceleration are calculated from the signals of the four detection circuits. Fig. 4 shows the results of FEM simulation in the cases when X, Y and Z-axis acceleration (1 g) are applied to the accelerometer. The die size of the FEM model is 3×3 mm^2, and the length and the width of the beam structures are 1550 μm and 50 μm, respectively. If X-axis acceleration is applied [Fig. 4(a)], the mass moves to X-axis with rotational motion because there is a distance between the chip surface and the center of gravity of the mass. Due to the rotational motion, the beam 1 and 2 are deflected downwards while the beams 3 and 4 are moved upwards. As the amplitude of deflection is equal among the four beams, the amplitude of each output voltage also becomes equal. X-axis acceleration is detected with calculation using the outputs from the four detection circuits as expressed with (2)

$$V_{\text{out}x} = (V_1 + V_2) - (V_3 + V_4) \quad (2)$$

where V_1, V_2, V_3 and V_4 are the output voltage of the detection circuits corresponding to the beams 1–4, respectively. Y and Z-axis acceleration can be detected in the same manner as

$$V_{\text{out}y} = (V_2 + V_3) - (V_1 + V_4) \quad (3)$$

$$V_{\text{out}z} = V_1 + V_2 + V_3 + V_4. \quad (4)$$

These operations of voltage addition and subtraction are performed by integrated circuits on the same chip. With this detection principle, each component of acceleration can be extracted without cross-axis sensitivity in ideally balanced structures. Although, the principle of three-axis detection is similar to our previous device [10], circuit configuration of signal detection is much simplified and optimized for integration of total signal processing circuits in this study.

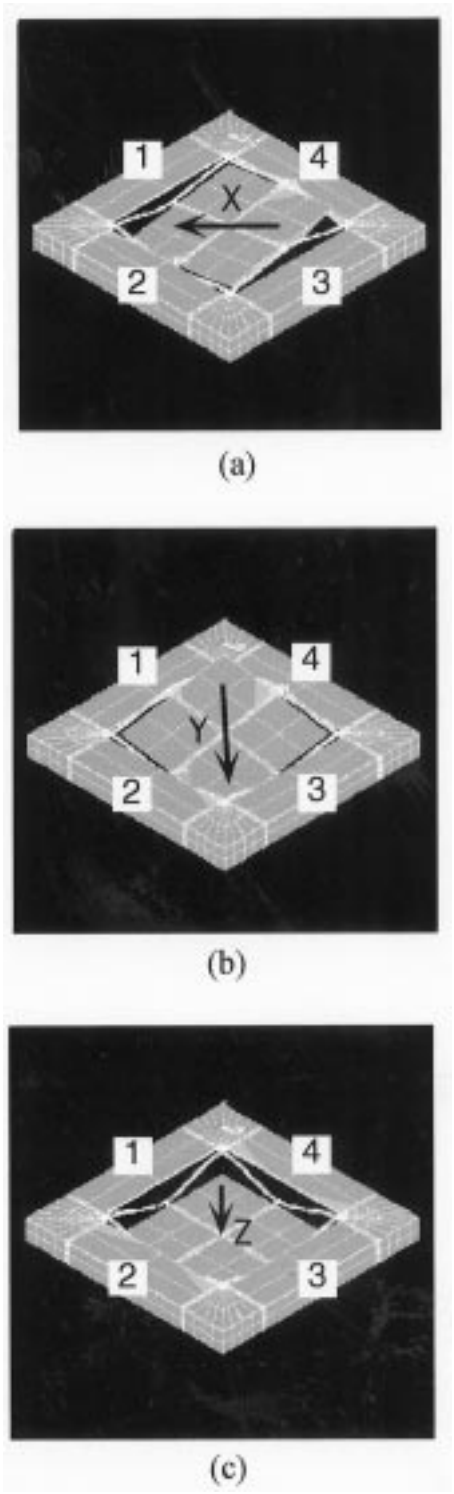

Fig. 4. Shapes of beam deformation for three-axis acceleration input obtained by FEM analysis (ANSYS): (a) X-axis 1 g-input, (b) Y-axis 1 g-input, and (c) Z-axis 1 g-input.

Mobility change in sensing p-MOSFETs was predicted from piezoresistive coefficient of p-MOSFET reported in previous literatures and the stress level obtained by the FEM analysis. The

calculated mobility change due to applied 1 g acceleration was used in SPICE simulation to estimate the sensitivity of the accelerometer.

In the FEM model, all the elements are formed by single crystal silicon, and passivation layers formed on the integrated CMOS circuitry are not considered. Comparison of estimated sensitivity and measured sensitivity of fabricated devices is discussed in the later section.

III. Fabrication Process With CMOS Post-Process Micromachining

The three-axis accelerometer was fabricated to evaluate the device performance. In the developed device fabrication process, most of commercial CMOS fabrication technology is available, because it does not depend on the thickness of wafers and condition of the wafer backside. The outline of the developed fabrication process is shown in Fig. 5 [11].

1) First, signal processing circuit was fabricated in a commercial 0.8-μm CMOS production line. In this study, 6-in SOI wafers with 10 μm-thick active silicon layer were used as the starting material for the purpose of precise beam thickness control as explained later. Since the active layer is enough thick for CMOS-LSI to consider it as "bulk silicon wafer" (not as SOI layer), standard CMOS technology can be used to fabricate bulk-CMOS circuits on it. After CMOS fabrication, the thickness of complete 6-in wafers was roughly controlled from 550 μm to 400 μm by grinding the backside of wafers.
2) The backside was etched and polished at the same time using chemical spin etching process [12], [13]. This process is a standard LSI fabrication process, and its throughput is quite high due to its fast etching rate of silicon (more than 10 μm/min depending on the process condition). The defective layer formed during the backside grinding process is removed perfectly in the spin etching process. In this step, the backside was etched by 100 μm, and the wafer thickness was controlled to 300 μm. The variation in the wafer thickness after spin etching process was within 5% of the etching depth over the diameter of 6-in wafers. Thus, thickness variation within 5 μm was guaranteed for this backside process. Fig. 6(a) and (b) show AFM images of the backside of CMOS wafers before and after the chemical spin etching process, respectively. The roughness of the backside surface was much reduced, and the RMS value became from 150 nm to 0.88 nm after the spin etching process. It was enough smoothness for the anodic bonding process in the later step. If any etching stop technique is not used to obtain thin diaphragm structures, smooth backside is necessary to obtain smooth etched surface after anisotropic wet etching.
3) PVD SiO_2 layer was deposited on the polished backside as the masking layer for the bulk-etching process with TMAH solution. PVD SiO_2 layer is a good masking material for mesa structure formation in post-CMOS anisotropic etching [14]. The 2 μm-thick PVD SiO_2 layer was formed on the backside without any electrical damages in the frontside submicrometer CMOS devices.
4) The masking layer was patterned, and silicon substrate was etched for 380 min in TMAH solution at 90 °C. Silicon etching was automatically stopped by the buried SiO_2 layer in SOI wafers [15] because of slow etching rate of SiO_2 in TMAH solution. By this step, precisely controlled 10 μm thick silicon diaphragm was formed. After that, the masking layer and etching stop SiO_2 layer was removed by HF solution. The variation in the wafer thickness after the spin etching process (within 5 μm) is not so serious on the device performance because the diaphragm thickness is controlled precisely using SOI wafers in this case. If electrochemical etch-stop technique with n-well or n-epitaxial layer [16] is used for thickness control of

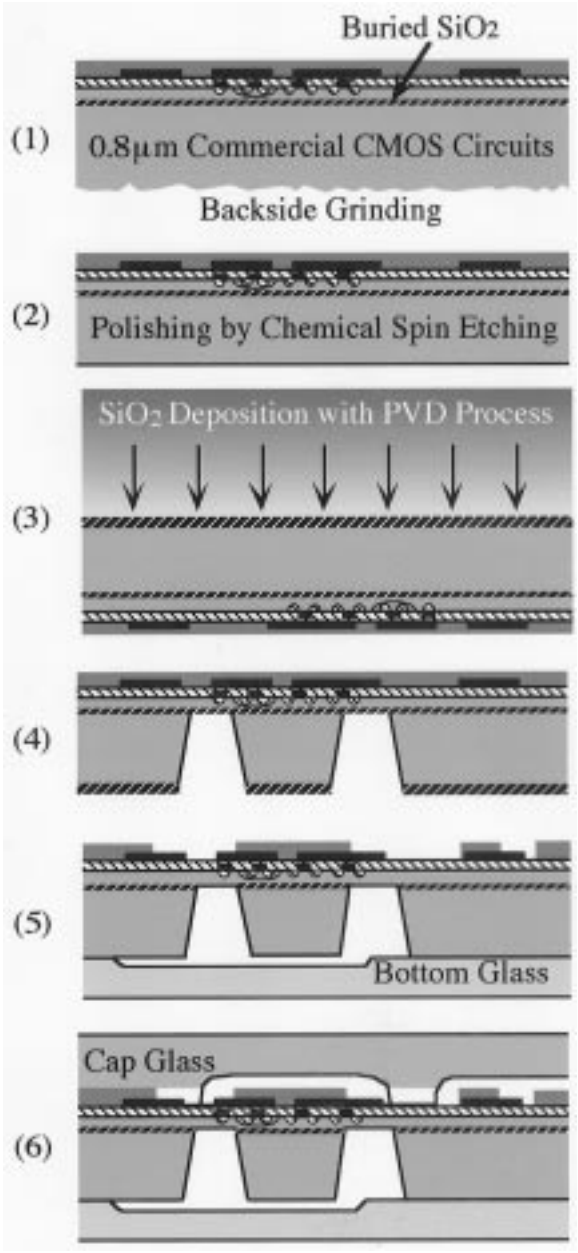

Fig. 5. Outline of the developed fabrication process of the accelerometer including CMOS post micromachining.

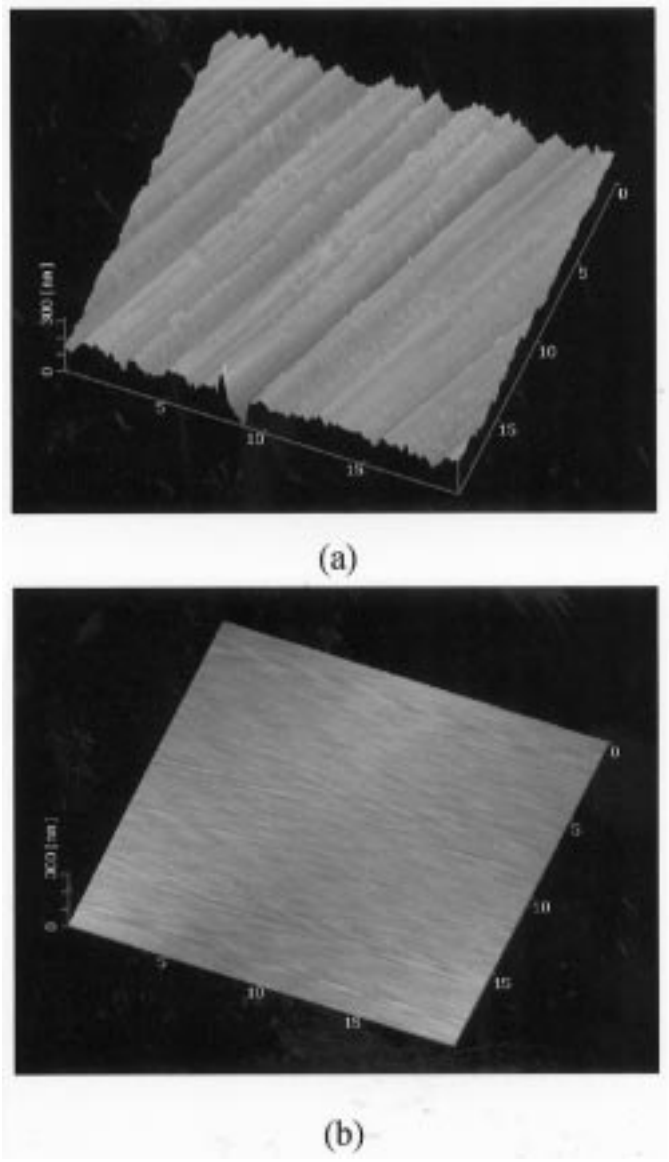

Fig. 6. AFM images of the backside of 6-in CMOS wafer: (a) before chemical spin etching (after backside grinding) and (b) after chemical spin etching.

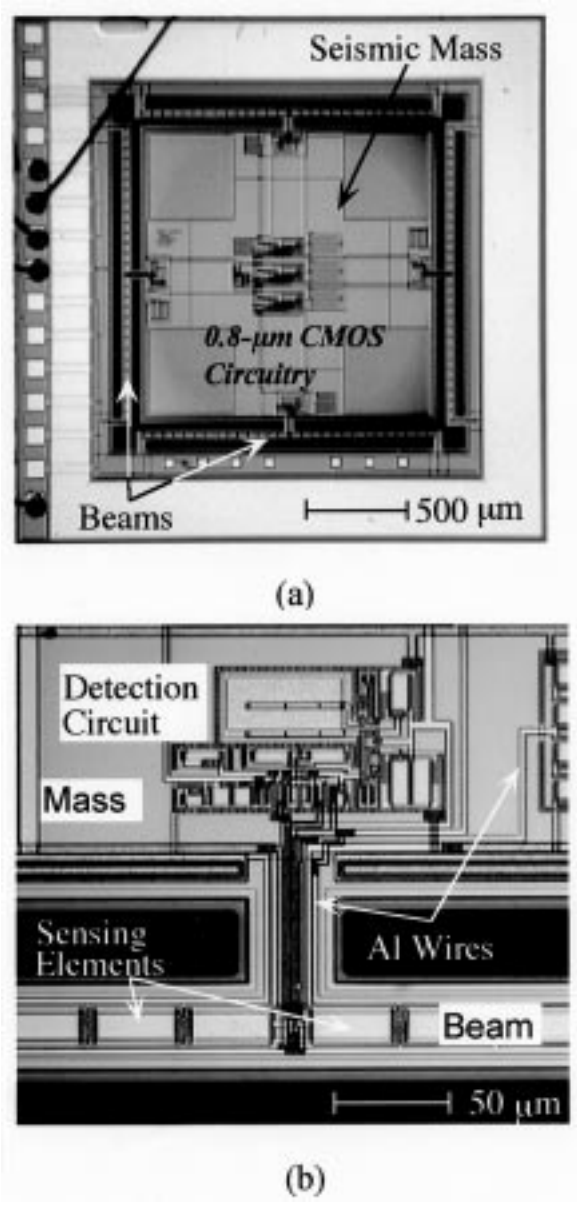

Fig. 7. Photographs of the fabricated accelerometer with 3×3 mm^2 die size: (a) overall chip and (b) photograph around the center of a folded beam structure. The detection circuit for this beam, and sensing p-MOSFETs formed on the beam surface can be seen.

the beam structure, this accelerometer can be fabricated with normal (non-SOI) silicon wafers with lower cost.

5) Anodic bonding glass was etched in HF solution to form 10 μm depth gaps for the mass movement. The patterned glass and the micromachined CMOS wafer were bonded with anodic bonding technology. Then, the silicon beam structures were formed by removing the unnecessary part of the 10 μm-thick diaphragm using reactive ion etching (RIE) with SF_6 gas and photoresist mask.
6) Cap glass for device sealing was patterned and bonded to the frontside surface of the CMOS wafer using Benzocyclobutene (BCB) layer as the adhesive layer [17]. BCB was coated by spin coating method on the patterned glass cap. After the bonding process, the accelerometers were diced and packaged for device evaluation.

The die size of the fabricated accelerometers are 3×3 mm^2 and 6×6 mm^2. Fig. 7(a) shows a photograph of the fabricated three-axis accelerometer with 3×3 mm^2 die size. In this figure, the cap glass is not bonded on the chip surface. Fig. 7(b) shows a photograph around the center of a beam structure. The piezoresistive p-MOSFETs and Al wires are seen on the surface of the 50 μm width beam. Each sensing p-MOSFET ($L = 45$ μm and $W = 140$ μm) is formed by connecting several small p-MOSFETs in parallel. The detection circuit for each beam structure corresponding to Fig. 3(a) can be seen on the mass.

Using the developed post-CMOS bulk-micromachining process, functional smart sensors with sophisticated CMOS processing circuit can be realized in a reasonable fabrication cost.

IV. Device Characterization and Discussions

A. Basic Performances

The fabricated devices were evaluated with a shaker system. Fig. 8(a) and (b) show the measured output characteristics of

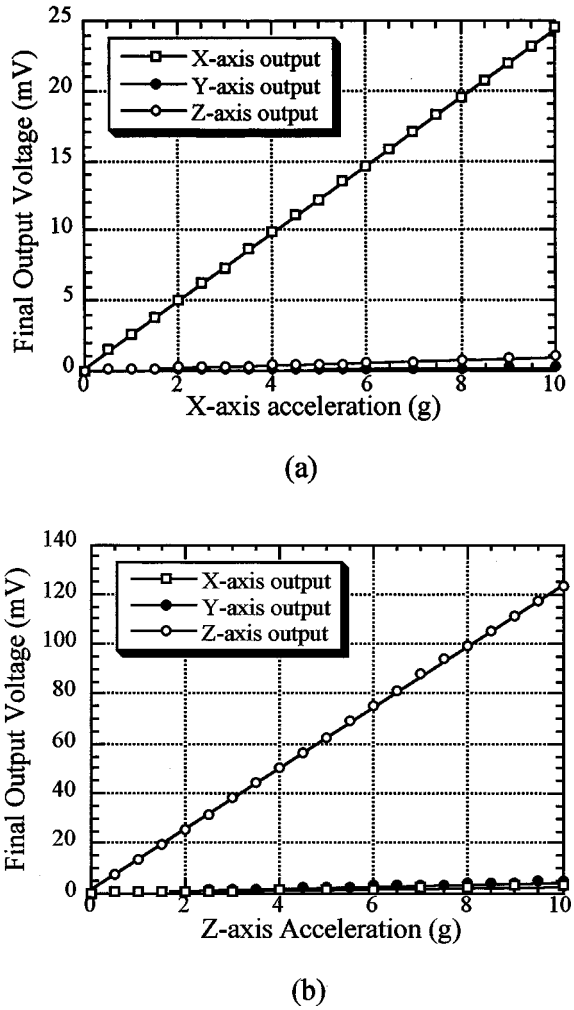

Fig. 8. Output characteristics of each axis circuit in 3×3 mm^2 accelerometer: (a) for X-axis acceleration input and (b) for Z-axis acceleration input.

the fabricated 3×3 mm^2 accelerometer for X and Z-axis acceleration input, respectively. X-axis sensitivity of the device is 2.45 mV/g, and Z-axis sensitivity is 12.5 mV/g. Only the principal axis output appears selectively for the input axis signal. In Fig. 8(a), Y- and Z-axis outputs are well suppressed for X-axis acceleration by the operation principle expressed with (3) and (4). Similarly, X and Y-axis outputs are well suppressed for Z-axis acceleration. The output characteristic for Y-axis acceleration is almost the same with that for X-axis acceleration input, because the detection principles of the two axes are equivalent. Non-linearity of the output is below 1% in the measured range. As Z-axis has the highest sensitivity among three axes, cross-axis error caused by Z-axis acceleration in X and Y-axis outputs becomes the maximum cross-axis sensitivity of the three axis accelerometer. In the fabricated devices, the maximum cross-axis sensitivity varied in a range from 5% to 7%. It depends on the degree of fabrication error such as device misalignment. Cross-axis sensitivity in Z-axis output caused by X or Y-axis acceleration was below 2% in the device.

In 6×6 mm^2 accelerometers, measured Z-axis sensitivity was 167.5 mV/g, and X, Y-axis sensitivity was 31.0 mV/g. Larger size accelerometers have higher sensitivity for the same fabrication technology. Comparing the measured sensitivities

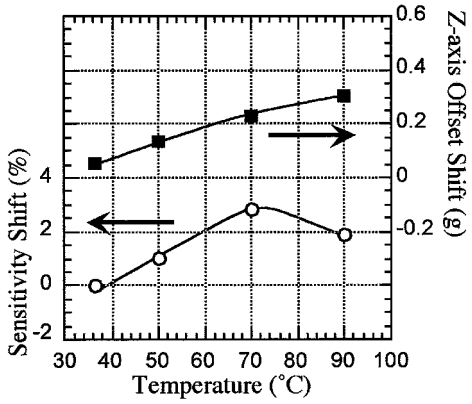

Fig. 9. Temperature dependence of the sensitivity and acceleration equivalent offset of the fabricated accelerometer with 6×6 mm^2 die size.

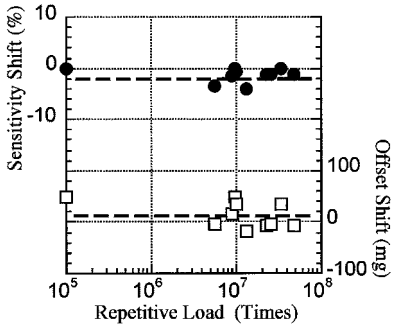

Fig. 10. Measured shift of sensitivity and offset of the fabricated accelerometer caused by repetitive vibration load.

with the estimated sensitivities using FEM analysis, the measured values were about 45% to 50% of the estimated values. It is considered that passivation layers with 3 μm thickness formed on the CMOS circuitry cause remarkable sensitivity reduction. Because the total beam thickness increased from 10 μm to 13 μm in the real device, average stress on sensing p-MOSFETs are much reduced. Thus, influence of CMOS passivation layers can not be ignored in device design of CMOS integrated piezoresistive sensors.

The minimum resolution of detectable acceleration (i.e., noise level) is determined by the ratio between the output noise of the circuits in a bandwidth and each axial sensitivity for unit acceleration. The measured output noise of CMOS circuit was in agreement with estimated noise obtained with SPICE simulator. The bandwidth of the circuit was limited to 100 Hz using a low-pass filter. The obtained minimum resolution of the 6×6 mm^2 accelerometer was about 2.0 mg$_{\rm rms}$ for Z-axis acceleration, and 10.8 mg$_{\rm rms}$ for X and Y-axis acceleration, respectively. On the other hand, the minimum resolution of the 3×3 mm^2 accelerometer was about 26.8 mg$_{\rm rms}$ for Z-axis acceleration, and was 119.0 mg$_{\rm rms}$ for X and Y-axis acceleration. Since the output noise from each axial circuit was almost same among the accelerometers, minimum resolution of each accelerometer depended on only the acceleration sensitivity of each device in this case.

B. Temperature Characteristics

Temperature characteristics were evaluated with a temperature control unit and the shaker system. Measured temperature

TABLE I
SUMMARY OF THE DEVICE CHARACTERISTICS OF THE FABRICATED THREE-AXIS ACCELEROMETERS IN THIS STUDY AND THOSE OF OUR PREVIOUS CMOS INTEGRATED ACCELEROMETER PRESENTED IN [2]

Die Size (mm^2)		*Previous Device 8 × 8 mm² [2]*	6 × 6 mm² For ±10g	3 × 3 mm² For ±30g
CMOS Technology		*5.0-μm CMOS in Lab.*	Commercial 0.8-μm CMOS	Commercial 0.8-μm CMOS
Minimum Resolution	Z	*24.0 mg_{rms}*	2.0 mg_{rms}	26.8 mg_{rms}
	X, Y	*230.0 mg_{rms}*	10.8 mg_{rms}	119.0 mg_{rms}
TCS		*2000 ppm/°C*	550 ppm/°C	←
Offset Drift		*842.0* mg/°C	4.55 mg/°C	60.9 mg/°C

dependences of input equivalent offset and sensitivity are shown in Fig. 9. These are the characteristics of a fabricated accelerometer with 6×6 mm^2 die size. The sensitivity shift in the temperature range from room temperature to 90 °C was within 3%. As explained with (1), sensitivity of the detection circuit depends on some parameters such as piezoresistive coefficient of p-MOSFET and design parameters of the circuit. The piezoresistive coefficient had a negative temperature dependence, and the bias current of the differential stage was set to have positive temperature dependence. As a result, the temperature dependence of sensitivity was much reduced due to the counteracting effect between them [2], and a peak was observed in the sensitivity shift due to the effect. The input equivalent offset shift of Z-axis was below 0.3 g in the temperature range. On the other hand, the offset shift of the accelerometer with 3×3 mm^2 die size was about ten times larger than that of 6×6 mm^2 accelerometer, because the sensitivity of 3×3 mm^2 device was below one tenth of sensitivity of 6×6 mm^2 accelerometer. This is similar with the case of minimum resolution. There is clear tradeoff relationship between the device performance and its die size (i.e., chip cost), if the same fabrication technology is used.

C. Reliability Test with Repetitive Load

Reliability for repetitive bending of the beam structure formed by this fabrication technology has been investigated by applying vibration to the accelerometer. *For* the repetitive load, a 20 MPa stress was applied to the sensing p-MOSFETs formed on the edges of the beam structures. The stress level applied on the p-MOSFETs was predicted using FEM analysis. Fig. 10 shows the shift of sensitivity and input equivalent offset for repetitive load cycles. No significant change in the characteristics was observed after applying 6×10^7 times repetitive load. As shown in the figure, both characteristics showed the same drift tendency. Thus, the main reason of this tendency is considered to be temperature variation during the reliability test taking for a long time.

D. Effects of Design Rule Shrinking in the Integrated Accelerometer

The characteristics of the fabricated three-axis accelerometers are summarized in Table I. The fabricated accelerometer with 6×6 mm^2 die size showed about 21.3 times better Z-axis minimum resolution of acceleration for the unit die area as compared to our previous device [2]. The minimum resolution of X and Y-axis acceleration was also much improved by 37.8 times. The same improvement was obtained in the accelerometer with 3×3 mm^2 die size. The reasons for the improvement of minimum resolution are considered as following.

1) *Reduction of Chip Area Occupied by the Integrated Circuitry*: In our previous CMOS integrated accelerometer, 5.0-μm CMOS technology was used. So, the area of signal processing circuit can be reduced to 1/39 approximately with 0.8-μm CMOS technology. In other words, a larger seismic mass can be formed in the same die size resulting in improvement of acceleration sensitivity. If the noise level of the circuitry is same, minimum resolution of acceleration is much improved by this effect.
2) *Reduction of $1/f$ Noise from the Circuitry*: $1/f$ noise is the dominant noise component in the accelerometer because MOSFETs are used as stress sensing elements. In advanced CMOS technologies, gate-oxide thickness has been scaled down according to the Moore's law. Assuming the same surface state density and the same gate area of MOSFETs, $1/f$ noise power spectrum is inversely proportional to the thickness of the gate-oxide. So, dominant $1/f$ noise from the circuitry can be reduced using advanced CMOS technology in MOSFET type sensors [18]. This also results in improvement of the minimum resolution of acceleration.
3) *Narrowed Width of Beam Structures*: Because of the narrowed width and multilayered configuration of metal wires in advanced CMOS technologies, width of beam structures can be narrowed as compared to accelerometers using previous CMOS technologies. Therefore, more sensitive structures are formed by narrowing the beam width using advanced CMOS technologies.

From the economical point of view, advanced CMOS technologies make it possible to produce small size (i.e., low cost) integrated accelerometer keeping the same performance on minimum resolution. As a result, cost-performance ratio of CMOS integrated accelerometers will be much improved.

V. CONCLUSIONS

In this paper, a bulk-micromachined three-axis accelerometer fabricated with commercial submicrometer CMOS wafers has been presented for low cost realization of smart accelerometers and improvement of device performance. The signal processing circuitry for detection of three-axis acceleration was formed by a commercial 0.8-μm CMOS technology. In the device fabrication, CMOS post bulk-micromachining processes were perfectly separated from CMOS fabrication process. This makes it possible to utilize many of commercial standard CMOS technologies for fabrication of CMOS integrated bulk-micromachined sensors.

Accelerometers with 3×3 mm^2 and 6×6 mm^2 die size were fabricated with the developed post CMOS bulk-micromachining process. As a result of device evaluation, 2.0 mg_{rms} resolution of Z-axis acceleration, and 10.8 mg_{rms} resolution of X

and Y-axis acceleration were obtained by the accelerometers with 6×6 mm^2 die size. The accelerometer in this study showed much better performance per unit die area on minimum resolution of acceleration as compared to our previous accelerometer fabricated with 5.0-μm CMOS technology. Temperature dependence and reliability for repetitive vibration loads were also evaluated. Through these evaluations, basic performance of the CMOS integrated three-axis accelerometer has been confirmed. As the performance per unit die area increases, cost-performance ratio of CMOS integrated accelerometers will be much improved using advanced CMOS technologies for their circuit integration.

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