3D TSV Processes and its Assembly/Packaging Technology

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Abstract

Demand for Through Silicon Via (TSV) is being driven by the need for 3D stacking to shorten interconnection length, increase signal speed, reduce power consumption and reduce power dissipation. Increasing demand for new and more advanced electronic products with a smaller form factor, superior functionality and performance with a lower overall cost has driven the semiconductor industry to develop more innovative and emerging advanced packaging technologies.

3D packaging using the z-axis TSV stacking concept has been and continues to be investigated by a number of semiconductor manufacturers and research institutes and is believed to be one of the most promising technologies. There is a growing interest in the development and application of this new chip stacking approach to existing and future devices. There are several steps involved in 3D chip stacking using TSV technology. Each of these steps requires different techniques, materials and processes. Applications have to be well understood and integrated in order to successfully be applied.

This paper addresses TSV fabrication processes as well as TSV assembly and packaging. The key TSV processes to be discussed in this paper are TSV formation, thin wafer handling, Cu plating and wafer thinning/CMP to form 3D interconnects. Characterization, advantages and challenges associated with each of these process steps and various TSV technologies will be presented. Packaging challenges and experimental results will be presented for CTW (Chip-to-Wafer) bonding with ultra fine pitch microbump interconnections.

I.INTRODUCTION

One of the hottest topics in the semiconductor industry today is 3D Packaging using Through Silicon Via (TSV) technology. While many research programs have been underway for years, no commercial product has been realized yet. Driven by the need for improved performance and the reduction of timing delays, methods to use short vertical interconnects have been developed to replace the long interconnects found in 2D packaging. The industry is moving past the feasibility (R&D) phase for TSV technology into the commercialization phase, where economic realities will determine the technologies that can be adopted. Low-cost, high aspect ratio, reliable via formation and via filling technologies are the need of the hour. Choosing the right process equipment and materials with innovative design solutions addressing thermal and electrical issues will be the key winner. As functional integration requirements increase, assembly and wafer fabrication companies are looking to 3D TSV technology, which allows stacking of LSIs thereby enabling products to be made smaller with more functionality. 3D technology realizes miniaturization by 300-400% compared to conventional packaging.

Understanding this need well in advance, 3D TSV packaging achieves physical size reduction, shorter interconnect between chips allowing higher operating speeds, lower power consumption, and reducing the need for large input/output drivers. Also understanding the system integration requirements as projected by ITRS roadmap 2008, an ultimately more important reason, is the opportunity for heterogeneous integration of different technologies requiring diverging process flows-such as analog, logic, memory, and MEMS-being finally stacked to build a system. Heterogeneous integration provides many advantages, particularly with respect to cost, performance, time to market.

The demand for high density and multifunctional microelectronics leads to the development of 3D and wafer level packaging, which provides an optimal solution for the shortened interconnects, increased performance and functionality, miniaturization in size and weight, integration of hetero-generous technologies and complex multi-chip systems as well as reduced power consumption. Such packaging technology normally requires the use of ultrathin devices (less than 100μm in thickness). The key benefits from thinned wafers include improved heat dissipation and reduced electrical resistance which offers better flexibility for 3D stacking. However, it brings up a challenge for assembly and packaging; thinning and handling ultrathin semiconductor devices in both front-end and back-end processes due to its fragility and tendency to warp. [3]

In this paper, key topics of TSV formation and assembly/packaging issues, microbump, thin wafer handling, underfill and warpage are to be discussed with experimental data.

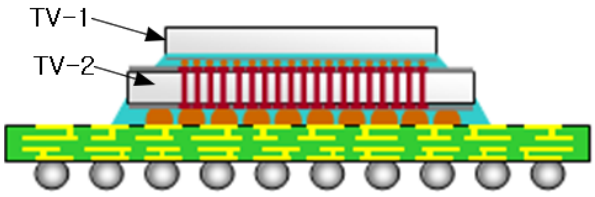

Figure 1. Schematic of 3D stacking of the Si chip of microbump and TSV in flipchip packaging

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II. TSV TECHNOLOGY

TSV technology requires TSV formation, post-TSV process and assembly as well as design/test/characterization techniques. All should be well established for TSV products. For TSV formation technology, there are three technologies as shown in Fig.3; tapered via, vertical lining via and vertical solid via. The application depends on process and device requirements.

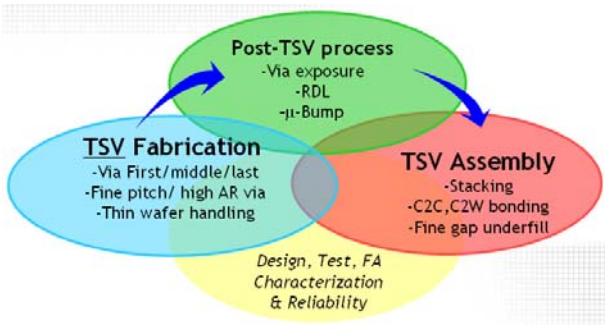

Figure 2. TSV Enabling Technologies

i) Vertical via - vertical via is suitable for finer pitch (<100μm). The interconnection will be partial metal disposition (lining) or solid metal filling. Lining has less thermomechanical stress (Si CTE is ~3ppm/K but Cu CTE is 20ppm/k) and an easy process compared to solid via, but emptiness of the via will cause reliability issues.

ii) Tapered via - Taper Via is suitable for lower I/O Count device, with larger pitch (> 150 um). It is used for power amplifier (PA) backside ground applications and CMOS TSV image sensors.

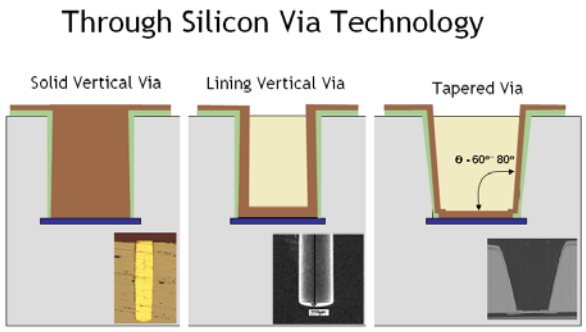

Figure 3. Various TSV technologies

III. TSV FORMATION PROCESS

The various critical technology challenges associated with integration of high-aspect ratio through silicon via (TSV) to form a reliable through-silicon interconnect structure can be identified as deep damascene copper via filling, CMP and finally by wafer thinning process. Process intergradations of TSV are quite critical for reliable interconnection. Though there are a wide range of techniques for forming high aspect ratio deep silicon via structures like Bosch etch process[4], cryogenic etch process[5], laser drilling[6] and powder blast micromachining[4], these methods in their original form yield extremely vertical profiles which makes them less suitable for realizing a reliable void-free through silicon interconnection. The main challenges that need to be addressed are to achieve (a) smooth via sidewalls, (b) uniform deposition of dielectric isolation layer over the via sidewall, (c) continuity of copper diffusion barrier and copper seed metallization and (d) void-free copper electroplating. As the aspect ratios of deep silicon, vias continue to increase it becomes more challenging to accomplish any of these requirements without making modifications to via profile. The via shape is to gradually taper the via profile to mitigate the problems associated with plasma enhanced chemical vapor deposition (PECVD) and physical vapor deposition (PVD) processes which are ion-assisted processes and hence tend to yield non-conformal film deposition. Via profile tapering further helps in accomplishing a void-free copper electroplating process [7].

A. TSV process

Via-first process is to design it in at the start and then physically create the via before CMOS or BEOL metallization. With via-first, the dimensions of the vias are typically smaller (5–20 μm wide), with aspect ratios of 3:1 to 10:1. This is the approach typically taken by IDMs. The other alternative, "via-last", is to create the via after BEOL or bonding, essentially when the wafer is finished. In this case, the processing can be done by the IDM or packaging house. The dimensions in this case are wider (20–50 μm), with equally challenging aspect ratios of 3:1 to 15:1. And there are a wide range of TSVs demonstrated from as small as 1 μm that may only be about 10 μm deep to, on the other end, 90-μm-vias more than 400 μm deep.

Part of the reason for the wide disparity in via sizes is that packaging houses (which, by nature, are doing a via-last process) typically have access only to lower-tech PVD equipment for depositing the barrier/seed layer, and these tools are not capable of handling aspect ratios much beyond 3:1 to 5:1. Because the vias need to be fairly deep through thicker wafers in the 200–300 μm range, the via needs to be correspondingly large (i.e., 100 μm wide) to have a low aspect ratio. The route to smaller vias with higher aspect ratios is either through investment in more advanced PVD, CVD equipment or through "electrochemical seed-layer enhancement" technologies by wet coating process.

B. Cu electroplating

For solid via Cu plating, there are several concerns on;

i) plating time

ii) minimum overburden

iii) void-free plating

Copper filling must be performed so that the final copper plug is void-free to allow normal electrical performance of stacked device at elevated temperatures. If there is a CTE mismatch between copper and silicon, there is likely to be reliability problems. It could be as bad as cleaving the wafer during annealing.

The Cu plating chemical bath and plating tool are quite closely related to each other thus each industry is working together to achieve high aspect ration plating with faster process time. In addition to these developments, control of organic additives also play critical role in conformal and void-free copper filling of TSVs. With the TSV process gaining full acceptance in high-volume manufacturing of the next generation of semiconductors, reliable metrology is of utmost importance. When combined with non-reagent techniques used for the analysis of inorganic components, the metrology tool becomes fast and effective with a low cost of ownership.

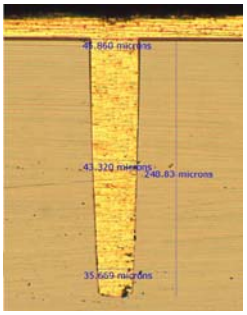

Figure 4. Solid Cu via plating of 50um via and 250um depth

C. Thin wafer handling

To save TSV area on Si and Cu plating time, smaller via size is preferred thus wafer thickness is also thinner. So handling this thin wafer (~50μm) is quite challenging and critical for the overall TSV process. In the thin wafer handling process, there are 3 major approaches in the industry;

i) UV curable epoxy/glass bonding – Using glass wafer as supporting, dispensed UV curable epoxy to bonding and debonding

ii) Polymer adhesive – Using high temperature polymer materials to meet process temperature needs and debond from support wafers @ 200~250^{o}C

iii) Electrostatic bonding – Using electrostatic bonding, wafer can be temporary attached to electrostatic chuck for several hours.

Each process has its own advantages and problems to be solved. But still there are many ways to overcome current issues to get better process stability and repeatability of handling TSV thin wafers to meet industries' different and varying needs, such as temperature and chemical stability, temporary adhesion strength et al. For example, Polymer bonding/debonding process is based on high temperature, so it may not suitable for solder bumped wafers. And 12" wafer applications have more challenges than 8" applications and need to optimize the process as well as materials for larger area bonding/debonding.

C. TSV Wafer Thinning/CMP

Exposing the buried copper via in the silicon wafer is a challenge because it requires grinding brittle silicon and ductile copper simultaneously. Also machining copper leads to smudging on the wafer surface and further contamination of the substrate. The conventional backgrinding wheel is resin bonded, which is not suitable for ductile copper. Therefore, a special grinding process using low mesh density verified bond wheel is necessary. The wafer surface is smooth after via exposing and no contamination of copper on the wafer surface.

IV. TSV ASSEMBLY AND PACKAGING

A. Microbump process and reliability

To evaluate the interconnection with microbump, test vehicles were fabricated on 8 inch size wafer. A test chip of 5 X 5 mm2 size was designed with >10000 I/O off-chip interconnects at 40 / 50 μm pitch in fully populated rows using Re-distribution layer (RDL) to evaluate the chip-to-wafer (CTW) bonding interconnections. Test vehicles fabrication is based on photolithography and electroplating processes, which is compatible with conventional IC fabrication.

Flip chip package assembly was carried out to investigate the bonding quality and interconnections with microbump flip chip. After flip chip die fabrication with bump, the die attachment was carried out with thermo-compression flip chip bonders. Several DOEs were carried out to find optimized process conditions as functions of time, stage temperature, pickup tool temperature as well as pressure.

40μm and 50μm both microbump test vehicles were sent to JEDEC standard reliability tests. Reliability samples passed MSL-3 with 3x reflow process at Pb-free 260^{o}C peak temperature. All samples passed unbiased HAST and HTS reliability tests. There was no failure found after 500 T/C and 1000 T/C is still under testing.

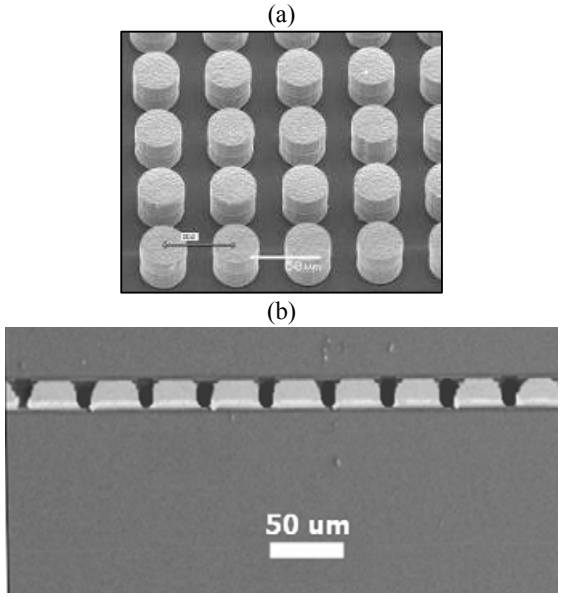

Figure 5. SEM micrograph of 50um pitch; (a) bump and (b) cross-section of CTW bonding.

B. TSV assembly

Thin wafer handling system

There are many ways to overcome current issues to get better process compatibility and repeatability of handling TSV thin wafers for packaging process. Because the TSV wafer is thinned down to 50um thickness, handling of this wafer for

packaging process is another challenge in order to meet the different and varying needs, such as temperature and chemical stability, temporary adhesion strength et al. For example, polymer bonding/debonding process is based on high temperature, so it may not suitable for solder bumped wafer. And 12" wafer applications have more challenges than 8" applications and need to optimize the process as well as materials for larger area bonding/debonding.

Thin Die Warpage

Package warpage is also a challenge in the assembly process and reliability so the test vehicle as shown in Fig. 6 was fabricated with 50µm thin die and 150µm pitch Pb-free solder bump. The warpage was measured with a reflow temperature profile with THERMOIRE-PS400 as shown in Fig. 7. It showed after reflow process, the thin flip chip die warpage difference was 60 um at room temperature between before-reflow and after-reflow. This serious warpage causes higher stress in TSV structures thus catastrophic failure will happen at the package level. Therefore, it should be studied more and characterized with further experiments.

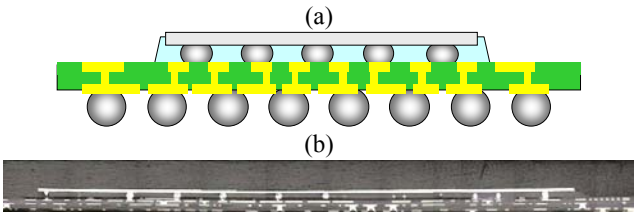

Figure 6. Package warpage test vehicle of (a) schematics and (b) optical micrograph of cross-section.

Table 1. Warpage behavior with reflow profile.

Temperature		R.T.	125℃	235℃	175℃	125℃	75℃	R.T.
50 um	3D Contour Plot							
	Actual Behavior	Smile	Smile	Smile	Smile	Neutral	Crying	Crying

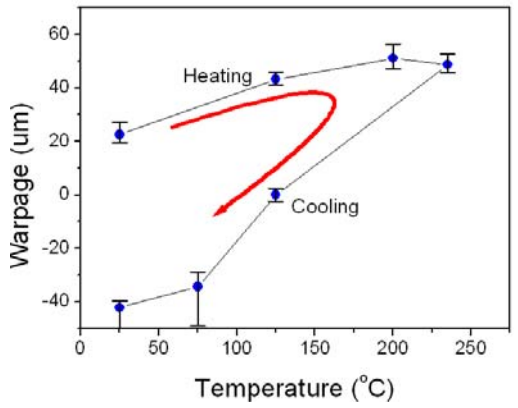

Figure 7. Plot of warpage behavior with temperature profile for thinned flipchip packaging after underfill process.

Evaluation of underfill of thin die

The gap between the microbump joint of CTW bonding is about 15 ~ 20 µm; therefore, it is important to evaluate the flow-ability of underfill and the void formation in underfill which contains silica-filler. Considering the fine chip-to-wafer (CTW) gap, fine filler size underfills were used to evaluate the underfill process. Scanning Acoustic Microscope (SAM) analysis was carried out to investigate the void formation or non-filled area by underfill. Through-SAM photograph of underfilled, it was observed that good filling without any void could be achieved with underfill resin containing very fine filler.

Using the test vehicle in Fig. 6, underfill performance was evaluated and process was optimized for two different aspects; bleeding and overflow on top. The flip chip die is thin, so overflow may contaminate RDL layer of TSV. Fig. 8 showed the overflow of underfill material on top of thin flip chip packaging. For Fig.8(a) overflow on top was observed around 270µm. In this case process optimization is not as effective to minimize the overflow so the material was changed to lower Tg (glass transition temperature), higher viscosity and finer and less filler material. After reoptimized the process with new underfill material, the overflow was decreased to 40µm as shown in Fig.8 (b).

As shown in Fig. 9(a), bleed-out was serious and around 1000µm distance was observed. After process reoptimization of stage temperature and dispensing time and quantity control, it was reduced to 200µm as shown in Fig. 9(b)

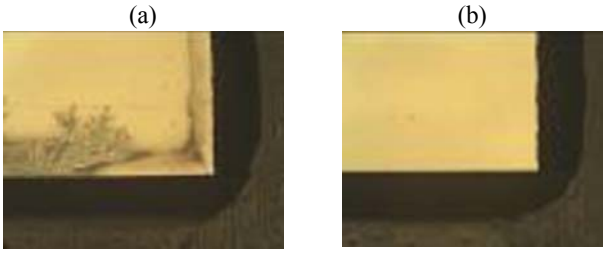

Figure 8. Optical micrographs of underfill overflow.

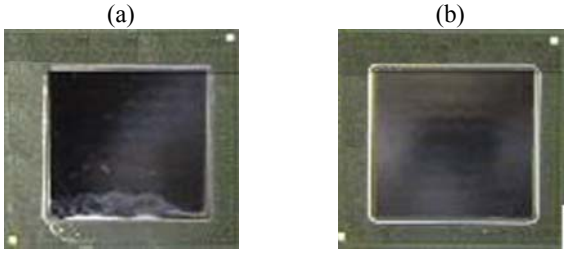

Figure 9. Optical micrographs of underfill bleed-out; (a) before process optimization and (b) after optimization.

V. CONCLUSION

In this paper, TSV processes and TSV packaging/assembly issues were discussed. For successful implementation of TSV technology to microsystem products, TSV process and TSV

packaging/assembly both should be well prepared and established with close collaboration and clear understanding.

There is no question that 3D TSV will be adopted, but the timing for mass production depends on how the TSV technology compares in terms of cost with existing technologies. CIS mage sensors for camera modules are already in mass production. For other applications, the adoption time is longer than originally expected, as is quite common with the introduction of new technologies. TSV technology itself is not a packaging technology apart from a few exceptions. 3D TSV and 3D packaging do not have to be considered as competitors but more as complementary areas. In recent years, the semiconductor industry has expressed some growing interest in these ideas and put some significant efforts in allowing the emergence of these new breakthrough technologies. Still, some challenges remain ahead for a wide adoption including cost, a shift in the design method paradigm, system co-design, new CAD tools, new architectures, and more new challenges. While progress is being made, design, thermal, reliability and testing issues remain a barrier to TSV adoption in some applications.

There should be further study and understanding of TSV cost-ownership analysis, value-chain and systematic analysis of competitive advantages of TSV in business perspectives in order to move into high volume manufacturing. There is a common awareness that, although TSV could be adopted quickly in RF and memory based applications as described before, the industry is still lacking real test strategies to evaluate the reliability of these TSV interconnects. TSV engineers and researchers have been very focused on developing 3D TSV processes, but testing of these interconnects is still at its early stage. This is a very similar situation to SoC, SiP and WLP. A test strategy and methodology have to be defined in order to decide which type of measurements need to be made at which level (wafer, micro bumping, Chip-to-Wafer/Wafer-to-Wafer) bonding, packaging/assembly, final test) and which test infrastructure needs to be set up.

In conclusion, the design, wafer fab process, packaging/assembly process, materials and reliability considerations as well as testing should be well integrated and understood as a whole value chain for final manufacturing of 3D TSV integration and interconnects technology.

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