Chapter 2
System Integration by Advanced Electronics Packaging

Klaus-Jürgen Wolter

2.1 Introduction

System integration, the combined integration of circuits, components and devices with the goal to create a higher functionality of electronics, has a long tradition in electronics and has been using different methods so far. Well known are the applications of printed circuit boards (PCB), of multi-chip modules (MCM), package on package (PoP) and system on chip (SoC) and system in package (SiP) solutions on the first and second interconnection level of electronics packaging [8, 16].

Development in packaging and interconnect technologies was driven by increasing functionality of semiconductor devices and higher end user expectations in the recent past. Silicon integration has reached the "System on Chip" level for some applications, requiring fewer chips and less circuit board integration. Especially SoC integration meets the consumer demands for compact and highly reliable electronic products. The top three categories within the total semiconductor market using SoC integration and requiring increasing packaging density were computers, consumer electronics and communications.

The computer industry has driven the packaging industry for the past 30 years, first of all to support mainframes and then to support PCs. High pin count ceramic packages and high density MCMs were needed for high end computers in the 1980s. Low-cost plastic packages and printed circuit boards were the response to PC requirements in the early 1990s. The communication industry has leveraged almost the same technologies as the computer industry. The ASICs with their higher number of I/Os, used for communication applications, pushed the packaging technology also to higher frequencies.

The consumer market, especially the portable market, was undergoing the most and revolutionary growth. The need for low cost, small sizes and low power has

K.-J. Wolter (✉)
Electronic Packaging Laboratory, Technische Universität Dresden,
01062 Dresden, Germany
e-mail: wolter@avt.et.tu-dresden.de

G. Gerlach and K.-J. Wolter (eds.), *Bio and Nano Packaging Techniques for Electron Devices*, DOI: 10.1007/978-3-642-28522-6_2,

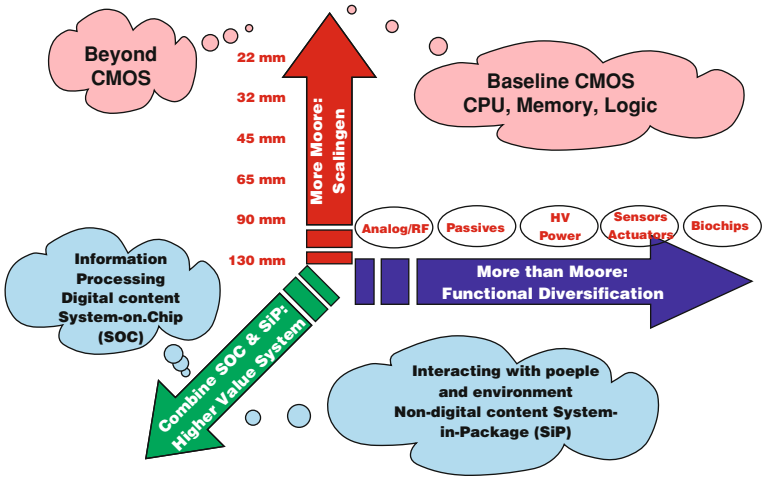

Fig. 2.1 Trends in scaling and integration of electronics [16]

driven the development of thin and small plastic packages, chip on board and direct chip attach technologies as well as fine-line substrates. The market drivers and the requirements for performance pushed the semiconductor devices to scaled geometries, less power, smaller sizes and lower cost. The scaling of CMOS structures "more Moore" will not be able to meet the actual and future demands of the drivers due to the functional diversification of electronics, physical limits of CMOS-technology and growth of costs.

SoC and SiP are technologies which have the potential to continue the improvement in performance, size, power, and cost of electronic systems (Fig. 2.1). Both technologies have advantages and disadvantages with the respect to system integration.

- SoC is a way to increase functional integration by including sub-systems on a single chip. For this more than just digital functions have to be incorporated into an integrated circuit, e.g. analogue-to-digital and digital-to-analogue conversion.
- SiP combines of multiple active electronic components of different functionality, assembled in a single unit. This enables multiple functions inserted into a system or sub-system. A SiP may also integrate passives, MEMS, optical components and other packages [16].

Three-dimensional integration is an attractive way for bringing together of various functional blocks in a vertical fashion. Hence the reduction of package sizes leads to shorter signal and power interconnects and results into lower signal propagation delay and power consumption [5].

The advances of 3D-integration can be also used for "more-than-moore" approaches, where a hetero system integration of processors, memories, sensors and actuators forms an interface between electronics and environment.

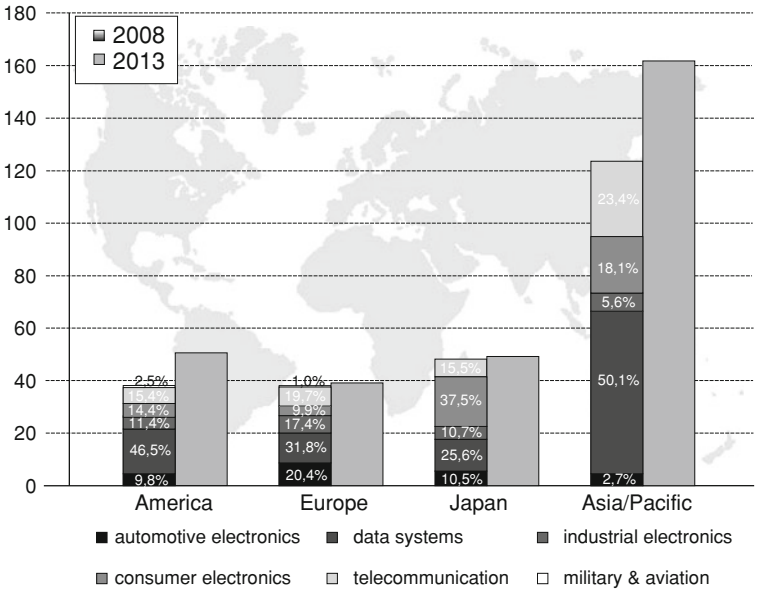

Fig. 2.2 Semiconductor market by regions and products [37]

2.2 Drivers of System Integration

In the past system integration technologies were driven mostly by semiconductor devices, by their signal frequencies, power consumption, pin counts, pitches, and sizes. Nowadays it can be observed that system integration technologies are more and more driven by diverse applications of electronic systems [17]. Figure 2.2 illustrates the semiconductor market for different market segments and for different regions.

The worldwide semiconductor market was achieving a volume of 249 billion US $ in 2008 and will grow up to 301 billion US $ in 2013 [37]. Data systems market captures 42% of the worldwide semiconductor market followed by communication and consumer markets each with 21% and industrial electronics with 9.3% and automotive with 8% of semiconductor market.

2.2.1 Drivers of System-on-Chip-Technology

SoC technology was originally developed for high volume custom devices by using design elements from different semiconductor devices or by using of reprogrammable logic. The advantages of this technology are a high density of functions, high on-chip frequencies, high reliability and moderate unit costs. SoC has also significant disadvantages which are a strong dependency of system functionality from selected

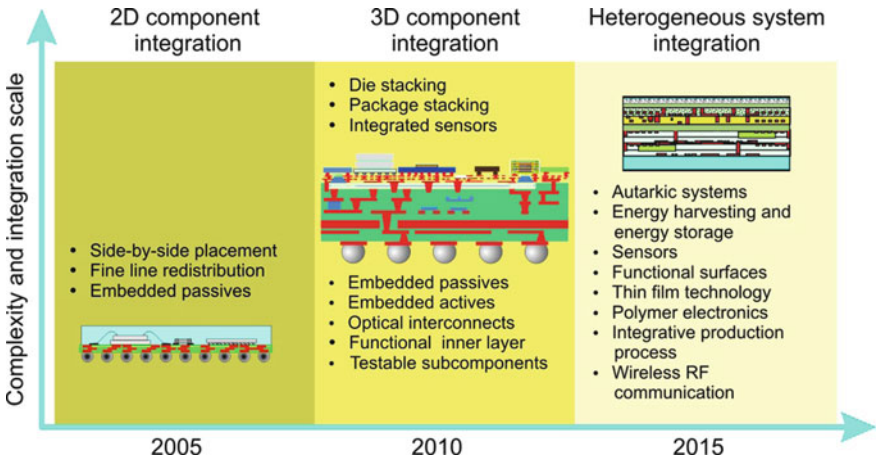

Fig. 2.3 Trends in System-in-Package technology [38, p. 32]

chip technology, higher onetime costs for system design and testing and a longer time to market.

The applications of semiconductor devices in multicore processing and portable consumer electronics are the main market drivers for SoC.

2.2.2 Drivers of System-in-Packages-Technology

SiP technologies are more and more penetrating products of the mentioned market segments due to their benefits of a rapid time to market and lower overall costs. These technologies enable systems with high functional density by use of a wide range of chip technologies.

Starting with a side-by-side placement of devices, SiP is now going to use 3D-integration to shorter circuit-to-circuit interconnect lengths and to enlarge interconnect densities. In this way 3D-integration offers a higher bandwidth and lower power consumption of interconnects. 3D-integration can be realized by 3D-packaging like package-on-package or by die stacking with high efficiency by use of through silicon vias (TSV) [36].

SiP and especially 3D-integration technologies will be the basic technologies for realizing smaller portable and hand-held products, for faster networking and communications, for medical and bioengineering applications as well as for miniaturized sensors and actuators. These products will be achieved by so-called hetero system integration. They can be realized as autarkic systems with energy harvesting and wireless communications (Figs. 2.3 and 2.4).

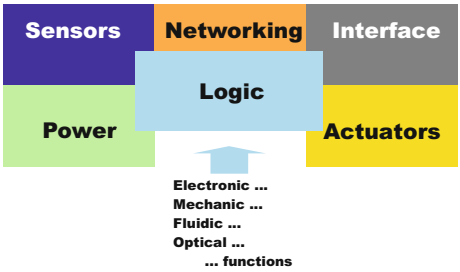

Fig. 2.4 Functional blocks for hetero system integration

2.3 System-in-Package Technologies

System-in-Package technologies enable the integration of circuits and discrete components in systems and thus getting an enhancement of performance and smaller sizes [35].

SiP can be made based on existing technologies (rigid and flexible interposer, lead frames, package on package, die stacking). Assembly technologies which are used cover through-hole assembly, surface mount assembly, direct chip attach and wafer level technologies. Interconnections between circuits and devices can be realized by well-known first level interconnection technologies like wire bonding (see Fig. 2.5; Table 2.1) and flip-chip techniques by using solder bumps [4].

Figure 2.5 presents an overview of state of the art SiP technologies.

Beside the advantages of SiP technologies one have to keep in mind also the challenges of SiP resulting from higher complexity and thus from higher density of power dissipation. In particular the large mismatch of the coefficients of thermal expansion of heterogeneous components has a decisive influence on interconnect reliability. Materials, interfaces and interconnect technologies have to minimize the mechanical stresses in interconnects.

2.4 3D-Integration

3D-integration offers a new way of increasing system performance and can be defined as any technology that stacks semiconductor elements on top of each other and utilizes vertical interconnects between the elements [34].

Different technologies are in use for 3D-integration to build up electronic systems with

- higher functionality
- lower volume
- lower electrical parasitics of interconnects
- higher density of interchip interconnects
- lower high-volume manufacturing cost.

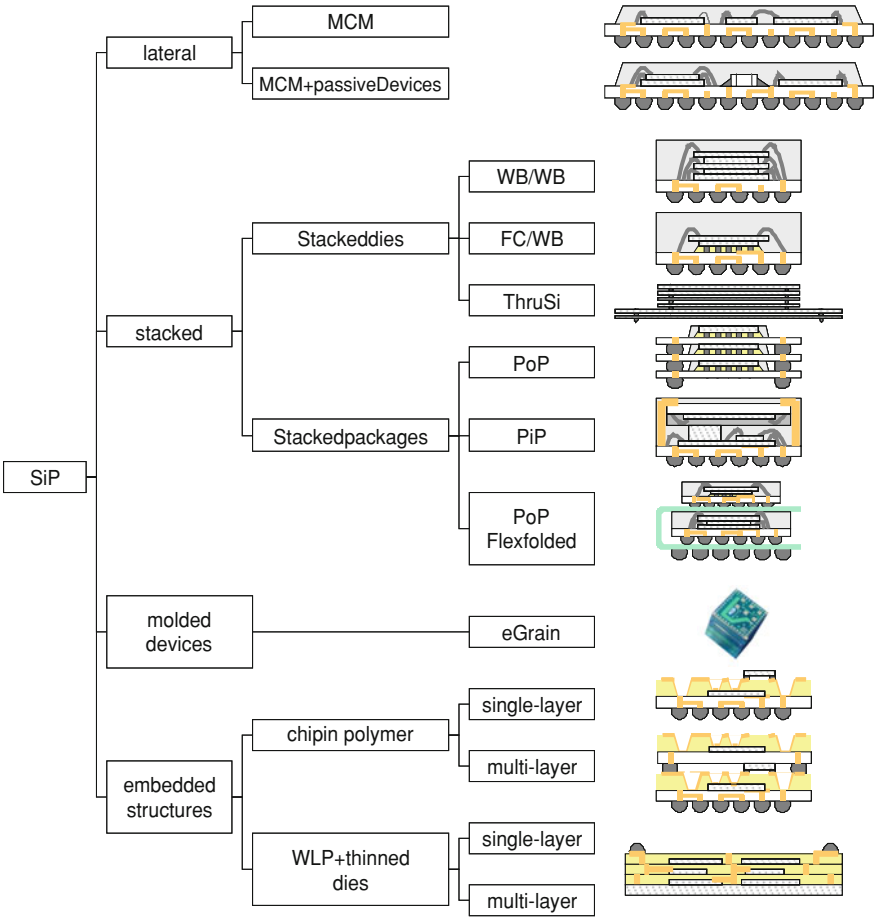

Fig. 2.5 State-of-the-art of System-in-package technologies [25, p. 3]

Table 2.1 Chip-to-package pitches [34]

Year of production	2010 (µm)	2013 (µm)	2015 (µm)
Wire bond single in line	35	30	25
Wire bond-wedge pitch	20	20	20
Flip-chip area array (organic andceramic substrate)	130	110	100
Flip-chip on tape or film	10	10	10

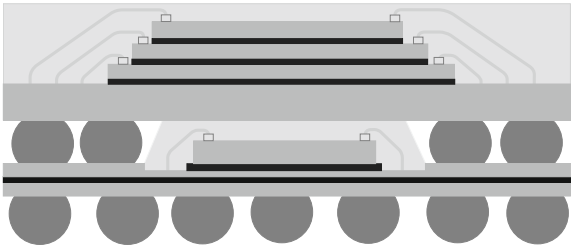

Fig. 2.6 Package-on-packages [16]

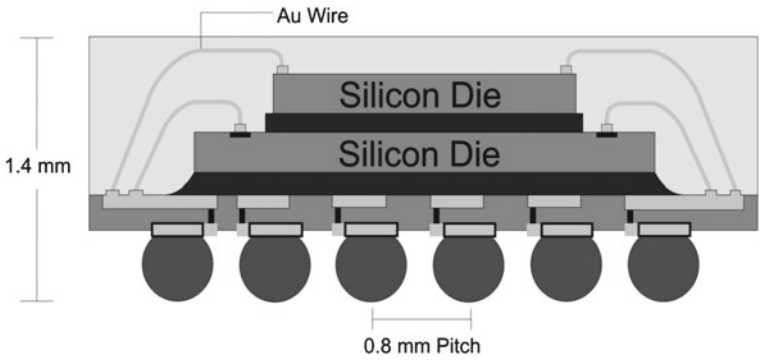

Fig. 2.7 3D-packaging [4]

2.4.1 3D-Integration Technologies

The 3D-integration technologies can be distinguished between homogeneous and in heterogeneous techniques. Integration of dies with the same functionality is named homogeneous 3D-integration and is used mostly for memory stacks [8]. Heterogeneous 3D-integration combines dies of different functions like processors, sensors, memories and RF-components in one stack packages [18]. The challenges which have to be met with respect to the wide range applications are

- die yield and its impact on 3D-integration,
- thermal management at high power densities,
- 3D design tools.

Technologies for 3D-integration which are used so far are (see Fig. 2.5)

- stacking of packaged dies (package on package) (Fig. 2.6),
- stacking of dies, chip to chip (3D-Packaging) (Fig. 2.7),
- wafer level 3D-integration (3D-WL), chip to wafer, wafer to wafer (Fig. 2.8),

Table 2.2 compares characteristic features of 3D-packaging and of 3D-WL packaging.

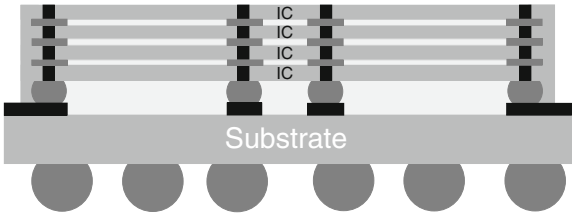

Fig. 2.8 3D-WL integration

Table 2.2 Features of D-integration [30]

Technology	3D packaging	3D-WL integration
Infrastructure	Packaging	Foundry
3D interconnect	Bond wires, FC	Through silicon vias
Active layer thickness	>50 µm	<50 µm
I/O density (cm^{-2})	10^4–10^5	10^5–10^8

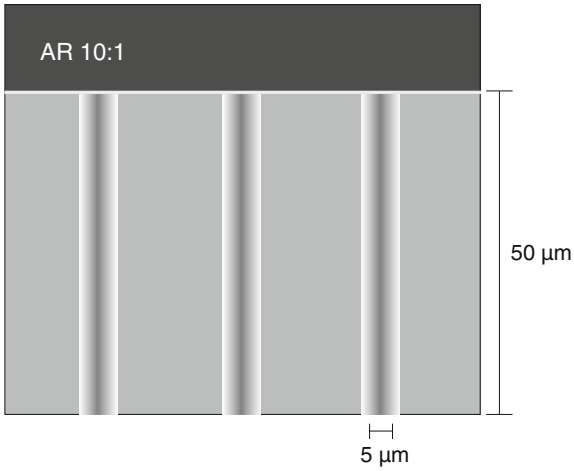

Fig. 2.9 Cross-section of a TSV for 3D-WL integration [31]

2.4.2 Through Silicon Via Technology

Through silicon vias (TSV) are the key feature in 3D-WL integration. The size of the TSV is substantially smaller than a wire bond or a solder bump (Fig. 2.9).

TSV technologies require wafer thinning, wafer drilling, via oxidation for electrical insulation and via filling with conductive material. There are two drilling technologies in use, plasma drilling and laser drilling. TSVs are mainly fabricated by the Bosch process, which is applies a repetition of oxidizing the silicon via and dry etching the bottom of the vias [26]. The aspect ratio (thickness of die to diameter of via) is limited due to the limitations given by the via filling technologies. Fine-pitch

Table 2.3 Technical parameters of TSVs [15]

Year of production	2010	2011	2012	2013
Number of stacked dies	>9	>9	>9	>9
Minimum TSV pitch (μm)	5.0	4.0	3.8	3.6
Maximum aspect ratio of TSV	10	10	10	10
TSV exit diameter (μm)	2.5	2.0	1.9	1.8
TSV layer thickness for min. pitch	15	10	10	10

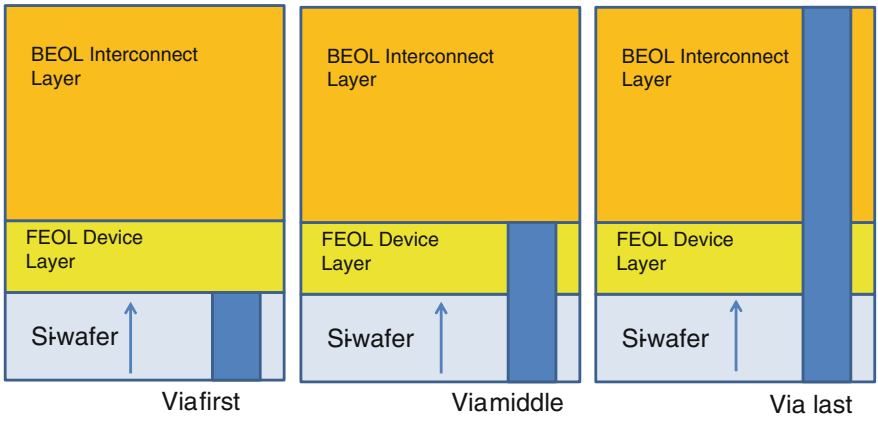

Fig. 2.10 Via technologies. *BEOL* back end of line, *FEOL* front end of line

vias are filled with copper or tungsten, laser drilled via can be filled with conductive paste and other materials.

Table 2.3 presents key technical parameters for stacked packages using TSV.

The process flow for fine pitch via can be configured as via-first, via middle or as via-last process, (Fig. 2.10) [3].

The small sizes of TSV enable a higher interconnect density and exhibit lower signal delay and lower power consumption. Table 2.4 compares parasitic parameters of TSV contacts with that of for wire bonds and flip-chip contacts.

As it was already mentioned before the high density of consumed power in 3D-integration is expected to offset the advantages of this technology due to the degradation of performance and reliability. It is obvious that the thermal management will become more challenging if many 2D chips are integrated by 3D stacking. In particular the heat transfer is becoming a limiting factor due to the low thermal conductivities of the dielectric layers between the dies [27].

A second limiting factor arises from the yield of untested dies combined in a 3D-WL package. The so called "known good dies" problem has a big influence on the cost structure for this type of packages. When combining n untested dies from wafers with a die yield y_i, the yield of the stacked package y_{3D} will be [6]:

Table 2.4 Comparison of parasitic parameters for different interconnect technologies [30]

	Wire bond	FC contact	TSV contact
Resistance	122 mΩ	1.2 mΩ	1.7 mΩ
Capacitance	25 fF	<1 fF	–
Inductance	2.6 nH	0.2 nH	0.05 nH
Pitch	100 µm	200 µm	4 µm

$$y_{3D} = \prod_{i=1}^{n} y_i \cdot y_s^{n-1}$$

where y_s is the yield of the stacking process.

2.4.3 3D-Die Assembly Technologies

Technologies for 3D-assembly are still very challenging. There are different approaches to arrange semiconductor dies in a vertical stack as chip-to-chip assembly, chip-to-wafer assembly or as wafer-to-wafer assembly.

The key assembly processes for 3D-integration by die-stacking are

- wafer thinning and singulation,
- handling of thin dies and
- low temperature bonding technologies for TSVs.

After wafer processing the wafers have to be diced into individual dies usually by mechanical sawing. Beforehand the wafers are mounted on a tape frame. The "dicing-before-grinding process" (Fig. 2.11) is in use for minimizing the backside chipping of thinned wafers. The wafers are only partially diced and the singulation occurs after backgrinding.

Another key process is the handling of wafers for processes like chemical–mechanical polishing, lithography, wet etching, vacuum deposition, plasma processing or backgrinding. For this purpose rigid substrates are used, mostly made out of silicon or glass. After completing all required processes the handle substrate has to be removed from the device wafer and will be supported by tape frames for dicing or later for die to wafer bonding.

Following key processes are the assembly and the bonding either as die to wafer or as wafer to wafer processes [20]. Alignment accuracy for these processes is a challenge and will limit the number of TSV to TSV interconnects.

Die-to-wafer bonding permits the integration of dies from different wafers and allows the assembly of "known good dies" to "known good receiver dies", which is a great economic advantage. Bonding processes for the 3D-integration are still under investigation [1]. Technologies for bonding play a significant role for achieving the desired functional performance, the reliability and low cost for the stacks.

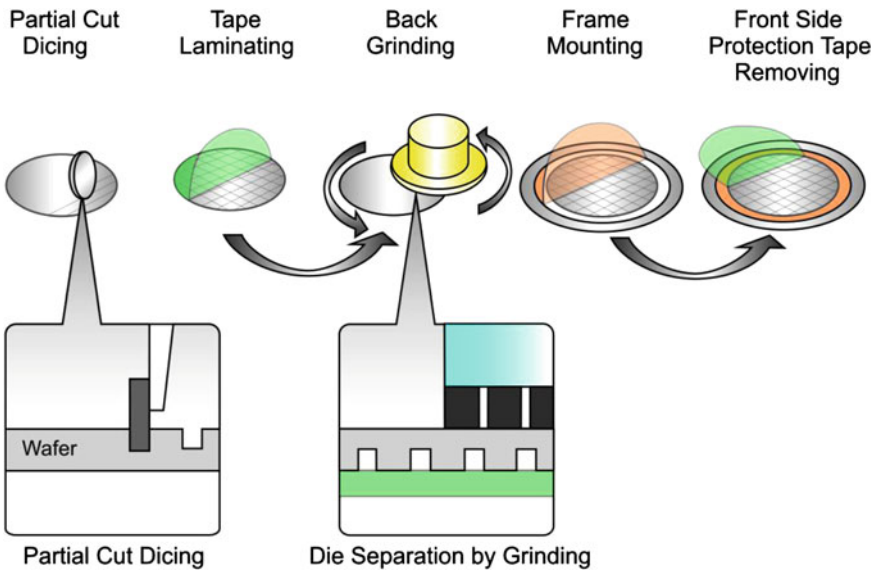

Fig. 2.11 Dicing-before-grinding process for singulation [10]

Two approaches are favored:

- The solder-based bonding uses the solid-liquid interdiffusion (SLID) of Cu with thin layer of Sn. SLID is applying soft-soldering material with a low melting temperature resulting in a high-melting and brittle joint, formed by intermetallic compounds (IMC), (Fig. 2.12). The difference between the low melting temperature of the solder material and the melting temperature of IMCs allows a sequential multi-level chip stacking at low process temperatures without remelting of joints [19, 30].
- Cu-to-Cu bonding can be performed as surface activated Cu bonding at room temperature or as thermal compression bonding which is more spread in 3D-integration. Cu pads demand uniform height and smooth and free of oxides surfaces. The bonding process has to be arranged in a vacuum chamber by application of high contact pressure and temperatures up to 350°C for 2 h [7].

2.5 Challenges for Packaging Materials

The demands for higher miniaturization, higher integration of functions, higher clock rates and higher reliability influence almost all materials used for advanced electronics packaging. The most important challenges regard the:

- electrical,
- thermal and
- mechanical properties

of conductors, semiconductors and isolators.

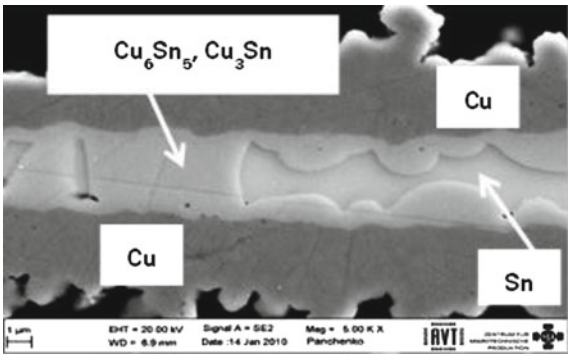

Fig. 2.12 Cross section of Cu-Sn SLID interconnection [24]

2.5.1 Substrate and Interposer

Substrate or interposer materials have a big influence on a wide range of performance of SiPs. The requirements on substrate materials depend very strongly on the application of the electronic system. Most used types of substrates are rigid or flexible organic substrates as well as ceramic, glass and silicon substrates. The substrate material has to be chosen considering the following physical properties [23]:

- dielectric constant
- dielectric losses
- coefficients of thermal expansion in all three special directions
- thermal conductivity
- water absorption
- Young's modulus
- peel strength

Organic rigid or flexible interconnect substrates with base materials like epoxy glass, polyimide or bismaleimide triazin are widely used in electronic products due to their excellent electrical properties and low costs, but these materials have limitations with respect to their thermal and thermo-mechanical properties [9, 13].

Currently, silicon substrates are attracting more and more interest. Silicon substrates allow a higher wiring and interconnecting density, better thermal management and a higher reliability due to the same thermal expansion of die and substrate [39] (Fig. 2.13).

Glass as an interposer material offers also several advantages, in particular, a coefficient of thermal expansion well matched to that one of silicon, excellent surface flatness, dimensional stability, high electrical resistivity and the availability in thin and large panels [29].

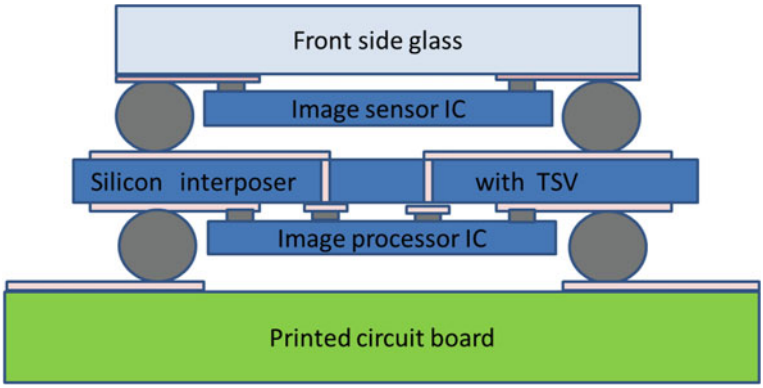

Fig. 2.13 Image sensor with silicon interposer

2.5.2 Interconnection

a. Metals

State-of-the-art interconnections for SiP are manufactured either by wire bonding or by flip-chip technology. These technologies will dominate the mass production of SiP also in the near future. Materials used for bond wires are gold (Au), aluminum (Al) and copper (Cu). To meet the demands for interconnection density the diameter of wires will shrink down to 10 µm or even lower. Solder bumps and copper pillars are elements for interconnections for stacking dies. Further shrinking of pitches (<10 µm) and the application of environmentally friendly materials (lead-free solder) are in the focus of investigations [11]. Especially the microstructures of these materials and interfaces influenced by manufacturing processes and aging exhibit a high interest because of their decisive influence on reliability.

b. Carbon Nanotubes

Since there is a demand for higher density of interconnections, new materials have to be introduced which are able to cover the needed current densities and to avoid electro migration. Carbon nanotubes (CNT) or metallic or carbon nanowires are attracting growing interest of researchers.

CNT are carbon allotropes offering remarkable electrical, thermal and mechanical properties. The structure of a CNT is a cylindrical hollow tube which consists either of one layer of graphene (Single wall CNT—SWCNT) or of two or more shells of graphene (Multi wall CNT—MWCNT). The diameter of CNTs are in the range of 1 nm (SWCNT) to 30 nm (MWCNT). CNTs exhibit a typical length in the µm- to mm-range. CNT are metallic or semiconducting depending on the chiral angle of the grapheme sheet rolled up. For electrical interconnections the high current carrying

capacity (up to 10^9 A/cm^2) and the high resistance to electromigration of metallic SWCNT or MWCNT are of interests [22].

Another attractive application of CNTs is their use as thermal interface material in electronic packages. 3D-packaging and wafer level packaging require materials with improved thermal properties. For better heat flow in 3D-packages, materials are needed with a higher thermal conductivity, lower interface resistance and improved adhesion.

The application of CNTs as interconnection or thermal interface material is facing many challenges:

- difficulties for separating the metallic and semiconducting CNT,
- realization of effective and reliable contacts at CNT junctions and
- handling of CNTs.

The most remarkable mechanical properties of CNT are their high Young's modulus, high tensile strength and low thermal expansion. They are the reason that CNT were applied as filler materials in polymer composites to increase thermal conductivity and to decrease thermal expansion. Polymer-CNT composites applied in isotropic conductive adhesives were offered to secure reliability of interconnects. The compliancy of those interconnects can reduce the thermo-mechanical stress associated with CTE mismatch of materials [14].

The application of Cu-CNT composites also pursues the goal to decrease the mismatch of thermal expansion between copper and silicon [2].

2.5.3 Embedded Components

Embedding of passive components into packages is very important for further miniaturization of electronic systems. Due to the higher number of passives in a system in comparison to active components miniaturization of passive components is of increasing interest. In particular, to maintain large-enough capacities, high k-materials are needed for embedded capacitors (Fig. 2.14).

Table 2.5 presents typical values for wafer level embedded passive devices [15]:

2.5.4 Nanomaterials

One way to improve packaging materials consists in the application of nanomaterials. Physical properties can change by shrinking dimensions into the range of nanometers:

- improved electrical conductivity increase due to ballistic transport of electrons between nanoparticles,
- melting point depression,
- sintering by surface self-diffusion,
- mechanical strength increase,
- chemical activity enhancement.

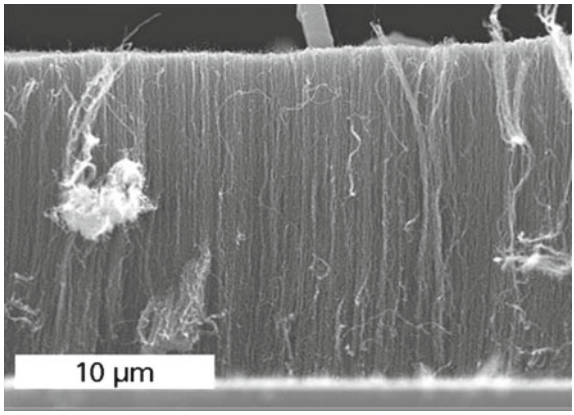

Fig. 2.14 Aligned CNTs on substrate for thermal interconnection [14]

Table 2.5 Typical values for wafer level embedded passive devices

Passive device	Value range	Example of material
Resistor	10 Ω . . . 150 kΩ	NiCr, 100 Ω/sq
Inductor	(1 . . . 80) nH	
Capacitor	(1 . . . 3) nF	Ta_2O_5, $\varepsilon_r = 23$

Noble metal nanoparticles (e.g. Ag nanoparticles) allow lower sintering temperatures resulting in the improvement of the electrical and thermal conductivity in conductive adhesives [22].

Nano-Ag-particles are used for direct-writing of conducting lines on substrates by inkjet printing or by aerosol printing where the nano-Ag-particles are transported by a liquid. Printed conductor lines of nano-Ag-inks with particle sizes in the range of 20–60 nm require thermal treatment to sinter the particles to achieve high electrical and thermal conductivitie [32] (Figs. 2.15, 2.16).

Nano-Ag-wires with diameters in the range of 60–80 nm and with a length in the µm-range are under investigations for developing anisotropic conductive adhesive films for heat and current transport in 3D-packages [12].

Other applications of nanoparticles concern the usage of reactive or nonreactive additives to solder materials to increase the creep resistance [21, 28] and the application as additives in underfiller and high-k dielectrics [33].

2.6 Outlook

The continuing scaling of the structures of semiconductor devices and the demands of electronic products, especially of portable products, have driven the development of system level integration. Higher functional density at smaller sizes, higher operational frequencies, higher reliability and lower cost require SiP-3D-integration with different functional devices assembled into one package.

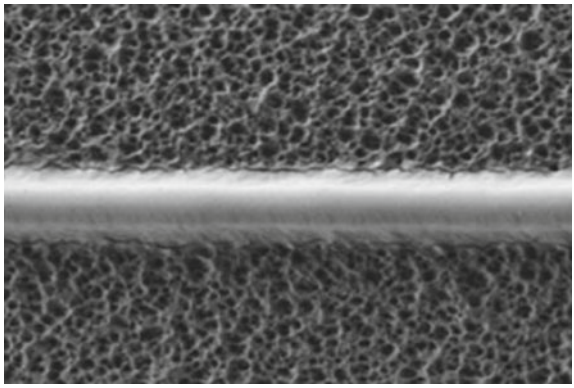

Fig. 2.15 Printed conductor line (line width 15 μm) by using Nano-Ag-Ink (source FhG IKTS, Mosch, Wanke)

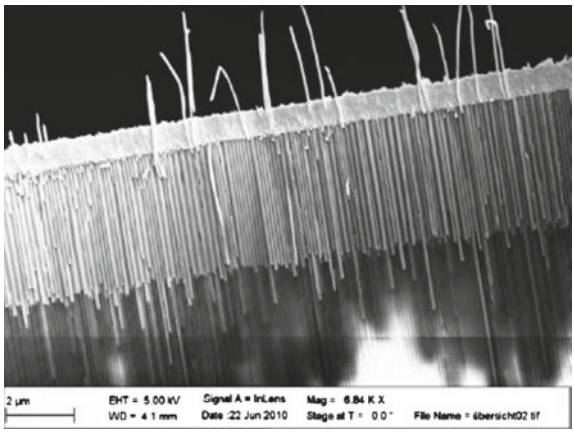

Fig. 2.16 Electroplated Ag-nanowire by using Al_2O_3 templates [12]

Two major approaches for 3D-integration are in use today, package on package and stacked-die packages. The advantages of PoP include the application of tested individual packages, while stacked-die packages need the application of known good dies. The stacked die packages, especially by using TSVs, have particular advantages such as reduced wire length between different dies and high-density interconnections.

Nanomaterials are considered as particularly beneficial in the future due to their key role for increasing performance in heterogeneous 3D-integration.

References

1. Ang, X.F., Lin, A.T., Wei, J., Chen, Z., Wong, C.C.: Low temperature copper–copper thermo-compression bonding. In: Proceedings of the 10th Electronics Packaging Technology Conference (EPTC), pp. 399–404. Singapore (2008)
2. Aryasomayajula, L., Rieske, R., Wolter, K.J.: Application of copper-carbon nanotubes composite in packaging interconnects. In: Proceedings of the 34th International Spring Seminar on Electronics Technology (2011)

3. Beelen-Hendrikx, C.: Trends in IC packaging. In: Proceedings of the 17th European Microelectronics and Packaging Conference (EMPC), pp. 1–8. Rimini, Italy (2009)
4. Beica, R.: Advanced metallization for 3D integration. In: Proceedings of the 10th Electronics Packaging Technology Conference, pp. 212–218. Singapore (2008)
5. Beyne, E.: The rise of the 3rd dimension for system integration. In: Proceedings of the 9th International Interconnect Technology Conference, pp. 1–5. Burlingame, USA (2006)
6. Beyne, E.: Solving technical and economical barriers to the adoption of through-Si-via 3D integration. In: Proceedings of the 10th Electronics Packaging Technology Conference (EPTC), pp. 29–34. Singapore (2008)
7. Chen, Q., Zhang, D., Wang, Z., Liu, L., Lu, J.: Chip-to-wafer (C2W) 3D integration with well-controlled template alignment and wafer-level bonding. In: Proccedings of the 61st Electronic Components and Technology Conference (ECTC), pp. 1–6. Orlando, FL, USA (2011)
8. Cognetti, C.: The impact of semiconductor packaging technologies on system integration—an overview. In: Proceedings of the 35th European Solid-State Circuit Conference, pp. 23–27. Athen, Greece (2009)
9. Combs, J.: Printed Circuit Handbook, 6th edn. McGraw-Hill, New York (2007)
10. DISCO Cooperation: Dicing before grinding process. http://is01.disco.co.jp/psc/aphp.nsf/0/F25F83635A938BAD49256FE3001E5987
11. Gerber, M., Beddingfield, C., O'Connor, S., Yoo, M., Lee, M., Kang, D., Park, S., Zwenger, C., Darveaux, R., Lanzone, R.K.P.: Next generation fine pitch cu pillar technology—enabling next generation silicon nodes. In: Proccedings of the 61st Electronic Components and Technology Conference (ECTC), pp. 612–618. Orlando, FL, USA (2011)
12. Graf, M., Eychmüller, A., Wolter, K.J.: High aspect ratio metallic nanowire arrays by pulsed electrodeposition. In: Proceedings of the 11th International Conference on Nanotechnology. Portland OR, USA (2011)
13. Greig, W.: Integrated Circuit Packaging, Assembly and Interconnects. Springer, New York (2007)
14. Heimann, M., Meißner, F., Schönecker, A., Endler, I., Wolter, K.J.: Nano-scaled functional layers for current and heat transport in electronics packaging. In: Proccedings of the 2nd Electronics System-Integration Technology Conference (ESTC), pp. 333–338. Greenwich, London (2008)
15. International Technology Roadmap for Semiconductors (ITRS): Assembly and packaging, edition 2007. Technical report, Semiconductor Industry Association. http://www.itrs.net/Links/2007ITRS/2007_Chapters/2007_Assembly.pdf (2007)
16. International Technology Roadmap for Semiconductors (ITRS): The next steps in assembly and packaging. Technical Report, Semiconductor Industry Association. http://www.itrs.net/links/2007ITRS/LinkedFiles/AP/AP_Paper.pdf (2007)
17. International Technology Roadmap for Semiconductors (ITRS): System driver, edition 2009. Technical Report, Semiconductor Industry Association (2009)
18. Jiang, T.S.L.: 3D integration-present and future. In: Proceedings of the 10th Electronics Packaging Technology Conference (EPTC), pp. 373–378. Singapore (2008)
19. Kettner, P., Burggraf, J., Kim, B.: Thin wafer handling and processing—results achieved and upcoming tasks in the field of 3D and TSV. In: Proceedings of the 11th Electronic Packaging and Technology Conference (EPTC), pp. 787–789. Singapore (2009)
20. Knickebocker, J.U., Andry, P.S., Dang, B., Horton, R.R., Patel, C.S., Polastre, R.J., Sakuma, K., Sprogis, E.S., Trang, C.K., Webb, B.C., Wright, S.L.: 3D silicon integration. In: Proceedings of the 58th Electronic Components and Technology Conference (ECTC), pp. 538–543. Orlando FL, USA (2008)
21. Li, Z.X., Gupta, M.: High strength lead-free composite solder materials using nano-Al_2O_3 as reinforcement. Adv. Eng. Mater. **7**(11), 1049–1053 (2005)
22. Lin, W., Wong, C.P.: Applications of carbon nanomaterials as electrical interconnects and thermal interface material. In: Wond, C.P., Moon, K.-S., Li, Y. (eds.) Nano-Bio-Electronic, Photonic and MEMS Packaging. Springer, Heidelberg (2010)
23. Morris, J.E. (ed.): Nanopackaging. Springer, New York (2008)

24. Panchenko, I., Wolter, K.J.: Interconnect technology for 3D chip integration. In: Proccedings of the Electronics and Nanotechnology Conference. Kyiv, Ukraine (2011)
25. Röllig, M.: Beiträge zur Bestimmung von Mechanischen Kennwerten an Produktkonformen Lotkontakten Der Elektronik. Verlag Dr. Markus A. Detert, New Yok (2009)
26. Roozeboom, F., Blauw, M., Lamy, Y., Grunsven, E., Dekkers, W., Verhoeven, J., Heuvel, E., Drift, E., Kessels, E., Sanden, R.: Deep reactive ion etching of through silicon vias. In: Garrou, Ph., Bower, Ch., Ramm, P. (eds.) Handbook of 3D Integration, vol. 1. Wiley-VCH Verlag, Weinheim (2008)
27. Sapatnekar, S.: Handbook of 3D Integration, Chap. Computer-Aided Design for 3D Circuits at the University of Minnesota. Wiley-VCH Verlag, Weinheim (2008)
28. Shi, Y.W., Liu, J., Xia, Z.D., Lei, Y.P., Guo, F., Li, X.: Creep property of composite solders reinforced by nano-sized particles. J. Mater. Sci. Mater. Electron. **19**(4), 349–356 (2008)
29. Sukumaran, V., Bandyopadhyay, B., Chen, Q., Kumbhat, N., Liu, F., Pucha, R., Sato, Y., Watanabe, M., Kitaoka, K., Ono, M., Suzuki, Y., Karoui, C., Nopper, C., Swaminathan, M., Sundaram, V., Tummala, R.: Design, fabrication and characterization of low-cost glass interposers. In: Proccedings of the 61st Electronic Components and Technology Conference (ECTC), pp. 583–588. Orlando FL, USA (2011)
30. Tan, C.S., Gutmann, R.J., Reif, L. (eds.): Wafer Level 3-D ICs Process Technolgy. Springer, London (2008)
31. Vempati, S.R., Ho, S.W., Lee, W.S.V., Li, H.Y., Liao, E., Ranganathan, N., Chai, T.C., Xiaowu, Z., Pinjala, D.: TSV interposer fabrication for 3D IC packaging. In: Proccedings of the 11th Electronics Packaging Technology Conference (EPTC), pp. 431–437. Singapore (2009)
32. Wakuda, D., K., K., Suganuma, K.: Properties of Ag nanoparticle paste for room temperature bonding. In: Proccedings of the 59th Electronic Components and Technology Conference (ECTC), pp. 1557–1562. San Diego CA, USA (2009)
33. Wong, C.P., Moon, K.-S.: Nanomaterials for microelectronic and bio-packaging. In: Wong, C.P., Moon, K.-S., Li Y. (eds.) Nano-Bio-Electronic, Photonic and MEMS Packaging. Springer, Berlin (2010)
34. Xie, Y., Cong, J., Sapatnekar, S.: Three-Dimensional Integrated Circuit Design. Springer, New York (2010)
35. Yannou, J.M.: SiP and WLP-CSP trends: State-of-the-art and future trends. In: Proceedings of the 2nd Electronics Systemintegration Technology Conference (ESTC), pp. 3–6. London (2008)
36. Yoon, S., Yang, D., Koo, J., Padmanathan, M., Carson, F.: 3D TSV processes and its assembly/packaging technology. In: Proceedings of the International Conference on 3D System Integration of the Institute of Electrical and Electronics Engineering, pp. 1–5. San Francisco, USA (2009)
37. Zentralverband Elektrotechnik- und Elektronikindustrie: Mikroelektronik—Trendanalyse bis 2013. Technical Report, ZVEI (2010)
38. Zerna, T.: Aufbau- und Verbindungstechnik für Elektronik-Baugruppen der Höchstintegration. Verlag Dr. Markus A. Detert, New York (2008)
39. Zoschke, K., Wolf, J., Lopper, C., Kuna, I., Jürgensen, N., Glaw, V., Samulewicz, K., Röder, J., Wilke, M., Wünsch, O., Klein, M., Suchodoletz, M., Oppermann, H., Braun, T., Wieland, R., Ehrmann, O.: TSV based silicon interposer technology for wafer level fabrication of 3D SiP modules. In: Proccedings of the 61st Electronic Components and Technology Conference (ECTC), pp. 838–843. Orlando FL, USA (2011)

http://www.springer.com/978-3-642-28521-9

Bio and Nano Packaging Techniques for Electron Devices
Advances in Electronic Device Packaging
Gerlach, G.; Wolter, K.-J. (Eds.)
2012, XII, 628 p., Hardcover
ISBN: 978-3-642-28521-9