SOP: What Is It and Why? A New Microsystem-Integration Technology Paradigm-Moore's Law for System Integration of Miniaturized Convergent Systems of the Next Decade

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***Abstract*—In the past, microsystems packaging played two roles: 1) it provided I/O connections to and from integrated circuits (ICs) or wafer-level packaging (WLP), and 2) it interconnected both active and passive components on system level boards, referred to as systems packaging. Both were accomplished by interconnections or multilayer wiring at the package or board level. More recently, the IC devices have begun to integrate not only more and more transistors, but also active and passive components on an individual chip, leading the community to believe that someday there may be a single-chip complete system, referred to as system-on-chip (SOC). This can be called horizontal or two-dimensional (2-D) integration of IC blocks in a single-chip toward end-product systems. The community began to realize, however, that such an approach presents fundamental, engineering, and investment limits, as well as computing and communication limits for wireless and wired systems over the long run. This led to 3-D packaging approaches, often referred to as system-in-package (SIP). The SIP, while providing major opportunities in both miniaturization and integration for advanced and portable electronic products, is a subsystem, limited by the CMOS process just like the SOC. Some existing and emerging applications, however, include sensors, memory modules and embedded processors with DRAMs. More recent 3-D solutions, which incorporate stacked package approaches, offer solutions toward faster time-to-market and business impediments that have plagued MCM deployment for the past decade. There is a new emerging concept called system-on-package (SOP). With SOP, the *package*, not the board, is the *system*. As such, SOP is beginning to address the shortcomings of both SOC and SIP, as well as traditional packaging which is bulky, costly, and lower in performance and reliability than ICs, in two ways: 1) It uses CMOS-based silicon for what it is good for, namely, for transistor integration, and the package, for what it is good for, namely, RF, optical, and digital integration by means of IC-package-system codesign. The SOP package, therefore, overcomes both the computing limitations and integration limitations of SOC, SIP, MCM, and traditional system packaging. It does this by having global wiring as well as RF, digital, and optical component integration in the package, not in the chip. The SOP, therefore, includes both active and passive components in thin-film form, in contrast with indiscrete or thick-film form, including embedded digital, RF, and optical components, and functions in a microminiaturized package or board.**

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***Index Terms*—Consumer electronics, convergent electronics systems, integrated circuit (IC) packaging, integrated optoelectronics, interconnections, Moore's Law, multichip modules, optoelectronics, system-in-package (SIP), system-on-chip (SOC), system-on-package (SOP).**

I. Introduction: The Trend Toward Convergent Systems

THE electronic systems of today are primarily discrete systems with computers performing data computations, telecommunications providing voice-based communications, and consumer products providing audio, video, and other functions in portable products. There is a new and emerging trend in systems which is referred to as "convergent systems" and is characterized by the convergence of computer, communications, consumer, and biomedical product functions into one product. Convergent systems span consumer, infrastructure, automotive, aerospace, and biomedical industries. Examples of next-generation convergent systems include electronic products such as smart watches with cell phone, global positioning system (GPS), sensor and web mail access, and medical electronics such as smart medical implants with computing, sensing, imaging, and wireless communication characteristics, as illustrated in Fig. 1.

The technologies required to accomplish this convergence of data, video, voice, sensing, and other functions are digital, optical, RF, analog, MEMS, and sensors. While some of this convergence is beginning to take place in the industry, it is primarily by discrete and bulky components which do not take advantage of the synergy between the integrated circuit (IC) and the package the way the new SOP concept for highly integrated multifunctional systems does, as described in this issue.

II. Four Approaches to Convergent Systems

One can visualize four approaches to the above convergent systems

1) system-on-chip (SOC);
2) multichip module (MCM);
3) system-in-package (SIP);
4) system-on-package (SOP).

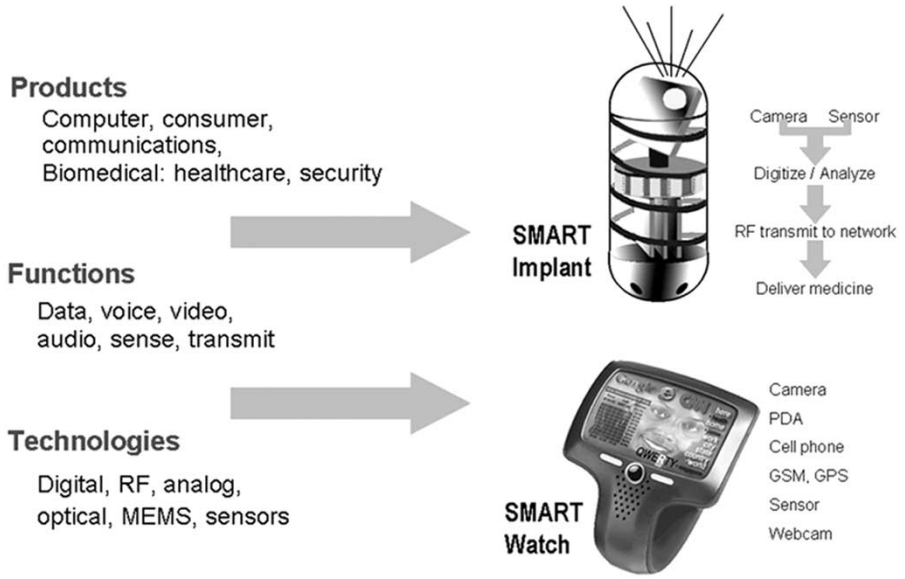

Fig. 1. Trend to convergent and miniaturized systems such as smart watch and smart implants.

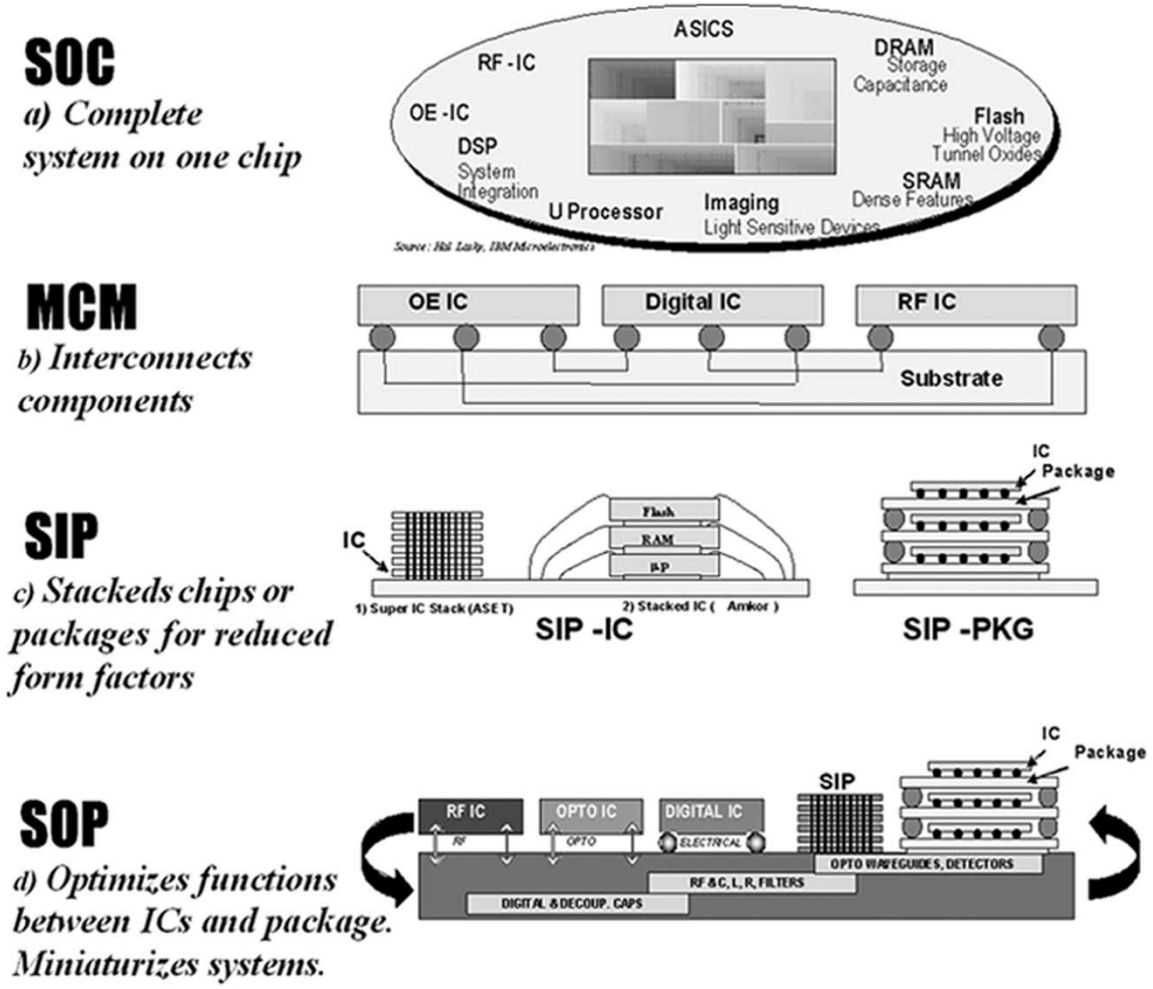

Fig. 2. (a) SOC-based on a complete system on one chip. (b) MCM-based on interconnected components. (c) SIP-based on a stacked chip/package for reduced form factors. (d) SOP offers the best of IC and systems packaging technologies by optimizing functions between ICs and the package while miniaturizing systems.

The SOC schematic shown in Fig. 2(a), for example, seeks to integrate numerous system functions on one silicon platform horizontally, namely the chip. If this chip can be designed and fabricated cost effectively with computing, communication, and consumer functions such as processor, memory, graphics, antennas, filters, switches, fibers, or waveguides and other com-

ponents required to form a complete end-product system, then all that is necessary to package such a system is to provide external connections, power, and cool. If this can be realized, SOC offers the promise for the most compact, light-weight system that can be mass produced. This has been and continues to be the roadmap of IC companies. So the key question is whether SOC can lead to cost-effective complete end-product systems such as tomorrow's leading-edge cell phones with digital and sensing capabilities or biomedical implants. Researchers around the world, while making great progress, are realizing that SOC, in the long run presents fundamental limits for computing and integration limits for wireless communications and additional nonincremental costs to both. Among SOC challenges are the long design times due to integration complexities, high wafer fabrication costs, test costs, and mixed-signal processing complexities requiring dozens of mask steps and intellectual property issues. The high costs are due to the need to integrate active but disparate devices such as bipolar, CMOS, SiGe, and optoelectronic ICs—all in one chip with multiple voltage levels and dozens of mask steps to provide digital, RF, optical, and MEMS-based components.

A new paradigm that overcomes the shortcomings of both SOC and traditional packaging, therefore, is necessary. The papers in this issue make a compelling case for the synergy between the IC, package and the system by means of the SOP paradigm.

III. Shortcomings of SOC for RF, Digital, and Optical Integration

Complete integration of RF, digital and optical technologies on a single chip poses numerous challenges. RF circuit performance, for example, is a tradeoff between the quality factor (Q) of passive components (inductors and capacitors) and power. Low-power circuit implementations for mobile applications require high Q passive components. In standard silicon technologies, the Q factor is limited to 5–25 due to the inherent losses of silicon [1]. This can be improved by using esoteric technologies such as thick oxides, high-resistivity Si, SiGe, or GaAs which increase the cost substantially. In addition, these passive components consume valuable real estate and occupy more than 50% of the silicon area. Antennas are another example that cannot be integrated on silicon due to size restrictions [2]–[6]. Another example involves RF circuits which function in the microvolt range. Integration of dissimilar signals requires large isolation between them. On standard silicon, a major concern is substrate coupling caused by the finite resistivity of the silicon substrate. Though solutions have been proposed using high resistivity silicon or N-well trenches, the isolation levels achieved are insufficient. For multiple voltage levels, distributing power to the digital and RF circuits while simultaneously maintaining isolation and low EMI can be a major challenge [7]. These issues can be addressed quite easily with SOP using embedded filtering and decoupling technologies [8]–[12]. SOP has already been demonstrated with Q values in the range of 100–400 using low-loss dielectrics and copper metallization that enable low-power solutions. With advances in digital processing speeds, embedded optical waveguides in the package have the potential of bringing photonics directly into the processor. This integration in the package can eliminate the serialization and deserialization of data and, therefore, provide a compact platform for integration with higher data bandwidth. In synchronous systems which support large ICs, a major problem is the clock skew between various logic circuits on silicon. A potential solution for such problems is the use of embedded optical clock distribution in the package, which is immune to most noise sources [13]–[22].

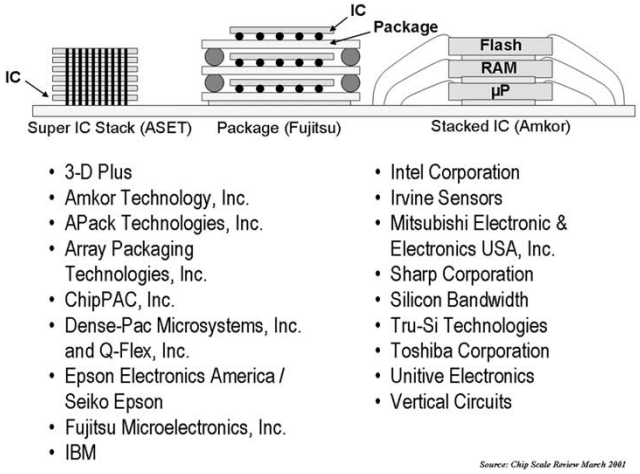

Fig. 3. Some of more than 30 companies currently pursuing SIP.

A. SIP is a Subsystem or Vertical MCM with Embedded Discrete Components, Unlike SOP With Thin-Film Embedding of System Components

SIP is defined in this paper as the vertical stacking of similar or dissimilar ICs, in contrast to the horizontal nature of SOC, which overcomes some of the above SOC limitations, such as latency if the size of the chips and their thicknesses used in stacking are small. The intellectual property issues as well as yield losses associated with dozens of sequential mask steps and large area IC fabrication are also minimal because of the challenges associated with cooling a stacked structure, SIP is also limited to the use of low power ICs. Clearly, this is the semiconductor companies' dream in the short term. But there is one major issue with this approach. If all of the ICs in the stack are limited to CMOS IC processing, the end-product system is limited by what it can achieve only with CMOS processing at, or below, nanoscale. The above fundamental and integration barriers of SOC, therefore, remain. There are clear major benefits, however, to SIP: simpler design and design verification, a process with minimal mask steps, minimal time-to-market, and minimal IP issues.

Because of the aforementioned SIP benefits, however limited, about 30 IC and packaging companies, alike, are gearing up in a big way to produce SIP-based multichip modules (Fig. 3). SIPs seem to come in three flavors: 1) as a 3-D-stacking of similar ICs, such as DRAMS; 2) the stacking of dissimilar ICs such as processors, DRAMs, or flash memory designed to approach part of the system's needs; 3) the stacking of packaged ICs with embedding of **discrete** active and passive components. It also seems to come in both bare-chip stacking and packaged stacking [23]–[26].

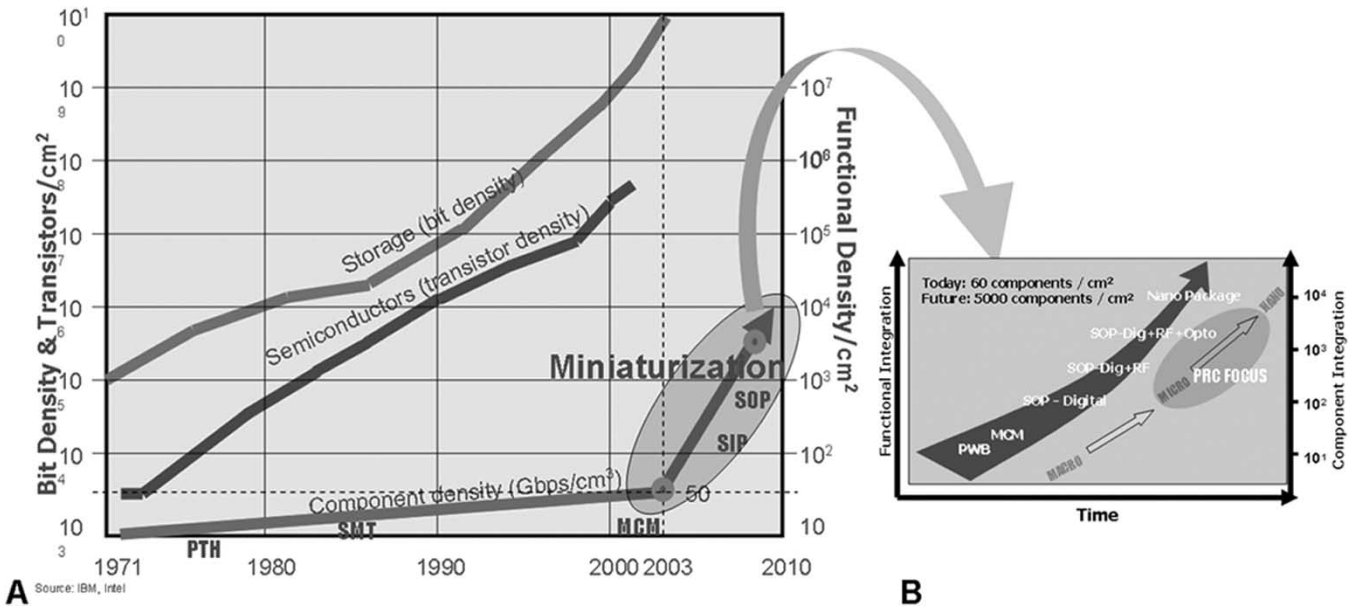

Fig. 4. SOP: Moore's Law for system integration.

B. MCM Interconnects Chips

MCM was invented back in the 1970s at IBM for the sole purpose of regrouping good bare ICs directly onto a ceramic package, since larger chips could not be produced with any acceptable yields on the original silicon wafer. These original MCMs were horizontal or 2-D. The new SIP-based MCMs, however, are vertical or 3-D. Both provide nothing but wiring to interconnect ICs. The shortcomings of CMOS-based ICs, therefore, are not overcome with the MCM approach.

C. Shortcomings of Traditional Packaging

Today's traditional packaging, on the other hand, presents a different set of problems. The IC packaging that is used to provide I/O connections from the chip to the rest of the system is typically bulky and costly, limiting both the performance and the reliability of the IC it packages. Systems packaging, involving the interconnection of components on a system level board, is similarly bulky and costly with poor electrical and mechanical performance.

D. SOP, as Moore's Law for System Integration, is More Than MCM and SIP

SOP goes one step beyond all three of the aforementioned approaches in overcoming both the fundamental and integration shortcomings of SOC, SIP, and MCM, which are limited by CMOS processing and the shortcomings of current packaging for cost, performance, size, and reliability [27]–[30]. While silicon technology is great for transistor density improvements from year to year, according to Moore's Law, it is not an optimal platform for system integration of RF, optical, and certain digital components, as stated earlier.The SOP is akin to Moore's Law for ICs, except it integrates system components by thin-film technologies at microscale in the short term and nanoscale in the long run for mixed-signal electronic and bioelectronic systems, as shown in Fig. 4. Unlike SIP, MCM, or

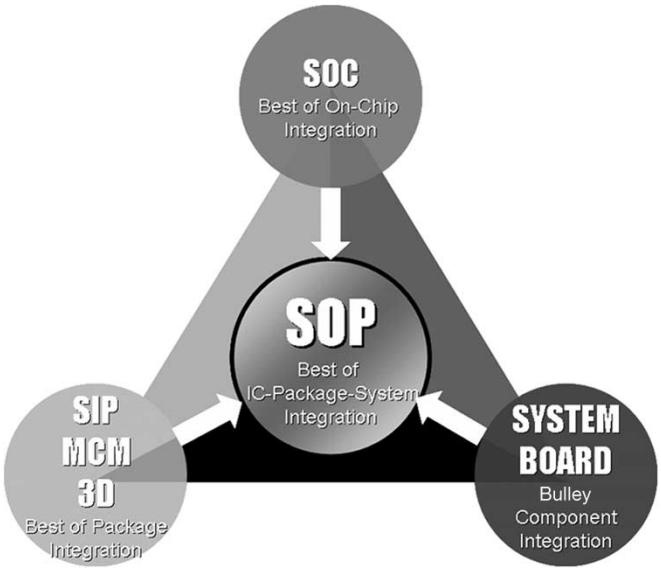

Fig. 5. SOP is the system level in contrast to SIP as a package level packaging.

SOC, it is a system level technology with all the system functions and interconnections and takes advantage of the synergy between IC, package, and the system, as illustrated in Fig. 5.

The SOP concept overcomes a number of the engineering limits of SOC. As IC integration moves to nanoscale and wiring resistance increases, the global wiring delay in SOC becomes too high for computing applications [31]. This leads to what is referred to as "latency" which can be avoided by either moving global wiring from the nanoscale on ICs to the microscale on SOP, or making the digital chips much smaller. SOP handles both of these. Wireless integration limits of SOC are also handled well by SOP. RF components such as capacitors, filters, antennas, switches, and high-frequency and high-Q inductors, are best fabricated in the package rather than on silicon. To meet the need for the amount of decoupling capacitance necessary to suppress the expected power plane noise associated with very

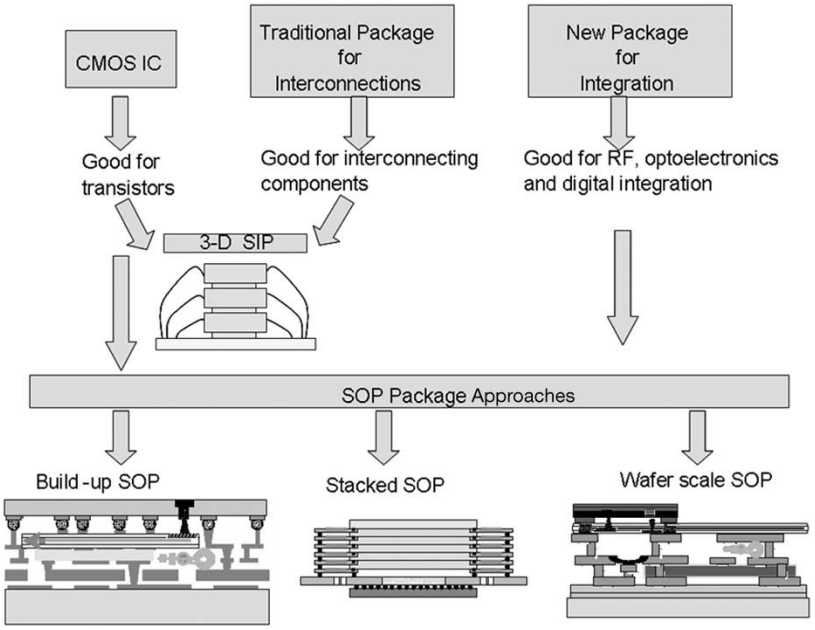

Fig. 6. Difference between SIP and SOP concepts as well as various options for both.

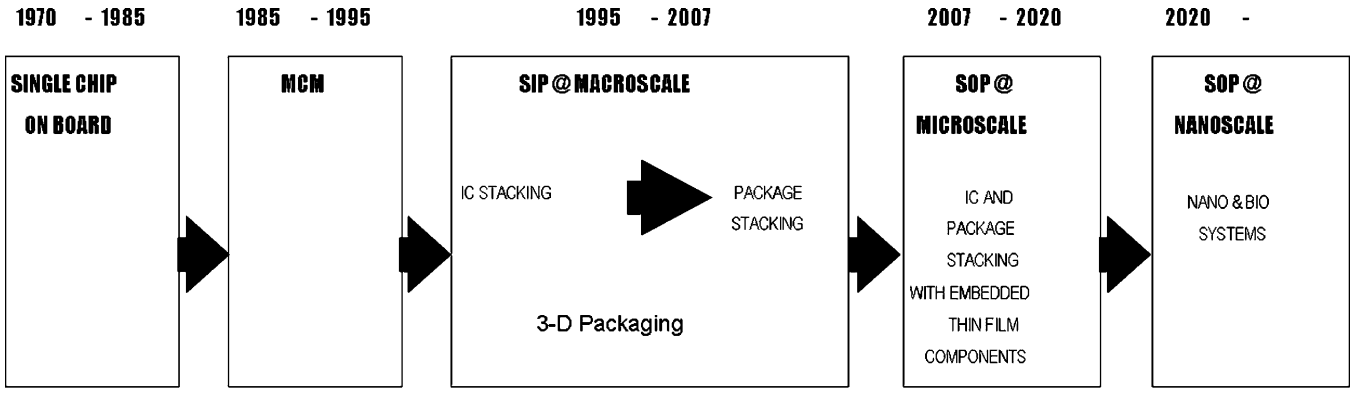

Fig. 7. Systems packaging evolution and trend.

high-performance ICs which require more than 100 W per chip, a major portion of the chip area would have to be dedicated to decoupling capacitance alone. Semiconductor companies are not in the capacitor business; they are in the transistor business. The highest Q factors reported on silicon are about 10–25, in contrast to 100–400 achieved in the SOP package. Optoelectronics, which today finds use primarily in the back planes and is used for high-speed board interconnects, is moving onto the package as chip-to-chip for high I/O and high-speed interconnections, replacing copper, and thus, addressing both the resistance and crosstalk issues of electronic ICs. Optoelectronics is not seen as moving onto the SOC chip to replace copper wiring anytime soon.

The SOP concept seeks to integrate multiple system functions into one compact, lightweight, thin-profile, low-cost, high-performance packaged system. The system design may call for high-performance digital logic, memory, and graphics, and analog signals for RF and video, as well as broadband optical functions. Unlike SOC, however, no performance compromises have to be made in order to integrate these disparate technologies since each technology is separately integrated into the SOP package. System design times are expected to be much shorter, and the testing is expected to be simpler. In addition, the SOP concept allows for shorter time-to-market and greater flexibility with which to take advantage of emerging technologies. With the SOP concept, the chip size can be as small as required to be manufacturable with high yields and its wiring length can be as small as needed to overcome the high resistance-imposed global signal delays.

E. SIP Can be SOP if it Integrates Embedded Thin Film and Not Thick and Bulky Discrete Components

SIP can also be looked upon as SOP. In this concept, the individual ICs are first packaged, and such packages are then stacked to form 3-D circuits [32], [33]. When horizontal SIP-to-SIP wiring and embedded thin film components are included in the substrate, SIP becomes SOP as illustrated in Fig. 5. The individual packages can have not only the best IC technology, but they can also have the best package integration technology such as RF, optical, and certain digital component integration. However, if the package provides only wiring to interconnect ICs vertically, then the package contribution is

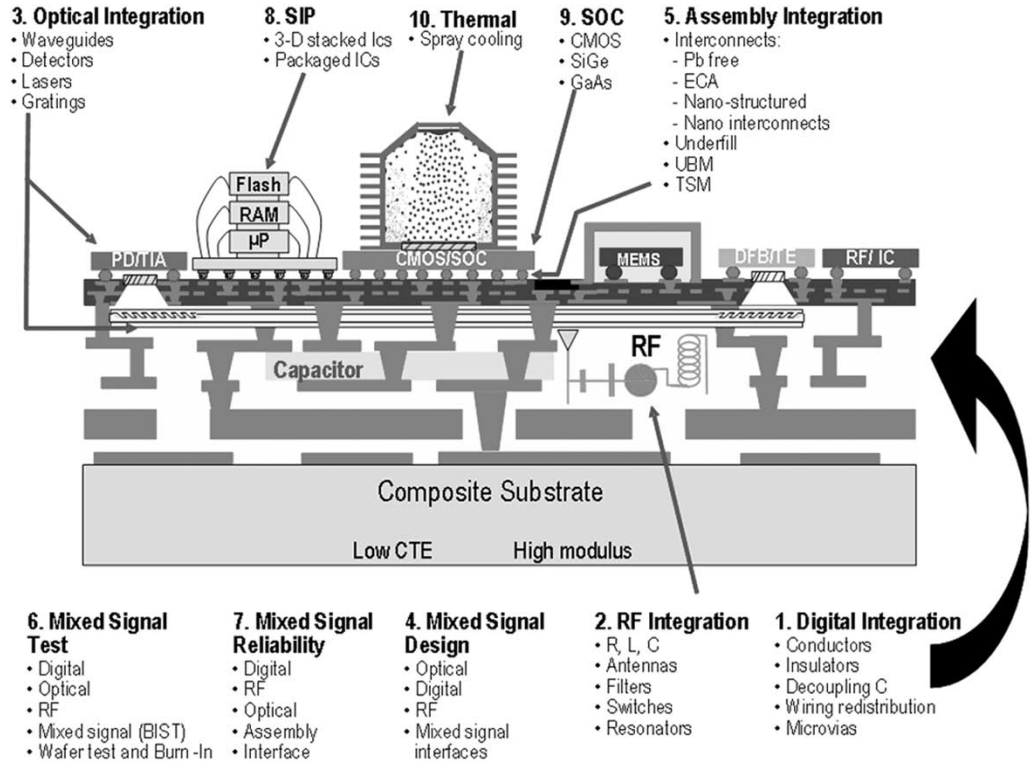

Fig. 8. SOP concept for system integration of thin film components.

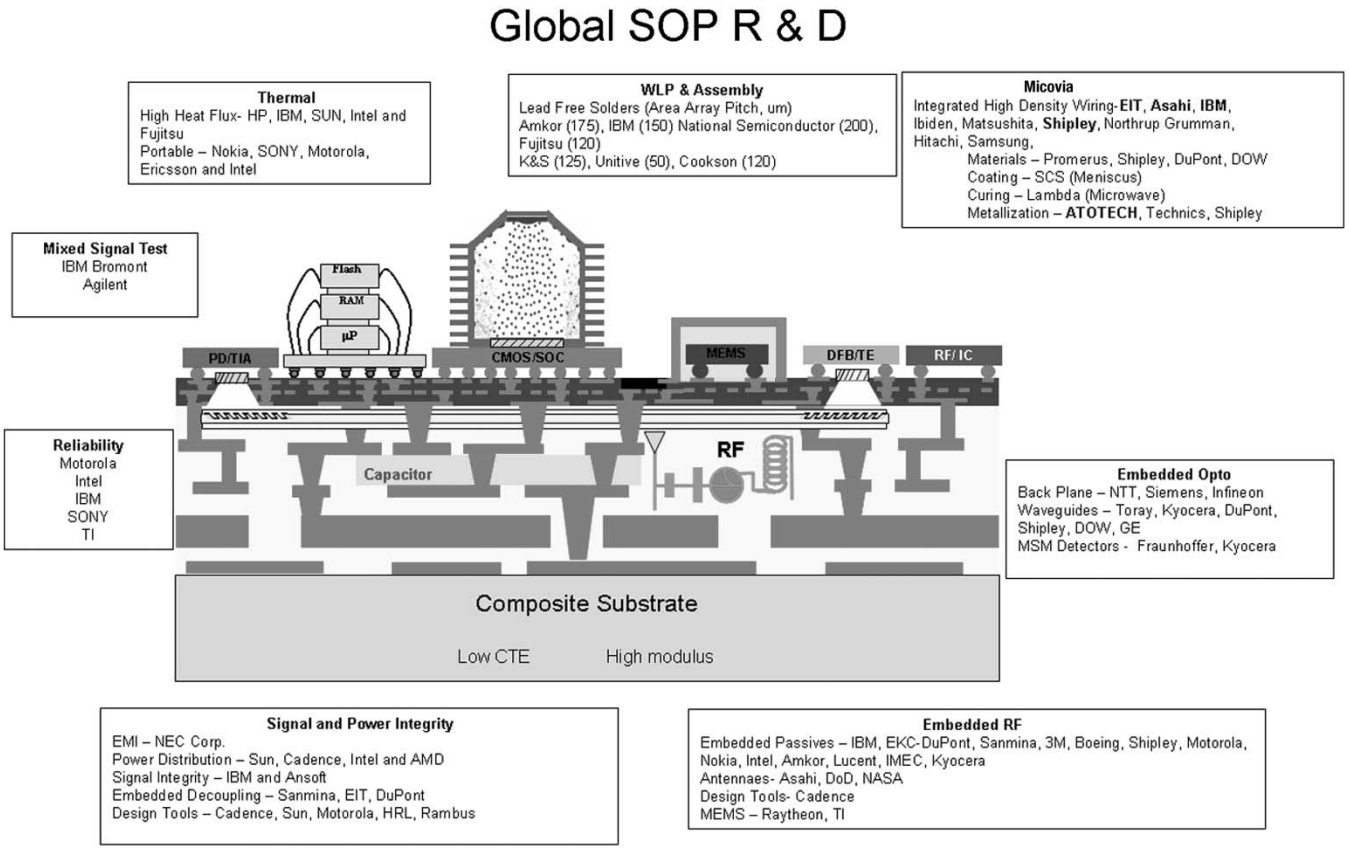

Fig. 9. Global research and development in SOP.

limited and the structure is SIP; it is simply a vertical MCM, vertically packaged. But such a structure provides partial system integration in addition to power distribution and heat removal and is considered to be MCM-vertical. In fact, one

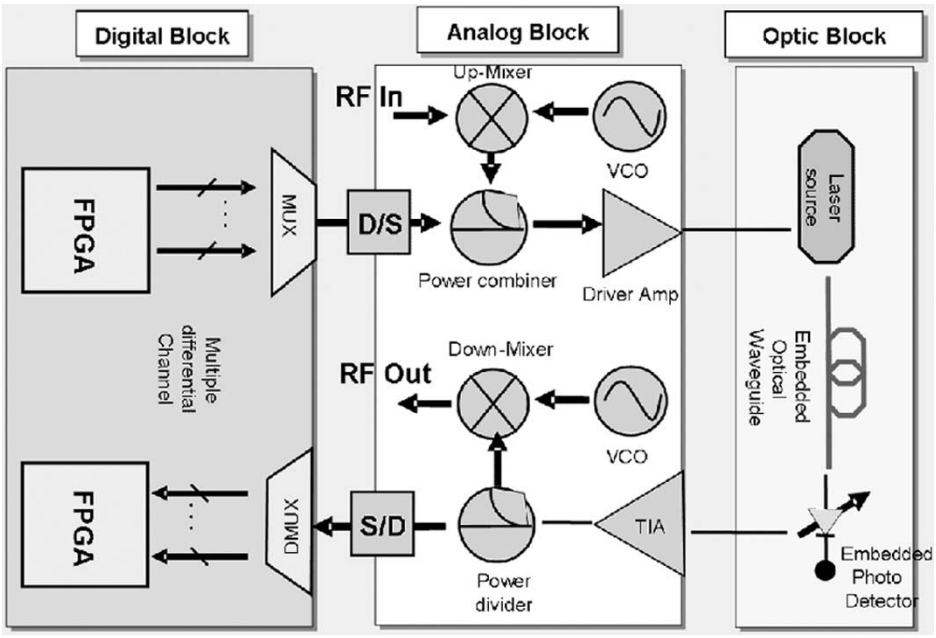

Fig. 10. Multifunction SOP architecture prototype.

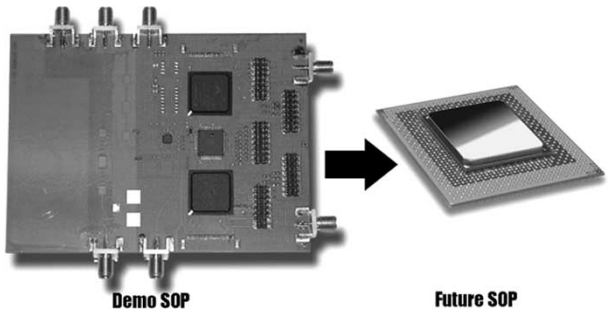

Fig. 11. Demonstration and ultimate size potential of SOP technology.

could visualize such a stack to be bulkier than the above SIP-IC approach.

The integrated systems packaging evolution and trend is depicted in Fig. 6 showing the progress from single chip to MCM to SIP. SiP is divided into two parts depending on whether the stacking is at IC level or packaged IC level, driven by the yield of ICs. SOP is distinguished from SIP, the former with embedded thin film integration of components in the package or the board.

IV. Global Status of SOP

The SOP concept of embedding RF, optical, and certain components by means of thin films in the package began in 1994 at the Georgia Institute of Technology with funding from the National Science Foundation, the Georgia Research Alliance, and partnerships with 50 global semiconductor, packaging, and systems companies. Today, the concepts being pursued in SOP R&D are pervasive as indicated in Fig. 7.

Since SOP was defined as the synergy between the IC and the package—going beyond simply wiring in today's components, MCMs, or boards—dozens of activities can be seen in the United States, Europe, and Asia. Some of these activities are included in Table I [32], [33]. The most concentrated effort is still at the Georgia Institute of Technology; that is where a large research center called the Packaging Research Center (PRC) is exploring and fabricating SOP-based prototypes in a $30 M, 300-mm SOP wafer facility in partnership with 50 global electronics companies, 250 Ph.D. and M.S. students, and 30 faculty from electrical, mechanical, materials, and chemical engineering disciplines. The PRC continuously explores materials and design concepts in order to bring the SOP paradigm to reality [34]–[38]. Concepts in broadband RF, optoelectronics, and high-speed digital integration are tested in the 300-mm SOP wafer facility. This type of research led the Georgia Tech team to demonstrate SOP technology with the first integrated optical, RF, and digital functions in one module (Fig. 8) for a broad-

TABLE I
Companies Involved in SOP-Related Product Technologies [31], [32]

Company/Institutes	SOP-Related Involvement
Conexant	Organic-based dual-band Power Amplifier with embedded matching circuits
Anacom	Radio-on-Fiber for Cellular Base Station
LynkSys	Wireless LAN module with embedded antennas in the organic board
Mini Circuit	Tri-band Mixer Module using LTCC
SyChip	Embedded Passives
Di-Trans	Embedded Passives LTCC
Etenna	Integrated Antenna Technology
Rambus	3.2Gbps Yellowstone Technology
Intel	Digital Transceiver - 16X622 Mbs to 10 Gbs and 10 Gbs to 16X622 Mbs
Xilinx, Vitesse, Texas Instruments & NEC	10Gb/s transponder module
Tessera	SIP on flex substrate
IMEC	Chip package co-design for transceivers and VCOs
APack and Lucent	3-D stacked SIP
University of Texas	Embedded VCSEL and MSM detector

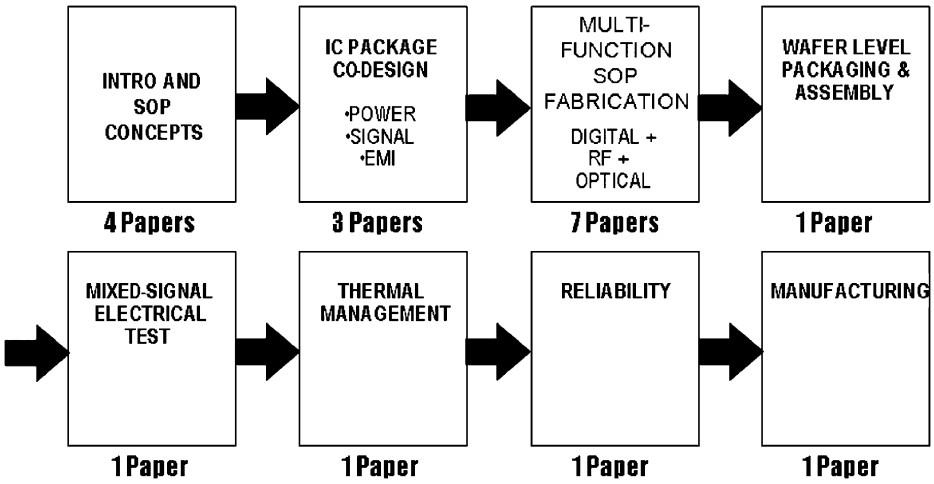

Fig. 12. The sequence of technologies necessary for a system, and number of papers on each technology.

band application called the Intelligent Network Communicator (INC), Fig. 9, as described in a relevant paper in this issue. By about 2007, the SOP concept is expected to be widely, and perhaps fully, used.

V. SOP Papers in This Issue

Any new technology such as SOP must have potential applications. Any such application requires system design and architecture leading to IC-package-system codesign addressing signal and power integrity, EMI, and wiring layout. These, then, lead to a spectrum of fabrication and integration technologies. In the case of SOP, these technologies are mixed-function in nature, such as digital, optical, and RF. The fabricated package, or board, needs to be assembled at the IC or wafer level and tested for functionality with thermal solutions provided. In view of thermal expansion mismatches between various materials and the temperature gradient created as a result of the IC being the source of heat, thermomechanical stresses are developed, potentially leading to reliability failures. The manufacturing of new technology to the system application completes the process.

This entire process is illustrated schematically in Fig. 9 for SOP and the 18 papers covered in this issue are logically related to these technologies.

Acknowledgment

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