TOPICAL REVIEW

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Wafer level packaging of MEMS

Masayoshi Esashi

The World Premier International Research Center Advanced Institute for Materials Research, Tohoku University, Sendai, Japan

E-mail: esashi@cc.mech.tohoku.ac.jp

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Abstract

Wafer level packaging plays many important roles for MEMS (micro electro mechanical systems), including cost, yield and reliability. MEMS structures on silicon chips are encapsulated between bonded wafers or by surface micromachining, and electrical interconnections are made from the cavity. Bonding at the interface, such as glass–Si anodic bonding and metal-to-metal bonding, requires electrical interconnection through the lid vias in many cases. On the other hand, lateral electrical interconnections on the surface of the chip are used for bonding with intermediate melting materials, such as low melting point glass and solder. The cavity formed by surface micromachining is made using sacrificial etching, and the openings needed for the sacrificial etching are plugged using deposition sealing methods. Vacuum packaging methods and the structures for electrical feedthrough for the interconnection are discussed in this review.

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Packaging for MEMS (micro electro mechanical systems), which includes encapsulation and electrical interconnection, is indispensable for practical applications. The process of packaging a wafer prior to dicing is called wafer level packaging. It is recognized that a major part of the MEMS cost is the packaging and testing. MEMS have moving parts and hence the MEMS chips cannot be molded directly with plastics. Furthermore, in many cases MEMS cannot be tested on a wafer, and therefore packages of the defective MEMS result in a higher cost due to low yield or extra packaging. These problems can be solved by wafer level packaging [1]. The concept of wafer level packaging is shown in figure 1. MEMS are fabricated on a silicon wafer and the MEMS wafer is bonded to a lid wafer which has electrical interconnections from the cavity to the outside. A lid wafer with holes for electrical interconnection is used in figure 1. Finally, by dicing the bonded wafer we can get many packaged chips. It is advantageous to seal the cavities in the early stage of the wafer process. The MEMS in the cavity are protected mechanically and are not contaminated during the fabrication process, such as dicing. We can make small packaged MEMS and eliminate extra packaging equipment. Common technologies needed for wafer level packaging are also used for making sealed cavities as the reference pressure chambers of absolute pressure sensors.

Various wafer level packaging methods are summarized in figure 2. Wafer level packaging methods by interfacial bonding are shown in figures 2(*a*)–(*d*) and described in section 2. Pyrex glass, which has a similar thermal expansion with silicon, is used as the lid wafer. It is anodically bonded to the MEMS wafer at approximately 400 °C by applying a negative voltage to the glass. Other interfacial bonding between metal and metal and plasma-activated bonding is also used. Electrical feedthrough is made using a via in the lid wafer.

Bonding with intermediate melting materials, such as low melting temperature glass and solder, is shown in figures 2(*e*) and (*f*) and will be described in section 3. These bonding techniques can be applied to a non-planer surface and hence lateral electrical feedthrough, which causes a non-planer surface, can be used.

MEMS can be encapsulated using surface micromachining, as shown in figures 2(*g*) and (*h*). The cavity is made by etching a sacrificial layer and the openings

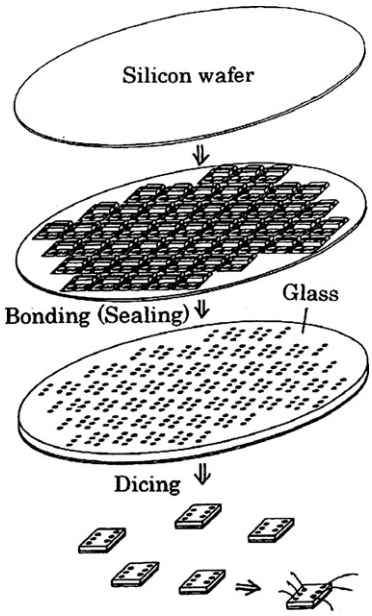

Figure 1. Concept of wafer level packaging.

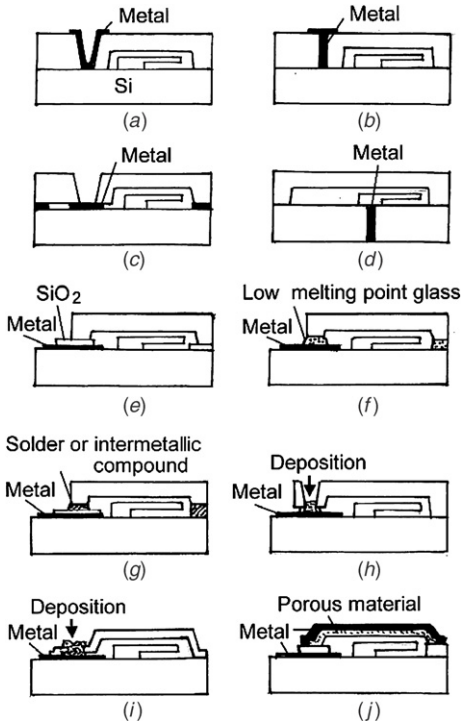

Figure 2. Various wafer level packaging methods. Each method is related to other figures, interfacial bonding ((*a*) figures 4–6, (*b*) figures 7, 19–21, (*c*) figure 8, (*d*) figure 22, (*e*) figure 18), bonding with intermediate melting materials ((*f*) figure 10, (*g*) figure 11) and deposition sealing ((*h* and *i*) figures 12, 17 and (*j*) figure 13).

needed for the sacrificial etching are plugged by deposition sealing as described in section 4.

A vacuum cavity is required for some MEMS devices, for example, resonators or infrared sensors. The vacuum packaging method and a structure to monitor the cavity pressure will be described in section 5.

The electrical feedthrough structures for the electrical interconnection are indispensable for wafer level packaging. These structures will be discussed in section 6.

2. Wafer level packaging by interfacial bonding

Interfacial bonding methods have been developed [2]. The lid used in interfacial bonding can act as mechanical protection for MEMS structures, as shown in figures 2(*a*)–(*e*). During the bonding process high temperatures, which damage the MEMS or the circuit, should be avoided and the surface of the processed MEMS wafer should be flat enough so that the wafers to be bonded can be atomically close. Si-to-Si direct bonding at high temperatures cannot be used for these reasons because it requires high temperatures and an atomically flat surface. It is difficult to make structures for electrical feedthrough on the surface of the MEMS chip as shown in figure 2(*e*), or vertical feedthrough in the MEMS wafer as shown in figure 2(*d*). The reason for the difficulties is the complicated process used to fabricate the electrical interconnections and the MEMS on the same wafer. For this reason, the electrical interconnections are made using the via in the lid wafer as shown in figures 2(*a*)–(c) in many cases.

2.1. Anodic bonding

A pioneering work of micromachining was carried out in the 1970s at Stanford University. A MEMS accelerometer was fabricated using wafer level packaging by glass-to-Si anodic bonding and is shown in figure 3(*a*) [3]. The electrical interconnections are made by connecting to the diffusion layers for the sensing piezoresistor to the outside of the cavity through a metal layer on the glass (figure 3(*b*)). This electrical interconnection causes a leakage current at the reverse biased pn-junction which contacts the glass.

Implantable oximetry developed at Stanford University is shown in figure 4 [4]. The electrical feedthrough for the interconnection was made through the holes in the glass lid, as shown in figure 2(*a*), and therefore the problem of leakage current could be solved. The holes in the glass were made using a CO_2 laser abrasion [5].

Electrical feedthrough using the via in the glass was applied to piezoresistive absolute pressure sensor [6] and also to the integrated capacitive pressure sensor shown in figure 5 [7]. Because of the integrated CMOS circuit used to convert from capacitance to frequency, a small change in the sensor capacitance can be detected and the sensor has been used for a low-pressure measurement. A study of circuits which can stand the anodic bonding process condition with high electric field at around 400 °C was carried out [8]. It was found that electrical shielding by metal on the oxide of a pn-junction surface could reduce the junction leakage current effectively [8]. Platinum on titanium was used for metallization on the glass because conventional aluminum metallization causes hillocks during the thermal process of anodic bonding. The hillocks should be avoided for capacitors

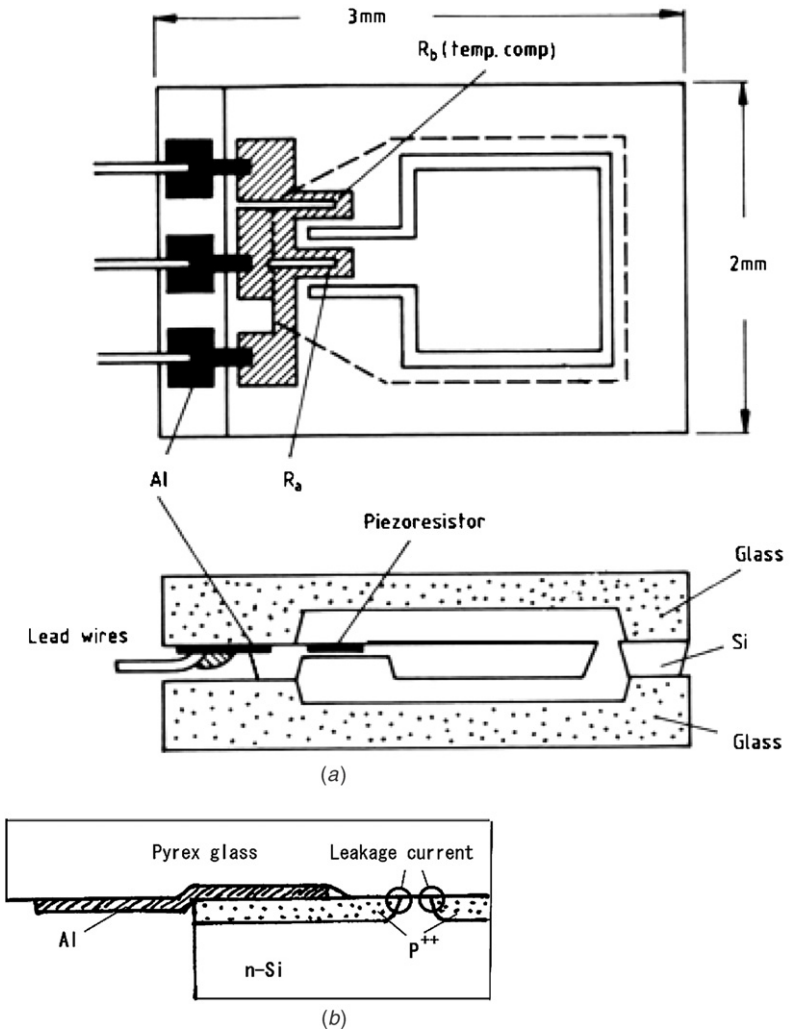

Figure 3. An accelerometer using lateral electrical feedthrough and the leakage current problem. (*a*) Accelerometer and (*b*) the leakage current problem.

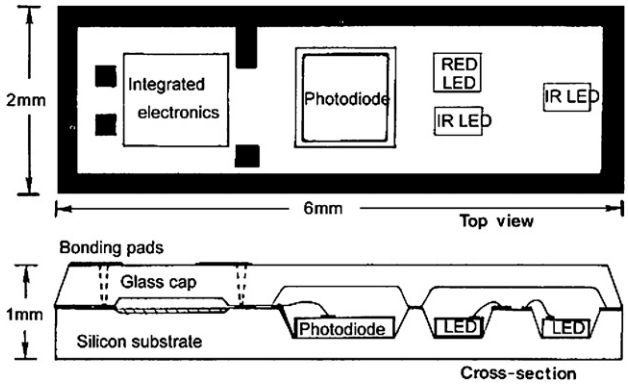

Figure 4. Implantable oximetry using electrical feedthrough of a glass hole (image reproduced from [4] with minor modifications, with permission from the authors and IEEE).

with a narrow gap. The metallization above the circuit was used for optical shielding from ambient light.

Wafer level packaging using the via in the glass was applied to a capacitive accelerometer. The fabrication process is shown in figure 6 [9, 10]. The etched silicon wafer, in which all components are mechanically connected, is anodically bonded to a glass wafer and then the support is etched out by dry reactive ion etching (RIE). The wafer is bonded with another glass wafer which has holes for electrical feedthrough, and finally chips are obtained by dicing the bonded wafer. The structural distortion caused by anodic bonding should be minimized to maintain a narrow gap of sensor capacitors. Using thick glass symmetrically on both sides and optimizing the bonding temperature can reduce the distortion caused by the mismatch of thermal expansion of the silicon and the Pyrex glass [11]. To prevent electrostatic attraction of the silicon seismic mass to the glass and unexpected sticking, the metal on the glass is electrically connected to the silicon during anodic bonding. After bonding it is disconnected by a laser from the outside of the chip [12].

MEMS switches also fabricated using wafer level packaging are shown in figure 7 [13]. The glass lid having

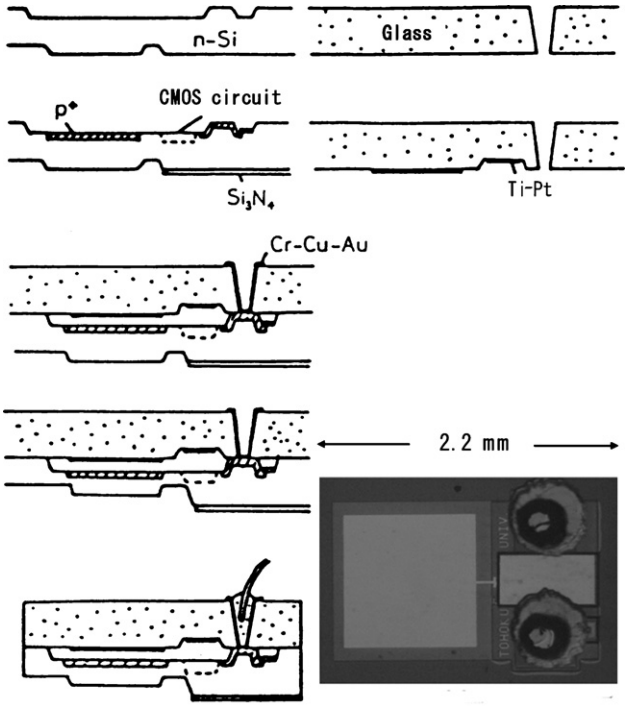

Figure 5. The process of an integrated capacitive pressure sensor.

electrical feedthrough was bonded to the silicon wafer in figure 2(*b*). A thermal actuator using different thermal expansion coefficients of aluminum and silicon dioxide was adopted for the switch. The surface of the electrical contact is kept clean because of the wafer level packaging, and a high reliability was achieved. The switch has been used for the latest LSI tester [14].

2.2. Other interfacial bonding (metal bonding and plasma-activated bonding)

If silicon is used as the lid wafer, the distortion caused by different thermal expansions of the glass–Si can be reduced and holes in the lid wafer can be made in the silicon by deep RIE. The fabrication process developed for a FBAR (film bulk acoustic resonator) is shown in figure 8 [15]. Gold is electroplated using a photoresist mold and the silicon is etched by deep RIE. The silicon lid wafer is bonded to the FBAR wafer by Au–Au thermo-compression bonding and the etched holes are exposed by grinding the lid wafer. Finally, the sealed wafer is diced into individual chips and wire bonding is carried out inside the exposed holes. This bonding scheme, shown in figure 2(*e*), allows for hermetic sealing and electrical interconnection simultaneously. Thermo-compressive Au–Au bonding [16, 17] and similar metal–metal bonding, Al–Al [18], Cu–Cu [19], can be carried out at temperatures acceptable for MEMS. Reproducible Au–Au bonding can be performed at low temperature by surface activation and cleaning using atom beam in a vacuum [20].

Wafers can be bonded at low temperature by activating the surface with plasma to leave the hydroxide group on it [21, 22]. Wafers can be bonded in atmosphere and hence can be

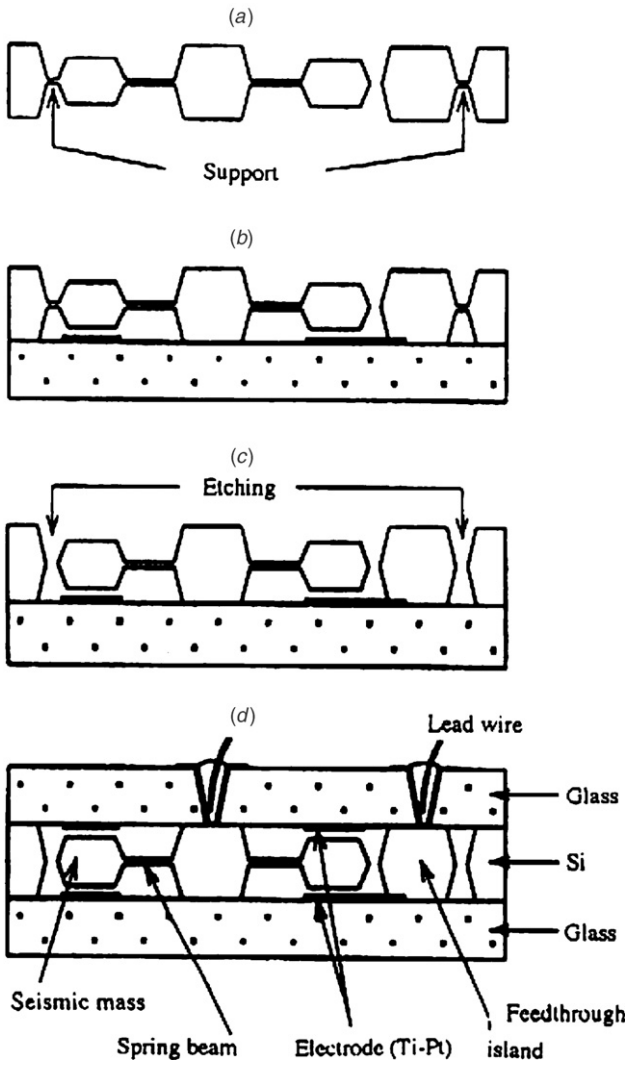

Figure 6. The wafer level packaging process of an accelerometer. (*a*) Wet etching, (*b*) anodic bonding, (*c*) reactive ion etching and (*d*) anodic bonding.

aligned precisely. Because of the low bonding temperature at around 300 °C, wafers which have different thermal expansion coefficients can be bonded. A GaAs wafer for a light emitting diode (LED) has approximately twice as large a thermal expansion coefficient as a silicon wafer, however owing to this low temperature bonding LEDs can be attached on the silicon CMOS wafer for an LED print head as shown in figure 9 [23].

If hermetic sealing is not required, the moving parts on the MEMS wafer can be protected by bonding a lid wafer with a polymer film [24–26]. A thin sealing film can be transferred to the surface of the MEMS wafer [27, 28].

2.3. Bonding with intermediate melting materials

The lid wafer can be bonded with intermediate melting materials as shown in figures 2(*f*) and (*g*). Even if the surface is not planar, the chip can be sealed by melting the intermediate

Figure 7. A MEMS switch using wafer level packaging.

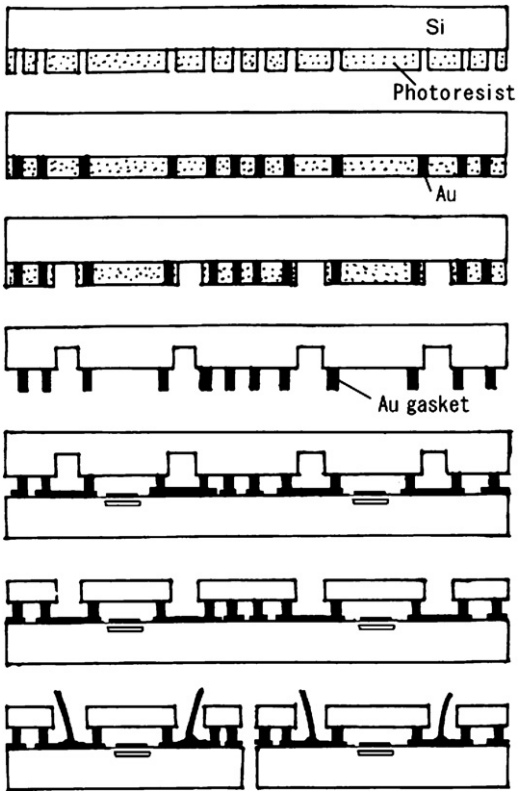

Figure 8. Wafer level packaging using metal bonding.

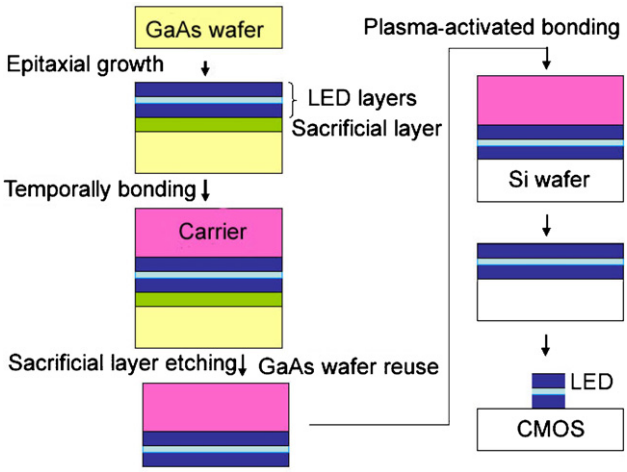

Figure 9. LED and the CMOS process by plasma-activated bonding.

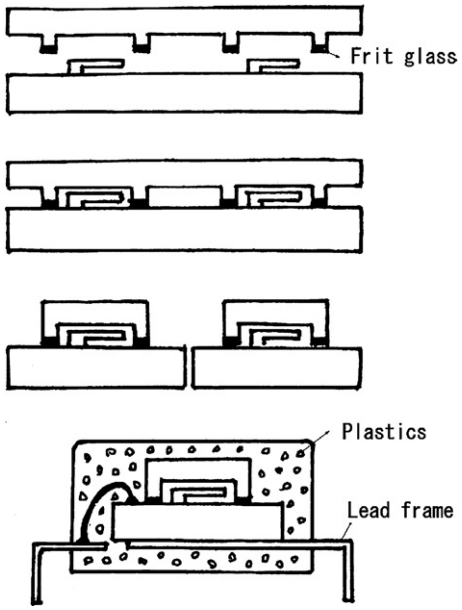

Figure 10. Wafer level packaging using frit glass bonding.

material. For this reason, lateral feedthrough on the chip can be used. Figure 10 is an example of the fabrication process for the structure shown in figure 2(f), which uses a low melting point glass (flit glass) as the intermediate material [29]. The flit glass is coated on the lid silicon wafer by screen printing. After assembling the lid wafer to the MEMS wafer, they are bonded by melting the glass at around 400 °C. The lid silicon is removed except where it covers the MEMS structure by dicing the bonded wafers and individual chips are separated. The chips are ready for wire bonding and plastic molding using conventional IC packaging.

Soldering [35] or Au–Si eutectic bonding can be also applied by melting it thermally as shown in figure 2(g). Local heating to melt the solder can be done by integrating an electrical heater under the solder on the chip [30, 31]. Because of the localized heating it could be applied even to sealing paraffin-filled micro cavities [32].

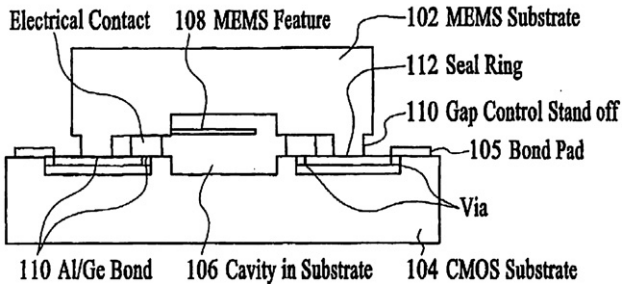

Figure 11. Application of Al/Ge bonding (image reproduced from [37] with minor modifications, with permission from the author).

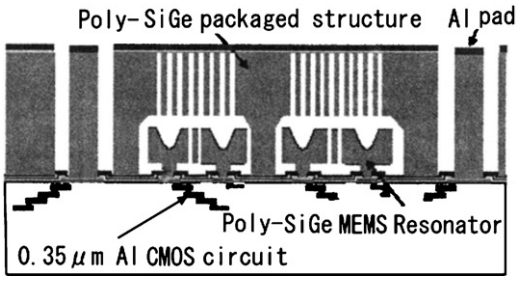

Figure 12. A wafer level packaged integrated gyroscope using thick poly-SiGe cover (image reproduced from [50] with minor modifications, with permission from the author and IEEE).

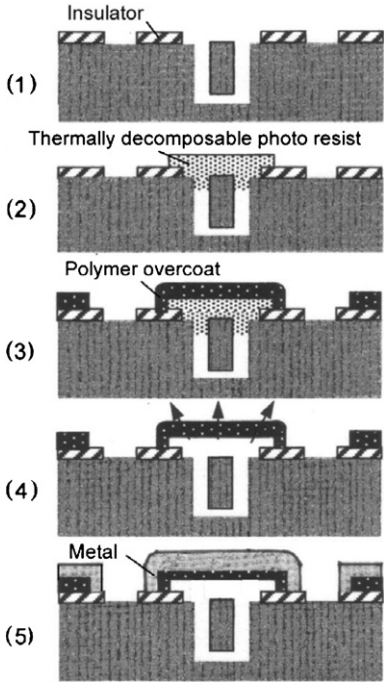

Figure 13. Wafer level packaging using thermally decomposable photoresist (image reproduced from [53] with permission from the author and IOP Publishing).

The disadvantage of bonding using the frit glass and the solder is that these can let out gas during melting, and the gap between the MEMS wafer and the lid wafer cannot be precisely controlled. However, these disadvantages are solved by following bonding with metals.

Bonding of silicon wafers with In on Au at around 200 °C [33] or that with Sn on Ni [34] and Sn on Cu at around 300 °C [35] can be performed with an external applied pressure. This is called TLP (transient liquid phase) bonding [34, 36] or SLID (solid–liquid interdiffusion) bonding [35]. Figure 11 is an example of the wafer level packaging using Ge to Al bonding [37]. The MEMS substrate having Ge on it was bonded to the Al layer on the CMOS substrate and this new method of wafer scale packaging has been utilized by a MEMS gyroscope company, InvenSense, USA, on their Nasiri Fabrication. The wafer level packaging by TLP bonding with Ni–Sn can be made by the transfer of temporally soldered lids [38]. This is because the TLP bonding causes intermetallic compounds at 300 °C, however the melting temperature of the joint is raised to over 400 °C after bonding and the transfer with a Pb–Sn solder layer can be carried out. The metal surface can be cleaned by removing the surface oxide to improve bonding or to reduce a contact resistance. Diluted hydrofluoric acid, chemical vapor cleaning using formic acid gas and atomic hydrogen by plasma or by catalytic hot filament are utilized for these purposes.

Adhesive polymer can also be used as intermediate materials [39–41], however the adhesive polymer is not suitable for hermetic sealing because gas permeates the polymer. Sealing of a liquid-filled cavity can be done by injecting polymer adhesives in a channel surrounding the cavity after stacking the wafers with liquid in the cavity [42].

3. Deposition sealing

Narrow gaps for electrical feedthrough made between the MEMS wafer and the lid wafer can be sealed by depositing material, as shown in figure 2(*h*) [43, 44].

MEMS structures protected by an overcoat can be made by sacrificial etching, which requires a port for the etching solution or gas to access in the cavity. The channels or the holes used as the access port can be sealed by depositing materials as shown in figure 2(*i*) [45–49]. Figure 12 shows an integrated resonating gyroscope in which the poly-SiGe resonator is protected with a thick poly-SiGe cover [50]. This was fabricated by etching out the sacrificial layer through vertical holes in the thick poly-SiGe cover; after sacrificial etching the holes were plugged by deposition. The MEMS chips covered with the thick poly-SiGe can be molded by a plastic material like conventional IC packaging.

Sacrificial etching can be carried out through porous materials such as porous poly-Si [51, 52] or through a gas permeable membrane, as shown in figure 2(*j*). The sealing can be done by depositing some material on the porous material. A permeable membrane is used in figure 13 by the following process sequence [53]. After making MEMS in the silicon wafer by etching (figure 13(1)), the MEMS are covered with patterned photoresist (figure 13(2)) and polymer overcoat (figure 13(3)). Since the photoresist thermally decomposes at 200 °C, the decomposed gas is diffused out through the polymer overcoat by heating (figure 13(4)). Finally, a metal is

deposited on the surface of the polymer overcoat for hermetic sealing (figure 13(5)).

The sealing methods other than deposition are those by soldering [54]. Narrow channels can also be plugged by reaction sealing in which the channel walls inflate by silicon oxidation [55, 56].

Deposition for the sealing should have minimal influence on the MEMS structure. The achieved cavity pressure depends on the deposition conditions, however this can be solved by evacuating the residual gas as will be explained for figure 17.

4. Vacuum packaging

Vacuum packaging is required for some MEMS devices, for example capacitive diaphragm vacuum sensors, resonators in which there is the need to avoid viscous dumping for high Q-factors or thermal infrared sensors in which thermal dissipation by convection should be minimized [57].

It was found that gaseous oxygen is generated at the glass–Si interface during the anodic bonding process. Figure 14 is evidence of the oxygen generation by electrochemical decomposition of the glass [58]. Silicon with a thin diaphragm is anodically bonded to a glass wafer in a vacuum. Samples with a large cavity volume showed a deflated diaphragm when it is exposed to the atmosphere. On the other hand, the diaphragm with the small cavity volume inflated because of the oxygen generation.

To make a vacuum cavity, anodic bonding is carried out in a vacuum with a non-evaporable getter in the cavity [59]. The getter adsorbs gases by activating at the temperature for anodic bonding. Examples of vacuum-packaged MEMS are shown in figures 15(*a*) and (*b*). Figure 15(*a*) is a capacitive vacuum sensor with a silicon diaphragm which has a vacuum cavity as the reference pressure [60, 61]. Figure 15(*b*) is an electrostatically levitated rotational gyroscope which requires a vacuum cavity to avoid viscous friction, while rotating at 2000 rpm [62]. The non-evaporable getter made on a wafer was developed for wafer level batch fabrication of the vacuum cavity [63, 64]. A getter film, 2 μm thick sputtered titanium, could be used for the wafer level packaged device made by transient liquid phase (TLP) bonding [30]. TLP bonding was

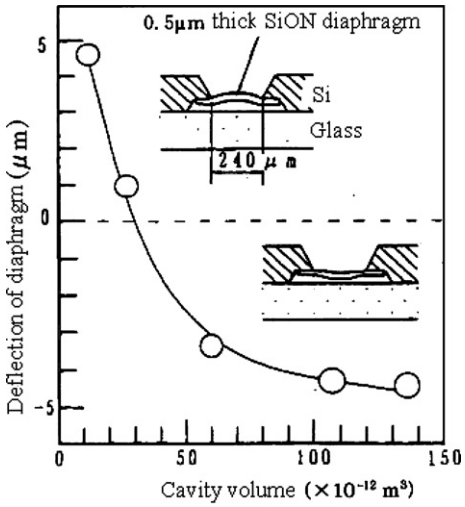

Figure 14. Evidence of electrochemical gas generation during the anodic bonding process.

carried out using wafers having Sn on Ni layers in a vacuum at 300 °C and then the bonded wafer stack was annealed at 400 °C to activate the titanium getter film.

The cavity pressure should be controlled for critical damping of the seismic mass for an accelerometer [65]. A silicon wafer is anodically bonded to a glass wafer in an argon gas environment with pressure (P bonding). The argon gas is not absorbed by the getter and therefore the measured cavity pressure (P measured) is determined by the absolute temperature for bonding (T bonding) and the absolute temperature for measurement (T measured) based on Boyle's law as follows [65]:

$$P \text{ measured}/P \text{ bonding} = T \text{ measured}/T \text{ bonding}.$$

The vacuum packaging can be characterized by different methods [66]. In figure 16(*a*), the cavity pressure is measured by determining the outside pressure when the diaphragm is flat or the outside and inside pressures are equal [67]. This structure can be also used to monitor gas leakage by accumulating the leaked gas. An example of the measurement

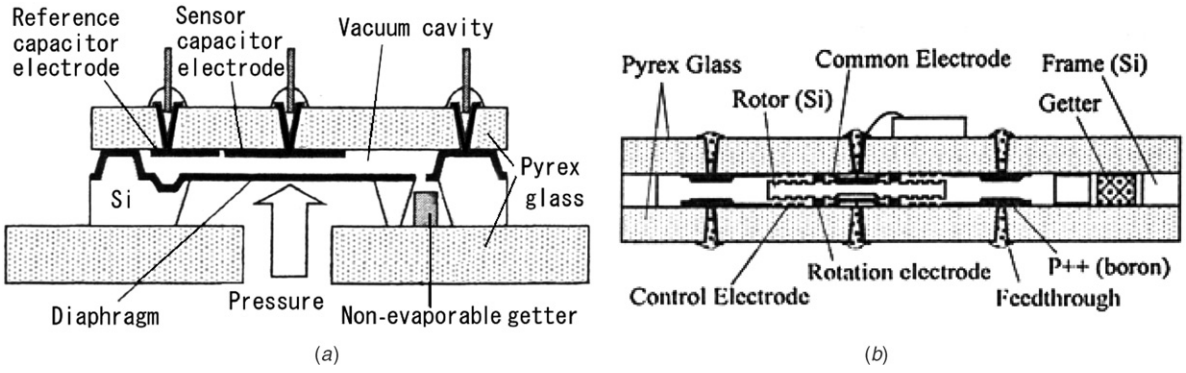

Figure 15. Applications of vacuum packaging. (*a*) Silicon diaphragm capacitive vacuum sensor and (*b*) electrostatically levitated rotational gyroscope.

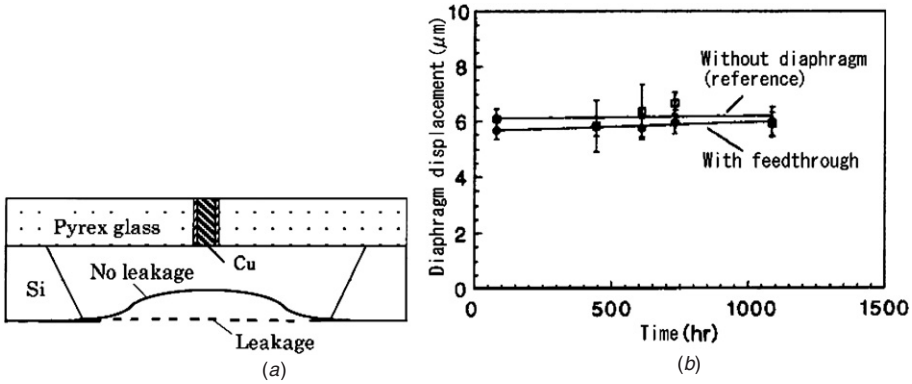

Figure 16. Cavity pressure measurement and gas leakage monitoring. (*a*) Structure and (*b*) example of monitoring gas leakage.

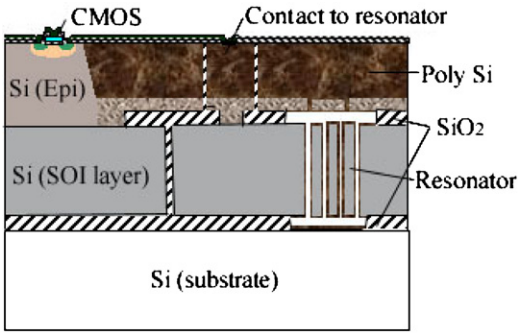

Figure 17. Micromechanical resonator formed inside the silicon wafer.

is shown in figure 16(*b*). The structure can be installed with a MEMS device having a vacuum cavity.

An example of vacuum packaging by deposition sealing is shown in figure 17 [68]. This is a micromechanical resonator for generating timing and frequency signals. A vacuum cavity is required to prevent the damping of the resonator. The resonator is made of silicon single crystal and sealed with chemically vapor deposited poly-Si [69]. The fabrication process is as follows. The resonator is fabricated by deep RIE of the active layer of a SOI wafer. After the deposition of silicon dioxide, the surface is polished and a thin poly-Si layer is deposited. The silicon dioxide is etched out through a hole made in the thin poly-Si layer. After etching, the hole is sealed by depositing a thick poly-Si layer. Trenches are made by deep RIE and refilled with deposited silicon dioxide, to make isolated electrical interconnections from the resonator. In the same process step as the poly-Si deposition, a single crystal silicon can be grown on the exposed silicon of the wafer and is used to make integrated CMOS circuits. Hydrogen gas resides in the cavity during the poly-Si deposition, however the residual hydrogen gas is diffused by keeping it in a hydrogen-free environment at high temperature and hence a vacuum cavity is made inside the wafer [70].

5. Electrical feedthrough

Electrical feedthrough is needed for interconnection from the encapsulated MEMS in a cavity. The process compatibility for the feedthrough and the MEMS is required. Normally metal is used as the feedthrough material, however highly doped silicon can also be used as shown in figure 17. The metal has low resistance, while the silicon has the same thermal expansion as the substrate. Stray capacitance and stray inductance have to be taken into account in the application of RF. Lateral feedthrough on the chip surface and vertical feedthrough using a through hole via will be described.

5.1. Lateral feedthrough

An example of lateral feedthrough on a chip is shown in figure 18 [71]. This has a metal layer embedded in silicon dioxide and the surface is sealed by anodic bonding with a glass lid wafer as shown in figure 2(*e*). After etching the silicon dioxide on a silicon wafer (figure 18(1)), the etched groove is filled with Cr–Al (figure 18(3)). The surface is coated with SOG (spin on glass) to insulate and to make a planar surface (figure 18(4)) and silicon is sputter deposited on it (figure 18(5)). This is anodically bonded to a Pyrex glass wafer (figure 18(6)). It was found that this lateral feedthrough is not so practically applicable compared with the vertical feedthrough described below, because the lateral feedthrough has to be fabricated on the same wafer as the MEMS. There are other lateral feedthrough technologies using a planarized surface by reflow [72] or a thin metal layer [73].

5.2. Vertical feedthrough

The electrical interconnection can be made using a through hole via in the wafer, as shown in figures 2(*a*)–(*d*) [74]. The advantage of vertical feedthrough in the lid wafer (figures 2(*a*)–(*c*)) is that the electrical interconnection can be fabricated on a different wafer from that of the MEMS wafer and therefore process compatibility is not required. Feedthroughs have to be made in a glass wafer for anodic bonding as described in section 2.1. However, it is not easy to make through holes in the glass because anisotropic etching cannot be applied to the amorphous glass. Sandblasting makes conical shape holes as shown in figures 5 and 6. The feedthrough is made by metalizing the inner wall of the hole after the glass–Si anodic bonding, as shown in figure 2(*a*). On the other hand, glass which has feedthrough in it can

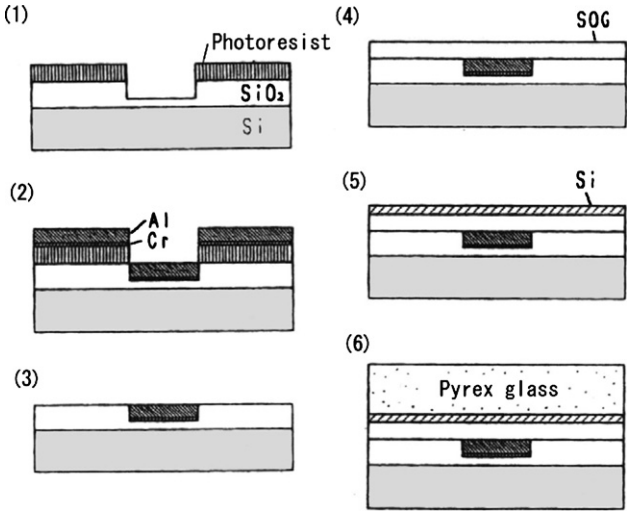

Figure 18. Lateral feedthrough. (1) Oxidation, photolithography. (2) Cr, Al evaporation. (3) Lift-off. (4) SOG coating, (5) Si sputtering and (6) anodic bonding.

be used for anodic bonding, as shown in figures 2(*b*), 7 and 16. Figure 19 is a picture of the cross-section of the glass in which feedthrough is made by filling the through hole with an electroplated copper [75]. The through holes are made in the glass with a femtosecond laser. The thermal stress caused by the different thermal expansion between the glass and the filling metal has to be minimized, otherwise it will cause a crack during the anodic bonding process. For this reason, the diameter of the hole should be small or the filling metal and glass should have similar thermal expansion coefficients [76].

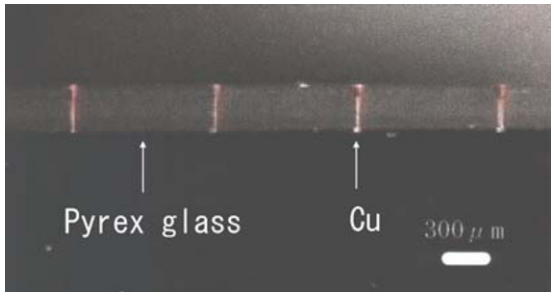

Figure 19. Electrical feedthrough with filled through hole in a glass.

The hole should not be conical in order to prevent the glass wafer from bending due to the gradient of the thermal stress.

Sandblasting, electrochemical discharge drilling [77], laser drilling [75], ultrasound drilling or mechanical drilling can be applied to make through holes in the glass, however these methods are not batch processes. Deep RIE is suitable for making many holes in batch process, however it is difficult to make deep holes in a glass wafer because the glass etching rate is slow (∼0.5 μm min^{-1}) [78]. The deep RIE of the glass wafers has been applied to wafer level packaging, using temporary bonding which will withstand the temperature for anodic bonding [78]. The process steps are shown in figure 20. A glass wafer is etched by deep RIE to make shallow holes (figure 20(1)) and the holes are filled with electroplated metal (figure 20(3)). After polishing the surface of the glass wafer, it is bonded to a handling wafer with polyimide (figure 20(4)). The handling wafer has grooves in it and germanium is deposited on the surface with the grooves. By grinding and polishing the glass, the metal is exposed (figure 20(5)) and the glass wafer is anodically

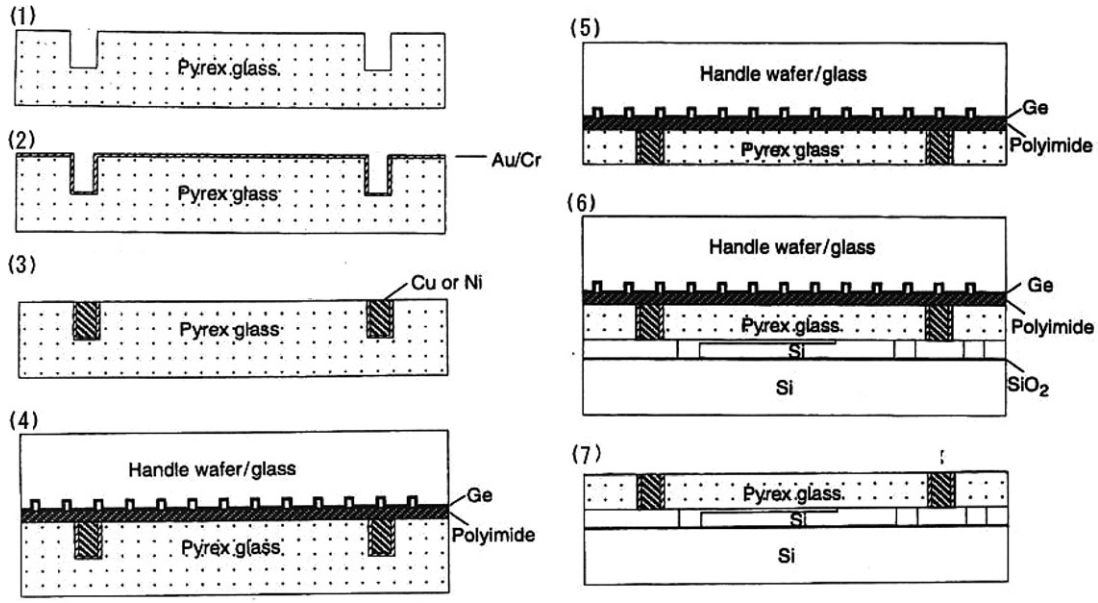

Figure 20. Wafer level packaging using glass RIE and temporally bonding. (1) Deep RIE, (2) deposit seedlayer (Au/Cr) by sputtering, (3) electroplating and chemical mechanical polishing, (4) adhere to handle wafer by polyimide, (5) pyrex glass polishing, (6) bond to silicon probe by anodic bonding and (7) Ge etching and polyimide etching.

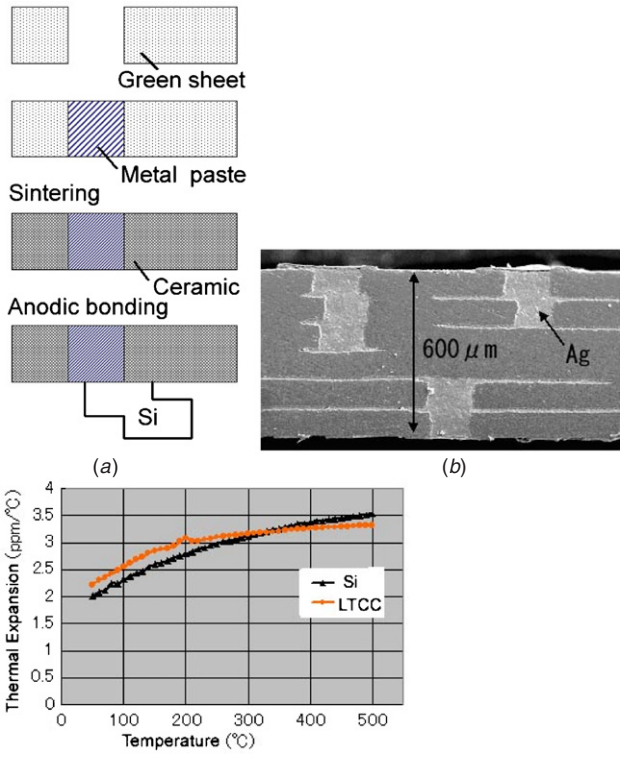

Figure 21. Feedthrough in LTCC with close thermal expansion with silicon. (*a*) Fabrication process, (*b*) photograph of the cross-section and (*c*) thermal expansion of the silicon and the LTCC.

bonded to the silicon wafer (figure 20(6)). Finally, the handling wafer is detached in boiling hydrogen peroxide as shown in figure 20(7), because the hydrogen peroxide penetrates in the grooves of the handling wafer and the germanium is etched out.

Feedthroughs can be made in LTCC (low temperature co-fired ceramics) [79, 80]. As shown in figure 21(*a*), the through holes are made by puncturing the soft green sheet and the holes are filled with a silver paste. The sheet is sintered to make a ceramic and the lateral dimension can be controlled by sintering under pressure. This LTCC wafer can be anodically bonded to a silicon wafer. A multilayered ceramic wafer is fabricated by laminating the green sheets before sintering. The photograph of the cross-section of the LTCC with feedthrough is shown in figure 21(*b*) [80]. The thermal expansion of the LTCC is matched with silicon, as shown in figure 21(*c*).

The LTCC with feedthrough was applied to a MEMS probe card for the wafer level burn-in test [81]. The fabrication process and photograph are shown in figure 22. Nickel probes are made by electroplating Ni into a silicon mold and then soldered with AuSn to the LTCC wafer. Finally, the silicon mold is etched out. The probe card has similar thermal expansion to silicon, which makes reliability testing at elevated temperatures on a wafer possible.

Vertical feedthrough can be made in a silicon wafer on which MEMS are fabricated [82], as shown in figure 2(*d*) [83]. The vertical feedthrough in a silicon wafer is also used for 3D stacked LSI [84]. That with reduced stray capacitance can be fabricated as follows [85]. After making a trench in a silicon wafer by deep RIE, silicon islands are metalized by copper CVD and then the trench is refilled with silicon dioxide without void using ozone-TEOS (tetra-ethoxy ortho silicate) CVD [86]. Finally, the backside of the silicon wafer is ground and both sides are metalized.

6. Conclusion and discussion

The wafer level packaging of MEMS is important for the production of practical MEMS because this can reduce the cost of packaging and testing and also improve the yield and reliability. Wafer level packing is made by bonding a lid wafer to a MEMS wafer or by sealing the opening used for sacrificial etching. Vacuum cavities can be made for micromechanical resonators and other devices. Fabrication methods for electrical feedthroughs were also presented. Deep RIE of glass and low thermal expansion LTCC can be applied for high-density vertical feedthrough.

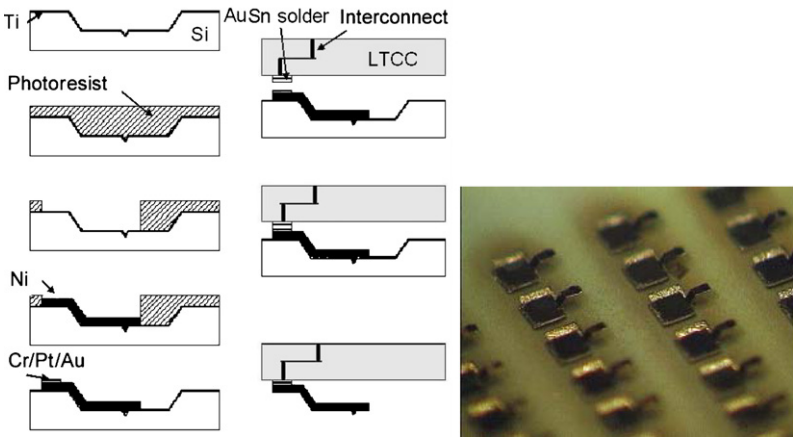

Figure 22. Probe card for wafer level burn-in using LTCC with close thermal expansion with silicon.

Laser dicing methods by making cracks in silicon [87] and glass [88] have been developed. These are effective to separate chips from the MEMS wafer, where the MEMS devices are not sealed. Laser dicing does not need water and hence the MEMS are not contaminated.

Even for the assembled MEMS like catheter chip devices, it is effective to make MEMS suitable for assembly in the wafer process. This will reduce the assembly cost and ensure reliability [89].

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