Wafer Level Packaging and 3D interconnect for IC Technology

R. Islam[1)], C. Brubaker[1)], P. Lindner[2)], C. Schaefer[2)]
[1)] EV Group US Inc., 3701 E. University Drive, Suite 300 Phoenix, AZ 85034, USA,
E-mail: Sales@EVGroup.com, Phone: +1 602 437 9492
[2)] EV Group, St. Florian, A-4780 Schaerding, Austria,
E-mail: Sales@EVGroup.at, Phone: +43 7712 5311 0

***Abstract*--The packaging of an IC chip (die) encompasses a multitude of assembly and packaging issues. The important factors for packaging technology are costs of IC packaging, the impact of the package on the circuit and system performance, and on the reliability of the package. Wafer level packaging technology has shown to be a promising solution for future IC generations. This paper reviews wafer level bumping process and it's requirement for thick resist coating and full field aligned exposure.**

3D interconnect technology is a viable solution for increasing electronic device functional density and reducing total packaging costs[1]. The critical issue is the ability to align and bond with precision, one micron or less, two silicon wafers or a silicon wafer to another substrate. For CMOS devices this technology will be applied for chip-scale packaging and also for advanced 3D interconnect processes. In this paper we will describe a new approach to wafer-to-wafer alignment using alignment targets at the bond interface i.e. face to face wafer alignment (SmartView™) that relies on precision alignment positioning systems to register and align wafers with one micron or better precision.

Keywords: 3D interconnect, IC packaging, flip chip bumping, face-to-face alignment

I. Introduction

For high-price and high-speed microprocessors and ASICs, the complex IC designs require very high I/O and performance packaging. In wafer level packaging, cost per package is primarily determined by the number of chip or die per wafer rather than number of I/O per device. Therefore wafer level packaging is very cost effective compared to traditional wire bonding and tap automated bonding (TAB). For these types of ICs and subsystems, area array flip chip technology provides a viable answer to the needs. The past few years have witnessed explosive growth in the research and development efforts devoted to solder-bumped flip chips as a direct result of the higher requirements of package density, performance, and interconnection and limitations of wire bonding technology.

Today, more than 90 percent of the chips used have wire bonds. Fewer than 4 percent of the chips now used have solder bumps[2]. There are several coherent problems with wire bonding, especially for high I/O connections, peripheral technology, which are difficult to rework. In comparison with the popular wire-bonding face-up technology, flip chip technology provides higher packaging density (greater I/Os) and performance (shorter possible leads, lower inductance, and better noise control), smaller device footprints, and a lower packaging profile[2]. Just like many other new technologies, low cost solder bumped flip chips still face certain critical issues, as for examples, the infrastructure of flip chips is not well established, solder joint reliability is more critical, and sometimes uses underfill processes, which decreases manufacturing throughput.

In the advanced packaging field, thick resist layers and full field aligned exposure are needed. First of all, there is a need for a thick layer of resist, 5-20 μm thick, that will remain as part of the device in the redistribution layer. In addition, another layer of resist will be used as micromolds for bond pads. These bond pads can be made out of several materials, although the most common are solder, gold, and copper. Depending on the material used for creating the bond pads, resist thicknesses ranging from 2 μm to 100 μm can be required.

To obtain ultimate performance in terms of chip

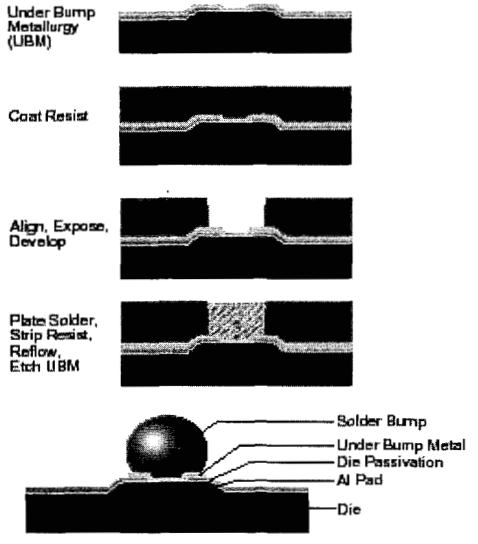

Figure 1. Flip chip technology and wafer bumping process

density and product performance requires "stacking" of multiple silicon wafers or substrates. These are necessary for the advancement of many devices such as PDAs, memory cards, smart cards, cellular telephones and gaming devices. Accomplished by stacking chips, modules, or wafers, devices can now be fabricated with multiple functionality or even high levels of device integration, such as IC-MEMS. For CMOS devices this technology will be applied for chip-scale packaging and also for advanced 3D interconnect processes.

3D interconnect bonding is the process of bonding two (or more) device wafers together with the intention of creating a three dimensional network of circuitry. The process steps involved in the aligned bonding procedure are the application of an intermediate layer, wafer alignment, and bonding. Because of the high density of interconnects required between the substrates, a large degree of alignment is necessary between the substrates to ensure proper assembly. An additional constraint is placed on the process by the fact that the IC industry almost exclusively uses single side processing. Therefore, process equipment has been developed that allows the high precision, face to face alignment of wafers[3]. Figure 2 shows two wafers, which are aligned and bonded together using an adhesive layer. Copper vias connect the conventional interconnects on both wafers, with high aspect ratio backside contacts.

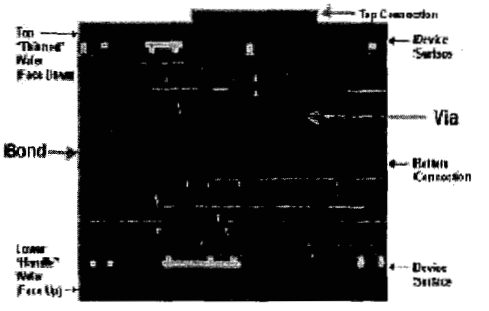

Figure 2. Schematic view of 3D chip stacking. Courtesy of Focus Center – New York, Rensselaer: Interconnections for Gigascale Integration.

II. The Challenges of Thick Resist Processing for Bumping Application

Photoresist processing requirements for wafer bumping applications vary greatly from the requirements for VLSI (Very Large Scale Integration) photoresist processing. VLSI photoresist processes use thin layers to transfer small features with submicron tolerances. Bumping applications require thick photoresist, typically in 5 – 150 μm films, to transfer large (50 – 250 μm) features, with tolerances approaching micron scale.

Several bumping applications exist, each having a different requirement for resist thickness and sidewall profile. Typically, bumping applications will make use of a positive tone photoresist. For the patterning of a redistribution layer, a 5-10 μm resist layer possessing vertical sidewalls is required. This can be achieved by AZP4620. Gold bumping requires a layer of 20-40 μm thickness, again with vertical sidewall, which can be produced using Shipley 5740 photoresist. Solder bumping and copper posts can require a film thickness of up to

150 μm, for which JSR THB611P resist can be used. In addition, some negative tone photoresists, such as BCB can be used.

Coating is the first step for photoresist processing. The properties of thick resists, such as a relatively low solvent content and an increased viscosity, require special considerations in the coating process. These properties can cause issues with coating uniformity. Because of the low solvent content, use of a cover integrated with the coating system can be used to improve coating uniformity. The purpose of this cover is to trap any evaporating solvent within the coating chamber, creating a solvent rich atmosphere. This prevents the loss of solvent within the resist, allowing the resist to spread evenly to the thickness that is determined by the rotational speed. This effect can be further optimized by the addition of an exhaust/purge system that can be used to precisely control the level of solvent within the spinning chamber.

In addition, with all thick resists, the high viscosity of the resist causes the development of an edge bead that can be several times thicker than the film thickness over the remainder of the wafer. This edge bead can cause problems in subsequent contact exposure steps, since the height of the edge bead will actually cause a proximity exposure rather than a contact exposure.

In order to avoid this, the edge bead must be removed. One effective manner in which to do this is by integrating the edge bead removal process into the coating process. Through use of a programmable arm that can be extended over the coating bowl, a stream of solvent can be delivered to the edge of the wafer that will dissolve the edge bead.

Once the wafer has been coated, it is then necessary to bake the wafer. Baking is key in achieving straight sidewalls in thick resists. All solvent must be driven from the resist, or else the sidewall profile will suffer. However, care must be taken so that the solvent is not driven out too rapidly, as cracks and bubbles in the resist may result. Use of proximity pins to perform a ramped proximity bake, in combination with a programmable exhaust system, can be used to control the rate of solvent removal to eliminate these effects. In addition, good temperature uniformity is vital to ensure that solvent is removed evenly from the entire surface of the wafer.

In addition to specific requirements for coating systems, contact/proximity exposure systems are also suitable for advanced packaging. There are many advantages in the use of contact/proximity exposure systems over the stepper use in semiconductor industry. Some of the benefits over exposure are for 1x proximity exposure with a mask aligner the very edge chips can be integrated to the mask design, It is even possible to expose the wafers edge in order to get a very precise edge bead removal. Multiple chips are generally within one exposure field on a 1x stepper for bumping, single chips per exposure for stepper would reduce throughput dramatically, and after all the cost of ownership is too high for stepper.

III. 3D Interconnect through Aligned Wafer Bonding

Three-dimensional interconnect technology has the capability to truly allow the expansion of IC into a new dimension. By allowing the extension of circuitry from purely planar to spatial regime, 3D interconnect technology provides a new avenue for an increase in electronic device functional density. The benefits of this are well known. The fact that wire lengths are shortened to the micro scale will reduce the signal time delay, parasitic power loss, and overall power consumption. Additionally, it will result in an increase in speed, an increase in the number of neighboring devices, and bandwidth. Additionally, devices can be created with multiple functions, extending the "system on chip" concept.

However, 3D interconnect performed on a chip scale is simply not an economic process. The overall throughput that can be achieved is limited. Wafer level alignment and bonding processes are an enabling step that will allow a truly economic method for the productions of 3D interconnect devices. The basic process for wafer level 3D interconnects begins with the alignment of two wafers.

Prior to alignment, the wafers had vias patterned into the wafer, and metal interconnects are placed through the vias. Once the wafers are aligned, they are bonded via a variety of methods.

After bonding, one of the wafers is thinned to just a few microns. Then, another wafer is aligned and bonded to the stack. The process can be repeated several times to increase device density. See figure 3 for a diagram of the process.

Key to this process is the ability to perform highly accurate wafer to wafer alignment, usually better than one micron. Because of the extreme conditions required for most wafer level bonding processes, it is not possible to perform alignment with this level of accuracy in the bonding apparatus. Highly precise stage motors and precision optics cannot withstand the high temperatures involved. Instead, a separate tool is required to perform the alignment.

Several methods exist for the alignment of two substrates. Use of infrared light to illuminate alignment keys through the substrates is one, but this method is not suitable for all materials, as the doping level of the silicon or the presence of metal can make it impossible to see through the wafers. The use of backside alignment keys was developed in the MEMS industry to allow aligned bonding. However, the manufacturing of MEMS often involves, and sometimes requires, double side processing of wafers. In order for a process to be fully accepted into the IC industry, only single sided patterning can be allowed. Thus, only a method that will allow face to face alignment of two substrates is acceptable.

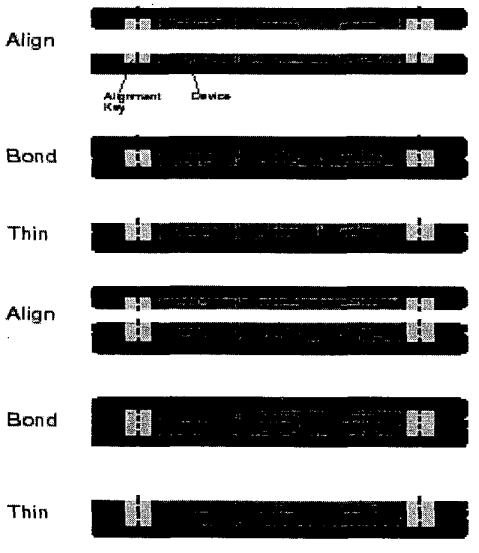

Figure 3. 3D Interconnect with multi-wafer stacking

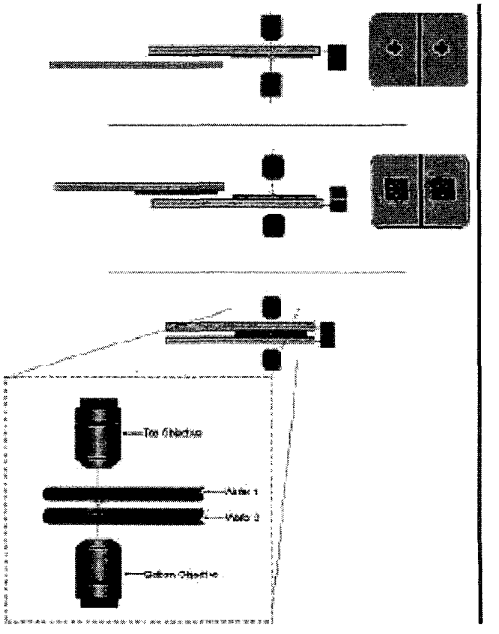

Figure 4. SmartView® Process

Two methods exist to allow face to face alignment of two wafers. One, called inter-substrate alignment, involves the use of optics located between the two substrates for alignment. However, several problems exist with this method. First, parallax concerns for the optics observing the top wafer, vs. the optics observing the bottom – a one degree misalignment between top optics and bottom can create a misalignment of several microns between the two wafers. Second, because of the large travel distance required to bring the two wafers into contact (at least 100 mm), there a large risk of alignment shift.

A second method, called SmartView®, makes use of optics located above and below the wafer

pair to perform the alignment. The process begins with a calibration of top and bottom optics to a single image. Then, stage motors move the top wafer into view of the bottom optics. A digital image is created of the alignment keys on the face of the top wafer. The top wafer moves back and is replaced by the bottom wafer. The top optics are used to align the keys on the bottom wafer to the digitized image from the bottom optics. Once alignment is complete, the top wafer is moved back in and, using highly precise position sensors, placed in the exact same position as it had initially rested, providing an alignment accuracy of better than one micron. The substrates are placed together (with a z-axis motion of ~50 μm), and clamped into place on a removable bond fixture. This fixture would then be transferred to the bonding equipment. See figure 4 for a description of this process.

Wafer alignment is accomplished using encoded stage motors allowing X and Y movements in increments of 0.1 μm steps and minimized Z-axis travel controlled by three software controlled spindle motors to preserve planarization between the top and bottom wafers. The repeatability of the measurement system is <0.35 μm.

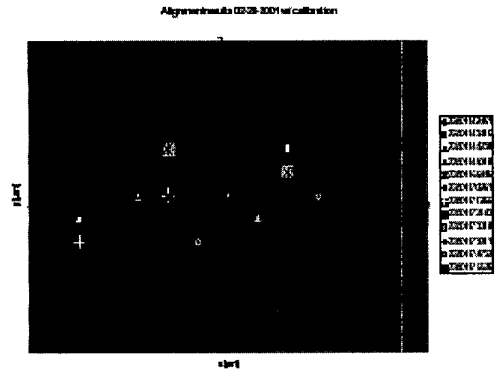

Figure 5. SmartView™ Alignment Results

Figure 5 shows typical alignment results between pairs of 200 mm wafers by using the SmartView® wafer-to-wafer bond alignment system. All pairs of wafers are within 1.5 micron alignment in X and Y. The standard deviation in this is between 0.3 and 0.4 microns.

Once the wafers are aligned, several methods exist to allow bonding. One of these is the use of a metal intermediate layer (for example, aluminum, gold, copper, etc.) as a "glue" between the two layers. Bonding is accomplished by the application of high temperature (from 360°C to 550 °C, depending on the materials) and force (up to 40 kN). Additional parameters, such as ambient atmosphere and vacuum, can be controlled as well.

Another method is the use of silicon direct bonding, which involves the bonding of two highly polished surfaces without the use of an intermediate layer. Instead, the two extremely smooth (surface roughness < 0.5 nm) surfaces are brought into close contact, at which point Van der Waals forces will cause the two wafers to become weakly bonded. Wet chemical methods can be used, prior to bonding, which will strengthen this bond. The bond is further strengthened and made permanent by placement into an annealing furnace. Typically, this furnace will require temperatures in excess of 1000°C. However, methods exist that can reduce this temperature requirement[4].

Yet another possibility is to use polymers as intermediate layers, allowing a lower processing temperature requirement (in the order of 150 – 300°C) compared to most metal to metal bonds. Among the possible materials are low-k dielectrics such as BCB (Cyclotene™) and spin on dielectrics (SOG). A variety of other polymers are currently under investigation[5].

IV. Conclusion

Over the years, semiconductor packaging has lagged behind wafer fabrication in process sophistication and manufacturing demands. The advent of VLSI-ULSI era in chip density has forced a radical upgrading of chip packaging technology and production automation[6]. Advanced wafer level packaging is becoming a key element for a high density, low cost chip packaging solution. Consumer demands have pushed for a shrinking of device size and an increase of functional density, most predominantly in the consumer product sector. 3D interconnect through wafer level aligned bonding is used to build stacked wafer devices that succeed in accomplishing the increase in functionality. To facilitate the fabrication of stacked wafers devices, a

face to face alignment systems the SmartView® were presented. The SmartView® allows micron level wafer to wafer alignment to be achieved by use of sophisticated electronic control and limited axis motions between alignment and contact modes. Introduction of new and unique production tools is required to enable advanced packaging to build tomorrows electronic devices.

References

[1]. S. Savastiouk, O. Siniaguine and E. Korczynski, "3D stacked wafer-level packaging," Advanced Packaging, March 2000, pp. 28-34.

[2]. J.H. Lau, Low Cost Flip Chip Technologies, New York, McGraw-Hill, 2000.

[3]. Brubaker, C. W.; Glinsner, T.; Lindner, P.; Schaefer, C., "One Micron Wafer to Wafer Alignment For 3D Interconnecting Device Integration", Proceedings 2001 Joint International Meeting of The Electrochemical Society, Sept. 2001

[4]. Farrens, S.; Dekker, J.; Smith, J.; Roberds, B. "Chemical Free Room Temperature Wafer to Wafer Direct Bonding", J.Electrochem. Soc., Vol. 142, No. 11, Nov. 1995, pp. 3949-3955

[5]. Y.Kwon, J.-Q.Lu, R.J.Gutmann, P.P.Kraft, J.F. McDonald and T.S.Cale, "Wafer bonding Using Low-k Dielectrics as Bonding Glue in Three-Dimensional Integration" - The Electrochemical Society, 2001 Joint Meeting, September 2-7, 2001 San Francisco

[6]. Z. Peter, "Microchip Fabrication: A Practical Guide to Semiconductor Processing" Third Edition, New York, McGraw-Hill, 1997.