An Advanced 3D Interconnect and Packaging Technology: Through Silicon Via (TSV)

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***Abstract*—The idea of using through-silicon-via (TSV) technology has been around for many years. However, this technology has only recently been introduced into high volume manufacturing. This paper gives a comprehensive summary of the TSV origins, applications, manufacturing process and commercialization trend. Benefits and drawbacks for using each approach to manufacture TSVs are discussed including via-first, via-middle, and the via-last process. Several applications for TSVs are discussed including memory arrays and image sensors.**

***Index Terms*—through silicon via (TSV), 3D interconnection, 3D packaging, wafer level packaging, stacking**

I. INTRODUCTION

Facing the challenges of physical limits, systems integration is clearly a driving force for innovation in packaging and the need for miniaturization has led to new architectures which combine disparate technologies. In particular, when several dies have to be connected in a small package, stacking would appear to be the best solution. Thus, 3D packaging technology has increasingly become the focus of the microelectronics industry.

Advanced 3D packaging techniques such as wafer bumping, 3D interconnect, and chip scale packaging allow different components of an IC to be stacked on each other and directly connected, rather than side by side on a printed circuit board. These new packaging methods enable the production of ICs with high interconnections density and high data throughput in conjunction with good signal integrity, and reliability while maintaining a low cost.

Today, several different approaches have been developed in order to perform 3D packaging. Those include technologies such as SiP (System in Package), SoC (System on Chip), SoP (System On Package) [1], or SoW (System On Wafer) [2].

One of the key technologies for 3D integration and wafer level packaging is through silicon via (TSV). It is a very promising technology,especially for the point of view of size reduction, performance enhancement and cost reduction.

In electronic engineering, a through-silicon via (TSV) or through-chip via is a vertical electrical connection (via) that passes completely through a silicon wafer or die [3]. It is inspired by the design concept from the printed circuit board (PCB), which drill small holes in the chip by etching or lasering, and then fill the holes with conducting material(such as copper, poly-crystalline silicon, tungsten, etc) in the middle and metal from the bottom. Figure 1 shows a schematic cross-section of examples of 3D integration with TSVs [4].

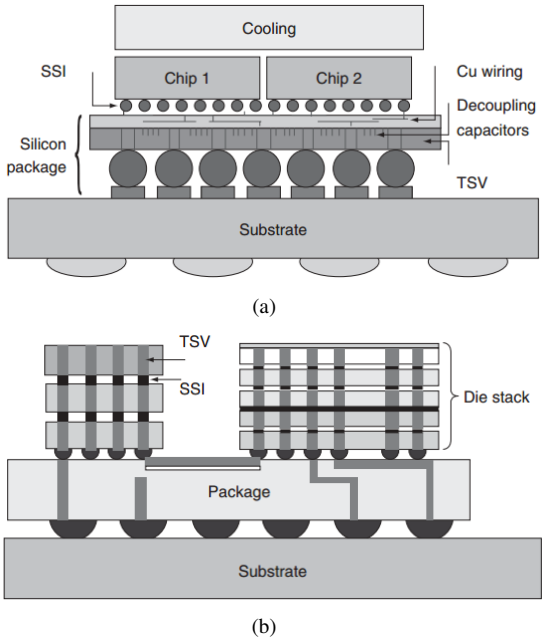

Fig. 1. Schematic cross-section for (a) 3D silicon package with through-silicon vias (TSVs) interconnecting two dies and (b) multiple stacked die using TSVs and siliconsilicon interconnect (SSI) on a base package [25]

As an alternative to wire bond and flip chips, the primary benefit that comes from the use of TSVs is reduced interconnect length with short vertical connections through thinned silicon die. The TSV enables reduced latency, lower capacitance, lower inductance and permit higher speed communications, higher numbers of interconnections and lower power level communication links between circuits. Compared to alternatives such as package-on-package, the interconnect and device density is substantially higher, and the length of the connections becomes shorter, effectively improving the integration and efficiency of the system at a lower cost. The thinned die and stacked die also permit miniaturization of integrated multi-chip systems. The smaller device size together with the power savings is expected to enable new products for mobile, the Internet of Things (IoT), and Bio-Medical applications.

II. ORIGINS OF THROUGH SILICON VIA

The origins of the TSV go back to 1958, when William Shockley filed a patent to describe deep pits to connect two

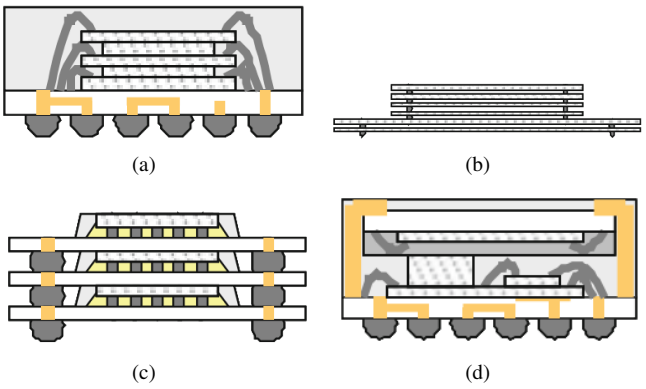

Fig. 2. 3-D IC stacking options; (a) stacked-die with wirebond; (b) stacked-die with TSV; (c) package-on-package stacking (PoP); and (d) package-in-package stacking (PiP) [9]

wafers together [5]. However, many in industry credit Merlin Smith and Emanuel Stern as the inventors of the TSV with their patent filling in 1964 [6]. As smaller sizes shrink below the 28 nm node, we are increasingly reaching physics based limitations of silicon based scaling and the cost benefit of fabricating smaller devices is disappearing [7]. By using 3D die stacking, high density or high performance devices can be used in a subset of the components, where the economics of lithographic scaling are viable. While some in industry believe transistor scaling will continue; almost all concede that each new technology node is getting more difficult and more expensive to bring to volume manufacturing [8].

III. 3D Integration Options

There are many different types of 3D packages [9]. As shown in Figure 2, these can be grouped into four types; (a) stacked-die with wire bond; (b) stacked-die with TSV; (c) package-on-package (PoP) stacking, and (d) package-in-package (PiP) stacking.

Some advantages of die stacking are as follows; (1) thin die and package profiles can be achieved by using wafer thinning; (2) a high interconnect density can be obtained, resulting in high bandwidth with lower power; (3) the packaging cost can be reduced. Possible disadvantages of die stacking are as follows: (1) the design is more complex because there more options for wire layout; (2) there is added cost of TSV and wafer thinning; (3) there is added cost for assembly and testing of known good die (to ensure high yield), and (4) more difficult power delivery, distribution and cooling of die in the 3D stack. Die stacking technology is often used for memory [10], with memory products of up to nine die currently in manufacturing [11].

Some advantages of package stacking are (1) flexibility in die selection and (2) devices can be tested at package level (providing high yield for assembly). Disadvantages of package stacking are a higher package profile and additional packaging cost. Stacked packages are commonly used for assembly of different types of dies, such as memory with logic or flash with SRAM.

TABLE I
COMPARISON OF SYSTEM-ON-CHIP (SOC), SYSTEM-IN-PACKAGE (SIP) AND 3D IC TECHNOLOGIES [13]

Performance (speed, frequency, power)	Medium	Worst	Best
Signal process packing density	Medium	Worst	Best
Manufacturing cost in high quantities	Medium	Worst	Best
Heterogeneous integration	Worst	Best	Medium
Manufacturing cost in low/medium quantities	Best	Medium	Worst
Manufacturing ready	Medium	Best	Worst

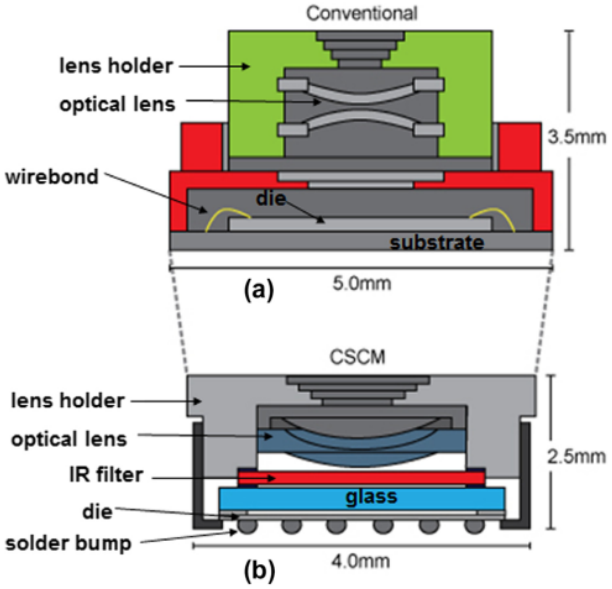

Fig. 3. Comparison of camera module size for (a) image sensor with wirebonds and (b) image sensor with TSVs [14]

As shown in Table I, there are many different die and packaging options at the system level [12]. The system designer must decide which approach is best for a given product. For example, for a mobile device, many different functions are required (digital logic, memory, analog/mixed signal) with a small form factor. Hence, there has been a trend toward 3D SiP for mobile devices, which allows integration of heterogeneous devices with a relatively small form factor. 3D IC could provide further improvements in form factor and performance, but the cost is currently high and manufacturing is not mature.

IV. Applications for TSV wafers

There are many applications for TSVs. These applications can be broadly classified into three types; (a) vertical connection to the back of the wafer, with no die stacking (i.e., simple-backside-connection); (b) 2.5D integration, where dies are attached to a Si interposer, with TSVs in the interposer; and (c) 3D integration, where dies are stacked and TSVs are in active dies.

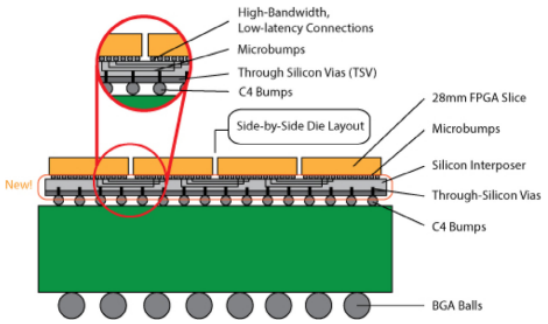

Fig. 4. FPGA dies are bonded to a silicon interposer, and appear to the designer as a single, high capacity FPGA [17]

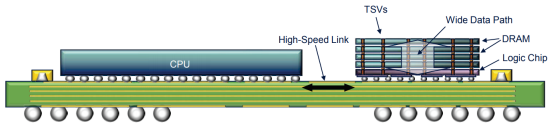

Fig. 5. Wide I/O DRAM provides a high bandwidth connection between the memory and the microprocessor [22]

A. TSVs as simple backside connections

The simple-backside-connection structure is the easiest to implement and is the first use of TSVs in volume production. Two examples of products are CMOS image sensors and SiGe power amplifiers. There are a number of advantages to using TSVs for CMOS image sensors. One advantage is that the size of the camera module can be reduced, by using TSVs instead of wirebonds [14], [15]. Another advantage is that wafer level packaging (WLP) of the image sensors is simplified [16].

B. Silicon interposer with TSVs

The 2.5D silicon interposer requires a finer TSV pitch compared to a simple-backside-connection. One of the first products to use silicon interposers are field programmable gate array (FPGA) devices (Figure 4) [17]–[19]. Building FPGA devices with large die sizes is challenging early in the production cycle due to defects in the wafer fabrication process. An alternative to a single large die is to attach multiple, smaller FPGA dies on a silicon interposer. The silicon interposer provides high connectivity between the die, so that the integrated structure appears to the user as a single, large FPGA die.

C. 3D stacked die with TSVs

One of the first applications for 3D stacked die with TSV structures are for memory stacks. The initial products using 3D stacked die with TSV are wide I/O DRAM devices (Figure 5), which provide high bandwidth and improved power efficiency [20]–[24]. (Note that I/O refers to the Input/ Output interface between the memory and the processor.) The product requirements are small size, low power, and high bandwidth between the memory and the processor.

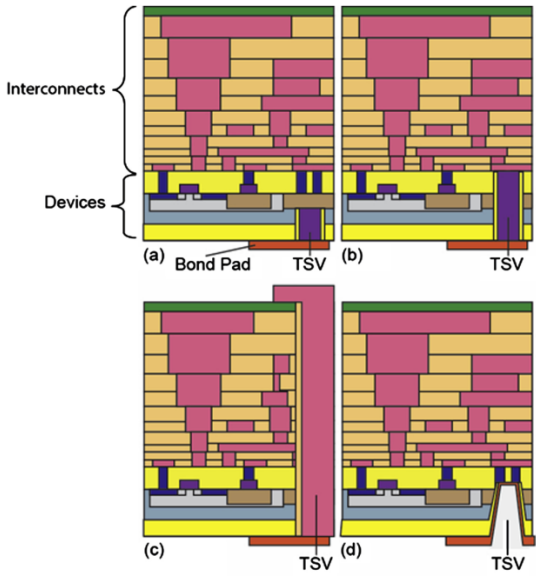

Fig. 6. Schematic of (a) frontside via-first, (b) frontside via-middle, (c) frontside via-last, and (d) backside via-last structures [28]

V. Manufacturing Processes

Based on the specific manufacturing process, there exist three different kinds of TSVs as shown in Figure 6 [25], [26]. Via-first TSVs are fabricated before the individual devices (transistors, capacitors, resistors, etc.) are patterned (front end of line, FEOL). Via-middle TSVs are fabricated after the individual devices are patterned but before the metal layers (back-end-of-line, BEOL). Via-last TSVs are fabricated after (or during) the BEOL process. Via-middle TSVs are currently a popular option for advanced 3D ICs as well as for interposer stacks [26], [27].

VI. Connections with 3D Packaging and 3D Integrated Circuits

TSV technology has significant applications in advancing specific designing and manufacturing technics such as 3D packaging and 3D integrated circuits (ICs).

A. 3D packaging

A 3D package (System in Package, Chip Stack MCM, etc.) contains two or more chips (integrated circuits) stacked vertically so that they occupy less space and/or have greater connectivity. An alternate type of 3D package can be found in IBM's Silicon Carrier Packaging Technology, where ICs are not stacked but a carrier substrate containing TSVs is used to connect multiple ICs together in a package. In most 3D packages, the stacked chips are wired together along their edges; this edge wiring slightly increases the length and width of the package and usually requires an extra interpose layer between the chips. In some new 3D packages, TSVs replace edge wiring by creating vertical connections through the body of the chips. The resulting package has no added length or width. Because no interposer is required, a TSV 3D package

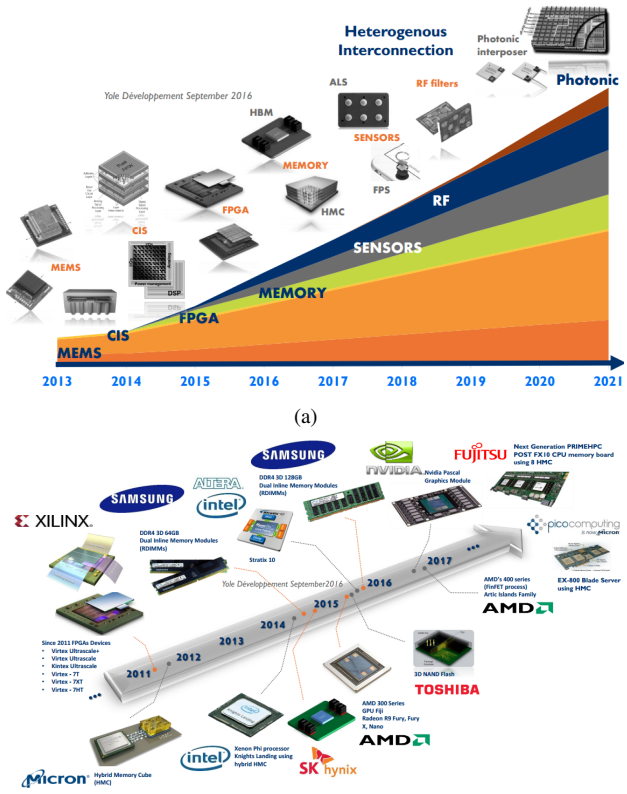

Fig. 7. (a) Summary and forecast of the Wafer Market (2013-2021) for TSV applications and (b) 3D TSV Products [31]

can also be flatter than an edge-wired 3D package. This TSV technique is sometimes also referred to as TSS (Through-Silicon Stacking or Thru-Silicon Stacking).

B. 3D integrated circuits

A 3D integrated circuit (3D IC) is a single integrated circuit built by stacking silicon wafers and/or dies and interconnecting them vertically so that they behave as a single device. By using TSV technology, 3D ICs can pack a great deal of functionality into a small footprint. The different devices in the stack may be heterogeneous, e.g. combining CMOS logic, DRAM and III-V materials into a single IC. In addition, critical electrical paths through the device can be drastically shortened, leading to faster operation. The Wide I/O 3D DRAM memory standard (JEDEC JESD229) includes TSV in the design [32].

VII. COMMERCIALIZATION TREND

So far, the business behavior of chip manufacturers using TSV technology is limited, only a few CMOS image sensors (CIS), Memory and so on.

CMOS image sensors (CIS) were among the first applications to adopt TSV(s) in volume manufacturing and keep being the biggest application for TSV technologies in the nearest years [29]. In initial CIS applications, TSVs were formed on the backside of the image sensor wafer to form interconnects, eliminate wire bonds, and allow for reduced form factor and higher-density interconnects. Chip stacking came about only with the advent of backside illuminated (BSI) CIS, and involved reversing the order of the lens, circuitry, and photodiode from traditional front-side illumination so that the light coming through the lens first hits the photodiode and then the circuitry. This was accomplished by flipping the photodiode wafer, thinning the backside, and then bonding it on top of the readout layer using a direct oxide bond, with TSVs as interconnects around the perimeter [30].

TSV in Memory is going mainstream for high end applications. In April 2006, Samsung said it had successfully applied TSV technology in wafer level process stack package (WSP) and renamed it NAND Flash stack technology. In this technology, eight 2Gb NAND Flash chips were stacked with 0.56mm laser drilling TSV processes. In April 2007, Samsung also announced its application of WSP technology in DRAM products, which stacked four 512Mb DRAM chips.

As shown in Figure 7, Yole Development's 2014 update of "3DIC & 2.5D TSV Interconnect for Advanced Packaging" report shows that driven by consumer applications such as smartphones and tablets, this market is expected to continue to grow over the next several years and TSV is on the road towards heterogenous interconnection [31]. For high-end memories, 2015 was the turning point for 3D adoption. Standards have now been established, therefore the industry will be ready to enter in high-volume manufacturing. Wide I/Os and logic-on-logic followed around 2016-2017. Emerging applications, such as photonics based on interposer, are also being developed for future products. However, their market entrance is most likely not going to happen before 2019-2020.

VIII. CONCLUSION

The idea of using through-silicon-via (TSV) technology has been around for many years. However, this technology has only recently been introduced into high volume manufacturing, and only for simple applications, such as CMOS image sensors. 3D integration using die stacking is expected to begin running in high volume manufacturing in the near future. However, there are many problems to be overcome, especially in design, assembly and test. It is expected that this will be an active area for research and development for many years.

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