Development of Advanced 3D Chip Stacking Technology with Ultra-Fine Interconnection

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Abstract

The development of 3D chip stacking technology with ultra-fine pitch interconnection initiated in 1999, which is a part of "Ultra High-Density Electronic System Integration" project. The development involves the backend of wafer fabrication process, packaging and testing. The extended study revealed possibilities and advantages of 3D chip stacking structure with ultra-fine interconnection.

I. Introduction

The higher performance of electronic system operation is currently demanded. It is very important for future electronics industries to recognize that the world will soon require seamless information exchange based on equipment or technologies that have the following properties: high performance, portability, environmentally friendly, low power consumption, and low price. Electronics packaging, however, has now reached a bottleneck in terms of extracting the full performance of high-speed microprocessor operation. The national project of "Ultra High-Density Electronic System Integration" started in April 1999 aims to develop integration technologies that break through the bottleneck of performance. [1-4]

There are three technology categories in this project. One is super-high-density three-dimensional (3D) LSI chip integration technology. The two others are optoelectronics hybrid integration technology and optimum circuit design technology. These technologies will be integrated at the end of this project (Figure 1). In this paper, a summary of the latest research activities in the first category is presented.

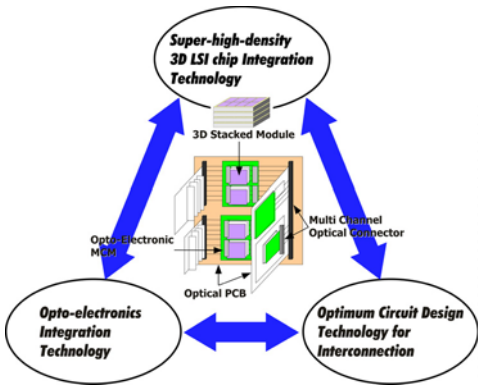


Figure 1 The image of "Ultra High Density Electronic System Integration"

3D LSI chip integration aims to develop 3D chip stacking technology as well as super-fine-pitch interconnection technology up to 20μm-pitch. The 3D chip stacking technology of LSIs has been under development for a long time, and it can be divided into package stacking and LSI wafer stacking technologies.

Package stacking technology is currently available as stacked thin small outline package (TSOP) or chip scale package (CSP) that based on conventional packaging technologies. Recently, stacking of thin packages such as paper thin package (PTP)[5] has been developed that matches better with memory devices, however, the long wiring length of the chip-to-chip interconnection may limit high-frequency performance.

Another 3D stacking technology is wafer stacking that based on wafer manufacturing technology.[6] Wafer level 3D integration can minimize the interconnect delay because of the short wiring length. These technologies are under development, but the practical use of 3D LSI using a specific wafer is planned for years in the future.

Our new approach to 3D LSI uses conventional device-ready wafers. They are processed to fit during the stacking and chips are stacked after dicing. Wiring length between chips is same as that obtained the case of wafer stacking. The technology include thorough via fabrication, wafer thinning [7], chip stacking [8-15], structure design, and inspection and testing, as shown in Figure 2. The 3D stacking and super-fine-pitch interconnection technologies are expected to be suited for building a system-in-a-package (SIP). Current SIP technology is generally based on the conventional packaging technologies such as die bonding, wirebonding and molding. Our development enables direct chip attach with super-fine-pitch interconnection that realizes high performance, low cost and short time to market system integration by packaging.

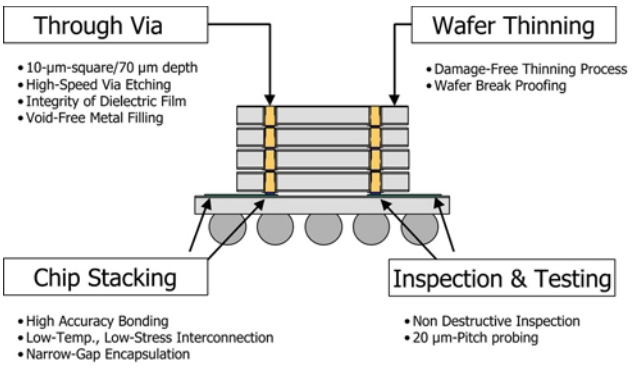


Figure 2 The technology involved in the 3D LSI chip stacking development.

In this paper, the research and development status of via fabrication, wafer thinning, testing and design issues are described, and some important points are discussed.

II. Research and Development Status

In this section, the research and development status of through via fabrication, wafer thinning, testing and design issues are summarized. Metal filling in deep via, testing of fine-pitch pads, and electrical modeling and simulation are discussed in detail.

(1) Through via fabrication

This procedure mainly contains blind via etching, dielectric coating, barrier/seed deposition and metal filling. The via was designed to be 10μm sq. and 70μm depth so that it adapt the 20μm-pitch interconnection. After wafer thinning up to 50μm, the blind vias become through vias.

Blind via etching

Reactive ion etching (RIE) was used to etch 10μm sq./70μm depth blind via. Thick SiO_2 was coated as a sacrificial layer and patterned prior to the process. The process showed good internal surface morphology in a short process time.

Dielectric coating

As for dielectric coating, plasma chemical vapor deposition (CVD)-SiO_2 showed acceptable coverage around the internal surface of the blind via and deposition rate. Figure 3 shows a SEM photograph of cross-section of a SiO_2 deposited via.

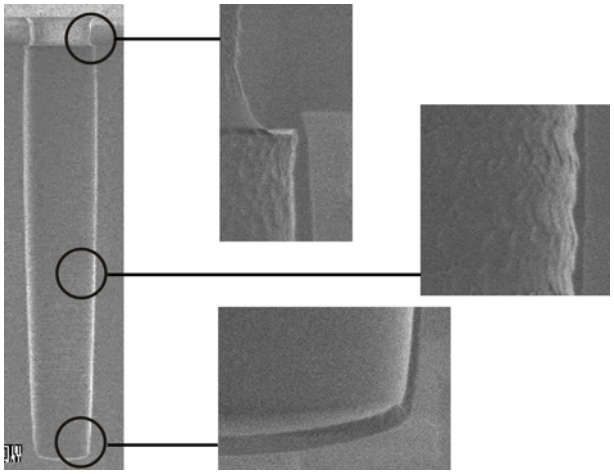


Figure 3 Cross-section of SiO_2 deposited via. The top, middle and bottom portions are covered with the film.

Barrier and seed deposition

Metal CVD-TiN/Cu was applied to barrier/seed deposition that showed good conformal coverage onto the CVD-SiO_2 around the wall of the via. Physical vapor deposition (PVD) is usually applied for seed formation in wafer fabrication process due to good physical and electrical properties, however, as for the via dimensions in this study, the overhanging shape of SiO_2 coat on the top surface obstructed uniform deposition.

Metal filling

Through via filling was attempted by electroplating of copper. The inside wall of the via was almost covered with metal. However there remained unfilled portion or void in it as shown in Figure 4.

To investigate the phenomena, electroplating was stopped before sufficient filling of the via for some chemicals and electroplating conditions, and cross-section of the vias were observed. Electroplating time was set to deposit 1μm and 3μm for the chemicals used for damascene and printed circuit board (PCB). Two electroplating conditions were applied.

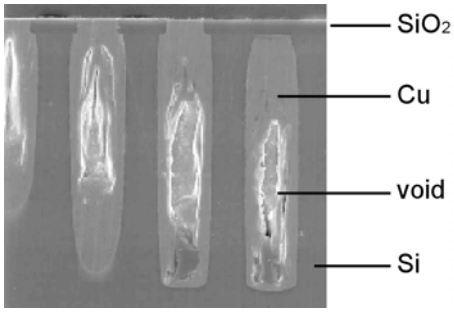
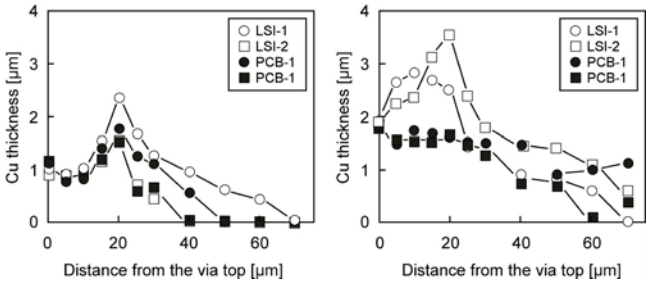


Figure 4 Cu deposited vias. Large voids are observed.

Figure 5 shows the results of deposited Cu thickness measurement at various positions of the via. In this figure, (a) is the result of 1μm deposition and (b) shows that of 3μm deposition, respectively. Both results show that the maximum thickness is obtained around 20μm depth from the via top and it gradually decreases for the bottom of the via. The chemicals did not show clear differences for 1μm deposition. For 3μm deposition chemicals for damascene showed more distinct profile than PCB chemicals. The conditions of electroplating also did not strongly affected to the results.



(a) 1μm deposition (b) 3μm deposition

Figure 5 Cu thickness profile in the via. (a) Electroplating was stopped after 1μm deposition that shows early status of deposition, (b) electroplating was stopped after 3μm deposition that show middle status of deposition.

It is important to have sufficient and uniform supply of Cu^{2+} in the via for void-free filling. Thick deposition at the middle of the via makes efficient via opening small that inhibits its sufficient supply of Cu^{2+} by either diffusion or convection. The mechanism of maximum deposition around 20μm depth is not clear, but it is assumed that the chemicals and via shape affect to it.

The damascene chemicals are usually designed for filling of small vias such as submicron opening, and PCB chemicals are used for larger vias of hundreds micrometers in size. The via size attempted for the investigation was much larger than that of LSI and much smaller than that of PCB. Further investigation of chemicals to deposit in "bottom-up" scheme is

needed. The via shape is also needed to improve. A relatively thick SiO_2 film is coated on the surface of the wafer as a cover sheet before via etching. The etching rate is significantly different between Si and SiO_2 , which helps deep via etching in Si substrate, however, Si just beneath the SiO_2 film is also etched horizontally that causes overhanging shape of SiO_2. The shape may cause unexpected flow of ion that results local deposition of Cu.

The void issue of metal filling is one of the most important one at this time, because the incomplete filling causes serious defects during the following processes. Improvement of chemicals, via shape, and electroplating condition as well is under development.

(2) Wafer thinning

The wafer with Cu plug of 70μm depth is thinned up to 50μm that makes the blind vias through vias. Back-grinding and etching are applied to the process. The wafer undergoes a back-grinding process to expose the Cu plug in the wafer back side surface so that the depth distribution of the blind vias in the wafer could be removed. We used the dry etching method for damage removal after back-grinding. The method was also expected to etch Si substrate selectively so that the copper plugs automatically projected like bumps. Research and development status, experimental results and some technical issues are discussed in the following. [7]

Back-grinding

Back-grinding of silicon wafer with embedded copper plugs is one of the key technologies in this study, because it requires simultaneous grinding of brittle silicon and ductile Cu. It may suffer from loading, surface burning and copper smearing on silicon substrate. The grit size and bond materials were used for evaluation. Table 1 shows the results.

Table 1 Grinding evaluation results

Bond	Resinoid			Vitrified
Grit No. (size [μm])	#800 (20~30)	#1200 (8~16)	#2000 (3~8)	#2000 (3~8)
Surface burning	No	Yes	Yes	No
Cu smearing	Yes	N/A	N/A	No

(a) #800, resinoid (b) #2000, vitrified

Figure 6 Cu plug ground by (a) #800 of resinoid wheel, (b) #2000 of vitrified wheel. Cu smearing on Si substrate is observed in (a).

The results showed that the vitrified bond was most suitable for grinding that no surface burning or Cu smearing was observed. Figure 6 shows the ground surface of #800 (resinoid) and #2000 (vitrified). The vitrified bond is known as hard and brittle material than the resinoid bond that contributed to decrease loading of the wheel by Cu. Surface roughness of the wafer ground by vitrified bond wheel was 0.04μm (Ra) that was almost same level as 8~16μm of resinoid wheel.

Damage removal by dry etching

The wafer was dry etched after back-grinding by a plasma-assisted etcher in which SF_6 gas was used. 5μm of the back-ground surface was etched off. The amount was chosen so that the mechanical damage could be completely removed. Stress measurement by Raman spectroscopy was carried out. The results showed that the maximum stress was observed at the ground surface. The stress decreased inside the Si substrate, and it became stable at 1.5μm or deeper. It suggests that 1.5μm or more removal of the back-ground surface by etching can reduce the stress value. TEM photographs after dry etching showed no defects on the surface.

Plug projection by dry etching

The Cu embedded wafer was dry etched after back-grinding. The amount of Si etch off was set to 5μm. Figure 7 shows the SEM photograph. Si substrate was etched and 10μm square plugs were successfully projected. SiO_2 film and barrier/seed films were remained around the sidewall of the plug. However, by-product of etching was reattached on the Cu that was identified as 28nm-thick sulfide. The residue was easily removed by cleaning agent (citric acid solution) with ultrasonic vibration. Optimal power control of ultrasonic is required, because excess power of ultrasonic caused chipping of SiO_2 film as shown in Figure 8.

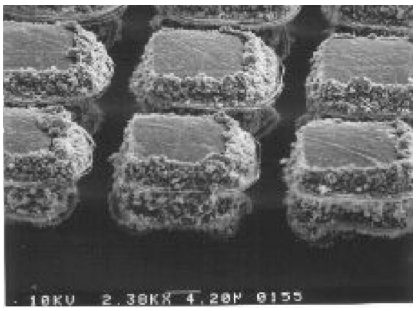


Figure 7 Cu plugs projected by dry etching. Si was selectively etched, but sulfic by-product was reattached around the sidewall.

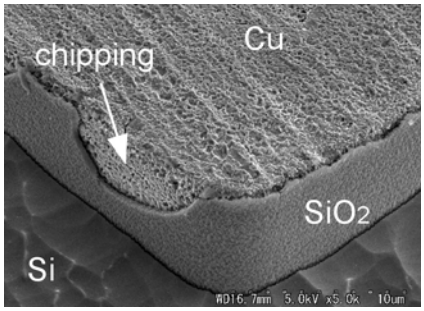
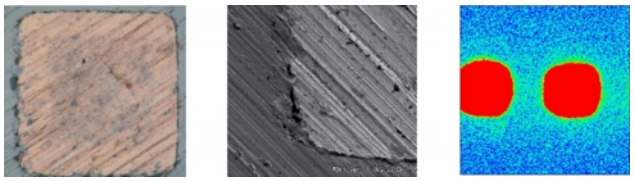


Figure 8 SiO_2 film surrounding Cu was chipped after ultrasonic cleaning of reattached sulfide.

Cu contamination on Si substrate

It is well known that Cu contamination in Si substrate degrades reliability of semiconductor devices, and the possibilities that the contamination on wafer backside also may cause reliability degradation.[16]

The process under development in this study has a possibility to contaminate wafer backside, because Cu plug and Si indirectly contact via grinding wheel. Figure 9 shows an EDX image of the plugs and Si of wafer backside after grinding which suggests Cu contamination on the Si substrate. The concentration is almost same level as a Cu-CMP finished wafer, thus the cleaning of the back-surface is necessary.



(a) Microscope (b) SEM (c) EDX image

Figure 9 Cu contamination of Si back surface. (a) Optical microscope, (b) SEM image and (c) EDX image of Cu. The rounded squares are Cu plug and Cu is also observed around the plug.

(3) Testing of fine-pitch pad

Electrical testing of the dies prior to stacking is very important so that only good dies are sent to the process to minimize yield loss of the 3D structure. However, current testing technology can be applied to only 40~50μm pitch that is mainly limited by probe fabrication. [17]

Among the available probe fabrication technologies, we chose Si whisker probe. It was most suitable for our requirement because of small and precise pin dimensions, and small contact mark. The silicon whisker pins are fabricated by single crystal growth of silicon through vapor liquid solid (VLS) process.

A 256pin probe was manufactured for feasibility check of pin design and requirement for equipment. Figure 10 shows a part of the probe. The dimension of pitch, diameter and length was designed 40μm, 12μm and 1200μm, respectively. The pin diameter is determined considering further pitch shrinkage.

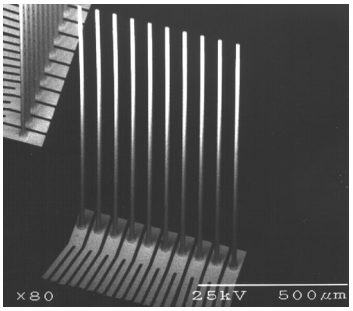


Figure 10 Si whisker probe manufactured by VLS.

The measurement results are shown in Table 2. The total deviation of bump and pin is calculated from the deviation of pin diameter, pin position, bump size (2.5μm) and bump position (1.5μm). Thus, the current total deviation is 3.7μm.

The accumulated deviation of pin, bump and equipment must be smaller than the distance of pin to bump. A high precision flip-chip bonder is evaluated in our development, which has almost same mechanism as the pressure equipment and a deviation of 2μm. If a pressure equipment that has same precision as the flip-chip bonder is developed, the total deviation of pin, bump and equipment becomes 4.2μm. It allows pin/bump design for 20μm pitch such as 16μm bump and 7.6μm pin diameter for example. The values are not realistic at this time, because a 16μm bump for 20μm-pitch bump is too large and 7.6μm pin diameter is too small for sufficient contacting force and strength. Deviation of pin diameter, pin position, bump size, bump position and equipment must be improved. In addition, pin and bump dimensions should be designed carefully so that the pin tip reliably contact to the bump.

Table 2 Pin dimensions of the 256pin probe

	Design	Average	3σ
Pin pitch	40 μm	39.6 μm	1.3 μm
Diameter	12 μm	12.1 μm	3.4 μm
Length	1200 μm	1214.9 μm	10.6 μm
Pin position	0 μm	0.2 μm	2.7 μm

(4) Design of 3D module

3D stacked modules can be regarded as a kind of MCM, however, the characteristics are different from those of conventional 2D MCM. The 3D module design is one of the most critical issues in the development so that the module can acquire optimum performance and reliability. Basic properties of thermal, mechanical and electrical are analyzed.

Thermal

The most important point in terms of thermal characteristics of the 3D module is that the power density is linearly overlapped and added on the same area. To clarify the fundamental thermal characteristics of the 3D module, thermal conduction analyses were carried out using the 3D finite volume method (FVM) as the first step of thermal management In conclusion, the design of connection bumps and the thermal conductivity of the interposer are significant factors in the thermal management of the 3D modules.[18]

Mechanical

The structure utilizes very thin chips of 50μm and small bumps for 20μm-pitch interconnection. The mechanical characteristics of thin chips and/or small bumps expected to play different behavior from that of conventional packages. Stress distribution in the 3D module and dimensional effects were analyzed by FEM and three-dimensional deformation measurement was carried out. The result showed specific stress concentration just above vertically connected bumps, which was observed as chip deformation by the measurement. Parametric study revealed that thinner chips, larger bumps and larger stack number made the stress concentration larger.

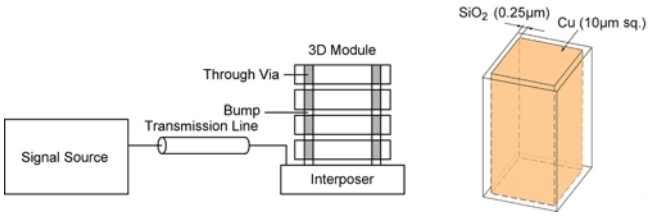
Thus, it was confirmed that 20μm-pitch interconnection with 10μm square bumps are suitable for 50μm-thick chip stacking.[19]

Electrical

One of the most expected properties of the 3D LSI chip stacking is the signal transmission capability. Two-dimensional structure, multi chip module (MCM) structure, for example, has a few centimeters of transmission line on the printed circuit board between two LSIs. The 3D LSI chip stacking structure, on the other hand, the length of the line is almost same as the die thickness.

Electrical parameters of through hole electrode were extracted and signal transmission was simulated. The through hole electrode showed 2 or 3 orders of magnitude smaller inductance value than MCM and the delay time was 2 orders of magnitude smaller.

Signal transmission properties of the 3D structure and a MCM were studied. Figure 11 shows the simulation model of the through of the 3D structure. In this model the through via was assumed as a square coaxial transmission line that embedded in silicon substrate, filled with copper and surrounded by 0.25μm thickness of SiO_2 as the insulator. Signal is supplied from the source outside of the module with 50Ω characteristic impedance through a transmission line. Figure 12 shows the circuit model. Four vias were connected so that a four-chip stacking is simulated. As for the 2D MCM, the traces were assumed as transmission lines of 50 Ω characteristic impedance.



(a) Overall model (c) Cu via

Figure 11 Simulation models of the 3D module. (a) Overall model and (b) Cu via model.

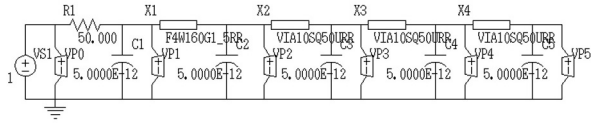
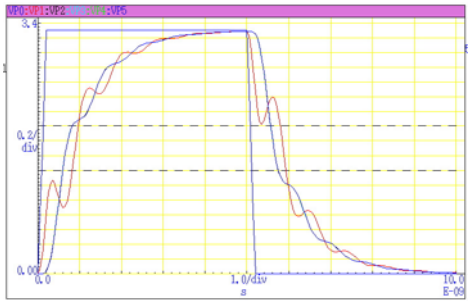
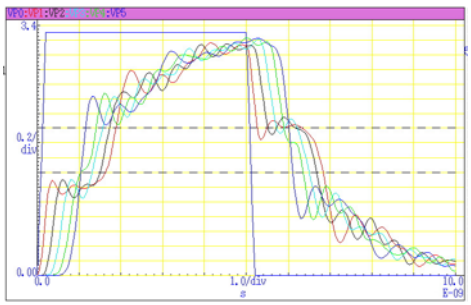


Figure 12 Circuit model of the simulation.

Figure 13 shows the calculation results of the 3D structure and the 2D MCM. The signal delay time of the 3D structure and 2D MCM was 0.8 ns and 1.1 ~ 1.7 ns, respectively. The results show that the 3D structure has better property for high-speed operation, however, the difference is not so big than expected. It is assumed that the signal delay is mostly dominated by the properties of signal source. The remarkable difference of the 3D structure from the 2D MCM is that the 3D has no signal delay among the four chips. It shows that the through via is so short that it does not act as a distribution constant circuit. Further investigation of signal source and measurement of actual sample is planned.



(a) 3D stacked module



(b) 2D MCM

Figure 13 Simulation results of signal transmission. (a) is the 3D module and (b) is a 2D MCM. The lines of VP1 to VP4 became same lines in 3D model that indicates no delay among the four chips. In 2D MCM case, the four lines can be easily distinguished.

III. Conclusions

The novel 3D stacking technology with ultra-fine interconnection has been investigated and evaluated. Although there are some issues to be solved, the results showed possibilities to accomplish the goal of this project and the advantage of the structure. Further development is emphasized on brushing up each process and process integration.

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