INVITED PAPER

System on Wafer: A New Silicon Concept in SiP

With this flexible, low-cost, high-yield packaging technique, which can be implemented by various technologies, components and chips are mounted on a silicon wafer.

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ABSTRACT | System integration is clearly a driving force for innovation in packaging. The need for miniaturization has led to new architectures that combine disparate technologies and materials. Today several different approaches have been developed. These include technologies like system in package. In this way, a new concept for heterogeneous integration is currently being developed at CEA-LETI and is called system on wafer (SoW). This concept is based on a chip to wafer approach. Every component is achieved by using wafer-level technologies, and the final system is performed by single component mounting on a silicon substrate. The main strength of this approach is to use silicon as a substrate for components and for basic support. To perform the SoW, a generic technological toolbox is needed. This includes every standard packaging technology such as flip chip, signal rerouting, and passive component integration as well as new advanced technologies such as microelectromechanical systems packaging, advanced interconnections, energy source integration, integrated cooling, or silicon through vias. In this paper, the SoW concept will be presented and the generic toolbox for SoW achievement will be described.

KEYWORDS | Micro insert; system in package; system on wafer; thin-film packaging; through silicon vias; 3-D integration

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I. INTRODUCTION

Several different approaches have been developed in order to perform three-dimensional (3-D) packaging, and one of the most advanced concerns the system in package (SiP) concept. In order to enable small device integration and to answer to the demands of heterogeneous systems packaging, CEA-LETI has developed an integration concept called system-on-wafer (SoW). SoW is a chip to wafer approach. Every component is achieved by using wafer-level technologies and the final system is performed by single component mounting on a silicon substrate. The main strength of this approach is to use silicon as a substrate for components and for basic support. To perform the SoW, a generic technological toolbox is needed. This includes every standard packaging technology such as flip-chip, signal rerouting, and passive component integration as well as new advanced technologies for 3-D integration such as microelectromechanical systems (MEMS) packaging, advanced interconnections, energy source integration, integrated cooling, or through silicon vias (TSV). TSV is a very promising technology for the replacement of wire bonding in SiP, system on package, or SoW approaches as well as chip stacking technologies [1]–[3].

In this paper, the SoW concept is presented and the generic toolbox for SoW achievement is described.

II. SYSTEM ON WAFER CONCEPT

In this approach, the base substrate is in silicon. The main advantage is to use standard microsystem technologies for the fabrication of chips and substrates and also to integrate active or passive functions directly into the silicon substrate. The main idea of SoW is to perform the majority of technological steps using wafer-level technologies and

to singulate different chips as late as possible in the process. From here, the final assembly of the system is achieved by using chip to wafer technologies on the substrate, which is also performed on silicon (Fig. 1).

The main advantages of this approach are the following.

- Silicon processes allow high-resolution lithography, so very small pitch and high-level integration can be achieved. This approach is also compatible with future trends such as reduction of pitch and of global size and introduction of nanodevices.
- There are no coefficient of thermal expansion (CTE) mismatches between chips and substrates (since both are silicon).
- The silicon base wafer can be an active substrate [complementary metal–oxide–semiconductor (CMOS) processed dies, an active cooling system, an energy source].
- Electrical and thermal performances can be improved by using silicon as a substrate instead of printed circuit board (e.g., Si permits shorter interconnects and therefore higher frequency operation).
- The cost of the packaging could be decreased by using wafer-level technologies.

III. A GENERIC TOOLBOX

The system-on-wafer approach requires the development of a generic wafer-level technology toolbox, containing different packaging processes (Fig. 2). This toolbox would comprise technologies for MEMS packaging, advanced interconnections, signal rerouting and passive component integration, chip thinning, chip to wafer positioning and bonding, cooling system integration, and energy source integration. Furthermore, 3-D connections through silicon are also required in order to connect the different faces of the components with the substrate and also to connect the substrate with the board. These developments are presented below (Fig. 2).

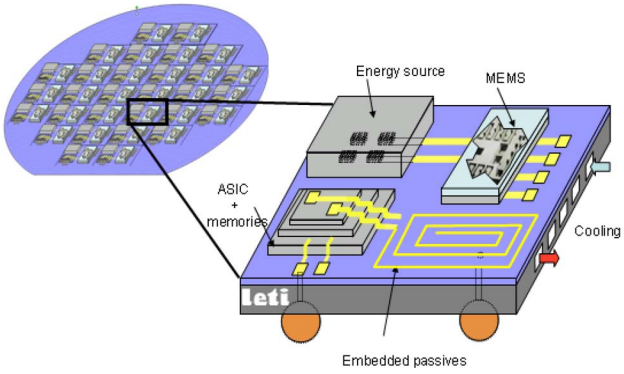

Fig. 1. *System on wafer concept.*

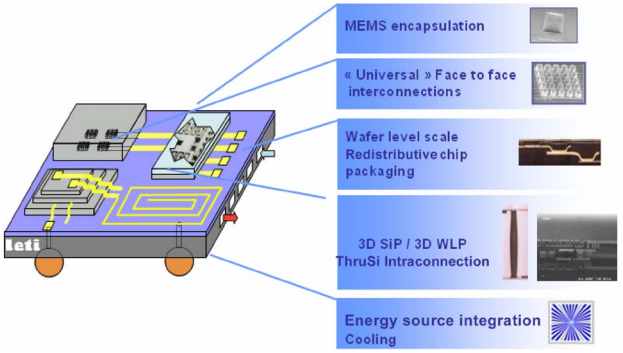

Fig. 2. *A generic toolbox.*

Initially, each process was developed individually. Then, we present examples of applications of these various technological bricks in order to integrate them in industrial processes.

IV. WAFER-LEVEL THIN-FILM ENCAPSULATION FOR MEMS

A. Technology

MEMS are now used in a wide range of applications. However, packaging represents a large part of the manufacturing cost for these devices. As MEMS contain fragile movable parts or the need to operate in a vacuum atmosphere, standard packaging technologies developed for integrated circuits cannot be directly used for MEMS devices. For example, die sawing or injection molding process of plastic package will cause damage to movable parts if they are not protected. To avoid these problems, new technologies were developed to encapsulate the devices at the wafer level (before die separation) [4]. These "prepackaging" technologies aim to allow the use of standard low-cost packaging even for very specific devices. We developed a thin-film packaging technology (Fig. 3). Closed cavities are formed above the devices with surface-micromachining techniques: the cavity is formed with a sacrificial layer recovered by a cap. The cap is then perforated to remove the sacrificial layer. Finally, a film is deposited on the cap to seal the cap holes.

As thin-film packaging uses standard IC technologies and consumes less die area, it should offer a lower system cost than wafer bonding packaging. Moreover, it does not

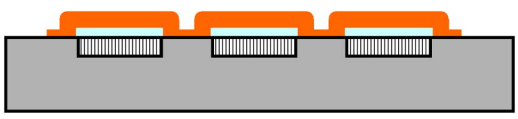

Fig. 3. *Thin-film package.*

require wafer to wafer alignment and backside process technologies, which are not common in IC fabs.

The main interest of the technology developed at LETI is the use of a polymer sacrificial layer, which is removed by dry etching. Moreover, as it is a low-temperature process (< 450 °C), it is compatible with IC and radio-frequency (RF) MEMS, such as RF switches. In the following section, an example of application of thin-film encapsulation is described.

B. Encapsulation of RF Switch

RF switches with electrostatic actuation were fabricated and packaged by thin-film technology. Fig. 4 shows a schematic diagram, describing in detail the steps needed to realize the encapsulation of an RF switch. The sacrificial layer used to form the beam of the switch is not etched at the end of the switch process, and the sacrificial layer of the packaging process is directly deposited and patterned above the device. Then, the cap layer is deposited and holes are etched to allow the removing of the sacrificial layers.

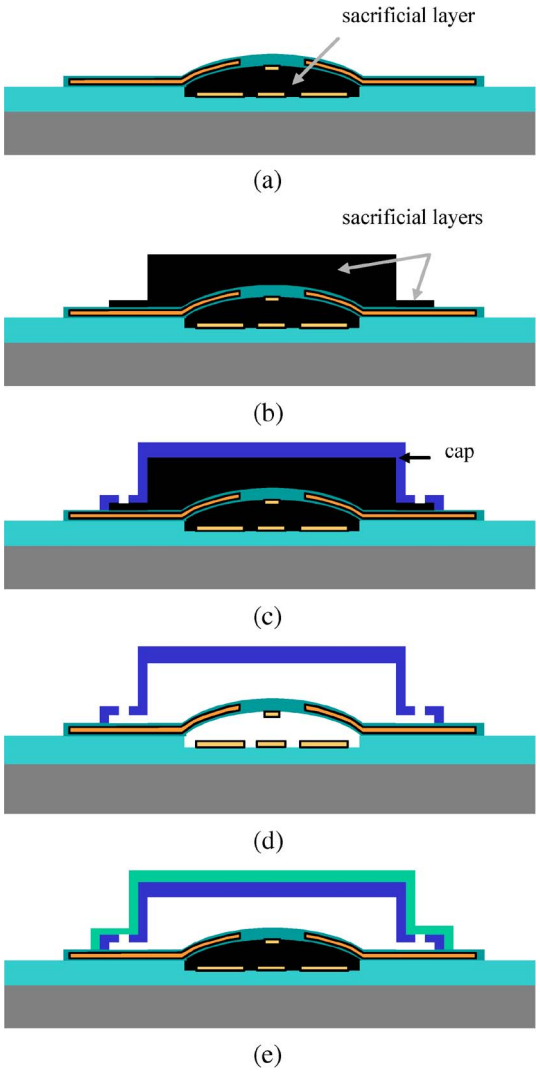

Fig. 4. *Schematic view of a package switch. (a) Switch before release, (b) packaging sacrificial layers deposit and patterning, (c) cap deposit and hole opening, (d) sacrificial layer etching, and (e) hole sealing.*

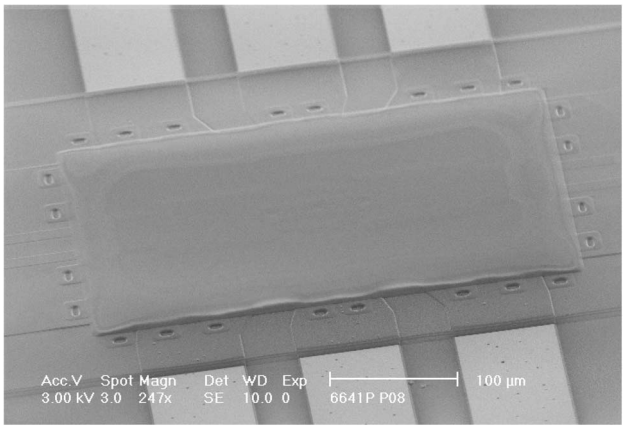

Fig. 5. *SEM view of a packaged switch.*

In this case, the sacrificial layers (for the package and for the switch) are etched at the same time. Then, the holes are sealed by a silicon nitride deposition and the contact pads are opened. To test the hermeticity of the thin-film packaging technology, resonators were fabricated and encapsulated with this technique. To measure the pressure inside the cavities, we use the dependency of the Q factor of such structures upon pressure. It was shown that with a plasma-enhanced chemical vapor deposition silicon nitride sealing the cap was hermetic [5]. A scanning electron microscope (SEM) view of a packaged switch is shown in Fig. 5. The cap is 400 × 240 μm. The topology induced by the package is extremely low, as the total height of the package is less than 10 μm. Electrical characterization showed that switches dc performance was not altered by the encapsulation process.

Once protected by thin-film packaging technology, MEMS can be further processed for integration in SoW or back-end packaging as standard components. Specific and costly packaging is no longer required.

V. MICROINSERT TECHNOLOGY FOR FACE TO FACE INTERCONNECTIONS IN SoW

A. Technology

In many complex mixed technology systems currently under development, the cost of integration and the compromises in performance that can result from the integration process can become prohibitive. Therefore, the establishment of a technology that enables the system-level integration of devices from different technological families at the package level can become very attractive.

Particularly, since each component can be built in its optimum technology flow and interconnections between the components can be very short, very high performance can be achieved. Many different approaches have been reported [6]–[9], which describe different methods for attaching two such components face to face.

Independently of the application, the practical requirements for the interconnection system between the two dies include:

- low-resistivity electrical interconnection;
- mechanical attachment;
- mechanical stability;
- thermal management;
- rerouting of interconnections to facilitate front surface attachment;
- CTE compensation.

In conventional flip-chip approaches, where a die is attached to a printed circuit board, interposer, or thin-film substrate, the interconnection between the die and the board is supplemented by the use of an underfill material. This fills the void between the two surfaces and when cured matches, as closely as possible the thermal expansion coefficients of the two materials (Si and substrate material). It also provides a degree of strength and mechanical stability to the system, In the microinsert approach, an appropriate glue layer that firmly joins the two chips together is required to take the role of the underfill. The approach used to form the interconnections between the two component parts of the system in this work is to adopt an approach entitled microinsert technology [2]. In this approach, small spikes of Ni are formed at the point of interconnection between the two circuits. These could occur at either a bond pad or at the termination of a rerouted interconnection. Microinserts are formed at these points by using a combination of photolithography and electrolytic plating, as shown in the sequence of diagrams in Fig. 6. The approach shown here is extremely flexible because it allows individual optimization of microinsert pitch, density, and size as a function of the masks used.

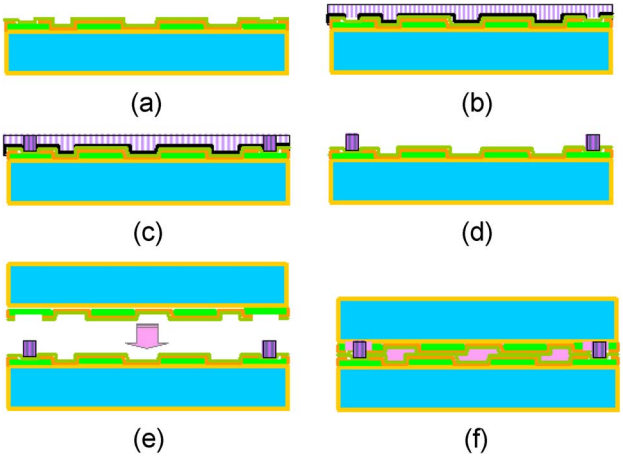

Fig. 6. *Process flow for the microinsert technology.*

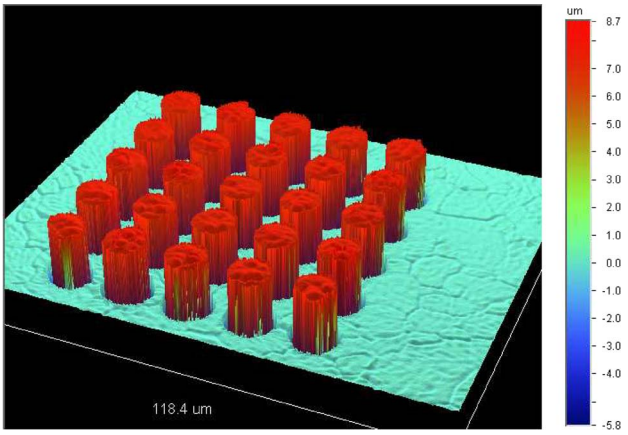

Fig. 7. *White light interferometry image of microinserts formed on a metal pad on wafer (Veeco equipment).*

Microinserts are an attractive methodology for interconnecting two die face to face for chip on wafer examples of heterogeneous integration. They permit small pads (pads as small as 20 μm^2 have been created so far, and 2 μm diameter microinsert has been achieved) and much better pitch possibilities than the more conventional flip-chip or ball bumping approaches (Fig. 7). They also form a very robust connection, which facilitates thinning of the combined system after attachment to suit the packaging scenario to be adopted. (In the case of smart card, the entire system needs to be thinned to a value of less than 180 μm to enable the system to fit inside the final packaged module.)

In addition, there is no additional processing required on the top die, and rerouting that interconnects the system at appropriate points can be incorporated into the process. High aspect ratio bumps that can alleviate CTE issues can simply be created as a function of the time required for the plating technology and resist thickness. However, in all instances, the choice of polymer/glue layer is crucial (Fig. 8).

B. Characterization

Fig. 9 shows the wafer-level part of the test chip used to evaluate the microinsert technology (a second complementary die is attached face down to complete the daisy chain and add the other plates of the capacitors) This test

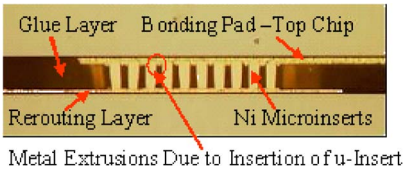

Fig. 8. *Cross-section through a single 50 μm contact point.*

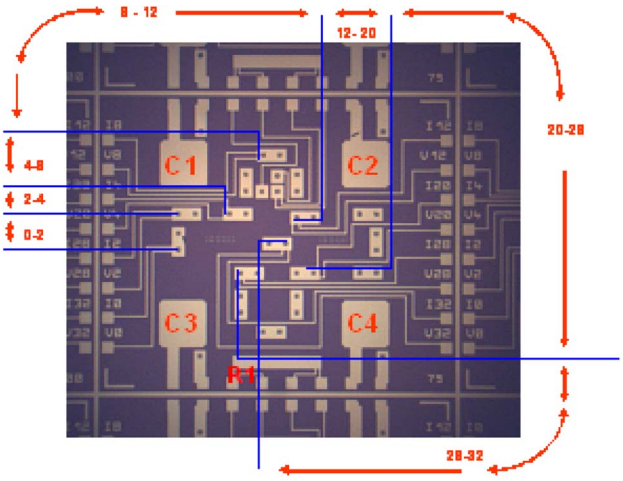

Fig. 9. ***Daisy chain test structure.***

structure has been used to evaluate the contact resistance of individual contact points in the chain.

It is a 32 contact daisy chain that permits Kelvin completed measurements from two to 32 contact points along the chain. This enables the identification of where open circuits have arisen and facilitates inspection of the regions where failures have occurred. In this structure tap points, metal lengths, and typical values of resistance measured between connections for a 50 μm^2 contact region are shown in Table 1.

Microinsert technology is a very interesting approach to use as the interconnection medium between two separate systems connected together face to face. It is reliable and has few of the constraints of conventional flip-chip mounting including the fact that no underbump metallization (UBM) is required and only one die needs to be treated at wafer level using a commonly accepted electrolytic plating process to provide the bumps and the rerouting on the chip surface.

However, the technology is planarity sensitive, and the mounting process needs to be optimized to obtain repeatable results. Electrical characterization, when benchmarked with technologies that permit the user to view through the overlying chip to the interface, can provide a great deal of information with regard to the link between system failures and process conditions.

Table 1 Resistance Measurements

Contact Point	Length (mm)	No Contacts	Mean Measured Resistance (Ω)
0-32	15069	32	1.30
0-2	677	2	0.06
2-4	1097	2	0.07
4-8	1759	4	0.15
8-12	2153	4	0.21
12-20	3310	8	0.29
20-28	4058	8	0.38
28-32	2015	4	0.16

VI. 3-D INTEGRATION

There is a strong demand for miniaturization and higher performance of microelectronic devices. Three-dimensional technology is one of the solutions with the best potential to extend Moore's law or to address innovative "more than Moore" devices. Lower cost, higher performance, smaller form factor, and heterogeneous integration are the most promising benefits. For 3-D IC Si processing, the major challenges are the patterning and the fill of the through wafer via, wafer thinning, die/wafer bonding, and its alignment.

A. Wafer to Wafer Bonding [10]

According to the ITRS 2005 edition, for the 22 nm node, planar bulk CMOS will face so many difficulties that ultrathin body devices and especially multiple gate devices with undoped channel are required to allow MOS field-effect transistors to scale down to the 10 nm range and below. The main challenges for these ultrathin body devices will be the control of the body thickness and its variability, and the optimization of the access regions in order to benefit from the intrinsic device performance. Planar technologies such as planar double gate appear to be highly scalable regarding the channel thickness control and its variability.

Thanks to molecular bonding, we have demonstrated high-performance double gate transistors with gate length as low as 10 nm and with Ion = 1130 $\mu m/\mu A$ (at Vdd = 1.2 V) using a non-self-aligned process (each gate was described thanks to a different lithography) (Fig. 10).

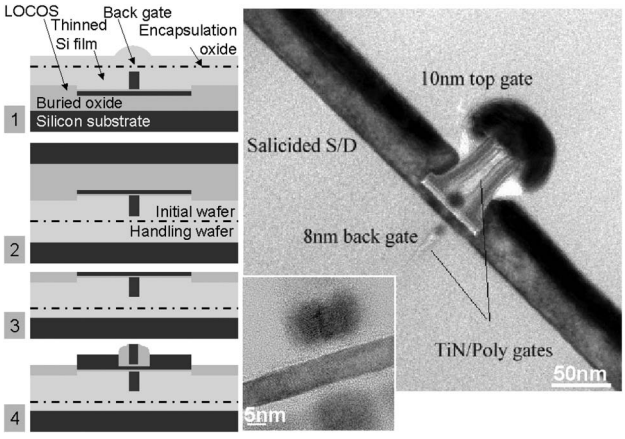

Fig. 10. ***(a) Process description to raised source and drain in a non-self-aligned process. (b) Transmission electron microscopy cross-section of a 10 nm gate length planar double metal gate transistor with a 10 nm channel thickness.***

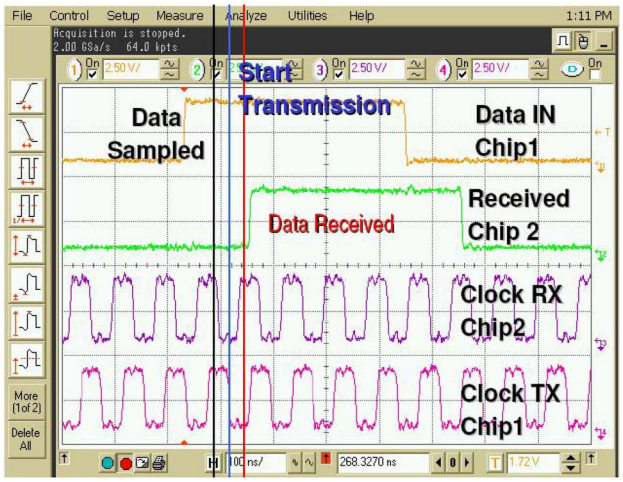

Fig. 11. *Data obtained by 3-D integrated chip with capacitive interconnections set up with a 1.2 V power supply.*

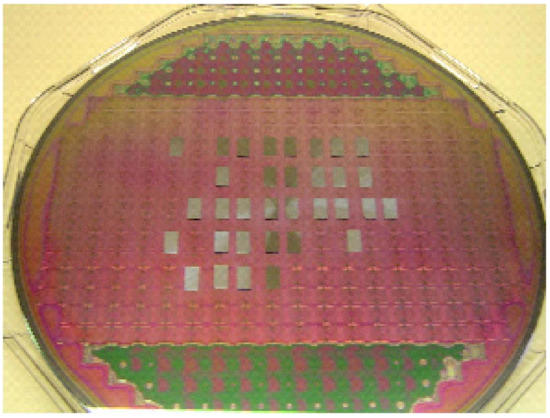

Fig. 13. *Source and PD InP die bonded on an optical layer on a CMOS substrate.*

B. Wafer to Wafer 3-D Technology [11]–[13]

New interconnection techniques between CMOS devices are required to improve communication speed, bandwidth, and dissipated power. Two concepts using 3-D integration are possible: wireless capacitive coupling was realized with capacitors generated by direct wafer bonding of two processed CMOS silicon wafers with accurate alignment; I/O is achieved after bonding by via opening from the upper thinned silicon and through all the active and passive layers of the CMOS (Fig. 11).

This can be done by thinning CMOS wafers on a handler before bonding; the vertical interconnects are then done through the whole stack. Alignment less than 1.5 μm has been achieved Fig. 12.

Electrical measurements indicate the continuity of the inter strata via with good resistance (0.25 Ω for 1 μm via diameter). Thermal simulation shows the thermal resistance due to local 3-D effects can be higher than one-dimensional thermal resistance. However, the maximum temperature in 3-D ICs remains relatively low if we consider a perfect packaging.

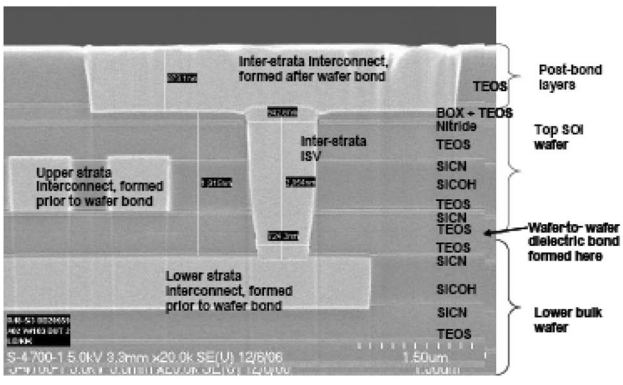

Fig. 12. *Cross-section SEM observation of the direct bonding of two processed wafers. The SOI upper wafer have been thinned down to the buried oxide, and then the via was processed in order to connect the two layers. [12].*

C. Chip on Wafer Bonding 3-D Technology [14], [15]

To successfully integrate heterogeneous microelectronic systems over CMOS or to develop efficient optical links with the miniaturization requirements, new bonding techniques are needed. The specificities of these bonding techniques will be postprocess steps feasibility, low-temperature process, topology adaptation, precise alignment, stress management, etc. We have demonstrated an optical link realization with III–V source and detector bonded on a stack of CMOS and a waveguide layer. The process was realized on a 200 mm Si line (Fig. 13).

D. 3-D Cointegration SoI/GeOI [16]

We propose a sequential and front-end 3-D stacking, i.e., each layer is processed sequentially starting from the bottom-most layer. As shown in Fig. 14, the process scheme

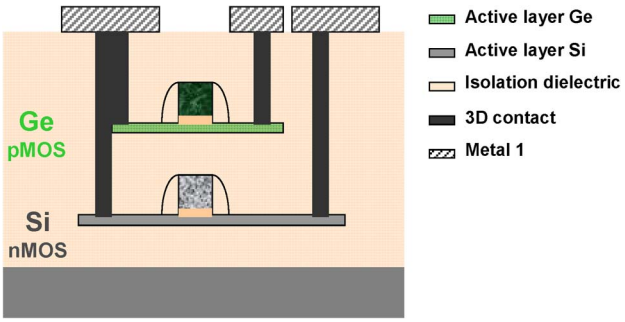

Fig. 14. *Integration scheme of the structure proposed by LETI.*

can be described as follows. On an SoI substrate, a single type of transistor (e.g., nMOS) is realized using a classical high-temperature process. After interdielectric deposition, another semiconductor film is reported using report techniques well controlled in LETI. On this second active layer, a second transistor layer is processed using adapted process for sequential integration (pMOS in Ge with a temperature budget <600 °C or Si transistors with local annealing for dopant activation in silicon) maintaining good performances in the underlying IC layers. A gain in integration density and in interconnect delay issues (as interconnections length is reduced) is expected.

E. Self-Assembly

Alignment is one of the challenges for 3-D in order to increase the throughput for die to wafer bonding. We have developed an original self-assembly method, using surface preparation methods, which are inherited from wafer bonding to create hydrophobic and hydrophilic binding sites. The alignment is obtained on the hydrophilic zones by capillarity forces. The bonding strength is high enough so that the assembly can handle postprocessing, such as thinning down or trough via etching for interconnects [17].

VII. SILICON THROUGH VIAS

There are, at least, four main benefits that accrue from using silicon through vias instead of wire bonds:

- size reduction of the system (Fig. 15): the surface required for connections can be decreased by a minimum of 30% due to the use of TSV; the cost of the system is also obviously decreased;
- complexity increasing;
- performance improvements;
- vias manufacturing: TSV are performed by using classical collective technologies from microelectronic and microsystems wafer-level packaging technologies.

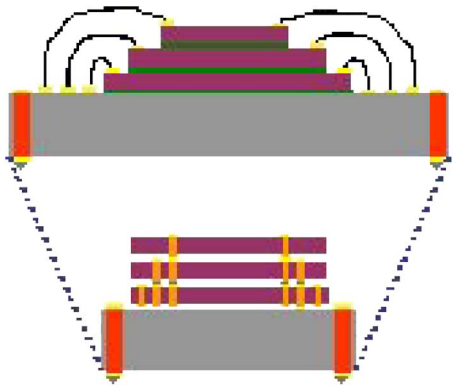

Fig. 15. *Size reduction of the system.*

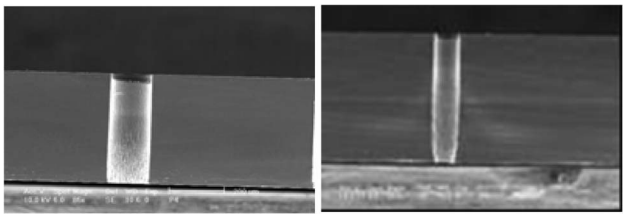

Fig. 16. *150 and 80 μm vias; 500 μm thickness.*

A. Technologies of TSV

The TSV have been performed by using microtechnologies. In LETI, a "technological toolbox" has been developed in order to meet our customer requirements:

- bonding and Si thinning;
- double side lithography;
- dry film technologies;
- deep etching (DRIE);
- electrical insulation by using deposited SiO2 or polymers;
- contact technologies including polysilicon deposit, metallic seed layer deposition, and metal electron capture detector (ECD);
- UBM technologies and bumping.

B. Technological Results

1) Bonding and Thinning: Different technologies have been developed in LETI for bonding. For permanent bonding, we currently use polymer bonding (full layer or patterned), anodic bonding, eutectic bonding (AuSn and AuSi) and classical silicon direct bonding. Developments for temporary bonding are also in progress. For wafer thinning, we developed Si grinding and stress releasing based on chemically mechanically polished process.

2) DRIE: Si etching technologies have been developed for thick wafers (300–500 μm thick; Fig. 16) and also for thin wafers after bonding on a carrier (40–100 μm; Fig. 17). The aspect ratio is between one and 30.

3) Insulation: For TSV insulation, we developed processes based on SiO_2 insulation at different temperatures

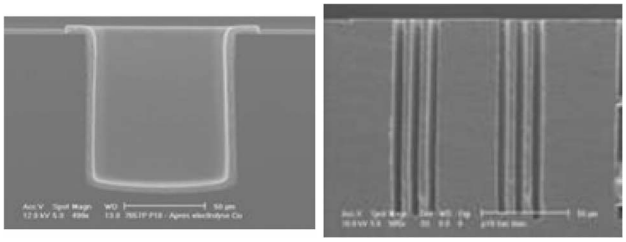

Fig. 17. *150 and 70 μm vias; 70 μm thickness.*

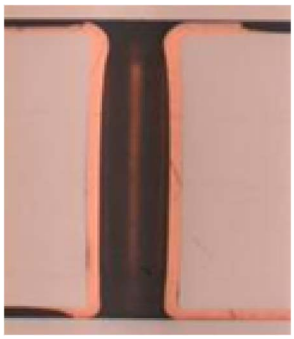

Fig. 18. ***Cu liner.***

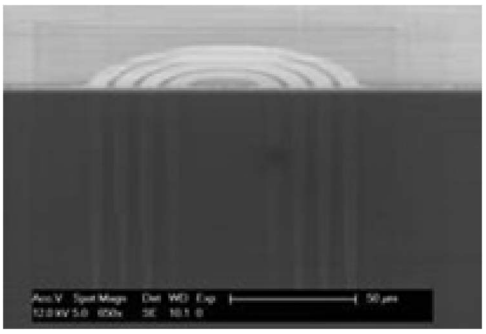

Fig. 19. ***Doped polysilicon filling.***

(150 °C to 1000 °C). One of the main issues for low-temperature insulation is the deposit conformity in the TSV, and we work with equipment suppliers to solve this problem. We also develop solutions based on polymer insulation.

4) Contact: Different solutions for contact have been developed:

- Cu liner by using ECD (Fig. 18);
- Cu filling;
- CVD tungsten liner;
- CVD tungsten filling;
- Doped polysilicon filling (Fig. 19).

We adapt the contact technology to our customer specifications (geometries, performances, cost, etc.).

5) Electrical Tests: TSV have been characterized by using Daisy chains.

a) Results for Cu Liner TSV:

- electrical continuity → 100% continuity;
- electrical insulation →> 200 MΩ;
- via resistance → <30 mΩ for the 80 μm diameter vias and <10 mΩ for the 150 μm diameter vias.

b) Results for Doped Polysilicon TSV:

- electrical continuity → 100% continuity;
- via resistance → <300 mΩ for the 100 μm vias with 5 μm trenches.

VIII. CONCLUSION

SoW is a new approach for advanced packaging based on wafer-level technologies and using silicon for both components and substrates. It is a chip to wafer approach, which is very flexible, has low cost, and exhibits high yields. This concept needs access to a technological toolbox including a lot of advanced technologies such as MEMS encapsulation, advanced interconnections, signal rerouting and passive component integration, chip thinning, chip to wafer positioning, and bonding and through silicon vias for 3-D intraconnections. In the future, energy sources and cooling systems will complete this concept to expanded SoW with SiP and 3-D roadmap. ■

REFERENCES

[1] R. Tummala and Al, "High density packaging in 2010 and beyond," in *Proc. IEEE 2002 Int. Symp. Electron. Mater. Packag.*, pp. 30–36.

[2] N. Sillon and Al, "Innovative flip chip solution for system on wafer concept," in *Proc. 3S Workshop*, Atlanta, GA, 2005.

[3] J. C. Souriau and Al, "Wafer level processing of 3D system in package for RF and data applications," in *Proc. ECTC*, Orlando, FL, 2005.

[4] K. Najafi, "Micropackaging technologies for integrated microsystems: Applications to MEMS and MOEMS," in *Proc. SPIE Micromach. Microfab. Process Technol. VII*, 2003.

[5] Gillot, N. Sillon, P. Robert, E. Dahan, X. Baillin, and E. Lagoutte, "Wafer level hermetic packaging for above-IC RF MEMS: Process and characterization," in *Proc. IMAPS Int. Workshop Microelectron.*, Long Beach, CA, Nov. 14–18, 2004.

[6] E. Laine, K. Ruhmer, E. Perfecto, H. Longworth, and D. Hawken, "C4NP as a high-volume manufacturing method for fine-pitch and lead-free flipchip solder bumping," in *Proc. Electron. System Integr. Technol. Conf.*, Dresden, Germany, 2006, pp. 518–524.

[7] A. Mathewson, J. Brun, C. Puget, R. Franiatte, N. Sillon, F. Deputot, and B. Dubois-Bonvalot, "Microstructured interconnections for high security systems," in *Proc. IEEE Electron. Syst. Integr. Conf. (ESTC)*, Dresden, Germany, 2006.

[8] P. A. Gruber, L. Beélanger, G. P. Brouillette, D. H. Danovitch, J.-L. Landreville, D. T. Naugle, V. A. Oberson, D.-Y. Shih, C. L. Tessler, and M. R. Turgeon, "Low-cost wafer bumping," *IBM J. Res. Dev.*, vol. 49, no. 4/5, pp. 622–639, Jul./Sep. 2005.

[9] R. R. Tummala, P. M. Raj, A. Aggarwal, G. Mehrotra, S. W. Koh, S. Bansal, T. T. Tiong, C. K. Ong, J. Chew, K. Vaidyanathan, and V. S. Rao, "Copper interconnections for high performance and fine pitch flip-chip digital applications and ultra-miniaturized RF module applications," in *Proc. IEEE ECTC*, 2006, pp. 102–111.

[10] M. Vinet, T. Poiroux *et al.*, "Bonded planar double metal gate NMOS transistors down to 10 nm," *IEEE Electron Device Lett.*, vol. 26, pp. 317–319, 2005.

[11] B. Charlet, L. Di Cioccio *et al.*, "Chip-to-chip interconnections based on the wireless capacitive coupling for 3D integration," in *Proc. MAM*, Grenoble, France, 2006.

[12] R. Chatterjee, M. Fayolle *et al.*, "Three dimensional chip stacking using a wafer-to-wafer integration," in *Proc. IITC 2007*.

[13] P. Leduc, F. de Crécy *et al.*, "Challenges for 3D IC integration: Bonding quality and thermal management," in *Proc. IITC 2007*.

[14] *Photonic interconnect layer on CMOS by wafer-scale integration (PICMOS)*. [Online]. Available: http://picmos.intec.ugent.be

[15] L. Di Cioccio, "New heterostructures and 3D devices obtained by the bonding and thinning technique," *Proc. 210th ECS Wafer Bonding Conf. 2006*.

[16] L. Clavelier, J. P. Joly, and O. Faynot, "Circuit intégré tridimensionnel de type CMOS et procédé de fabrication, FRA0600577.

[17] F. Grossi, L. di Cioccio *et al.*, "Self assembly of die to wafer using direct bonding methods and capillarity techniques," in *Proc. IMAPS 2006*.

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