Section IV

New Approaches

12

3D Interconnect Technology

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12.1 Introduction

Three-dimensional interconnected circuits (3DICs) offer great advantages for system applications. Examples of system advantages from silicon integration technologies can include: power reduction, performance improvements, product miniaturization, cost reduction, modular design for heterogeneous die and improved time to market. In order to take advantage of these 3D system benefits, the design and architecture circuits needs to be optimized to take advantage of emerging 3D technology. In addition, the materials, processes and assembly of stacked dies and integration of 3D modules including power delivery, test and cooling need to be able to be manufactured at cost-effective yields and meet system reliability requirements. 3D stacked dies can be integrated using traditional packaging laminate or ceramic packaging or can use emerging silicon and glass packages for higher bandwidth leveraging, higher wiring density between dies and/or stacked dies in multichip modules. Therefore, to optimize the system applications leveraging 3D interconnections, ongoing technical challenges include: (i) 3D system design and architecture, (ii) wafer fabrication with through-silicon vias (TSV), (iii) wafer finishing including wafer thinning, thin wafer handling and wafer backside processing, (iv) assembly using die-to-die, die-to-wafer or wafer-to-wafer stacking, (v) wafer test and burn-in, (vi) power delivery,

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(vii) cooling and (viii) module integration. This chapter will explore the system opportunities and technical challenges related to 3D silicon interconnections in systems. Examples of 3D test vehicles, data and results are reported for the technical challenges used in 3D design, wafer fabrication and module integration. The second part of the chapter analyses application of advanced microscopy techniques for evaluation of 3D structures.

12.2 Dimensional Interconnected Circuits (3DICs) for System Applications

John U. Knickerbocker

12.2.1 Introduction

On-chip interconnection has scaled over time from tens of circuits to billions of circuits over the last six decades [1, 2]. An example of memory density scaling over time is shown in Figure 12.1 [3]. Unlike on-chip integration, off-chip interconnect has not scaled at the same rate or level over the same period of time. Over the last two decades, die stacking using a wirebond interconnect and package-on-package (POP) technology using peripheral connections have been reported. However, wirebond die stacking, SIP, SOP and POP technology is not the focus of this chapter since aspects of these technologies have previously been reported [1, 4, 5] and prior examples typically have limited system interconnect density, bandwidth, frequency, power efficiency and performance. This chapter will focus on emerging three-dimensional (3D) integrated circuits and interconnect using 3D die stacking of thinned silicon with through-silicon vias (TSVs) and 3D advanced packaging system solutions such as silicon packaging and glass packaging, which offer 3D, short vertical wire lengths and high interconnect density for product applications. Figure 12.2 shows a schematic cross-section of examples of 3D integration with TSVs [6].

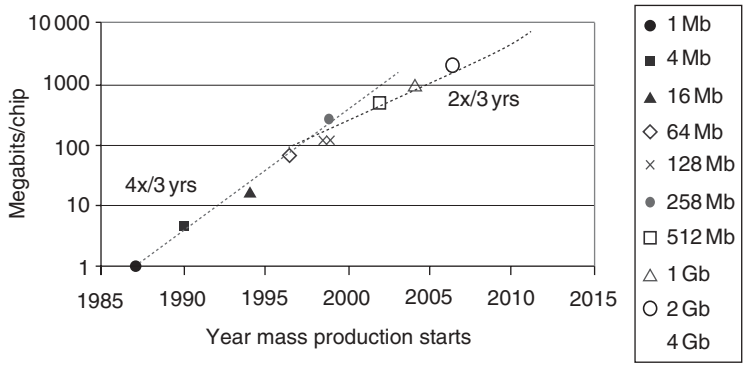


Figure 12.1 *Evolution of memory density over time* [3]

Figure 12.3 shows a relative comparison of interconnection density comparing traditional packaging such as ceramic and laminate packaging using area array interconnects, higher density silicon and glass package interconnect and highest interconnection density within a stacked die for silicon circuit integration [7].

Universities, consortia and industry have led research and early demonstrations for this emerging technology with TSV, thinned silicon and high-density interconnects. Unlike prior off-die integration technologies, these new 3D structures offer an opportunity for superior electrical characteristics and high-density vertical interconnect between circuits on silicon die or strata levels by reducing interconnection distance and electrical parasitics. This new technology offers potential advantages compared to a traditional system on a chip (SOC), a system in a package (SIP) and peripheral wirebond die stacks and package-on-package (POP) technologies. Moreover, the short distance between circuits can permit silicon die or strata to be customized using homogeneous technology and thereby to simplify wafer processing and reduce wafer costs. For example, manufacture of custom 3D microprocessor wafers, memory wafers, I/O communication wafers, digital wafers, analog

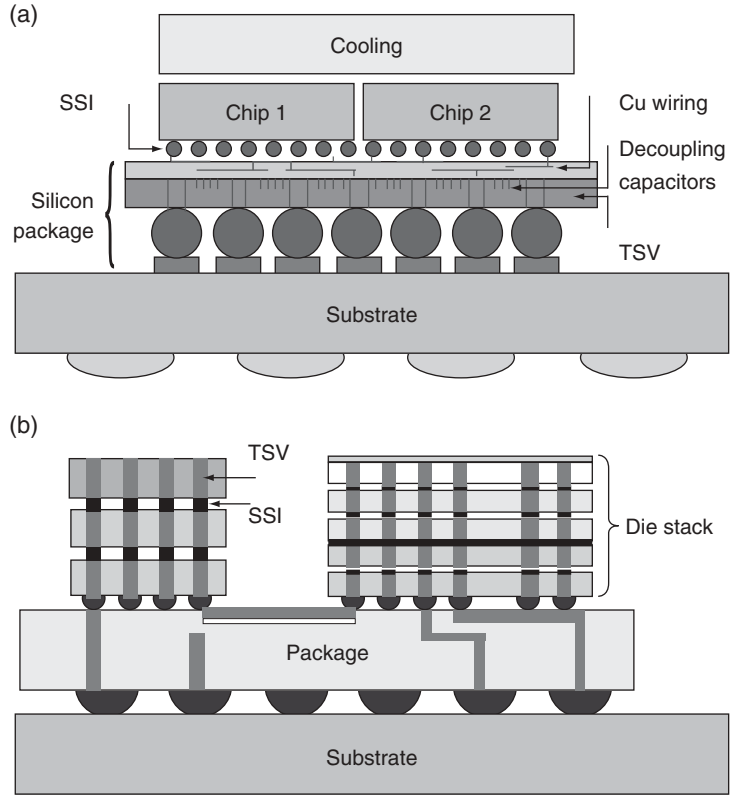


Figure 12.2 *Schematic cross-section for (a) 3D silicon package with through-silicon vias (TSVs) interconnecting two die and (b) multiple stacked die using TSVs and silicon–silicon interconnect (SSI) on a base package* [6]

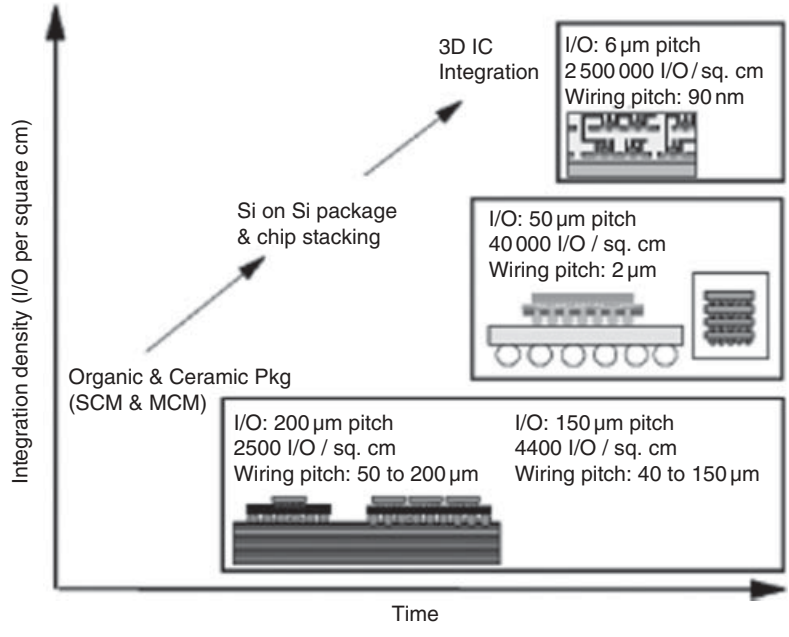


Figure 12.3 *Silicon integration comparison for ceramic and organic packaging, silicon carrier or glass carrier and chip stack and 3D silicon circuits and wiring*

wafers, photonic wafers and high-performance silicon packages with TSVs could be used to permit a wide variety of product applications when integrated into 3D die stacks or integrated 3D modules. TSV, thinned silicon and interconnect scaling from under 10 to over 10^8 I/O per cm^2 or per die, depending on structure (see Figure 12.3), compared to traditional off-chip integration scaling up to about 10^3 cm^2 I/O fills the gap between 'on-chip' integration density and traditional 'off-chip' I/O interconnection. The wide range of TSVs and die-to-die interconnect density applied to heterogeneous chip integration comes at a time when Moore's law for semiconductor chip scaling is slowing down or reaching an end as the technology scales to atomic dimensions [1, 2, 8]. Therefore, these newly created high-density 3D technology integration options offer potential for new applications from miniature-sized products to highly integrated 3D products. The design, architecture and form factors for 3D technology can be prioritized toward a number of product benefits such as performance enhancement, power efficiency, low cost, time to market, miniature size or other attributes that bring value to the application.

Research on 3D integration with TSV, thinned silicon and fine-pitch silicon-to-silicon interconnect has been evolving for more than a decade. Figure 12.4 summarizes 3D system technology components and importance to the system [9]. 3D test vehicle designs have been followed by build, assembly and characterization studies to provide an understanding of design, architecture, structure and process integration capabilities and limitations. Results from these design, modeling and technology studies provide guidance on 3D performance, power efficiency, design rules, structures, processes, test and reliability, which

System Technology Component	3D System Impact / Comments
1.3D Design & Design Library	Design Rules, Performance, Power Density, Thermal Issues, Cost
2. Architecture	System Performance, Heterogeneous Integration
3. 3D Design Tools & Modeling	Floorplanning, Layout, Routing, Interconnect, Power, Thermal & Electrical Models, ...
4. Chip Technology	CMOS, Bulk, SOI, Technology Node,
5. Package & Interconnect	Silicon, Glass, Laminate, Ceramic, Hybrid, Area Array, Peripheral
6. Assembly & Bonding	Chip to Chip, Chip to Wafer, Wafer to Wafer, Solder, Metal, Oxide, Adhesive.
7. Test	Wafer Test, BIST, Module Test, Burn-in, Known Good Die (KGD), KGD stacks, Cost
8. Module Integration & Cooling	Module Integration, Board Interconnect, Power Delivery & Distribution, Thermal & Cooling
9. System Reliability	Robust Materials, Structures, Processes and Modules, Self-repair, Sparing

Figure 12.4 *3D technology integration components and system impact* [9]

can support a growing variety of product requirements. Data from these investigations provide guidance toward robust groundrules and processes, which can support manufacturing and product reliability requirements. Practical design, technology fabrication and interconnect approaches need to be considered for targeted TSV and assembly processes to achieve interconnect density, silicon thickness and power densities of the system application. Options such as TSV conductor material and interconnect material and an assembly approach between die-on-die, die-on-wafer and wafer-to-wafer processes should be taken into consideration. At the same time, one must also consider not only the specific new 3D technology features of TSV, thinned silicon and silicon-to-silicon interconnect but also a range of technology elements needs to be considered around the product requirements. A balance between application design objectives and a high yielding process, such as including feature redundancy for interconnections if needed, die size, manufacturing throughput, cost and test methodology, is also an important consideration for specific applications. In this chapter, we report on examples of test vehicles designs, fabrication and characterization.

12.2.2 System Needs

System design, silicon technology and packaging integration for system applications are reaching a time in the semiconductor industry where severe limitations from evolutionary trends are evident [8, 10, 11]. Frequency scaling for microprocessors has been limited by escalating power consumption and leakage current technology nodes below 65 nm. Semiconductor scaling trends are fast approaching atomic limits. As semiconductor manufacturing moves from 32 nm and 28 nm node to 22 nm, 15 nm, 11 nm and perhaps 8 nm dimensions, we might expect that Moore's law [2] and Dennard's semiconductor

scaling rules [12] will be slowing down and reaching an end. As we approach semiconductor scaling limits, quantum mechanical properties take over and thus traditional semiconductor CMOS scaling based on silicon node advancements will reach limits and end. As we approach these semiconductor limits, use of new technologies or hybrid integration of technologies could be needed. Custom application accelerators, carbon nanotubes, graphene, use of quantum computing or alternate new technologies may be necessary for future systems [8].

System performance scaling challenges are also growing. Historical system trends have benefited greater than a 60 % system performance advantage due in part to processor chip performance improvement per generation to 65 nm technology. System scaling has also been limited in part by less than 15 % improvements in memory access time, less than 10 % growth in off-chip interconnection density and limitations in chip cooling [10, 13]. It is expected that direct system performance scaling from semiconductor processor node advancements can be < 20 % for each new semiconductor generation. Even with lithography scaling giving circuit density growth for each new technology node, challenges such as leakage power, latency in memory and interconnection bandwidth to memory could impact future systems performance [10, 13]. In order to achieve continued system performance scaling at better than 60 % per generation, the attributes of a system stack including hardware and software are needed. For example, increasing the numbers of software threads combined with an increasing number of cores per processor die is expected to help system performance improvements. In many systems, gate leakage limits power efficiency at higher frequencies but introduction of high-*k* metal gates has helped reduce leakage current. For advanced lithographic nodes, increased numbers of chip repeaters are needed due to smaller wire sizes and long-distance interconnections at these smaller feature sizes, but they can impact total power and power efficiency. As these multicore processors scale in systems usage, so too will they need to scale access to cache and memory with increased bandwidth.

Increased subsystem communications can help system scaling both through the use of 3D electrical interconnection with a shorter interconnect length between circuits and through the use of optical communications. In a 2D logic and memory die, the interconnection length for domains can range in length up to a few or even tens of millimeters. Use of 3D integration can offer domain interconnections at lengths of a few tens of micrometers, thereby providing 2 to 3 orders of magnitude reduction in wire length for reduced latency. 3D also offers the opportunity for significant interconnection density increases between silicon layers in a stack or with the use of silicon packaging, which can directly improve the interconnection bandwidth by 100 times to 10 000 times compared with traditional off-chip interconnection density or bandwidth [7, 10, 14]. Thus system challenges and semiconductor scaling limits need not limit system scaling, power reduction and miniaturization. For example, to compliment semiconductor advancements, subsystem scaling using three-dimensional, high-performance die stacks and 3D integration packages can benefit system advancements [8]. The subsystem scaling can include 3D integration with high-bandwidth electrical and optical interconnection between large numbers of multicore processors and memory [6, 8, 10, 13]. Appropriate architecture and software that can leverage 3D multicore, multithreaded structures will also be critical to optimize the benefit for system scaling for future systems. It is expected that a combination of semiconductor scaling, 3D subsystem scaling (use of 3D electrical and optical interconnection), use of

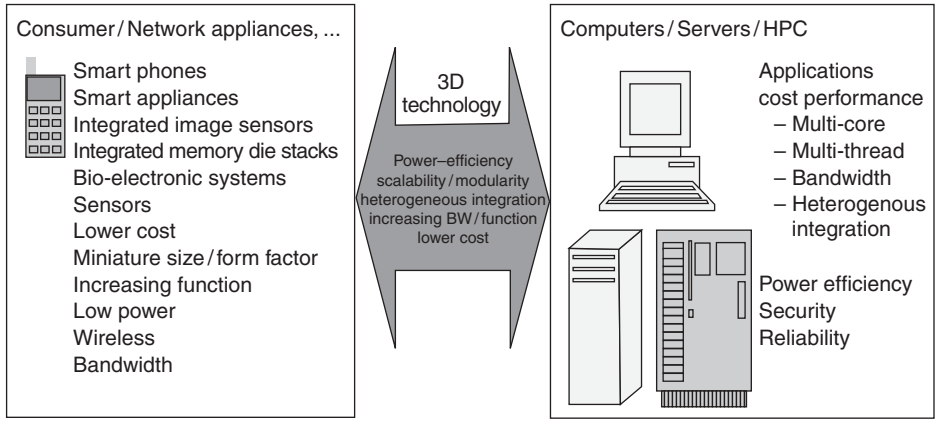


Figure 12.5 *3D technology offers system advantages for mobile applications needs and high-performance system needs* [12]

multicore, multithread processors, system accelerators and system software enhancements will be necessary to support system performance scaling at greater than 60 % per generation. In addition, traditional off-chip packaging interconnect input–output (I/O) connections have taken a circuit area that limited scaling to a finer pitch and have required >10 mW/Gbps power levels to connect to on-board circuits. System requirements are increasing demands for more I/O and at much better interconnect power efficiency. For mobile systems, increased I/O are required to support higher data rates such as streaming video for hand-held devices. For high-performance computing, increasing I/O, increasing bandwidth and more power efficient interconnect are needed to support power efficient computing. These requirements are becoming important for both mobile platforms and high-performance systems, respectively driven by 'on demand' access to the internet, limitations in mobile platform battery life versus weight and the rising cost of energy for high-performance computing systems operations.

Emerging three-dimensional (3D) technology can offer close proximity interconnect that can translate into system benefits including higher performance, miniaturization of system hardware, short interconnection lengths offering lower latency and high bandwidth, lower power interconnect, lower cost and other benefits. Figure 12.5 shows how 3D technology can support system needs for mobile and network applications systems as well as satisfy high-performance computing applications [15]. Portable electronics systems such as smart telephones, internet platforms, smart sensors and smart appliances need increasing function in small form factors, wireless connections with high bandwidth, low cost, manufacturing for large volumes and low power consumption for longer battery life to meet the demands of an ever-increasing function in hand-held systems. High-performance computing systems such as servers, cloud computing and supercomputing systems need high performance using multicore, multithread, high-bandwidth interconnects, high power efficiency and efficient cooling solutions, high security and high reliability to meet the demands of 100 % availability, trusted and cost-effective computing systems.

12.2.3 3D Interconnect Design and Architecture

The greatest system benefits for 3D technology require design and architecture optimization leveraging 3D design rules and 3D fabrication advancements in order to gain the greatest product advantages when it is introduced. Development of a 3D competitive product requires differentiation in the market place, competitive cost and timely introduction. A great opportunity exists as 3D technology advancements are made to create new products that have attributes that non-3D technology cannot provide. A great risk may also exist if the product requires design rules that do not achieve high yield and competitive costs for volume production.

As discussed above, 3D technology can provide performance benefits, power savings, high bandwidth and/or lower costs where system optimization requires design and architecture toward one or more of the targeted product benefits. Against product requirements or objectives, a comparison of 2D and 3D potential design and architecture options should compare relative advantages and disadvantages of structures that might be considered. Advantages of 3D technology and structures may include shorter wire lengths, higher bandwidth interconnections, low latency, lower power, smaller size and potentially higher performance and lower costs. Depending upon application and the integration structure, disadvantages of 3D structures may include increased power density, which could lead to challenges in power delivery including voltage and current distribution as well as challenges in cooling the 3D structure. Depending on the complexity of a 3D product, challenges may also exist in design tools and manufacturing, including wafer fabrication, wafer thinning, wafer handling and finishing, assembly, test and module integration. Some products may not be best suited to utilize 3D technology and others may have advantages using 3D structures that cannot be achieved with 2D technology.

A 3D integrated circuit (3DIC) design using TSVs can consist of 3DIC fabrication using thinned die or thinned bonded wafers where TSVs may be in peripheral interconnect IC, area-array interconnect IC or alternative IC patterned layouts [1]. A 3D packaging design may consist of system-on-package (SOP), system-in-package (SIP), such as wire-bonded, peripheral interconnects packaging, area-array interconnect packaging, package-on-package (POP) or alternative package layouts [1, 4, 5, 7]. The focus of this chapter is toward 3D integration using vertical interconnect TSVs for integrated circuits such as stacked die in systems and short-length (non-wirebond) vertical interconnections in 3D packaging systems.

Physical Design

Efficient floor planning of 3DICs and/or 3D packaged systems may include single- or multistep approaches and single- or multiobjective approaches [15–18]. The objective in 2D floor planning is typically to minimize the total area of the 2D integrated circuit blocks and packaged systems, which can lead to smaller size, shorter wire lengths and lower costs. For 3DIC and 3D packaged systems, circuit blocks may be in the same plane or on another plane. A design with many circuit blocks must then consider a floor plan to interconnect these circuit blocks to achieve small size, short wire length and timing while optimizing placement of these blocks for performance, power and minimum complexity, which impacts cost. The 3D floor plan and trade-offs become more complex for interconnects,

timing, wiring and, furthermore, must consider power density for power delivery/distribution and thermal considerations/cooling. 3D layout tools and routing must take into consideration the 3D hierarchy to account for circuits at multiple levels such as 1, 2 and 3 and vertical interconnections between these circuits such as interconnect levels 1 and 2, which may consist of TSVs and an interconnect structure. Thus design tools and design need to accommodate traditional routing techniques along with hierarchy for the third dimension. Furthermore, these structures should take into consideration design for manufacturing and an appropriate test methodology. Design and test must consider either appropriate redundancy, test level repair and/or a built-in self-test to permit known good die (KGD) and/or known good wafers to lead to known good 3D ICs and 3D packaged systems.

Timing

Two-terminal and multiterminal interconnect timing across multiple planes or levels of circuits may result in different impedances [1]. The timing is dependent on the TSV and interconnect manufacturing processes (such as using one or more manufacturers) and is dependent upon the 3D structure, such as face-to-face circuits, face-to-back circuits, back-to-back circuits or some interlayer combination. Optimization of timing usually includes optimization of the longest wire interconnections and from modeling the electrical characteristics of all the interconnect segments. Minimizing the interconnect delay requires optimization of wire characteristics as well as placement of vias, and interlayer TSVs and interconnects.

Clocking

Symmetrical H-tree and X-tree structures for 2D circuit clocks can permit a clock signal to simultaneously arrive at the multiple branched circuits to provide synchronous data processing [19, 20]. The intralayer and interlayer interconnects associated with 3D clock structures make the challenge of clock distribution to multiple levels within the 3DICs inherently more difficult. Clock distribution can be distributed to a global network and to multiple smaller local networks. Especially for longer distances and higher frequencies, load imbalances, process variations and cross-talk can impact the arrival time of the clock at various locations; this variation is called clock skew. Modeling and measurements of the clock distribution as segments of a transmission line can aid in understanding reflections at branch points and the speed and power consumed by the clock network. 3D clock structures and test circuits compared H-tree structures, local mesh topologies and global rings for 3D structures and showed that the local mesh structures consumed the least power for the structures studied [1].

3D Circuit Architectures

3D heterogeneous integration offers great opportunity for enhanced performance and novel systems. Examples such as integration of FPGA with memory, processors with memory, GaAs or SiGe analog circuits with digital circuits, and sensors with microprocessors are but a small list in a growing variety of heterogeneous systems opportunities from 3D technology. Design and optimization of the architecture leveraging the third dimension of integration that vertical TSV's and interconnect between layers of circuits offers, can lead

to orders of magnitude of increased interconnects and much shorter connection lengths. These attributes of 3D design and architecture then lend themselves to minimize latency and power consumption for communication channels. These advantages can be leveraged to improve system performance and power efficiency. Proper partitioning of cache memory in the 3D structure and ability to provide multiple layers of memory in close proximity to others layers of circuits such as processors can provide reduced time to access memory. In addition, use of low power memory layers adjacent to processors can increase total memory size and bandwidth while staying within an acceptable thermal budget for a 3D structure. Similarly, FPGA to memory, sensor to processor and other 3D heterogeneous architectures can profoundly lead to revolutionary new systems [10].

3D Industry Standards

Over the last decade, design and technology advances in 3D chip integration have been making progress at universities, consortia and in industries from around the world [1, 6, 7, 9, 10, 21–36]. Initial product applications using TSVs and 3D integration have begun to slip since about 2008 including image sensors and power amplifiers for wireless applications [37, 38]. These first applications have had limited numbers of vertical interconnections and have not required design standards and industry compatibility. These initial products have also not required 3D engineering design automation (EDA) tooling, which will emerge as more complex 3D designs are needed for product applications. As complexity increases and integration of heterogeneous technologies begins to emerge, the need for 3D compatibility between multiple wafer and assembly manufacturers will also become more important. It is expected that over the next decade the next generations of complex 3D product applications, industry design and compatibility standards will begin to emerge. Recently, SEMATECH, the Semiconductor Industry Association (SIA) and SRC have announced formation of a 3D Technology Enablement Center to establish 3D industry standards and enable growth using 3D technology by working with SEMI, Semiconductor Research Corporation (SRC) and industry participants [39]. 3D designs and products are beginning to be announced, such as use of a silicon package with TSVs to integrate multiple die such as that from Xilinx [40] using TSMC 3D technology and from Semtech [41] using IBM 3D technology. In addition, wide I/O memory using stacked memory die and a logic controller die are nearing industry readiness, such as that from Elpida [27], Samsung [42] and Micron [43].

12.2.4 3D Fabrication and Interconnect Technology

3D Technology Advancements

Over the last decade, publications have described research including approaches for wafer fabrication with TSVs and interconnect assembly to form stacked die, bonded wafers and/or integrated 3D modules with silicon packages or high-bandwidth vertical interconnected packages. From the late 1990s to the present, 3D technical publications and research progress from organizations and companies including ASET Consortia of Japan, Fraunhofer Institute of Germany, Massachusetts Institute of Technology (MIT), CEA-Leti, imec, Sematech, Elpida, Samsung, IBM, Amkor and many others [22–36]. Research investigations

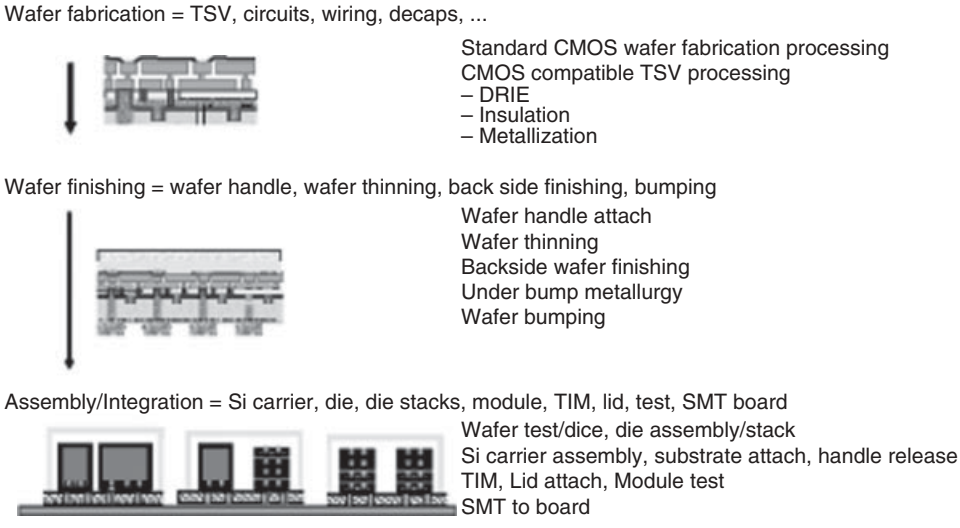


Figure 12.6 *An example of a 3D process flow including wafer fabrication with TSVs, wafer finishing and assembly* [14]

have examined a variety of materials, structures and wafer fabrication processes with TSVs, 3D die stacking, wafer bonding and 3D packaging/module integration approaches. Researchers have recognized the importance of developing fine-pitch vertical interconnections using through-silicon vias, developing wafer handling and thinning technology for silicon wafers and interconnection processes for joining thinned silicon die into die stacks, die to silicon or glass packages and developing wafer-to-wafer bonding technologies. Figure 12.6 shows an example of a high-level 3D process flow including wafer fabrication with TSVs, wafer finishing and a 3D die stack assembly [14]. In addition, 3D process and assembly advancements and the increased power density for some 3D applications are driving advancements in materials and structures capable of supporting higher current flow and power delivery per unit area. Advancements in vertical interconnection density demonstrations also support increased signal interconnections for increased bandwidth. Researchers continue to study the best approaches for thermal cooling and modeling of heat removal from thinned silicon and 3D stacked structures with TSVs. Each 3D application will have its own integration challenges. Common requirements for successful 3D product applications include design, fabrication, assembly and timely introduction of competitive products. Figure 12.7 shows the 3D challenges and readiness of the technology that can apply to 3D applications [44, 45]. Advances in 3D technology have begun with 3D products using low TSV interconnection density and pitch. A continuing extension of understanding for design, architecture, wafer processing, wafer finishing, assembly, test and module integration as well as standards to ease the use of die and components from multiple suppliers will also need to compliment 3D technology advancements for more complex products.

Many technical publications have reported on a wide variety of TSV processes and sizes [7, 9, 21–23, 27, 30–32, 46, 47]. TSV diameters, TSV pitch and silicon thickness for

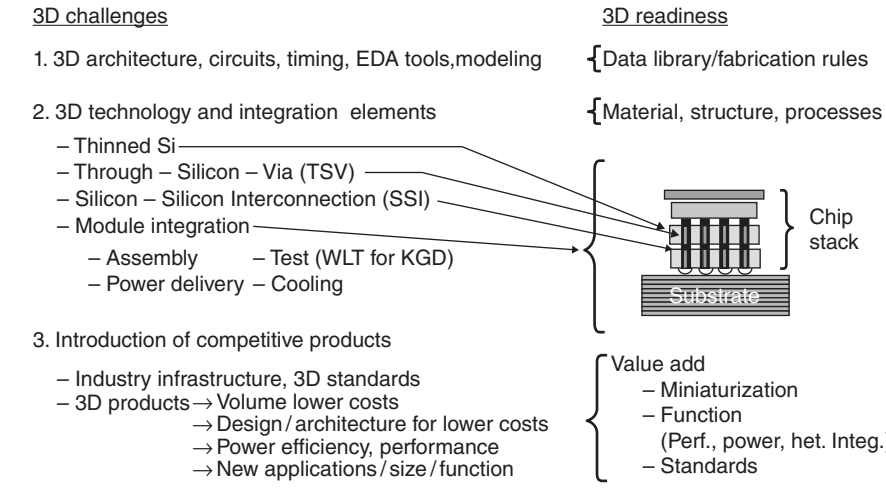


Figure 12.7 *3D-technology challenges and readiness including 3D design, technology and introduction of competitive products* [44, 45]

vertical connections have ranged from large sizes to small sizes. Large TSVs have included about 80–100 µm via diameter, over 200 µm pitch and silicon thickness of over 100 µm to 300 µm, and have been targeted for image sensors, power amplifiers, analog devices and advanced packaging technologies. Small TSV sizes include via diameters from under 20 µm to less than 0.5 µm, via pitch of 50 µm to under 3 µm and silicon thickness of 60 µm to under 1 µm and have been targeted for advanced CMOS semiconductor applications, memory die and die stacks, heterogeneous product applications and small form factor mobile electronics. TSV conductors reported include tungsten, copper, nickel, composite, paste, doped polysilicon as well as other electrical conductors. Takahaski *et al*. investigated 10 µm copper conductors utilizing through-silicon vias for electrical interconnection at 20 µm (Figure 12.8) [22]. Another report by Topol *et al*. [48] and one by Guarini *et al*. [49] were on TSVs or vias under 0.2 µm diameter, pitch under 6.7 µm and TSV or via height of under 1 µm to 2 µm. In these silicon-on-insulator (SOI) vertical interconnect examples, the vertical copper via does not need to go through silicon because the bulk silicon is removed. Joseph *et al*. [50] and Stamper *et al*. [51] reported on the use of about 100 µm height TSVs with a high aspect ratio (see Figure 12.9). The high aspect ratio tungsten TSVs supported next-generation SiGe power amplifiers for wireless communications where noninsulated tungsten-filled vertical connections provided a low inductance path to ground to enhance product performance and insulated tungsten TSVs for some stacked die applications.

Numerous technical publications have reported high-density silicon interconnect technologies for die stacking, silicon assembly to silicon packages or thinned silicon assembly including use of anisotropic conductive adhesives, lead containing solder, lead-free solder interconnect, Au–Sn interconnect, thin intermetallic composition interconnect, Cu–Sn to Cu

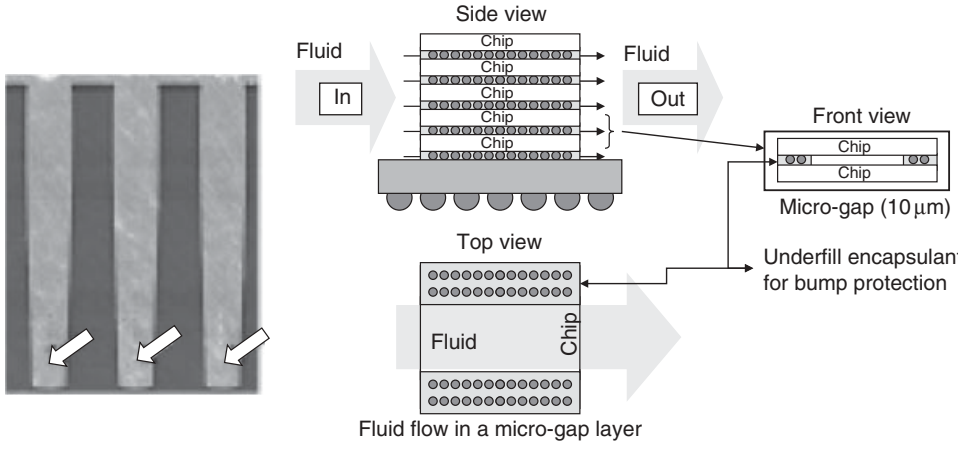


Figure 12.8 *Takahaski et al. investigated 10 μm copper conductors utilizing through-silicon vias for electrical interconnection at 20 μm and die stack integration with fluid flow for cooling* [22]

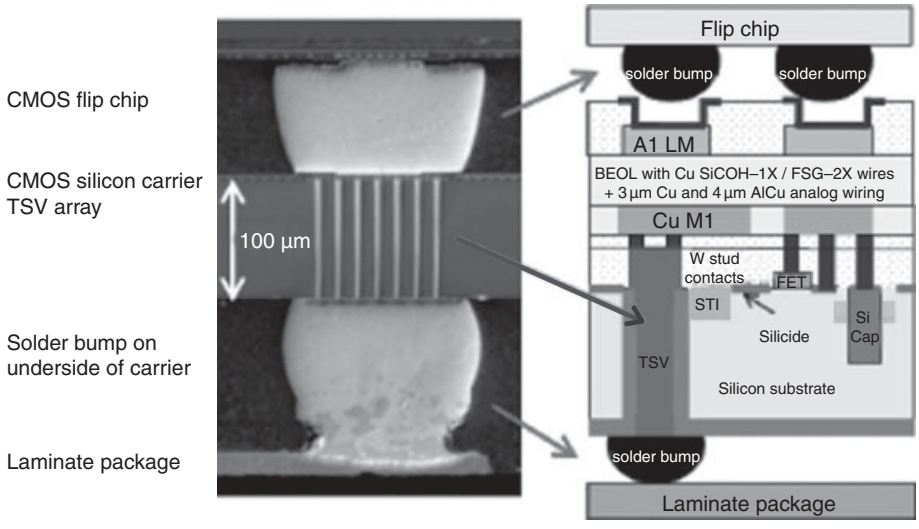


Figure 12.9 *3D tungsten TSV cross-section and schematic* [51]

joins and Cu–Cu bonding [7, 24, 25, 29, 52–56]. Each of this interconnects drives a variety of structures and processes to achieve vertical interconnects in combination with TSVs that permit a short-length electrical connection between circuits of adjacent silicon layers. Product applications may drive specific electrical requirements such as a current-carrying capability, capacitance, resistance, inductance, signal data rate, cross-talk, reliability and cost, depending on the targeted application requirements. Feil *et al*. have shown bonding

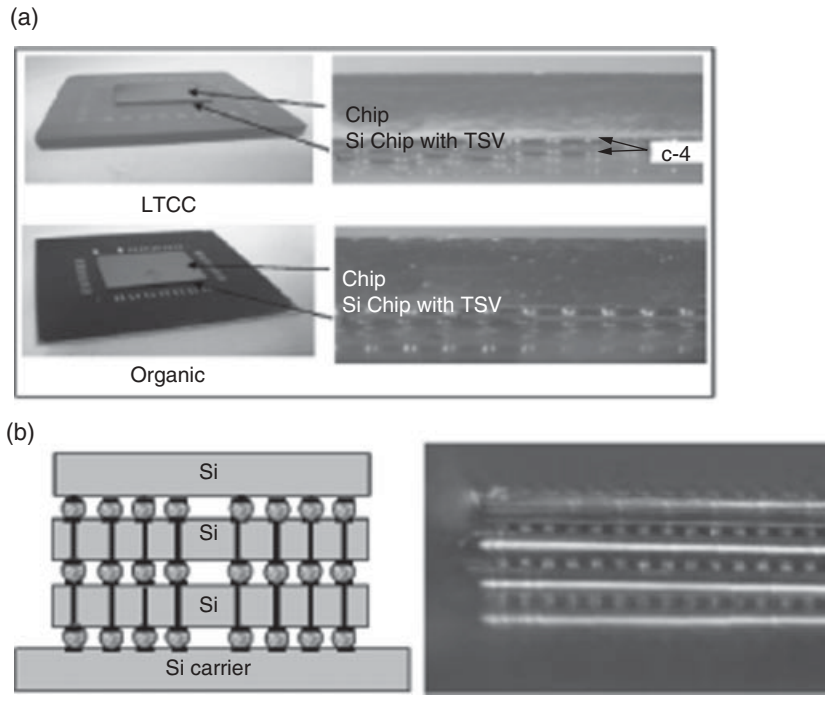


Figure 12.10 *3D solder interconnection examples including: (a) stacked die with 200 μm pitch and (b) stacked die with 50 μm pitch*

with anisotropic adhesive for 25 μm thin silicon where the bonding requires a continuous force during curing [24]. Hunter *et al*. have assembled silicon 50 μm diameter Au/Sn interconnects and reported on reliability [25]. Reed *et al*. [52] and Agarwal *et al*. [53] have more recently reported 10 μm pitch interconnect using Cu/Sn to Cu or Cu to Cu bonding for 3D integration and Cu/Sn microbump interconnect for 3D TSV chip stacking, respectively. Wright *et al*., Dang *et al*. and Maria *et al*. have reported on assembly and reliability of 25 μm diameter solder microinterconnect compositions with PbSn, and high Sn-containing, Pb-free solders for high-density silicon integration [54–56]. Figures 12.10 and 12.11 show examples of solder and solder fine-pitch interconnection used for a die stack and 3D multichip package and 3D fine-pitch multichip integration to support high /I/O, wide-bandwidth silicon circuit integration, respectively. These microbump controlled collapse chip connection (uC-4) papers reported on the use of high-density interconnection for silicon package interconnection, reworkability of uC-4, die stack assembly of multiple, thinned silicon layers and reliability of these solder interconnects. Technical challenges for successful fine-pitch interconnect include interconnect alignment, coplanarity of the interconnection, contamination control, assembly yield, adhesive underfill for fine-pitch interconnection or no-flow adhesives, current capacity of the interconnection to avoid electromigration and thermal migration, consistent electrical characteristics of resistance, inductance, capacitance and high thermal conductivity. Ultimately as TSV and

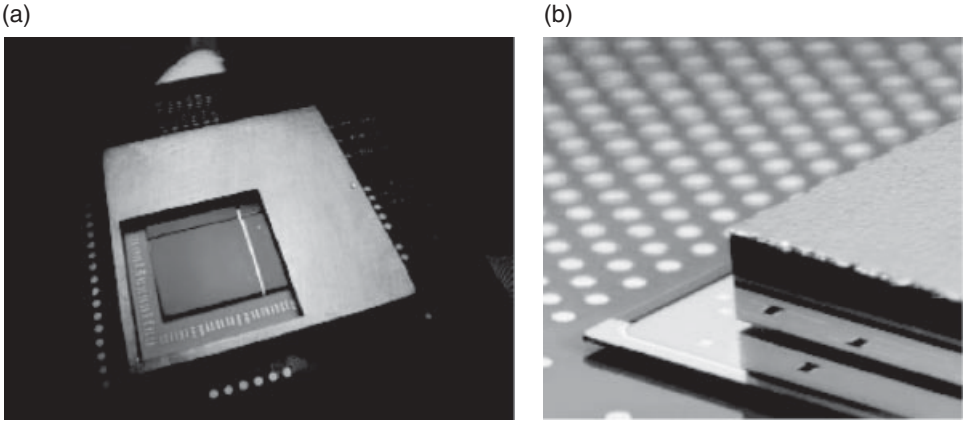


Figure 12.11 *3D solder interconnection examples including: (a) an integrated silicon 3D package with multiple die with 200 μm pitch and (b) 3D silicon interconnect package with fine-pitch interconnection*

interconnections are adopted for products, optimization of the 3D structure, materials and processes will lead to robust solutions that meet product and reliability specifications. As 3D technology adoption leads to higher volume product shipments, more significant statistical data on manufacturing, yield and product reliability will be available. Relative costs for TSV, wafer thinning and 3D silicon interconnection will be reduced through manufacturing continuous yield improvements and productivity improvements in future generations of tooling and associated processes for growing volume production.

This chapter section will provide more information and discussion associated with 3D technologies.

Wafer Fabrication with Through-Silicon Vias (TSVs)

Applications may need only a few, tens, hundreds, thousands or millions of vertical interconnections that are product dependent. Product design, architecture and specifications will determine the appropriate 3D technology, materials, structures and processes needed to manufacture the hardware. As discussed above in Sections 12.2.3 and 12.2.4, use of 3D technology should provide a competitive benefit for the product. Examples of TSV quantities, sizes, structures, fabrication processes, wafer finishing processes and subsequent integration will impact wafer fabrication process choice with TSVs. For example, the range in TSV size includes diameter or *X–Y* sizes from $<0.5\,\mu m$ to about $100\,\mu m$. The silicon thickness includes SOI or silicon on the thin side of $<1\,\mu m$ to $10\,\mu m$ and up to a full wafer thickness of $730\,\mu m$ to $785\,\mu m$ for the thickest silicon TSV (although most reports have been at $300\,\mu m$ or less and more recently at $100\,\mu m$ or less). TSV height to diameter aspect ratios reported included evaluations from a low aspect ratio of about 2 to 1 to values of over 20 to 1 for copper fill and up to about 40 to 1 for tungsten TSV conductors, respectively. These structures, sizes and aspect ratios impact the physical process as well as resulting electrical, mechanical, thermal and reliability characteristics of the TSV.

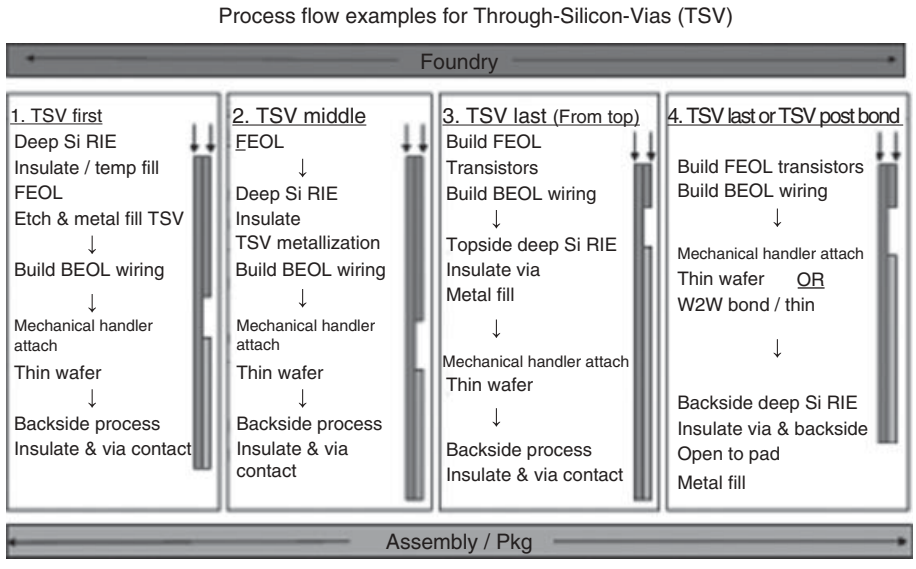


Figure 12.12 *3D TSV comparison processes including TSV first, TSV middle and TSV last processes* [6]

TSV Process Sequence

A comparison of process sequences for TSV formation resulting in vertical electrical connections through thinned silicon structures is shown in Figure 12.12 [6]. In this example, the TSV process sequence is compared for TSV first, TSV middle and TSV last processes. In a TSV process, typically an isotropically etched hole is formed in silicon, followed by deposition of a dielectric layer for electrical insulation of the via from the silicon, followed by metallization, which includes a liner deposition, seed and metal fill operations. Figure 12.13 shows an example of via schematics and photographs for TSV formation [31]. When initiated prior to circuit fabrication, the TSV process is often referred to as the TSV first process and when TSV formation follows circuit fabrication but prior to wafer finishing steps, the TSV process is often called a TSV middle process. TSV last processes can be employed from the top side of a wafer, from the wafer backside to a landing pad on the circuit side following wafer thinning or may also refer to creation of a vertical interconnect after bonding two wafers and thinning one wafer, as previously discussed [31, 32, 35]. Next steps for vias first or middle processing would include circuits processing and back-end-of-line (BEOL) or just BEOL processes to complete the top side of a wafer, attaching a mechanical wafer to the top of the wafer using a glass or silicon wafer to provide mechanical support while the active or passive circuit wafer is thinned from a standard wafer thickness of about 730 µm (200 mm) or 785 µm (300 mm) to the desired product thickness. The mechanical wafer can be attached by means of a polymer adhesive, which can later be removed by means of chemical etch, heat, laser or an alternative method. Adhesive properties can limit subsequent process steps depending on the adhesive material and mechanical handle wafer used The wafer can then be thinned by mechanical grinding in one or more

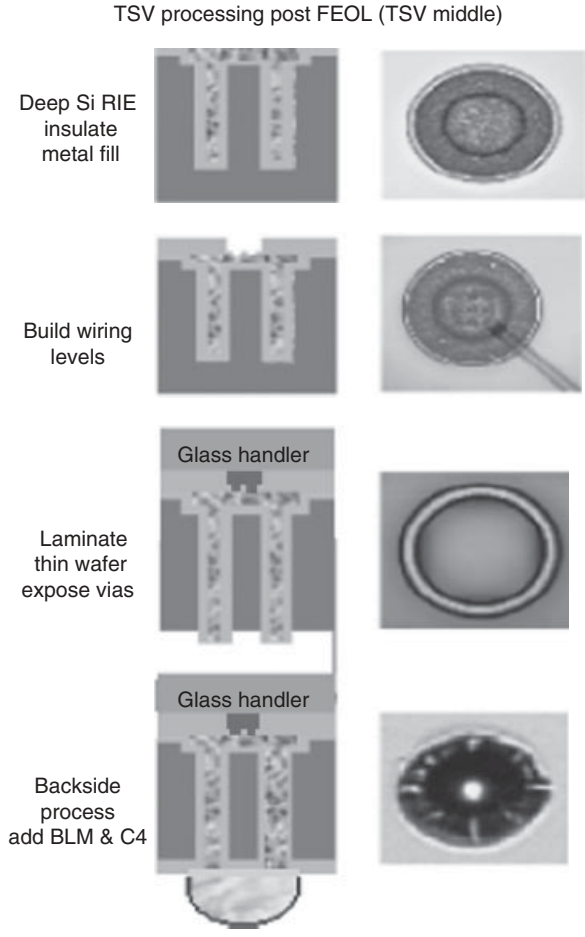


Figure 12.13 *An example of via schematics by process step and photographs for TSV formation* [31]

process steps, polishing or chemical–mechanical polishing, chemical etching (wet or dry) or a combination of mechanical and etch methods. Next the backside metallization and redistribution wiring processes for backside electrical insulation around the TSV and electrical interconnection to the TSV would be completed followed by the creation of an interconnect metallurgy for subsequent assembly. Several wafer finishing and thinning processes have been reported using mechanical attach wafers with bonding and debonding processes [57–60].

There are many combinations of TSV formation using wafer processes that may be possible. Fabrication of active circuit wafers with vertical interconnections from TSV first, TSV middle and TSV last sequence steps that can also lead to robust structures are all possible, but in all cases care must be given to avoid damage to active circuits based on design rules, TSV materials and structures and fabrication process temperatures employed

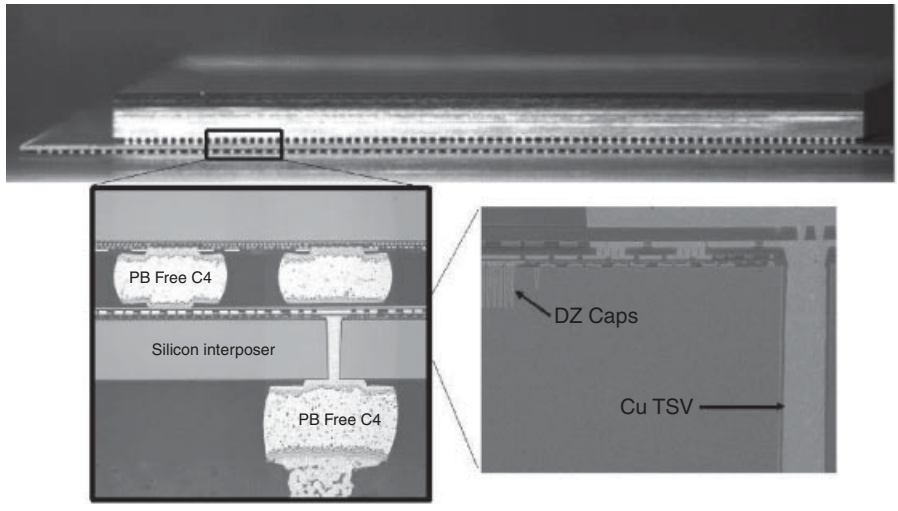


Figure 12.14 *3D Sematech press release photograph with cross-section of copper TSV and silicon interposer from IBM* [41]

during wafer fabrication. Simple passive silicon packages can utilize TSV processes such as TSV first or TSV last steps with fewer constraints compared to wafers with active circuits. Additional perspectives on through-silicon vias have been reported [31, 32, 35, 51]. Examples of TSV cross-sections for tungsten and copper vertical conductors are shown in Figure 12.9, Figure 12.14 and elsewhere [32, 35] for SOI bonded wafers. A dielectric insulator, adhesion layer, liner, seed layer and conductor fill and excess conductor removal steps may also be used in preparation for TSV fabrication. A variety of TSV shapes can be considered in order to be compatible with polysilicon, tungsten, copper or composite TSV conductors. Examples include annular TSV, bar-shaped TSV or high aspect ratio TSV, as previously reported [22, 23, 31, 32, 35, 50, 51, 61]. Shape and size of the TSV can be determined by a combination of considerations, such as the cross-sectional area required to meet electrical resistance specifications, current carrying specifications, and taking into consideration the manufacturing yield and thermomechanical stress of TSVs based on shape, conductor and dielectric. For passive silicon packages and thick silicon, low vertical interconnection needs, larger area TSVs may be acceptable; however, for an active circuit die especially requiring high numbers of vertical interconnect, a small cross-sectional area for TSVs is desired. For wafer processing, a thick silicon such as one from 150 μm to 300 μm, many BEOL and wafer handling or dicing process steps, a free-standing silicon wafer can be processed. In some instances, a thick silicon along the wafer perimeter with a thinner silicon thickness across the rest of the wafer may be acceptable. In contrast, a bonded wafer pair consisting of a glass or silicon handle wafer adhesively attached to the wafer to be thinned is typically required to support the active wafer for backside processing. The thin wafer can be released from the mechanical wafer by several different options when thinner silicon structures (such as less than 100 μm thickness) are desired [57–60]. The thinned silicon die or die stack can later be bonded to other die in a die stack, to a

package or to other module components for mechanical integrity after releasing from the mechanical support wafer. In the case of wafer-to-wafer permanent bonding, two wafers can be bonded such as with adhesive, oxide or metal bonding and then silicon from one can be removed or thinned while the other wafer provides mechanical support for processing and in the product application. This process can be repeated for multiple high circuit layers [32, 35].

TSV Etch Process

TSV structures can be fabricated by a number of methods of silicon removal such as wet processing using a chemical etch or dry etching such as laser drilling, reactive ion etch or deep reactive ion etch (DRIE). Combinations of these etch processes are also possible. Etching often begins with photolithography and use of a photoresist or a 'hardmask', such as patterned oxide or a nitride layer, to define the features to be etched.

Wet etching of silicon can use a mixture of nitric acid (HNO_3) and hydrofluoric acid (HF) diluted with water or acetic acid performed at room temperature for isotropic etching. Anisotropic wet etching can be achieved using diluted potassium hydroxide (KOH) or other etch chemistries such as tetramethylammonium hydroxide (TMAH), where in silicon preferential etching in the (110) and (100) crystal planes is compared to the (111) orientation. These etches can lead to many different etch morphologies depending on wafer bulk crystalline orientation, the mask and wafer orientation. However, for many 3D applications isotropic vertical etched shapes are desired and thus wet etching may provide shape adjustment in combination with a dry etch.

Dry etching using a laser can be used to create high aspect ratio holes. Alternatively, silicon can be etched using reactive ion etch (RIE), which uses a plasma etch consisting of source gases broken down in a plasma to create highly reactive electrons, photons, neutral species and positive ions that impinge with surface atoms, both removing them and forming stable compounds. The chemical and physical reactions etch the surface and remaining by-products can be removed, causing the plasma to continue to react. RIE has been used for semiconductor processing and can create high aspect ratio structures or TSV but can be slow. An enhanced process called time multiplexed deep etching or just deep reactive ion etching (DRIE) was patented by Bosch (US Patent 5501892), which combines cycles of deep silicon plasma etching with passivation sequentially to etch very high aspect ratios at high etch rates on the order of up to 10 µm per minute. The sequential operation with plasma radicals such as CF_x from octobluorocyclobutane (C_4F_8) followed by passivation can also lead to a scallop surface in the TSV.

TSV Dielectric

TSVs may be fabricated with or without dielectric insulation from the silicon. For simple structures with a desired short to the base silicon no dielectric is required. For application requiring electrical isolation from the silicon, a polymer dielectric, oxide, nitride or composite dielectric may be used.

Polymer dielectrics can be processed by means of a spray, spin coat or alternate deposition method where temperature limitations may be required, such as less than 200 °C

or less than 300 °C. Robust fill and uniform isolation can be dependent on the TSV diameter and aspect ratio and processing conditions. Following deposition, polymers are cured. For via last, post-FEOL and BEOL wafer finishing for TSV, polymer dielectrics may be appropriate. Similarly, for a larger size TSV, a polymer dielectric may be a low-cost method to isolate the conductor from the silicon.

Oxide and/or nitride depositions can be completed such as thermal oxide processing at temperatures of about 900–1100 °C, whereas plasma-assisted deposition of oxide or nitrides may be completed at temperatures down to about 200–250 °C. Other deposition techniques may also be employed and again TSV diameter, size and aspect ratio can impact the uniformity of dielectric isolation. A thick dielectric with a hard oxide or nitride, thick soft polymer dielectric or combined composite dielectric may be employed to isolate the conductor from silicon and thereby minimize TSV capacitance.

TSV Conductor

Deposition of a conductor begins with deposition of a thin conductive liner and seed layer. Similar to BEOL processing of copper lines, TSV can use a physical vapor deposition (PVD) of tantalum nitride tantalum (TaNTa) and copper (Cu) followed by a full metal deposition. The liner–seed deposition should be uniform and thus deposition quality can be dependent on TSV shape and aspect ratio. A top opening that is smaller than the corresponding vertically etched hole should be avoided as this can lead to top of the via fill completion prior to complete fill of the entire TSV, thus leaving a central void or defect in the TSV. Thus a vertically etched wall or one with a minimal taper is desired. Defects in the liner–seed layer can also lead to defects such as voids along the sidewall when filling a TSV and thus surface defects or disruptive morphologies should be avoided. Other liner–seed deposition materials and/or methods may be used to provide the same function of a continuous electrically conducting layer inside the TSV surfaces with uniformity and proper morphology.

Examples of TSV conductor fill materials include polysilicon, copper, tungsten and composite materials. Doped polysilicon used in TSVs can have the advantage of a coefficient of thermal expansion (CTE) match to silicon, compatibility with CMOS processing and simplified process sequences. However, doped polysilicon has the disadvantage of orders of magnitude higher electrical resistance and current-carrying limitations. Multihigh chip stacks, use of thick silicon layers or applications with high power density may have product specifications where polysilicon may not be an acceptable conductor of choice. For lower TSV electrical resistance and higher TSV current-carrying applications, a metal conductor may be a better choice. Conductors such as copper, tungsten or a metal-composite filled conductor may be required. Copper has a desirable low electrical resistance and a high current per unit cross-section. The disadvantages of copper include a high CTE of 18 ppm versus silicon of 3 ppm, which can give rise to high thermomechanical stresses during processing or in product use depending on size and shape of the TSV. Thus use of a copper TSV may be best for smaller diameters and limited length or may require a structure compatible with robust processing and application use. In addition, use of copper conductors must be compatible with active circuit wafer processes. Tungsten can also be considered as a TSV conductor and offers the advantages of a CTE of about 4.5 ppm, which is closer to silicon and can provide lower thermal–mechanical

stress compared to copper, but has a disadvantage in electrical resistance. Tungsten electrical resistance is three times higher than copper but far better than doped polysilicon and therefore may satisfy product specifications for many applications. Another benefit for tungsten is that it can be used to fill high aspect ratio vias, even in excess of 40 to 1. Metal composites may also be used for TSV conductors but their properties are dependent on the choice of conductor, matrix fill material and the composite microstructure. Silver-filled pastes, copper annular structures with central filled composites and other TSV structures can also serve some application requirements. A wide variety of TSV electrical parametrics is possible depending on the dielectric, thickness, conductor, size, shape and conductor material of the vertical interconnect. For the TSV conductors, the product TSV specifications are critical in determination of the best conductor, structure and process.

Other TSV conductor considerations include cost, compatibility with the desired semiconductor wafer and package. For each TSV conductor, wafer and 3D process compatibility should be established. Examples include processing the TSV prior to FEOL, post-FEOL or post-FEOL and BEOL from the top or bottom wafer surface. Another question may include other limitations, such as temperature limitations based on the application requirements and reliability, mechanical handler process and compatibility with semiconductor wafer fabrication processes. In addition, subsequent die stacking or wafer bonding process operations, test and module integration compatibility must be acceptable. For example, thermal limitations may preclude the use of some conductors that require high-temperature deposition or annealing steps. Ultimately the TSV material choice is dependent on the resulting microstructure, cost and properties against the application TSV specifications or requirements. In each application, consideration for cost and specifications such as electrical, mechanical, thermal and reliability are necessary.

Silicon test structures have been used to establish robust TSV materials, process, sizes and CMOS- and SiGe-compatible design groundrules. The TSV processes must achieve high yield with desired electrical parametrics and high reliability. Many demonstration test structures were characterized and the best structures established for various TSV objectives. Mechanical modeling and simulations compliment experimental measurements. 3D stress models were able to identify high stress regions in a TSV structure and permit modifications when necessary to improve TSV structures for process compatibility and reliability. Results have shown up to 100 % yields in wafer tests, elimination of defects and establishment of desired groundrules that satisfy compatibility with CMOS or SiGe wafer processing and that meet reliability objectives [31, 41, 50, 51].

Back-End-of-Line (BEOL) and Wiring

For 3D structures and wiring, standard back-end-of-line (BEOL) processes include dielectric insulation, photolithography, metal deposition, chemical–mechanical polish and dielectric deposition. Dielectric insulation layers such as plasma-enhanced chemical vapor deposition (PECVD) or a polymer-based dielectric can be deposited on the wafer surface by a spin-on process and bake. Next photolithographic processes include spin-on photoresists deposited at a given thickness on a wafer. The film is baked to remove solvents and then exposed to ultraviolet light. Post-exposure the film is developed and baked to create a stable film ready for subsequent processing, such as etch of a dielectric film.

Similar to the TSV process described above, BEOL metal wiring and vias are formed using PVD liner–seed deposition and copper electroplating. Electroplating of copper has been used for more than a decade in semiconductor processing, which involves use of an electrolyte against the wafer and use of a voltage potential applied between the seed layer (cathode) and an anode. The voltage potential drives a current in the anode or copper ions contained in a chemical bath to be reduced to copper metal on the surface of the cathode or seed layer. A copper plating bath can have many components including a copper electrolyte such as copper sulfate and sulfuric acid as well as chloride ions. Other additives in the plating bath can be accelerators, suppressors and levelers, which can aid in the deposition rate and quality of the copper film being deposited. Copper from copper anodes can be dissolved into the chemical bath replenishing the ions driven to the cathode seed layer. The copper surface deposition fills the etched photoresist, which later becomes the vias and wires on a wafer following copper removal from the surface of the photoresist, such as by chemical–mechanical planarization (CMP). The quality of the copper deposition is also dependent on the current flow, uniformity, tool and the waveform, such as a pulsed waveform during deposition, which can accelerate deposition rates.

Chemical–mechanical planarization (CMP) can be used to remove the over-plated copper. The copper damascene wiring levels use this CMP process, which has a combination of mechanical abrasion of the surface copper with a mechanical polishing pad and abrasive colloidal slurry, thus causing a combined mechanical material removal and a chemical reaction to remove excess copper. The polishing action of the slurry and polishing pad aids in material removal and creates a more uniform flat surface. During this operation the wafer is held with a backing film and pressure is applied to remove the excess copper uniformly to create a more planar surface. Single damascene processing can create a via or wire layer whereas a via and wire structure can be created using a dual-damascene process.

Signal Integrity and Electrical Characterization

For 3D structures, electrical characteristics of TSV, wiring, via and interconnect structures need to be measured and correlated with electrical models and simulation tools. For example, measurements from test vehicles to establish the *X–Y* wire width, thicknesses and spaces, vertical TSVs dimensions, via dimensions and silicon interconnect dimensions help to establish understanding for vertical buses through one or multiple layers of thin stacked silicon. Examples of test vehicle results have been reported [7, 28, 50, 51, 61]. For example, signal integrity has been characterized using frequency and time domain measurements [28, 45, 50, 51, 62–64]. Results were measured for signal transmissions from 2.5 mm to 75 mm line length and for frequencies between 1 and 10 GHz. Further results explored low-power I/O drivers and signal integrity using line lengths from 2 mm to 60 mm. In some test structures, TSVs had 0.2 mΩ of resistance per μm of silicon thickness and 0.15 pH inductance per μm of silicon thickness. Signal integrity measurements for horizontal silicon packages included wire sizes of 0.8 μm to 3 μm width with line lengths of 2.5 mm to 7.5 mm and line widths of 2 μm to 6 μm for transmission lines from 2 mm to 60 mm in length. A variety of line widths and spaces from 0.8 μm to 3 μm and different signal to ground structures showed that open-eye diagrams could be obtained for frequencies from 3 GHz to 8.5 GHz where the signal delay was measured from under 25 ps to 95 ps and far-end cross-talk noise was measured to be from 1.2 % to 35 %. Microbump

interconnection characterization showed direct current electrical resistance under 18 mΩ for 25 μm diameter solder interconnects between surface pads on silicon layers. Signal integrity and chip-to-chip I/O link characterization measurements are also important in order to increase bandwidth between the die in a die stack or between the die on a silicon package. I/O driver circuits can be reduced in size and reduced in power for short-reach communications.

Interconnection Material, Structure and Processes

Traditional off-chip interconnection has used wirebonding or area array flip chip solder bonding to provide interconnection to a package. For limited I/O wirebond applications, aluminum or gold wirebonds have often used up to four perimeter rows of interconnection with a bond pad pitch down to about 30 μm and total number of connections per die up to about 800 input/output (I/O). Area array off-chip interconnections such as with lead tin solder or more recently Pb-free solder have provided I/O pads at a pitch down to 150 μm where total I/O per die have been to about 10 000 I/O. The wirebond or solder interconnections have provided not only power and signal interconnections but have accommodated many product form factors such as wirebonded die stacking, organic and ceramic packages assemblies at high yield, wafer test compatibility and, where needed, use of overmolds and underfills to improve interconnection reliability against product specifications.

For emerging 3D die stacking and 3D silicon packaging, higher density interconnection densities are desired and possible for this new class of applications. In these applications, fine-pitch interconnection may be necessary for high bandwidth and low latency in either a 3D die stack or 3D package. These TSV and interconnects need to accommodate power delivery and distribution, electrical signal transmission, thermal transmission, mechanical integrity and reliability while also achieving 3D product form factors with a high assembly yield to meet product cost objectives. In many applications, use of the wafer test for known good die (KGD) and creation of known good die stacks will be needed to serve the marketplace. In applications using wafer-to-wafer bonding processes, a small-size die with a high wafer bonding yield is needed. Some products may leverage design redundancy or appropriate repair techniques to ensure good manufacturing yields.

Research and development silicon layer interconnect investigations for 3D circuit integration have included SOI structures, thin die stacks using face-to-face or face-to-back structures and silicon-on-silicon package interconnection investigations [21, 29–34, 45, 51, 54–56]. These investigations have included different bonding approaches including oxide-to-oxide bonding, copper-to-copper interconnection and solder interconnects for vertical silicon–silicon interconnection between silicon strata levels or silicon layers. Experiments included a thinned silicon interposer with TSVs placed between one or more die and either a ceramic or organic package or thinned die stacked and assembled on a base package. For these structures, many options can be considered for module assembly. Figure 12.15 shows a comparison of chip-to-chip, chip-to-wafer and wafer-to-wafer assembly approaches [6].

A 3D interconnect using solder can be used for die stacking, fine-pitch interconnects from die or die stacks to silicon packages and within 3D modules to ceramic, glass or laminate packages. Fine-pitch solder interconnects have used sequential die stack and parallel die stack assembly processes. Similarly, die and die stacks can be assembled to

Interconnection metallurgies, process & chip stacking

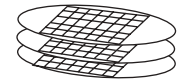
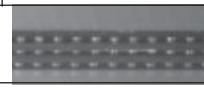
	Chip to chip	Chip to wafer	Wafer to wafer
			
Pro	Flexible, use of KGD	Flexible, use of KGD	Volume Mfg
Con	Handling and bonding	Handling and bonding	Overall yield, same chip size
Die or wafer thickness	< 4 µm to > 150 µm	< 4 µm to > 150 µm	< 4 µm to > 150 µm
Bonding technology	Solder Metal to Metal Adhesive	Solder Metal to Metal Adhesive	Solder or Metal Oxide bonding Adhesive
Demonstrations			

Figure 12.15 *3D assembly approach comparison including chip-to-chip, chip-to-wafer and wafer-to-wafer integration* [6]

silicon, laminate, ceramic or glass substrates or other base substrates. For both stacked die with TSVs and fine pitch interconnections and 3D integrated packages TSVs and fine-pitch interconnects, coplanarity of the thinned silicon and contamination control are important to achieve high yield. The solder, interconnect metallurgy, pad structure and associated process methodology for assembly and adhesive joining need to be optimized for a wide variety of 3D form factors. As the size and pitch of the electrical interconnect are reduced, alignment, bonding coplanarity, contamination control, mechanical integrity, process handling and adhesive enhancement become more challenging. Adhesive approaches such as capillary underfill, vacuum underfill and no-flow underfill have been investigated. An additional challenge for fine-pitch 3D assembly adhesive interconnect materials can be enhanced thermal conductivity adhesives to support higher thermal conductivity to aid in head removal from higher power density integrated 3D structures.

Test vehicle demonstrations have included 200 µm pitch with die-to-die stack assemblies with approximately 9000 I/O per layer and multiple die on a silicon package again with approximately 200 µm pitch and about 8000 I/O per die for a total of 32 000 I/O per layer. Figure 12.10 (a) shows the stacked die and Figure 12.11 (a) shows an example of the assembled module. In each of these demonstration test vehicles, 100 % assembly yields were demonstrated. Similarly for fine-pitch die stack test vehicles with a 50 µm pitch solder interconnection, 100 % assembly yields have been demonstrated for a range in die sizes and total I/O interconnection including approximately 2000, 5000, 10 000, 42 000 and 80 000 connections per layer. In these studies, either 97-3 Pb–Sn solder, 37-63 Pb–Sn eutectic solder or high Sn, lead-free solders were used for evaluations [51, 54–56, 64]. The 25 µm diameter solder uC-4 was formed using either plating processes or injection molded solder. Die assembly test vehicle demonstrations such as these permit assembly process learning to compare process options, study interconnection metallurgies, define

process specifications, support assembly characterization including yield statistics, alignment and physical characterization, electrical parametric characterization, thermal characterization and reliability characterization.

A 3D interconnect for a die stack assembly can also use alternate interconnection approaches such as use of intermetallic compounds or transient liquid phase sintering, copper-to-copper bonding, anisotropic conductive adhesive bonding or alternate approaches, as have been reported previously [24, 25, 29, 52, 53].

A 3D die-to-wafer assembly has been reported as a means to increase productivity [59]. In this assembly approach, known good die can be placed on to known good die sites using rapid pick-and-place tools. Following die pick and place for all good die sites on the wafer, a single-step attachment can join all die to their corresponding die on the wafer with one process. This may be using solder or copper-to-copper bonding or an alternate bonding approach. This approach can also be continued to create multihigh die stacks. An alternate approach to the die-to-wafer assembly is either a die-to-die assembly or die-to-wafer bonding; die can be pre-tested to help assure a high yield for two or more die in the die stack. In addition, the die may be the same size or may vary in size. For thinned die, care must be taken in handling the die to avoid edge damage and breakage. Also for fine-pitch silicon interconnections, a seal band or underfill adhesive may be used to reduce the potential for joint degradation during use due to corrosion or fatigue.

3D wafer-to-wafer bonding can utilize oxide-to-oxide bonding, adhesive bonding, metal-to-metal bonding or hybrid bonding such as combined metal bonding and oxide bonding in one joining process. Wafer-to-wafer permanent bonding can create high-density interconnection using small-diameter TSVs [7, 21, 30, 32, 35]. Wafer-to-wafer bonding and vertical interconnection of circuits includes wafer-to-wafer alignment, wafer bonding, wafer thinning and vertical interconnect formation. Alignment and bonding technical results for the interconnections between silicon levels have been reported with dimensions as small as approximately 0.14 µm diameter, 1.6 µm height, 0.4 µm pitch and density of interconnections of $10^8/cm^2$ [21, 30, 32]. Application requirements along with process integration maturity will expand over time and be expected to support interconnection densities such as $10^8/cm^2$ using wafer-to-wafer bonding for products. For 200 mm and 300 mm wafers, similar to wafer processing, wafer stacking processes will need to be robust to support millions of interconnections between each silicon layer. Wafer-to-wafer bonding and vertical interconnection still have challenges to achieve high yields. Wafer-to-wafer bonding challenges include wafer alignment, coplanarity, permanent bonding and high-yielding TSV or vertical via formation. Design redundancy, integrated repair and/or sparing may aid in the adoption and yield of 3D stacked structures using wafer-to-wafer bonding.

Wafer Level Test, Known Good Die and Reliability Testing

Known good die (KGD) can be identified from pre-testing die with a wafer level test. Statistical sampling may help reduce the need for a 100 % test. The creation of known good die stacks beginning with KGD can substantially improve the total yield. Understanding defect causes and putting in place corrections can improve yields. Redundant interconnections in some applications may aid die stack yields. To demonstrate a path forward for ‘known good die’ and ‘known good die stacks’ with fine pitch interconnections, a wafer

level test using a built-in self test (BIST) and existing probe technology has been demonstrated. Extensions to fine-pitch probes has begun but will drive learning in probe tips, wafer test and manufacturability in the future. Module level testing can complement the wafer level test to support known good die stacks and for burn-in [7].

Reliability testing for TSVs, fine-pitch interconnections, stacked die and 3D integrated modules has continued to be studied through the use of demonstration test vehicles. For example, stacked die advancing technology nodes, integrated TSVs and interconnects have been designed, fabricated, assembled and put into reliability tests. Test vehicles can range from simple electrical continuity tests with TSVs and uC-4 to active circuit test vehicles. Prior characterization using TSVs and solder microbumps at 50 μm pitch have shown that these robust structures can support reliability stress including electromigration results of over 2000 hours for 50 mA to 100 mA current at 150 °C, deep thermal cycle results of over 1500 to 25 000 cycles of −55 °C to +125 °C, temperature–humidity bias of over 1000 hours for 85°C, 85% relative humidity and 1.5 V, and over 2000 hours of high temperature storage at 150 °C [51, 54, 56, 61]. Results indicate that TSVs and fine-pitch interconnections can be fabricated and meet typical product reliability stress requirements. New test structures and form factors for TSV, interconnect structure, die stacks and 3D integrated packaging and modules continue to be evaluated for semiconductor active and passive applications using copper and tungsten TSVs and with numerous interconnect metallurgies and structures. These further studies of multichip and die stack test structures with increased interconnection densities between 10^3/cm^2 and 10^8/cm^2 are at various stages of design, build and characterization. They will permit ongoing experiments and data to be investigated including design rules, process, bonding, test structures/methodology and characterization. These ongoing investigations include die-to-die, die-to-wafer and wafer-to-wafer processing approaches to 3D applications. Assessments provide data on interconnection density, materials, structures and processes to help optimize applications and compatibility with manufacturing. Data collected can provide guidance to meet application reliability objectives for TSV, vertical interconnect and in a variety of 3D integrated package and module form factors. These tests, reliability studies and characterization support system level decisions for product applications.

3D Modeling

Many models and simulation tools exist for 2D applications and many now also exist using extensions of 2D tools for 3D applications. For example, within a chip design, 3D modeling tools exist that permit electrical design, electrical transmission modeling and simulations. However, for 3D structures with multiple levels of silicon strata or layers and module form factors, full 3D designs, models and simulations can require vertical layer identification, and with the expansion of 3D interconnections, the existing tool capacities have needed to be expanded to support the magnitude of modeling and simulations needed for 3D applications. Tools exist for mechanical and thermal modeling in 3D structures but tools for performance simulations, full design and comparison are not broadly available. Combination tools supporting mechanical, thermal and electrical assessments generally are not available at this time. However, extensions from existing tools have permitted great learning for design, modeling and simulations. In time, further

release of next generations of 3D design and modeling tools will be able to improve 3D comparisons, 3D electrical transmission models and simulations tools for die stacks, 3D packaging and 3D module structures. System level evaluations to understand performance modeling, power efficiency, cost and form factor trade-offs is more challenging but can be achieved with data analysis. As 3D manufacturing and industry adoption take place, greater experience and data on 3D processes, yield understanding and cost models will help to optimize 3D designs and structures for future applications. Examples of mechanical and thermal modeling comparing 3D die stacks and 3D packaging was summarized by Sri-Jayantha *et al*. [65].

Design, architecture and performance modeling provide a great opportunity to improve system solutions using 3D structures. Examples of architecture considerations and performance benefits for 3D have been reported [1, 10, 50]. Examples of electrical transmission measurements, modeling and simulation has been reported by Patel and Dickson *et al*., respectively [62, 63]. Mechanical models have been reported for TSV, 3D interconnect using small solder bumps and thermomechanical evaluations of 3D structures [7, 65]. Stress and deformation have been evaluated at each stage of the TSV manufacturing process at the temperature for each operation. Elastic properties were characterized by the elastic modulus and Poisson ratio [31]. For Cu TSVs, the yield strength of the material is likely to be exceeded and the nonlinear properties need to be included. A stress–strain curve can be incorporated but simple yield stress is usually sufficient. The range of process temperatures drove inclusion of the coefficient of thermal expansion, as discussed above. In addition, shear stresses needed to be evaluated at material interfaces and compared with the adhesion strengths between materials. The highest stress conditions are generally seen at the TSV to adjacent wiring and dielectric layers. Understanding mechanical aspects of via structure and process flow can be leveraged to minimize the maximum vertical stress for use in silicon-based technology. From an understanding of structure and stresses, such as for TSV in thinned stacked die or die on 3D silicon packages, the electrical and mechanical design specifications for the product application can be optimized and successfully applied.

For silicon interconnect modeling, initial development of a model to understand stress and strain levels in a solder μ-C4 began with the use of a macro–micro model [7, 65]. In the finite element model, the macro characteristics of the structure could be considered while still providing micro-level detailed understanding for the high volume of small features that were needed to understand mechanical characteristics. For example, the model would address the large quantity of micro joints used in the structure while being able to begin to understand actual stress and strain on an individual solder μ-C4 level. *X* and *Y* displacements could show the relative pressure loads in the macro model and distributed the stress to the solder interconnections for relative comparison. The macro and micro mechanical modeling of stress in the solder μ-C4 can then be evaluated across the various BLM and solder interconnections or compared to alternative fine-pitch interconnections such as with copper-to-copper bonding or when using oxide-to-oxide bonding for fine-pitch interconnections.

3D power delivery, distribution and cooling models and demonstration vehicles are under further investigation and should lead to improved understanding and application of products in time. Similarly, 3D knowledge for wafer build, assembly, yield and cost models is also leading to improved understanding over time.

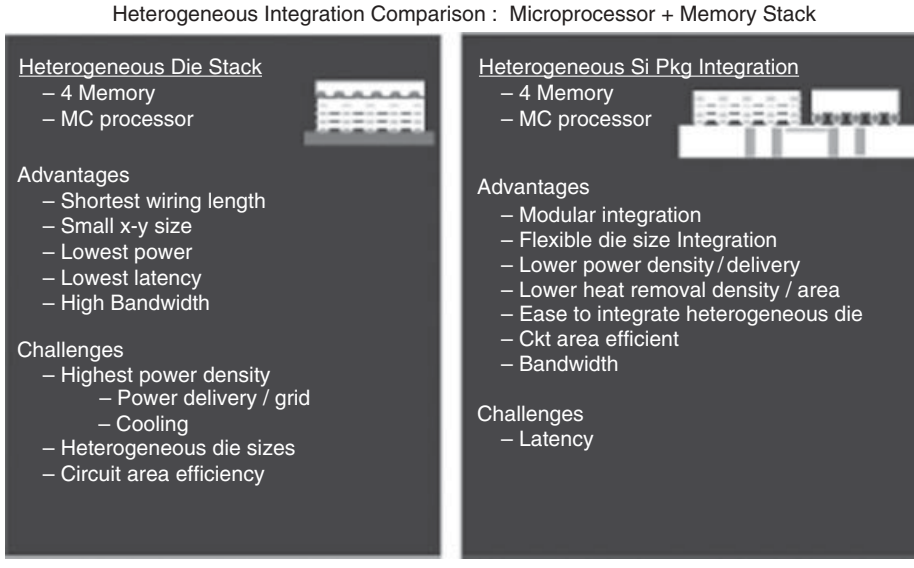


Figure 12.16 *Design form factor comparison of a 3D die stack and 3D silicon package interconnection*

12.2.5 Trade-offs in Application Design and Product Applications

Leverage of TSV, thinned silicon and vertical silicon interconnects for system integration permits a wide range of products covering varied interconnection densities. For example, simple wireless die with < 10 TSVs to applications for high-performance computing that may require 10^8 TSVs and vertical interconnects between silicon circuit layers may each benefit from emerging 3D technology.

Another consideration toward 3D integration is the form factor in which the product is designed. Figure 12.16 shows a schematic with form factor options of integration that could be considered as part of a 3D system application [44]. One option gains the highest bandwidth for silicon interconnection by means of a vertical stack of silicon die and the other high bandwidth silicon interconnection by means of a silicon package circuit that combines all heterogeneous silicon circuit layers into one die stack. In the die stack option, advantages can include the shortest wire length between heterogeneous die and an opportunity to reduce power for signal communications due to reduced capacitance and resistance in the wire lengths and sizes. Wire lengths for die to die in a die stack may be tens of micrometers. However, the design also has challenges including delivery of power to each level within the stack, the circuit density reduction due to a TSV area takeaway from each silicon layer to support vertical power delivery and signal communications. In addition, for a vertical stack, removing heat from the stack can also lead to power density or operational performance limits depending on the type of die being stacked. Thus this may be the best option provided the design can support power delivery, heat removal and have a minimal loss of circuits to support vertical interconnects. Another option for comparison could be a combination of die stacks with interconnection on a high bandwidth,

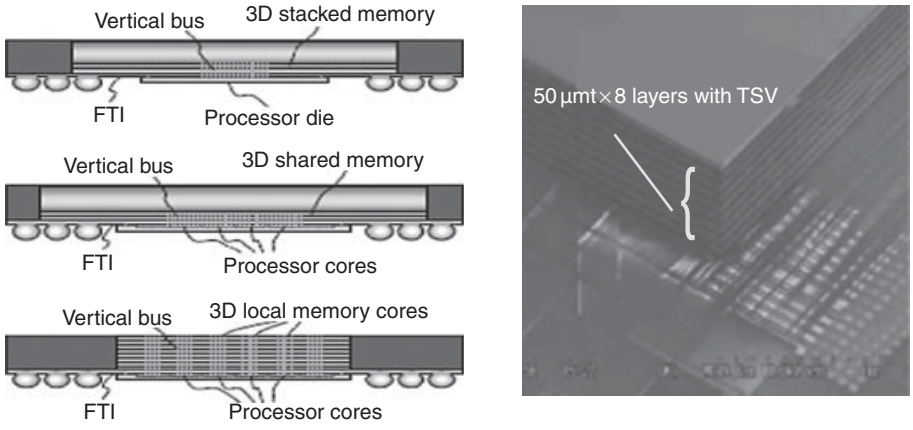


Figure 12.17 *Multihigh memory die stack from Elpida using a TSV and silicon interconnect* [27, 67]

3D silicon package. In this example, total power delivery to multiple die stacks can be spread over a larger area while maintaining high bandwidth between die stacks. This can help to reduce current flow per area, reduce power density and aid in heat removal as cooling can be across multiple die stacks. However, in this option, increased wire length leads to an increase in latency. A short wire length can be achieved at very high interconnect density for adjacent die stacks on a silicon package. Wire lengths for die-to-die or die-to-die stack interconnection across a silicon package or a glass package can be supported from a few millimeters length to tens of millimeters. Limitations in total length at high bandwidths are limited to power for interconnect at distances in excess of perhaps about 100 mm unless large cross-sectional wires are used, in which case the wire length could be increased.

Press announcements and technical publications have begun to show both first applications of products using TSV and 3D silicon vertical interconnects including image sensors and power amplifiers where these product have utilized low-density vertical interconnects [37, 38, 50, 66]. More recently, two new product application form factors have been announced. The use of a 3D silicon package with TSVs to support multiple die with wiring interconnection has also been announced by Xilinx and Semtech, respectively [37, 38, 40, 41]. In addition, Elpida, Samsung and Micron have had technical publications and/or press announcements about wide I/O bandwidth, stacked die memory applications that utilize TSVs and vertical silicon stacked die [27, 37, 38, 42, 43]. Figure 12.17 shows an example of a memory chip stack from Elpida [27, 67].

Wider industry adoption and acceleration of product application introduction might be expected as wide I/O memory die stacks begin to enter the marketplace during the next two years. Design and enablement tools are available for some applications but more complex products would benefit from expanded capability design tools that can better support 3D applications. Equipment for 3D technology is also available but next generations of 3D tools will need to continue to emerge to support high-productivity manufacturing. Examples of tools that need improvement include bonding and debonding tools, 3D

assembly tools for die stacks, wafer-to-wafer permanent bonding tools with high throughput and fine-pitch test probes and associated wafer testbeds. Another area that would help accelerate industry adoption of more complex 3D heterogeneous die, die stacks and integrated 3D packaged solutions is standards for bonded wafer pairs, standards for I/O pitch and floor plans, standards for chip-to-chip communication at low power and technical products that utilize multiple design shops, multiple foundries, multiple assemblers and test companies. Industry growth for 3D products is expected to continue as design, manufacturing and product demonstrations reduce barriers to new 3D product adoption. Like many new technologies, 3D is expected to provide advantages and disadvantages and therefore is not expected to displace traditional technology for all applications but rather will grow into markets where it has a competitive advantage. Markets that can take advantage of high bandwidth for performance advantages, wide I/O memory access and lower power will be likely to adopt the 3D technology.

Beyond traditional applications of 3D microelectronics, application expectations for 3D can be expected to be far reaching with time. Examples might include portable electronics such as cell phones, portable medical products and portable sensors. With the reduced power consumption, portable products may benefit from enhanced battery life, not to mention significantly more compact products with scaling functional capabilities. Additional applications could include military, information technology, communications, automotive and space applications. For computing applications, high bandwidth memory chip stacks for heterogeneous integration to microprocessors and field programmable gate arrays (FPGAs) could provide reduced power, system performance scaling and smaller products. In addition, it is likely that new applications and products will emerge between advancements in these microelectronics and nanoelectronics technologies and emerging biotechnology as well as other nano emerging technologies. It seems clear that the industry is just beginning to consider new applications and products that may take advantage of 3D silicon integration.

12.2.6 Summary

Emerging three-dimensional (3D) silicon integration using through-silicon vias (TSVs) and silicon interconnections has the potential to become used in a broad range of applications. Technology advancements and implementation using 200 mm and 300 mm tools is growing in the industry, including first-generation image sensors and power amplifiers to second-generation 3D silicon package integration modules and 3D wide I/O stacked memory die using TSV and fine-pitch interconnect. Further technology advancements toward heterogeneous die stacks and 3D integrated packaging and modules are expected to continue to advance for future applications. 3D technical and business challenges still remain in the industry but continued advancements in design, design tools, 3D manufacturing and manufacturing tools, 3D standards and industry compatibility will lead to more product applications. Future products are expected to take advantage of new 3D design, fabrication, assembly and characterization demonstrations. Heterogeneous integration of 3D products with TSVs and fine-pitch interconnect will benefit from collaboration between research, development, manufacturing, equipment suppliers, materials suppliers and standards defining organizations.

Acknowledgments

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The author wishes to acknowledge support from the 3D research team including Paul Andry, Bing Dang, Chris Jahnes, Yang Liu, Joana Maria, Robert Polastre, Cornelia Tsang, Bucknell Webb and Stephen Wright. In addition, the author wishes to thank the IBM Research – Materials Research Laboratory, Central Services Organization and collaboration with System and Technology Group.

12.3 Advanced Microscopy Techniques for 3D Interconnect Characterization

Lay Wai Kong, Sven Niese, Alain Diebold and Ehrenfried Zschech

The rapid development of the 3D IC stacking technology is driving the need for advances in microscopy methods. Overlay measurements after wafer bonding, defect detection and void inspection after copper plating are challenging due to the need to image through silicon and inside copper. Microscopy techniques for which silicon is not opaque, such as scanning acoustic microscopy (SAM) and confocal infrared (IR) microscopy are capable of inspecting the interface between bonded wafer pairs, while high-resolution X-ray computed tomography (XCT) is used to detect voids in metal TSVs. This chapter covers several analytical techniques for process and quality control. The current status of SAM, IR microscopy and nano-XCT, complemented by techniques for microstructure characterization, is discussed in terms of their application to process metrology and failure analysis for 3D IC integration.

12.3.1 Scanning Acoustic Microscopy

Scanning acoustic microscopy (SAM) provides the ability to image sub-surface features for bonded wafers and packaged integrated circuits. In SAM, sound waves propagate through elastic media reflecting from regions where the materials properties change. The principles of acoustic microscopy were thoroughly reviewed in Briggs and Kolosov's book [68]. Below, we describe only the basics of acoustic microscopy to aid the discussion of the application of SAM to interconnect materials based on Briggs and Kolosov [68].

Principles of Scanning Acoustic Microscopy

A scanning acoustic microscope visualizes changes in the reflected intensity of ultrasonic waves. The intensity of the reflected waves changes across a sample as local changes in the acoustic impedance, Z, occur at interfaces between materials. The acoustic impedance is

Table 12.1 *Density, acoustic wave velocity and acoustic impedance of several materials* [69]

Material	Density (g/cm^3)	Longitudinal Wave Velocity (m/s)	Acoustic Impedance ($\times 10^6$ kg/m^{2}s)
Water (20 °C)	1.00	1483	1.48
Alcohol (20 °C)	0.79	1163	0.92
Air (20 °C)	0.00	344	0.00
Silicon	2.33	8600	20.04
Gold	19.3	3240	62.53
Copper	8.90	4700	41.83
Aluminium	2.70	6260	16.90
Epoxy Resin	1.20	2600	3.12
Resin (IC Pkg)	1.72	3930	6.76
Glass	2.7	5570	15.04

the product of the density and the speed of sound in the medium, as given in the following equation:

$$Z = \rho V \tag{12.1}$$

where Z is the acoustic impedance, ρ is the density and V is the acoustic wave velocity.

Since the elastic properties of materials of different composition are different, SAM is an important method of imaging many structures of interest to the semiconductor industry. Another useful relationship is that between the acoustic wave velocity as well as the elastic constant and the density of a material, as indicated by

$$V = (C/\rho)^{1/2} \tag{12.2}$$

The elastic constant C can be calculated from the elastic properties of the material for a particular mode, which yields different speeds of sound, e.g. for transversal and longitudinal waves.

In Table 12.1, density, acoustic wave velocity and acoustic impedance of a variety of materials are listed. The mismatches between the acoustic impedance of air and most other materials results in reflection of the wave with little or no transmission. Therefore, samples are immersed in water, which is further described below. Water is the coupling medium that facilitates the transmission of ultrasonic energy from the transducer into the specimen.

In SAM, the transducer both transmits and detects the reflected ultrasonic waves. The SAM used in many of the studies illustrated in this chapter is equipped with a piezoelectric transducer that transmits and receives longitudinal waves. A high-voltage pulse is used to vibrate the transducer and to generate a plane wave. The plane wave is focused by a lens and then propagates through the coupling medium to the sample. Part of the wave is reflected back to the transducer and part of it transmits through the sample. Inside the sample, the wave is also partially reflected from the structure inside the sample. When the wave reaches the surface of any solid specimen, part of the wave remains as a longitudinal wave and part of the wave propagates as a transverse wave at a typical angle through the specimen.

Figure 12.18 shows a sample immerged in a coupling medium like water with a transducer generating an ultrasound toward the specimen, the initial ultrasound wave. The longitudinal wave from the transducer propagates through the water to the sample. At the boundary between the water and the sample, part of the initial ultrasound wave reflects

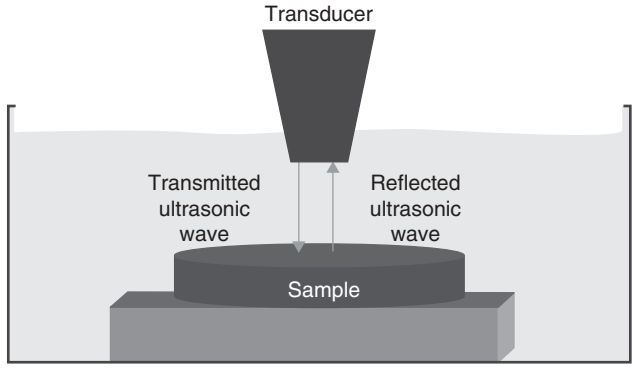

Figure 12.18 *Basic setup for scanning acoustic microscopy*

and part transmits. The amount of transmission and reflectance is given by the acoustic impedance of water, Z_1 and sample, Z_2. The fraction of this initial wave intensity that is reflected can be calculated with the following equation assuming normal incidence [68]

$$R = \frac{(Z_2 - Z_1)}{(Z_2 + Z_1)} \tag{12.3}$$

The term of Equation (12.3) is known as a reflection coefficient. The transmission coefficient T is $1 - R$ or as an expression of the impedances

$$T = \frac{2(Z_1)}{(Z_2 + Z_1)} \tag{12.4}$$

Resolution

The spatial resolution, W, of an acoustic microscope is based on the Rayleigh criterion and is given by [68]

$$W = \frac{0.51\lambda_0}{\text{NA}} \tag{12.5}$$

where NA is the numerical aperture and the wavelength, λ_0, is given by V_0/f (V_0 is the velocity of sound in that medium and f is the freqency). The resolution is proportional to the wavelength of the ultrasound, which depends on the frequency and the velocity of sound in the material. Equation (12.5) implies that the only limit on resolution is the frequency of the wave. Unfortunately, the attenuation of ultrasonic waves is proportional to the square of the frequency providing practical limits to resolution for a given minimum penetration depth. This is one motivation for thinning samples before measurement, and vice versa; the attenuation is the key to determine the most useful high frequency for imaging the object. The attenuation per unit distance is stated by

$$A = \alpha_0 f^2 \tag{12.6}$$

Here, A is the attenuation, α_0 is the attenuation coefficient of the material and f is the frequency of sound in the material.

The attenuation is caused by the combination of scattering and absorption. Scattering causes a change in the direction of propagation of the ultrasonic wave and absorption occurs if the ultrasonic wave is converted into other forms of energy.

The acoustic wave propagates through a lens before entering the coupling medium. Due to the relatively small amount of attenuation, single-crystal sapphire is an excellent material for an acoustic lens. Another factor is the attenuation coefficient of the coupling medium. Water has excellent coupling characteristics and, therefore, it is preferred over other mediums like air and oil.

When the pulse length and the time between pulses (t_0) are fixed, the minimum focal length is given by [68]

$$\mathrm{FL} = \frac{V_0 t_0}{2} \tag{12.7}$$

where FL is the focal length, V_0 is the velocity of the ultrasonic wave and t_0 is the time interval between echoes. From Equation (12.5), it is known that the attenuation is proportional to the square of the frequency [68]. An acceptable attenuation, α_{acc}, is needed to determine the maximum frequency that can be used. The frequency limit due to α_{acc} is given by

$$f \leq \sqrt{\frac{\alpha_{acc}}{2\alpha_0 \mathrm{FL}}} \tag{12.8}$$

where f is the frequency of the ultrasonic wave, α_{acc} is the acceptable attenuation and α_0 is the attenuation coefficient. This maximum frequency is then defined by the shortest wavelength, $\lambda_{\min}$, that can be used. This is stated by

$$\lambda_{\min} \equiv \frac{V_0}{f} = \sqrt{\frac{V_0^3 \alpha_0 t_0}{\alpha_{acc}}} \tag{12.9}$$

This allows us to define a resolution coefficient R_c:

$$R_c \equiv \sqrt{V_0^3 \alpha_0} \tag{12.10}$$

The resolution coefficient is proportional to the shortest wavelength that can be used with the given α_{acc} and t_0. The resolution coefficient for water is ~ 0.8 and for air is ~ 80 [68].

Applications of Scanning Acoustic Microscopy in Microelectronics

SAM characterization of bonded wafer pairs has been proven to be very useful during process development. SAM images of patterned sections of the wafer are not readily comparable to scanning electron microscopy (SEM) images of patterned circuit features, as shown in Figure 12.19 [70]. Several bonding materials have been used to bond wafer pairs. The so-called dendritic structure was observed in wafer pairs during development of the curing step for the bonding material benzocyclobutene (BCB). Figure 12.20 shows defect structures observed for unpatterned wafers bonded using BCB. The combination of SAM and IR microscopy has been proven to be a great aid during process development.

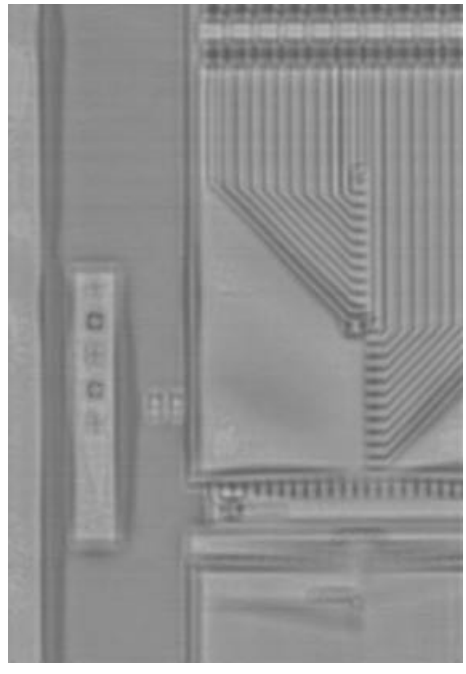

Figure 12.19 *SAM image of metal–metal alignment marks and features inside a bonded wafer pair composed of two 775 μm wafers. Figure is courtesy of SEMATECH*

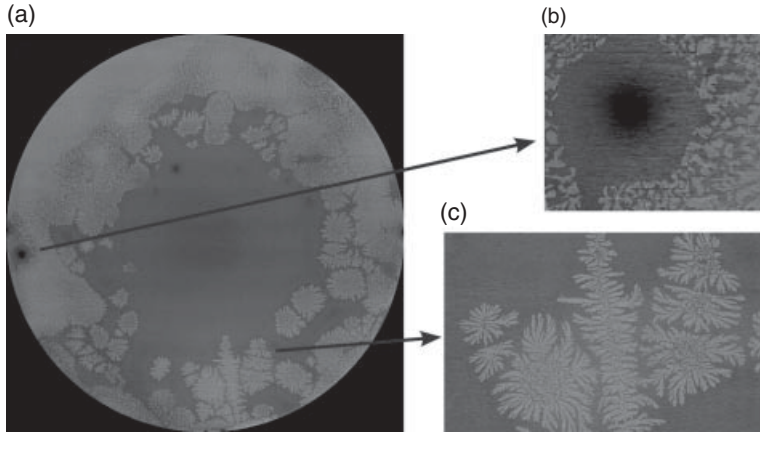

Figure 12.20 *(a) SAM image of a wafer pair bonded using BCB. (b) An area where the wafers touch due to missing BCB. (c) Dendritic structures that grow during solidification of the BCB if curing conditions are not optimized. Figure is courtesy of SEMATECH* [70]

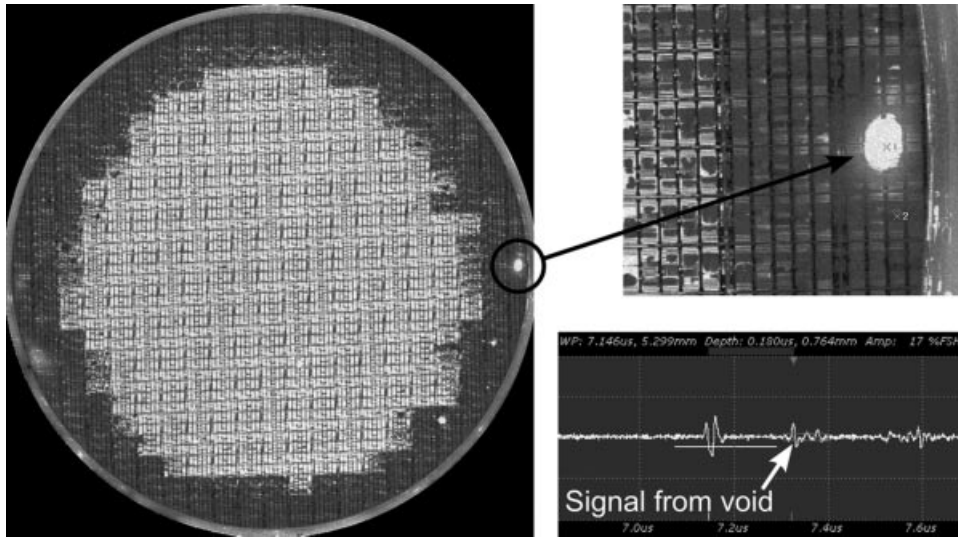

Figure 12.21 *SAM image of a bonded pair of patterned wafers (110 MHz, 1.45 h scan time, unbonded area shown in bright). Figure is courtesy of SEMATECH* [70]

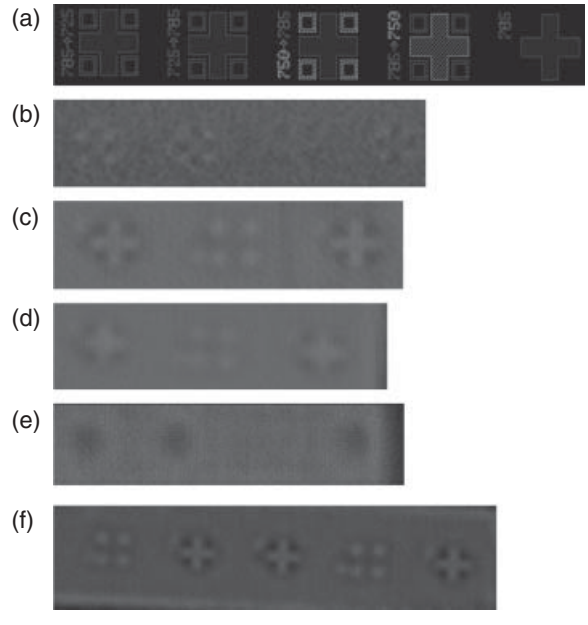

Figure 12.22 *Scanning acoustic microscopy image of overlay target structures: (a) gds. of alignment structures; (b) to (e) bonded wafer scanned with a 230 MHz transducer. SAM images show the alignment structures from 100 μm (b), 200 μm (c), 300 μm (d) and 400 μm (e) top wafer respectively. (f) Better resolution on alignment structures using 300 μm top wafer scanned with a 300 MHz transducer. All figures are courtesy of SEMATECH*

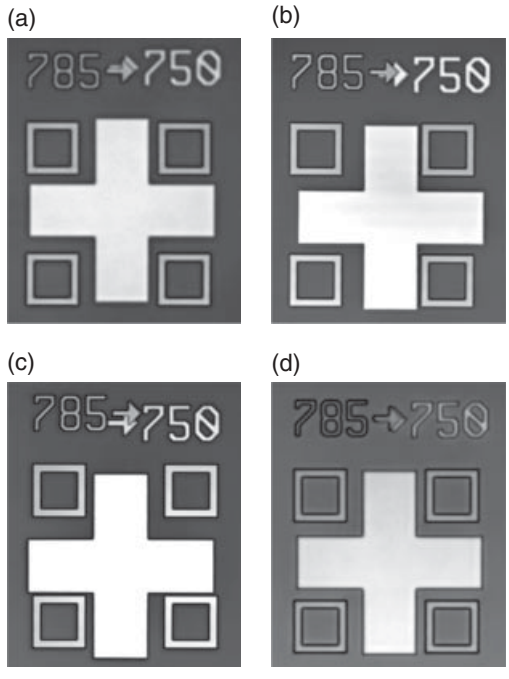

Figure 12.23 *IR microscopy images of overlay target structure: (a) alignment structure on a bonded top wafer with 100 μm thickness; (b) alignment structure on a bonded top wafer with 300 μm thickness; (c) alignment structure on a bonded top wafer with 400 μm thickness; (d) alignment structure on a bonded wafer with 775 μm thickness. All figures are courtesy of SEMATECH*

Figure 12.21 shows the presence of an area where two patterned wafers touch. Figure 12.22 clearly shows that IR microscopy is the preferred method for overlay metrology than acoustic microscopy.

12.3.2 IR Microscopy

Microscopy of 3D structures is challenged by the opaque nature of silicon for most energies. However, since silicon is transparent at infrared wavelengths from about 1.3 μm to 8 μm, it is possible to examine silicon dies or wafers, and particularly bonded wafers, with IR techniques. Infrared (IR) microscopy is a nondestructive microscopy technique that is used in 3D IC manufacturing to image sub-surface features at the interface of bonded wafers [71]. This practical solution enables a variety of through-silicon metrology, including overlay alignment, review of pre-existing defects from each wafer at the bond interface and detection of new defects created during the bonding process. The use of IR microscopy to measure wafer pair overlay and to study the interface defectivity of bonded wafer pairs is demonstrated in Reference [71].

IR microscopy measurements of overlay target structures at the interface of bonded wafers are demonstrated for bonded top wafers with wafer thicknesses varying from 100 μm to 775 μm in Figures 12.23 (a) to (d).

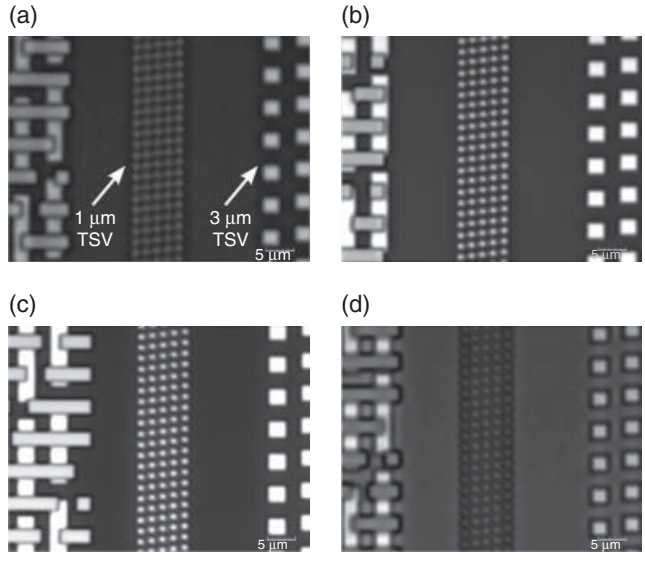

Figure 12.24 *(a) 1 µm and 3 µm TSVs in a bonded top wafer with 100 µm thickness; (b) 1 µm and 3 µm TSVs in a bonded top wafer with 300 µm thickness; (c) 1 µm and 3 µm TSVs in a bonded top wafer with 400 µm thickness; d) 1 µm and 3 µm TSV in a bonded top wafer with 775 µm thickness. All figures are courtesy of SEMATECH*

The effect of top wafer thickness on image resolution is demonstrated using TSV SEM bar test structures. We show images of a structure consisting of 1 µm and 3 µm TSVs in Figure 12.24 under an objective lens with specified working distance, NA, and magnification. Consistent with the alignment structure IR images, the bonded wafers with 400 µm top wafer show the sharpest image with the best contrast. These micrographs explain that the 400 µm top wafer has more in-focus reflected signal passing through the pinhole impinging on the detector. Therefore, the intensity using a 400 µm top wafer is higher for bonded wafers with other thickness values. This implies that matching the right IR objective lens to the thickness of the top wafer is important for obtaining the best resolution during inspection.

12.3.3 Transmission X-ray Microscopy and Tomography

High-resolution X-ray imaging with a spatial resolution as good as 10 nm on synchrotron-based and 30 nm for lab-based systems offers unique capabilities for process development and failure analysis in the semiconductor industry. Buried metal interconnect structures like copper on-chip interconnects and through-silicon vias (TSVs) for 3D IC integration can be studied with excellent element-specific contrast. Transmission X-ray microscopy (TXM) is done over a wide range of X-ray energies at synchrotron radiation sources. The selection of the X-ray energy is often a matter of convenience. However, selecting a useful energy range can improve resolution, contrast and penetration depth. X-ray tubes provide fixed energies like Cu-K_α radiation at 8.0 keV (characteristic X-rays) with an adequate intensity to limit the flexibility but enable X-ray microscopy to be used in the lab.

Furthermore, it is possible to reconstruct a three-dimensional dataset of the sample, the tomogram, based on the acquisition of a number of radiographs (projections), which is well known from nondestructive testing of macroscopic objects using microfocus X-ray tubes or from medical applications. The resulting radiographs usually show the transmissivity of the X-rays; i.e. regions with a high transmission appear bright and regions with a high absorption appear dark. The tomogram and hence the determined virtual cross-sections represent the distribution of the linear absorption coefficient in the sample. Features with a high absorption, e.g. copper in silicon, appear bright.

Principles and Implementation of TXM

This section provides a short review of the physical principles of TXM as well as basic information about synchrotron-based and lab-based microscopes.

Physical Principles. The refractive index of most materials is close to 1 for X-rays; i.e. it is hardly possible to use refractive lenses for imaging as in visible light microscopy. Focusing X-rays for high-resolution imaging requires different X-ray optics as on a Fresnel zone plate. The zone plate consists of a set of concentric rings that decrease in width and increase in radius toward the outermost zone ring, which has the smallest width. The resolution of the image is approximately determined by the outermost zone width and is expressed by

$$\sigma = 1.22\,R_n \tag{12.11}$$

where σ is the resolution and R_n is the outermost zone width. The resolution of the image is limited by how small the zone widths can be made as this prevails the Abbe criteria in the case of X-ray imaging [72].

Transmission X-ray microscopy is based on detecting the intensity of transmitted X-rays. The capability of the X-rays to transmit through the material is characterized by the linear attenuation coefficient. A material with a small attenuation coefficient is relatively transparent to X-rays, while a large attenuation coefficient means less transmission for an equal penetrated thickness. This relation can be described by the Beer–Lambert law, given as

$$I = I_0 \exp(-\alpha x) \tag{12.12}$$

The Beer–Lambert law describes the intensity of transmitted X-rays, I, after a beam with an initial intensity, I_0, passes through a material with a thickness, x, and linear attenuation coefficient, α [73]. For X-rays, α only depends on the mass density and the chemical composition, i.e. the present elements, of the sampled region. As the bond energies are usually small compared to the applied photon energies, TXM is not sensitive to chemical bonds. Therefore, the radiographs represent the integrated spatial variation of different elements weighted with the density. The absorption cross-section for a certain element changes drastically at an X-ray absorption edge. As a consequence, the ability to tune the X-ray energy at synchrotron radiation sources can be used to identify certain elements by taking radiographs at energies below and above an absorption edge.

As an X-ray microscope uses Fresnel zone plates that act as lenses to image the object, it is possible to get a Zernike phase contrast as a complementary imaging mode to the absorption contrast described above. For this purpose, a phase ring has to be inserted in the rear focal plane and hollow cone illumination has to be used, e.g. by using a capillary condenser. The non-scattered light gets an additional phase shift of, for example, half a wavelength and interferes with the scattered light of the object that was also shifted in

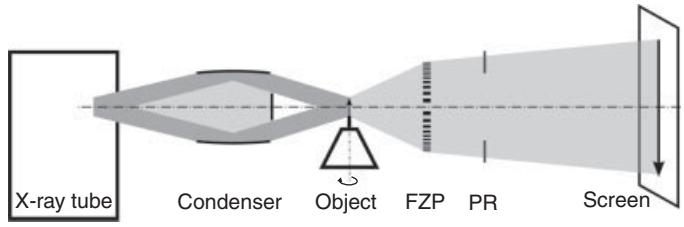

Figure 12.25 *Schematic drawing of the optical path of a lab-based TXM. The focus of the X-ray tube is focused on to the object plane by a capillary condenser. The object is then imaged to the scintillating screen by a Fresnel zone plate (FZP). A phase ring (PR) in the rear focal plane can be inserted to obtain Zernike phase contrast*

phase with respect to the refractive index of the transmitted material. Zernike phase contrast especially exaggerates the contrast in areas with gradients of the refractive index, e.g. at phase boundaries, and is overlaying the absorption contrast.

Besides the possibility to obtain single radiographs of the object, the acquisition of 3D data is desirable. There exist well-known algorithms such as filtered back projection (FBP) and various algebraic reconstruction techniques, which are available to reconstruct the 3D information based on a series of projections of the object that are taken at several angles [74]. Typically, the object has to be rotated by 180 or 360 degrees in certain angle steps. This method is called computed tomography. There is a variety of software available that implements these algorithms and performs the reconstruction of the tomogram, which represents the three-dimensional distribution of the linear attenuation coefficient. The availability of the tomogram enables further analysis like virtual cross-sectioning, pore and phase analysis and 3D visualizations.

Synchrotron-Based X-ray Microscopy. The experimental implementation of X-ray microscopy was driven by synchrotron facilities as they provide considerably higher brightness compared to lab-based sources. Thus, the main focus of TXM is still there. The available photon energy range depends on the specific storage ring, beamline optics and the attached microscope. In general, TXM at synchrotron radiation sources is performed with both soft X-rays at minimum photon energies down to 100 eV and hard X-rays up to 20 keV. TXM with soft X-rays is one step ahead in terms of achievable resolutions [75–78].

Synchrotron-based X-ray microscopy provides the full potential of TXM, i.e. using matching photon energies corresponding to the investigated materials and short acquisition times for time-resolved studies [79].

X-Ray Microscopy in the Laboratory. The development of high power rotating anode X-ray sources as well as efficient condenser optics and zone plates have enabled the use of X-ray microscopy in the lab. The beam path of a typical lab-based X-ray microscope is shown on the right-hand side of Figure 12.25. Anode materials used are, for example, copper or chromium. The X-ray beam is focused on to the object by a capillary condenser. The sample stage provides sample rotation during tomography as well as arbitrary translation. Transmitted light from the sample is then imaged on to a scintillating screen by a Fresnel zone plate and subsequently magnified by a folded visible light microscope to a CCD camera [80].

Such lab-based systems are able to provide both individual radiographs and tomography images, e.g. of multiple TSVs. Therefore, lab-based transmission X-ray microscopy

Table 12.2 *X-ray transmission of several thicknesses of copper and silicon for Cu-K_α radiation*

Material	Density (g/cm³)	Absorption length (µm)	Transmission (%)		
			50 µm	30 µm	5 µm
Silicon	2.33	70.8	49.4	65.5	93.2
Copper	8.96	23.0	10.6	26.0	79.9

represents the technique of choice to localize defects in copper TSV interconnects for 3D IC integration. The penetration depth for Cu-K_α radiation (8.0 keV) is summarized in Table 12.2. However, the acquisition times are significantly longer compared to synchrotron-based TXM. According to the required magnification, image size and noise level, the acquisition of a single radiograph or tomography might take several minutes or several hours to tens of hours, respectively.

Sample Preparation. As discussed in previous sections, the intensity of the transmitted X-rays depends on the penetrated thickness of the material and on the chosen photon energy. The penetration depth of hard X-rays is in the order of several tens of micrometers in the case of most of the typical materials used in microelectronic products. If soft X-rays are used, the penetration depth is reduced to several micrometers. In most cases sample preparation is needed to provide target prepared samples with a feasible remaining thickness of the region of interest.

Samples for TXM with hard X-rays can usually be prepared by common metallographic methods. With respect to the feature of interest either chip thinning by backside grinding, dimpling and polishing or dicing of a lamellae out of the chip are convenient approaches to prepare a sample with a thickness of, for example, 60 µm. Radiographs of such samples can be directly acquired. If three-dimensional information is desired, any approach to obtain tomography data from *flat samples* like limited angle tomography or tilted rotational axis tomography [81] can be applied. If the available penetration depth demands thinner specimens, more advanced sample preparation has to be done. Analogously to the preparation for transmission electron microscopy (TEM), the region of interest can be milled with focused ion beam (FIB) tools to the desired thickness out of a diced lamella [82]. Furthermore, it should be noted that upcoming methods like laser ablation and plasma FIB [83, 84] are promising techniques for sample preparation as they allow removal of large amounts of material in micrometer scale with the required precision.

Applications of X-Ray Microscopy in Microelectronics

The TSV characterization described here has been performed using a lab-based TXM *NanoXCT-100®* from Xradia Inc. as well as the soft X-ray microscope U41-TXM at the BESSY II synchrotron facility. Although the relatively high penetration depth of X-rays allows imaging an entire array of TSVs, some sample preparation is required, as discussed above. Since the region of interest remains intact, X-ray microscopy can be used to study the same sample during a series of process steps (e.g. annealing). If necessary, a subsequent analysis with other methods is possible as well [85].

Table 12.3 *Method comparison for void inspection in TSVs* [86]

	Spatial resolution	Probing depth	Sample preparation	3D imaging
TXM	~50 nm	~60 µm	Minimal, no physical cross-sectioning into TSV	Yes
SEM	~1–10 nm	< 10 nm	Medium, cross-sectioning into TSV	Yes, e.g. 'Slice and FIB'
TEM	~0.1 nm	< 200 nm	Extensive, thinning to < 200 nm by FIB	Yes, limited to lamella thickness

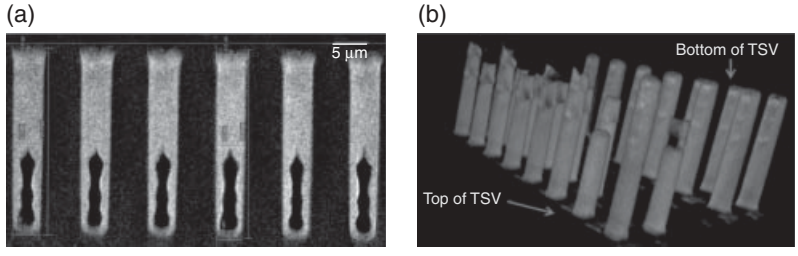

Figure 12.26 *(a) Cross-section of a tomogram of a row of 5 µm TSVs with partially filled vias. (b) 3D visualization of 4 µm (front rows) and 5 µm (rear rows) TSVs. All figures are courtesy of SEMATECH*

Void imaging Using X-ray Microscopy. The methods shown in Table 12.3, TXM, SEM and TEM, have the capability of inspecting copper-filled TSVs for voids. XCT has the advantage that it can characterize voids in an array of TSV structures nondestructively [86]. Although SEM and TEM studies provide a better resolution than TXM, the probing depth is very low and physical cross-sectioning of the TSV is required. SEM-based 3D information can be obtained using the FIB technique. This technique allows imaging of the TSV applying a serial-cut method, and the series of images can be assembled into a 3D tomography image. This process is not only time consuming but it also mills the TSV; i.e. a further analysis of detected features is not possible. For electron tomography in a TEM, the sample has to be thinned to ~100 nm.

Figure 12.26 shows a tomography of two arrays of TSVs with diameters of 4 µm and 5 µm, respectively, and 27 µm of depth, filled using the identical process. The photon energy was 8.0 keV and the field of view 67 µm. Defects observed in these TSVs were incomplete filling at the bottom (4 µm TSVs) and large voids at the bottom (5 µm TSVs).

Figure 12.27 shows cross-sections at identical sample positions of TSVs before and after annealing (225 °C/24 h). It is observed that the shape of the voids is changed and copper is extruded at the top of the TSVs.

Low-Energy Synchrotron-Based TXM Structure Imaging. Low-energy synchrotron radiation (< 2 keV) has a reduced penetration depth of less than 5 µm for silicon wafers with copper TSVs. Therefore, a lamella with an appropriate thickness was prepared. Figure 12.28 shows radiographs of several TSVs with an SiO_2 liner and TaN/Ta/Cu stack before copper

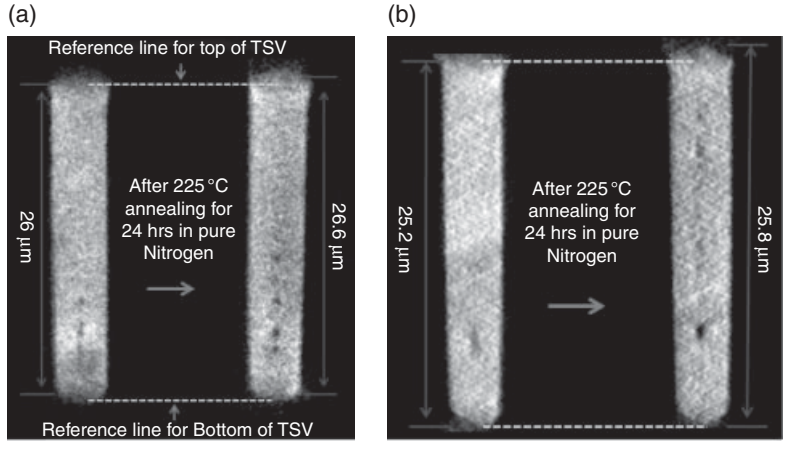

Figure 12.27 *Changes of the original defect after 225 °C/24 h for (a) 5 µm and (b) 4 µm TSVs* [87]

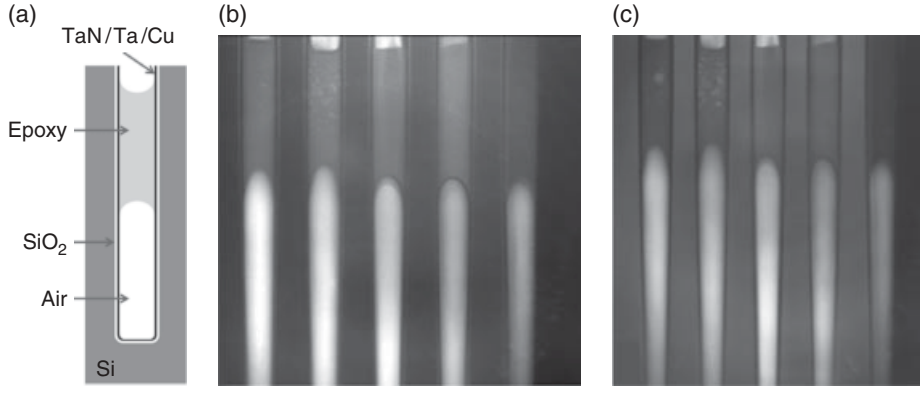

Figure 12.28 *(a) Scheme of the samples; (b) and (c) radiographs of dummy TSVs at 510 eV and 555 eV photon energy, respectively*

plating at two photon energies, 510 eV and 555 eV, respectively. The experiments had been performed at the U41-TXM at the storage ring BESSY II [88]. The vias are completely embedded in the lamella.

The radiographs offer the possibility to study, for example, the liner thickness and conformity. The influence of absorption edges can be seen by comparing the images at 510 eV and 555 eV. The SiO_2 liner appears dark at the higher energy since the X-ray absorption of the SiO_2 material increases significantly above the O-*K* absorption edge (543 eV) [86].

X-Ray Microfocus Tomography. As a complementary method, X-ray microfocus tomography provides the opportunity to investigate larger regions with lower resolution. The

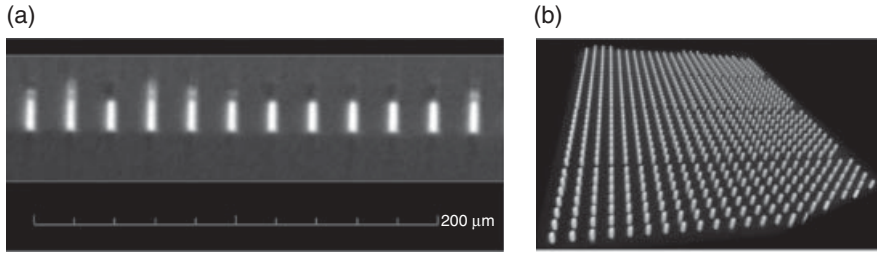

Figure 12.29 *(a) Upside-down cross-section and (b) 3D visualization of an X-ray microfocus tomography of a TSV array*

method is well known from nondestructive testing of chip packages and printed circuit boards. Commercial systems offer submicrometer resolution. Hence, they are applicable to the inspection of 3D chip interconnects. The photon energy of several 10 keV can be matched to the specific object to provide sufficient transmission and contrast. In general, no sample preparation is needed.

In Figure 12.29, 5 µm TSVs from via chain structures are shown, based on a tomography study (measurement time about 10 hours). Incomplete fill defects are detected at most of the bottoms of this sample. The 3D visualization offers an overview of the sampled region that includes a relatively large array of TSV structures.

12.3.4 Microstructure Analysis

The microstructure of metal TSVs can affect both the performance of active devices through the stress field in the surroundings of the TSV and the reliability, i.e. electromigration (EM) and stress migration (SM) [89]:

- The stress in the vicinity of the TSVs is influenced by geometry and materials, but particularly by the metal microstructure of the TSV. Since the elastic properties of copper are highly anisotropic (the anisotropy factor is 3.2), large copper grains and texture have a significant effect on the stress in the silicon next to the copper TSV.
- Both electromigration and stress migration are phenomena that are based on directed atomic transport, caused by gradients of the electric potential and of the stress, respectively. Interfaces and grain boundaries are fast pathways for atomic transport and affect the lifetime of interconnects.

This means that the characterization of the microstructure of the metal interconnects (e.g. TSVs) is of high importance.

The microstructure of on-chip interconnects has been studied extensively using X-ray diffraction (XRD), electron backscatter diffraction (EBSD) in a scanning electron microscope (SEM) and conical dark-field diffraction (CDF) analysis in a transmission electron microscope (TEM). Since the methodology can be transferred from on-chip interconnects to 3D TSVs, some of the examples shown here are from well-studied copper dual-damascene interconnect structures.

General Concept of Microstructure Characterization of 3D Interconnects

The following microstructure parameters of interconnect materials are of importance [90]: grain size, texture, stress and all kinds of defects of filled TSVs. In addition, liner, diffusion barrier and seed layer have to be characterized. The microstructure is completely characterized by the general microstructure function as defined by Bunge [91]:

$$G(x) = \begin{cases} i(x) & \text{phase} \\ g(x) & \text{orientation} \\ D(x) & \text{defects, lattice strain} \end{cases} \tag{12.13}$$

where $G(x)$ specifies phase i, crystal orientation g, as well as lattice defects D (including local residual stress) in any volume element of the material at the position x of the sample. The first part of this function, $i(x)$, is of concern if the microstructure of the barrier metal has to be included in the characterization of interconnect structures (e.g. TSVs). The whole texture information is contained in the term $g(x)$. Additionally, the mechanical stress is of particular interest, as mentioned above. The first-order strain or macrostrain $\langle\varepsilon\rangle$ is the quantity that is experimentally accessible by common X-ray diffraction methods. The first-order residual stress $\langle\sigma\rangle$ can be considered as one contribution to the term $\langle D\rangle$ rather than $D(x)$ in Equation (12.13), i.e. an average value over a specific volume [92]. Due to this fact, the measured stress is influenced by the texture of the copper inside the probed volume. Hence, a complete determination of the three-dimensional stress state of copper applying X-ray diffraction requires knowledge of the texture as well [93], especially due to the elastic anisotropy of copper (Young's modulus $E_{Cu}\langle 111\rangle$ = 191.1 GPa, $E_{Cu}<100>$ = 66.7 GPa). The most complete analysis would imply the simultaneous measurement of both the orientation of single grains (i.e. $g(x)$) and their local stress state $\sigma(x)$.

X-Ray Texture Analysis – Classical Orientation Distribution

X-ray diffraction is one of the most suitable nondestructive methods for texture analysis of copper interconnects. Several (*hkl*) pole figures of the material (e.g. (111), (200) and (220) for copper) have to be recorded in order to obtain the required information about the orientation distribution function $f(g)$ (ODF) of the crystallites [94]:

$$f(g) = \frac{\mathrm{d}V_g/V}{\mathrm{d}g} = f(\varphi_1, \Phi, \varphi_2) \tag{12.14}$$

The crystal orientation g (i.e. the orientation of the crystallographic axes with respect to the chosen sample reference axes) is expressed by the Euler angles φ_1, Φ, φ_2 [95]. The ODF considers the volume fractions $\mathrm{d}V_g$ of crystallites with orientation g in the irradiated sample volume V with an orientation spread $\mathrm{d}g$. Software for the calculation of the ODF is commonly based on one of two general approaches, either the harmonic method or the direct methods, e.g. the ADC algorithm (arbitrarily defined cells method) [96] and the WIMV algorithm (Williams–Imhof–Matthies–Vinel) [97, 98]. The direct methods provide an improved ODF approximation in the case of sharp textures. Quantitative information about the volume fractions of certain texture components can then be extracted from the

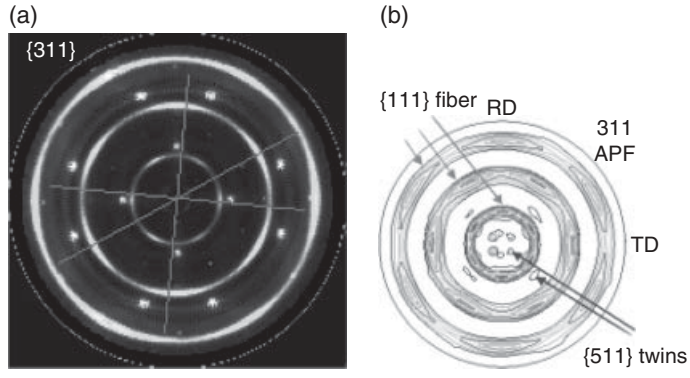

Figure 12.30 *(a) Cu {311} pole figure of copper lines with w = 180 nm, where the positions for stress measurements are indicated by lines. (b) A reconstructed {311} pole figure, calculated from the ODF, rotated by 90°. Contributions to the {311} pole figure from the {111} oriented grains (fiber) and {511} oriented grains (twins) are indicated* [90]

calculated ODF. Some complementary information is already contained in the pole figures themselves, e.g. the full-width-at-half-maximum (FWHM) of a pole, which gives the orientation spread of a texture component.

From the experimental point of view, the measurement of pole figures has become more convenient and less time consuming since sensitive X-ray area detectors became available [99, 100]. Area detectors with a high quantum efficiency allow very small diffracted signals to be detected, which is beneficial for test structures with a low density of Cu structures like Cu TSV arrays in Si, and reduce the required set of angles $\{\chi; \phi\}$ for the acquisition of a pole figure considerably due to the fact that a whole segment of the reciprocal space is recorded in just one frame. Additionally, the segments of several (*hkl*) diffraction cones (e.g. Cu (111) and (200)) can be captured simultaneously with an area detector [90]. The texture components can basically be described by the FWHM, but a quantitative description needs the ODF to be calculated.

Texture Characterization for X-Ray Stress Measurements

The use of an X-ray diffractometer with an area detector and a precise Eulerian cradle makes it possible to perform both stress and pole figure measurements. A triaxial stress data analysis [101] is needed for Cu TSVs for which a biaxial stress model cannot be assumed to be valid. In principle, the pole figure of a higher order (*hkl*) reflection of Cu like {311} has to be measured at first to find the orientation distribution of the {311} crystal planes as a function of the angles $(\chi; \phi)$. The stress measurements can then be optimized by choosing the optimum angles where the highest possible intensities will be obtained. Results for on-chip copper interconnects that prove this concept are given in Figure 12.30 [90].

Additionally, the (111), (200) and (220) pole figures can be recorded during the same measurement series. This set of pole figures is sufficient to calculate the ODF and to reconstruct the {311} pole figure from this ODF (Figure 12.30 (b)). As an advantage, the

texture of the copper structure is characterized at exactly the same position where the stress measurements are performed. During the 2D or 3D stress analysis, the distortions of the segments of the {311} diffraction cones are evaluated for multiple pairs of angles (χ; ϕ) and the complete stress tensor is calculated, including the shear-stress components. The anisotropy factor of copper is also taken into account. The advantages of this method are obvious. The opportunity exists to correlate the obtained stress values with possibly observed changes of the texture in the investigated copper test structures. Since the {311} pole figure has been measured, it is known which groups of crystal orientations contribute to the stress measurement at a certain set of angles (χ; ϕ), e.g. if the diffracted intensity includes the fiber as well as the engaged texture component or if it includes the fiber texture only.

EBSD and CDF – Complementary Orientation Imaging Microscopy

The main advantage of OIM (orientation imaging microscopy), including EBSD and CDF analysis, is that these methods directly provide the orientation location distribution $g(x)$. This is complementary to X-ray diffraction, which provides integrated information over a vast sample volume (resulting in $\langle g \rangle$ instead of $g(x)$) with penetration depths of at least several micrometers, containing a larger number of crystallites. Particularly for electromigration and stress migration studies, the orientation of single grains in specific TSVs is of interest. To get access to this location and to measure the local texture exactly there, EBSD or CDF analysis can be performed at cross-sections of the Cu TSV structures. Additionally, OIM provides information about the grain sizes. Due to the fact that the relative orientations of neighboring grains are resolved, twin boundaries (i.e. $\Sigma 3$) as well as small-angle and high-angle grain boundaries can be identified with EBSD and CDF analysis. Compared to the X-ray texture analysis, OIM provides the distribution of the different types of grain boundaries in copper TSVs. In the case of studies to understand reliability-limiting mechanisms in interconnects, it is most desirable to record OIM images directly on EM or SM test structures before and after the test, and to correlate the EM or SM behavior directly with the grain orientation, grain size distribution and the types of prevailing grain boundaries.

Microstructure Study Using EBSD Analysis

EBSD is a proven analytical technique to characterize the microstructure of Cu interconnects, even at FIB-prepared cross-sections. This technique requires minimum grain sizes of about 30 nm. In particular, inverse pole figure (IPF) maps are used to describe the microstructure. Figure 12.31 (a) shows an example for a plan-view EBSD IPF map of an array of 200 nm wide inlaid copper lines after plating, polishing and annealing. Typical experimental parameters are an SEM operating voltage of 20 kV, 70° sample tilt, 3 µm × 10 µm scan size and 40 nm step width. Most of the copper grains have a {111} orientation with respect to the wafer normal, as clearly seen in Figure 12.31 (a). The twin boundaries are marked by solid black lines on the EBSD image. Besides {111} oriented grains, a certain amount of {511} and {611} twins was identified. There is only a very small number of {100} or {101} oriented crystallites. Pole figures can be calculated from the EBSD patterns on inlaid copper lines as well (see, for example, Reference [102]), but their angular resolution is worse than that from X-ray texture analysis (Figure 12.32).

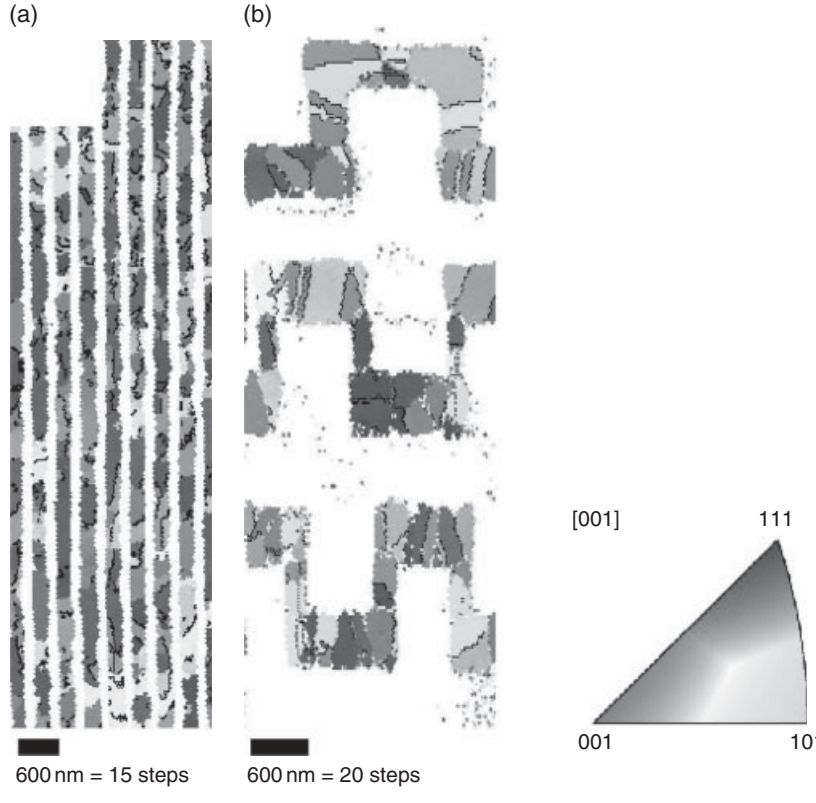

Figure 12.31 *EBSD inverse pole figure (IPF) map on 200 nm wide inlaid copper lines. (a) Plan view. (b) EBSD IPF map on cross-sections through via1, via3, via5 chains, showing the orientation of the Cu crystallites inside the vias. Orientations are defined by the coding of the orientation triangle at the bottom margin of the figure and are referenced to the wafer normal for both (a) and (b). Σ3 twin boundaries are marked by black lines. The orientation stereology g(x) is obtained with this technique* [90]

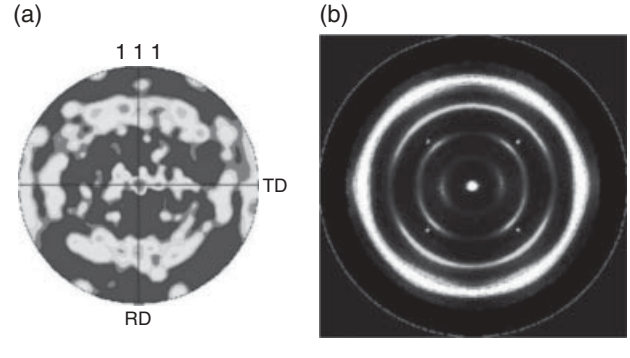

Figure 12.32 *(a) {111} pole figure, calculated from a 3 μm × 10 μm EBSD map of an array of 200 nm wide copper lines, like those shown, for example, in Figure 12.31 (a), and (b) {111} pole figure, obtained from X-ray diffraction with an 80 μm beam diameter on an array of 180 nm wide copper metal lines* [90]

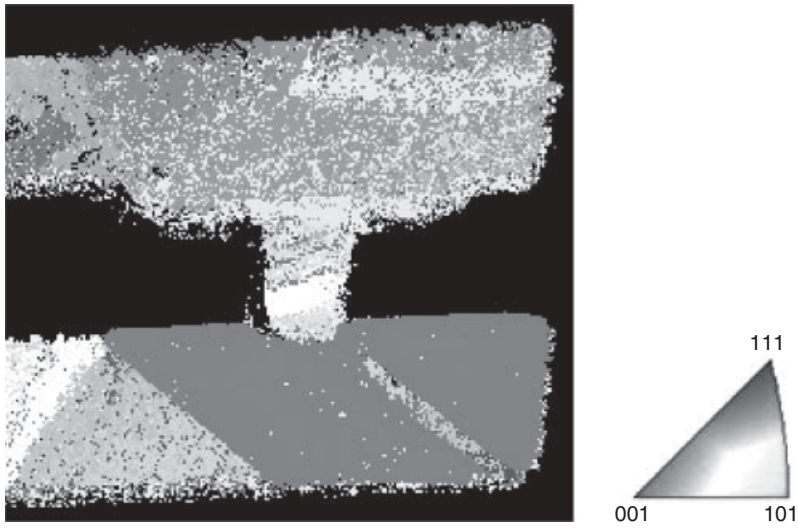

Figure 12.33 *[001] inverse pole figure map of a Cu structure* [103]

A typical EBSD scan of an array of copper structures, like the one shown in Figure 12.31 (a), covers an area of several tens of μm^2, containing a much smaller number of crystallites compared to X-ray diffraction. Therefore, the volume fractions of orientated grains that were obtained with X-ray diffraction are statistically more significant than those from EBSD, leading to more detailed pole figures. On the other hand, EBSD provides the orientation of single crystallites together with their coordinates, and thus directly determines the orientation function $g(x)$ as defined in Equation (12.30).

Microstructure Study Using CDF Analysis

In some cases, even for TSVs, the EBSD analysis reaches its limits with respect to texture and grain-size analysis because of grain sizes smaller than 30–50 nm. Therefore, a complete microstructure analysis of TSVs, including the barrier and seed layers, will only be possible using the CDF analysis as a complementary technique, even though it is more time-consuming. Due to a resolution better than 5 nm, the CDF circular scan technique in the TEM provides grain size distributions and complete grain orientation maps for grain sizes < 30 nm. Consequently, it allows characterizing the Cu microstructure of regions with small grains [103].

In a first step, centered dark-field images of a particular view of the specimen are recorded in a circular way for several tilt and rotation angles of the parallel electron beam. In a second step, spot diffraction patterns for every point of the field of interest are reconstructed using all recorded dark-field images. Based on the crystallographic structure of the polycrystalline material, the diffraction patterns are indexed. Finally, IPF maps and, hence, the crystallographic orientations of individual Cu grains can be determined [104]. As an example, Figure 12.33 shows a [001] inverse pole figure map of a Cu interconnect structure.

12.4 Summary

At the same time as research in 3D TSV technology is advancing quickly, the microscopy techniques used in the evaluation of 3D stacks must also advance in capability. Overlay measurements after wafer bonding, defect detection and void inspection after copper plating are challenging due to the need to image through silicon and inside copper. Microscopy techniques for which silicon is opaque, such as scanning acoustic microscopy (SAM) and confocal infrared (IR) microscopy, are capable of inspecting the interface between bonded wafer pairs, while high-resolution X-ray computed tomography (XCT) is used to detect voids in TSVs. With nano-XCT, voids in copper TSVs with sub-100 nm size can be visualized. For more detailed failure characterization, a target focused ion beam (FIB) cross-section through the localized region of interest (defect) and subsequent scanning electron microscopy (SEM) imaging is proposed [105].

X-ray diffraction and OIM techniques are applicable for TSV metal microstructure analysis. Texture, grain size and the first-order stress of Cu-filled TSVs can be thoroughly characterized using X-ray diffraction, EBSD and CDF analysis. The influence of the TSV geometry, the deposition conditions and the type of liner and barrier layers on the copper texture in filled TSVs can be studied. X-ray diffraction, EBSD and CDF analysis are complementary techniques to X-ray diffraction since the X-ray technique integrates over a larger sample volume, resulting in statistically more significant texture data, whereas EBSD and CDF additionally provide grain boundary distributions, grain sizes and the grain orientation stereology $g(x)$. EBSD and CDF analysis are also suitable methods for studying the local grain orientation, grain boundary distribution and grain size distribution in TSVs.

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