Enabling technologies for 3D integration:
From packaging miniaturization to advanced stacked ICs

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Abstract:

This paper presents an overview of current 3D technologies development at CEA/LETI Minatec. Three different 3D approaches are described, and can be seen as 3 generations for that emerging field. An original Through Silicon Via (TSV) process for CMOS Image Sensors (CIS) is presented, and electrical results showing very low resistances and high yields are described. A similar TSV process, combined with temporary bonding and low pitch interconnects is used to address the second generation of 3D integration, the active silicon interposer. A first demonstrator of a TSV process on thin wafer is described. Some reliability results on an innovative technology for flip chip, fully compatible with chip stacking, are detailed.
It will also be shown that by developing advanced technology like direct bonding and high density TSV, CEA-Leti is also preparing ultimate 3D integration, with very high density interconnects.

Introduction:

3D packaging is not a new concept, and some 3D solutions have already been proposed by several companies during the last 20 years. However, the main applications of these solutions were focused on markets where form factor and sometimes performance were the only drivers, and where cost constraints were not critical. As far as the consumer market is concerned, 3D was not really seen as a viable solution until recently. Several factors are today pushing the emergence of 3D integration even in the low cost end of the market. On the one hand, driven by the emergence of nomadic systems, the pressure on package dimensions is becoming higher and higher. On the other hand, it is becoming clearer for IC engineers that Moore's law will be hard to follow with 2D concepts (partially due to devices variability, lithography limitations and interconnect complexity). Furthermore, the introduction of non-IC silicon components, like MEMS, increases the difficulty of integrating all the functions on the same wafer. Simultaneous with these evolutions, some technologies initially developed for MEMS (like Deep Silicon Etching, wafer bonding or thick lithography), are becoming more and more mature, following growth of MEMS manufacturing volumes. As a consequence, 3D integration is now seen as a viable solution not only by packaging engineers, because it can be managed with wafer level technologies, and not only for high added value markets.

Image-on-board: First industrial application for TSV

TSV need for CMOS Image sensors

Flip-chip technology, allowing a reduction of both die size and package footprint on Printed Circuit Board, could be seen as the starting point of impressive electronics components evolution in term of form factor and cost reduction, during the last decade [1]. It has been applied for most of the silicon components in a mobile phone, for instance. However, the emergence of optical devices in nomadic systems, both for displays and camera, showed a limit in that approach: direct application of Flip chip to imaging devices is not possible, as they can only be mounted on a face-up basis (light coming from the top). A similar evolution for this kind of device, and specifically low cost integration of CMOS Image Sensors (CIS) for mobile camera, consequently required development of Through Silicon Vias (TSV), which allow a flipchip-like connection from back-side, as illustrated on Fig. 1. Moreover, TSV allow a reduction of pad size, and so a reduction of silicon surface and cost. Several papers have been recently published in this domain [2] [3].

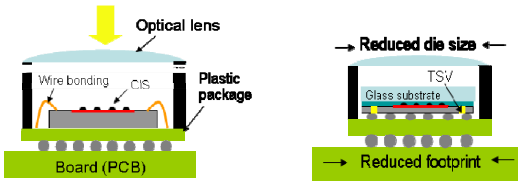


Fig 1. Evolution of CMOS Image Sensors packaging. Through Silicon Vias (TSV) allow a reduction of both die size and component footprint.

Process description

CEA-Leti has recently developed a medium density via-last TSV technology dedicated to CIS packaging [4]. Main advantage of CEA-Leti process compared to the others technologies developed [3] is that we use vertical walls for TSV, and not tapered vias. That allows smaller diameters and avoids complex lithography for oxide etching at the bottom of the vias. Moreover, that process is a low temperature one, in order to be compatible with CIS micro-lenses presence (< 200°C).

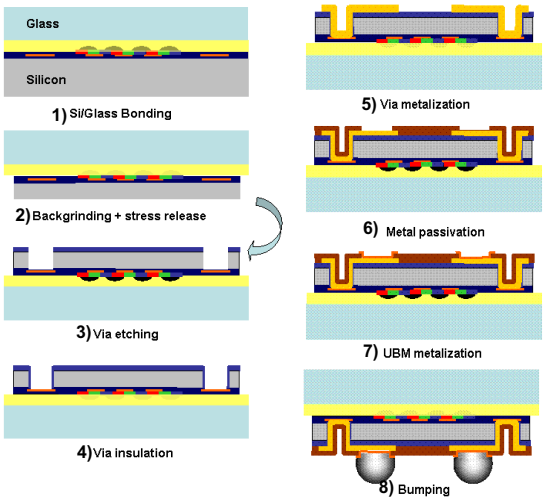


Fig 2. Main steps of the vias-last process flow.

The process flow, described in Figure 2, includes 8 main technological steps: the CIS wafer is firstly bonded on a glass wafer thanks to patterned polymer bonding (1). This glass wafer is used as a handler for the following steps. Active wafer is then thinned down to 70 µm thanks to grinding machine & chemical stress release (2). Bosh-process deep silicon etching is used to etch 70 µm

diameter vias through the silicon layer (3) and vias are insulated with low temperature PECVD oxide (4). A TiCu seed layer is then sputtered and metallisation is performed by electroplating (5). In that step, classic lithography can not be used because of via topology, so we used a photosensitive dry film [5]. A BCB passivation is then deposited (6) and Under Bump Metalization (7) and solder bumps (8) are achieved. More details on that process can be found in [4]. A cross view of a TSV is presented in Figure 3.

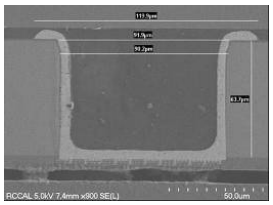


Fig 3. SEM Cross section of post process medium density TSV

Fig 6. Picture obtained after complete packaging (VGA).

Electrical tests

For TSV with a diameter of 70 µm, and a depth of 70 µm, electrical resistance lower than 1 mΩ per via was measured (Fig. 4), with yields greater than 98 % on 200 mm wafers (Fig. 5). The Figure 6 shows an image obtained with a TSV-packaged image sensor. The comparison with classically packaged sensors confirms that TSV process does not impact optical performances of the device, and does not degrade image quality.

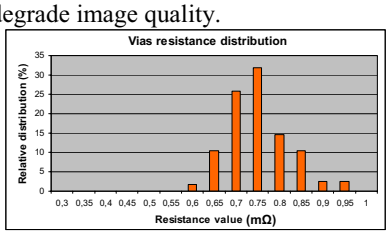


Fig 4. TSV resistance distribution on a CIS wafer, measured on two test via per die, on 1500 dies on one 200mm wafer.

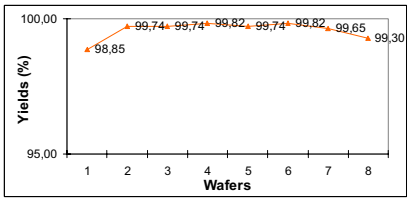


Fig 5. Electrical contact yields on 8 CIS wafers (1500 dies per wafers).

This process has been transferred to industry (STMicroelectronics) in 2008, but technological outputs of this program are currently the base of the 3D packaging program at Leti.

Active silicon interposer, Multichip stacking

Silicon interposer is widely used today to bridge the resolution gap between IC dies and plastic-based package [6]. We consider that 3D integration begins when this passive silicon interposer becomes an active component. The philosophy of those developments is really to integrate several dies or functions in a single package without any change in the back-end lines (i.e. to use standard and low cost packaging techniques).

The Figure 7 summarizes evolution of packaging: after flip-chip package (2), a trend is to add more than one dies (3) in the same package (TSV are required in the bottom die). In the future, we can think that at least for some applications, plastic package will be removed and the silicon interposer will be directly mounted on the motherboard (4). Multichip stacking (more than 2 layers) can be seen as an extension of silicon interposer, as the technology blocks needed are quite similar.

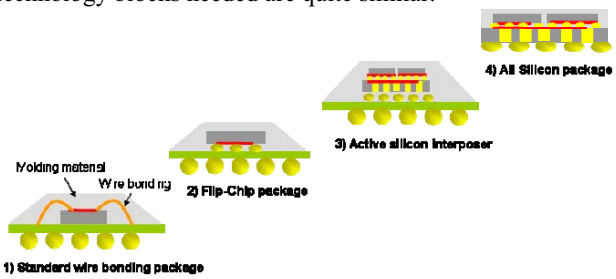


Fig. 7. Evolution towards Active silicon interposer:

Temporary bonding

It is clear today that TSV technology cannot be cost effective for wafer thickness higher than 200 µm, and handling of wafers thinner than 300 µm is difficult in standard fabs. Moreover, compared to imagers' process presented before, the glass handling wafer cannot be kept in the final package. For those reasons the use of a temporary carrier during TSV process seems to be mandatory. A temporary bonding with adhesives is currently in development at CEA-Leti, in collaboration with Brewer Science and EVG [7]. In that process, the active wafer is bonded on a handling wafer, thinned, and the TSV process described for imagers is applied. At the end of that process, the thin wafer is separated from its handler by heating and slide-off. Adhesives developed for that application must of course have adequate flow properties, mechanical strength, thermal stability, chemical resistance, and easy debonding and cleaning, and must withstand a complete TSV process.

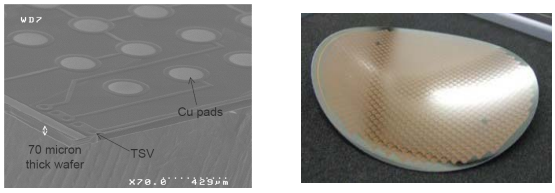


Fig 8. SEM and full wafer view of a post process TSV made on a temporary bonded 70 µm thick wafer (after debonding).

As a first demonstrator, a complete TSV process has been performed on a 70 µm thick wafer (Fig.8), using temporary bonding. Electrical test on 2-TSV chains before and after debonding shows that there is no degradation of resistance of the TSV before and after debonding (Fig. 9): the debonding process has no impact on TSV and pads.

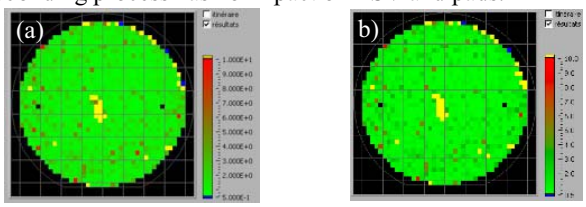


*Fig. 9. TSV resistance measurements on a 2-*TSV chains *(a) before debonding, and (b) after debonding. Test done on a 200mm wafer.*

Low pitch Interconnects

The second difficulty is linked to interconnections between layers. Classic solder bumps, with materials such as SnAgCu, are not suitable for 3D integration, in terms of pitch and also because it is not easy to manage multiple reflows corresponding to each stacked level. Solutions with Copper-pillar, Cu-Cu thermo compression [8], CuSn solders [9] have been proposed. The solution proposed by Leti, called µ-Inserts interconnects, is based on Nickel

µbumps [10] [11]. This technology presents the advantage that no solder is used, what is essential for 3D integration.

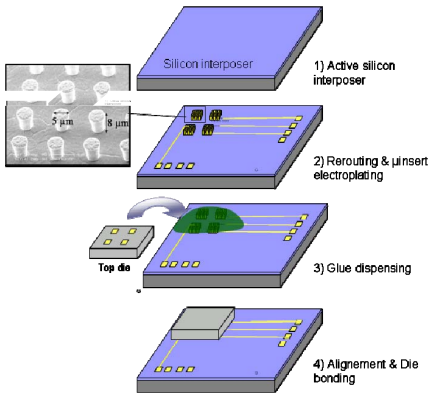


Fig 10. Process description of µinserts technology..

Microinserts technology is described on figure 10. A classic rerouting is done on the host wafer, and several Ni pillars are electroplated on each pad (2). They have a diameter of 5 µm, for a thickness around 10 µm. A glue is dispensed thanks to a pick & place tool (3). Then flip chip is done (4), and thanks to the pressure applied, Ni pillars are inserted in the aluminium pads of the top die. Thanks to the fact that a glue is deposited before flip-chip, no underfill is needed after assembly. That pre-applied underfill is a big advantage for 3D integration: because the gap between top and bottom substrate is small, underfill dispense with classic techniques becomes very problematic for low pitch assembly.

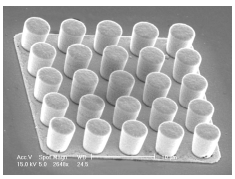


Fig.11. Ni µinserts Electroplated on an Al pad.

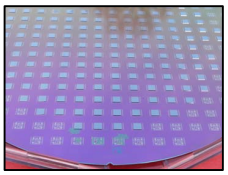
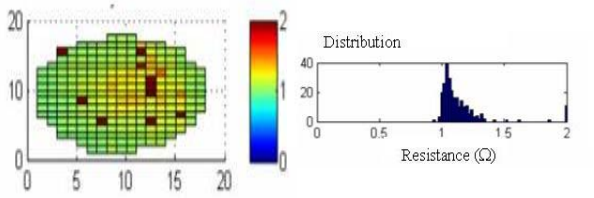
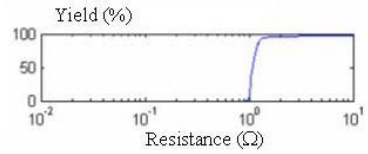


Fig 12. A 200mm wafer with dies flipchiped



a). Resistance value distribution at wafer level

b). Resistance histogram showing a skewed distribution



c). 93% yield estimation based on a 1.5Ω filter.

Fig. 13. Distribution and yeld for 32 contact daisy-chain. Measured are done on 100 dies bonded on a 200mm wafers.

Figure 11 shows a picture of an aluminium pad with 25 Nickel µbumps. For 50µm x 50 µm pads, a contact resistance of 7 mΩ per pad has been measured. Figures 13a to 13c show a wafer map and its associated value histogram and yield at 1.5 Ω for the resistances of a 32 contact daisy-chain, measured on a 10 x 10 matrix of dies bonded on a 200mm silicon wafer.

Reliability tests have been performed, and measurements of a 32 contacts daisy chain after more than 800 cycles (-40°C to 85°C) does not show any degradation of resistance distribution,. Further electrical stresses have been realized on the 32 contact based structures by applying a current of 400mA during 80 hours, and no significant change has been observed in resistance value.

In collaboration with Gemalto, µinsert technology has been successfully used for a smartcard application. A demonstrator of a Flash Memory + CPU has been manufactured and integrated in a smartcard module [12].

Ultraflat 3D: 3D at the IC level

If Active Silicon Interposer and Chip Stacking respond well to packaging technology needs, solving the problem of interconnect complexity of next-generation CMOS requires passing to the next level in technological developments. Indeed, even if basic tools are similar, the scale is not the same: interconnection pitch, TSV diameter and alignment accuracy are now in the micron range [13] [14]. To reach this range of dimension the thickness of each layer cannot exceed 15 µm.

To reach the required alignment accuracy and the targeted silicon thickness, one would prefer to work at the wafer level. However, that approach requires for the dies to all have the same size, and yield problems will arose as far as more than 2 levels are stacked. For these reasons, one can think that Wafer to Wafer will be limited to dedicated applications, and that a Chip to Wafer technology is mandatory. All developments currently done on bonding & TSV for Ultraflat 3D at CEA-Leti tend to be compatible with both approaches.

An example of Ultraflat 3D integration process is proposed in figure 14. After dicing, top die are flip chipped on the bottom wafer, thinned, and an oxide planarisation is done before TSV process.

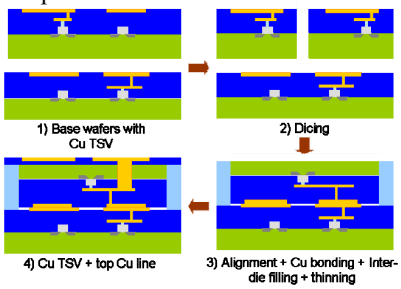


Fig. 14. Example of ultraflat 3D process (die to wafer).

Alignment, Bonding & Silicon thinning

If polymer bonding is suitable for the previous 3D developments, with regards to the temperature and accuracy constraints induced by the high Aspect ratio TSV, direct bonding seems to be the best candidate for Ultraflat 3D. Direct bonding requires flat and cleaned surfaces but allow post process of the bonded wafers in front end line and at high temperature. 200 nm Oxide/Oxide bonding of two CMOS wafers with 1 µm alignment accuracy has already been demonstrated [15], and is presented in figure 15.

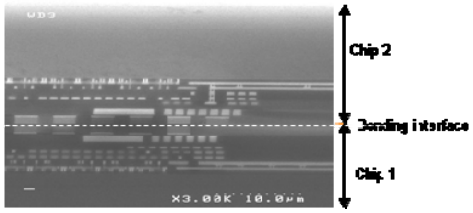


Fig.15. Demonstration of Oxide-Oxide bonding on CMOS wafers.

The main challenges for direct bonding are now to develop a chip to wafer process, and to replace the Oxide-Oxide

bonding by a patterned Copper-Copper bonding. This will allow localized electrical contact between two levels, like it was done previously with µinserts.
A proof of concept of die to wafer direct bonding has been made. On the figure 16, some dies (from 2x2mm up to 10x10 mm) have been successfully bonded on a 200mm wafers. The acoustic characterisation shows a good bonding quality (no defect at the bonding interface). One has to keep in mind that direct bonding allows the sticking of the die on the wafer surface at room temperature, and annealing strengthens the bonding energy. This is of great interest when high alignment accuracy is required.
The figure 17 shows a cross-section of a direct Cu/Cu bond [16]. Bonding is done at room temperature, ambient air and without pressure and a 3J/m^2 bonding strength is achieved after a 100 °C annealing. An ohmic contact has also been measured between the two wafers. The possibility to grind the top silicon down to 10 µm or the bonding of three thinned wafers has also been demonstrated.

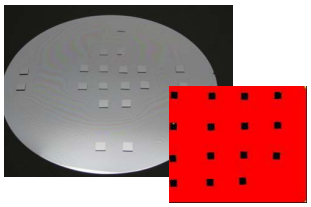


Fig. 16. Die to wafer oxide-oxide molecular bonding.

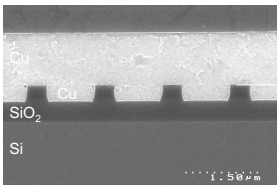


Fig.17. SEM view of a patterned wafer bonded to a copper blanket.

High density TSV

A high density TSV process has been developed on a wafer to wafer stack, bonded with oxide-oxide molecular bonding. A RIE process is used to etch the 15µm thinned silicon substrate and the dielectric stack. The TSV isolation is insured by the deposition of a conformal SACVD SiO2 film. 200nm SiO2 is deposited on TSV sidewall. 10nm MOCVD TiN is used as a barrier layer against copper diffusion. The copper seeding is achieved by successively depositing 50nm PVD Cu and 150nm MOCVD Cu. The TSVs are filled with 2µm ECD Cu, using specific ECD chemistry and process parameters to obtain voidless filling. After annealed, a standard CMP process was used to polish the excess Cu and the TiN barrier.

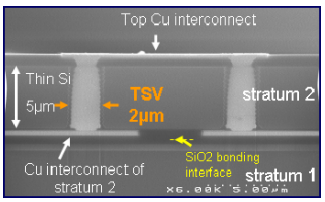


Fig. 18. 2 µm diameter / 5 µm thick TSV filled with copper.

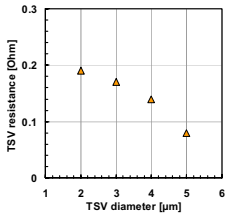


Fig. 19. Resistance evolution versus via diameter

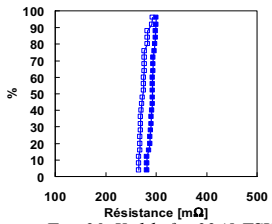


Fig. 20. Yields for 3248 TSV chains (via + line on two wafers).

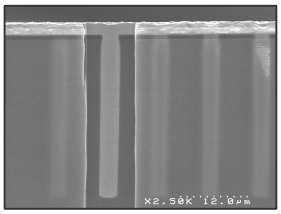


Fig 21. Void-less filling of TSV with Aspect ratio of 10.

The figure 18 shows a 2 µm diameter / 5 µm thick TSV filled with copper. Resistance evolution versus via diameter is represented in Figure 19, with value between 100 mΩ and 200 mΩ. A yield greater than 90 % for 3248 TSV chains on 200mm wafer has been obtained with 3µm diameter/15 µm deep vias (Fig. 20). Values plotted represent resistance for one via plus its access line.
Void-less filling of 30µm deep / 3 µm diameter vias has also been demonstrated, as presented in Figure 21.

Conclusions

From TSV for imagers to Ultraflat 3D, CEA-Leti is currently developing a complete 3D toolbox. A mid-density TSV process, initially developed for image sensors is now mature and transferred to industry. This technology, applied on temporary bonded wafers, is used to develop active silicon interposers for 3D stacks. In parallel, an original interconnection technology, allowing low pitch and low thickness without solder, has been developed. In order to address future challenges in 3D integration, meaning increasing interconnections density, CEA-Leti also develop advanced bonding processes for chip to wafer approach, and a demonstration of high density TSV has been performed and electrically tested.
All those developments in 3D integration can be seen as an anticipation of future heterogeneous system: System-On-Wafer concept [17] is an example of what could be heterogeneous integration in the near future: a macro silicon dies supporting several functions, all interconnections being managed at the wafer level. In that kind of system, all 3D integration schemes presented in that papers can be gathered to reach ultra compact and high performance systems, at a cost compatible with consumer market applications.

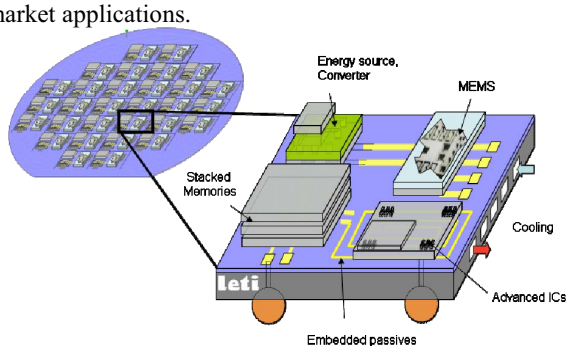


Figure 22. System On Wafer: All silicon approach for heterogeneous integration.

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