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Wafer-level bonding/stacking technology for 3D integration

Cheng-Ta Ko, Kuan-Neng Chen *

Department of Electronics Engineering, National Chiao Tung University, Hsinchu 300, Taiwan

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ABSTRACT

Enhanced transmission speeds, lower power consumption, better performance, and smaller form factors are reported as advantages in many devices and applications when using 3D integration. One core technique for performing 3D interconnection is stacked bonding. In this paper, wafer-level bonding technologies are reviewed and described in detail, including bonding materials and bonding conditions. The corresponding 3D integration technologies and platforms developed world-wide are also organized and addressed.

1. Introduction

Three-dimensional integrated circuits (3D IC) has been generally acknowledged as the next generation semiconductor technology with the advantages of small form factor, high-performance, low power consumption, and high density integration [1–3]. Through silicon via (TSV) and stacked bonding are the core technologies to perform vertical interconnect for 3D integration. For the fabrication approach, there are three stacking schemes in 3D integration: chip-to-chip, chip-to-wafer, and wafer-to-wafer. Wafer-to-wafer technology can be applied for homogeneous integration of high yielding devices. Wafer-to-wafer bonding maximizes the throughput, simplifies the process flow, and minimizes cost. The drawback for this wafer-to-wafer method is the number of known-good-die (KGD) combinations in the stacked wafers will not be maximized when the device wafer yields are not high enough or not stable. In this case, chip-to-chip or chip-to-wafer will be adopted to ensure vertical integration with only good dies. Considering mass production in future, the chip-to-wafer and wafer-to-wafer technologies have gradually become the mainstream for 3D integration.

Wafer-level bonding/stacking technologies can be further differentiated by the method used to create TSVs: either via-first or via-last. The common definition for via-first and via-last is based on TSVs formed before and after BEOL process. TSV fabrication after the wafers are bonded, using a "drill and fill" sequence, is definitely via-last approach. Whereas via-first and pre-bonding via-last approaches, build TSVs on each wafer prior to the bonding process, are generally more efficient and cost-effective. The leading wafer-level bonding techniques used in 3D integration include adhesive bonding (polymer bonding), metal diffusion bonding, eutectic bonding, and silicon direct bonding. Additionally, one emerging approach with high yield and high reliability is hybrid bonding technology. In this review paper, these wafer-level bonding techniques are introduced in detail. Corresponding 3D integration schemes using these bonding technologies and platforms developed in companies or research institutes are also reviewed.

2. Adhesive/polymer bonding

Adhesive bonding is a low temperature and patternable technique suitable for 3D IC, MEMS, VLSI packaging, and microsensor packaging. In 3D IC integration scheme, adhesive material can be used for wafer-to-wafer bonding followed by fabrication of TSV on proper position to form vertical interconnection between stacked wafers. The advantages of this bonding technology include low bonding temperature with required bonding strength, no metal ion contamination to device, excellent surface planarization property, and high plasticity to absorb the stress induced during bonding process.

In this bonding scheme, however, because TSV is fabricated after bonding, the higher aspect ratio increases the process challenge and cost especially for small via size. In addition, the high shrinkage characteristic of polymer materials decreases the bonding accuracy, which also limits its application. Therefore, adhesive bonding is usually adopted on wafer bonding with lower accuracy requirement, or collocated with other bonding methods to be an auxiliary to increase the bonding strength. The potential contamination of adhesive materials on devices and fabrication tools during process is a significant concern for the manufacturing line. As for the selection of adhesive material, in addition to the basic requirements such as excellent adhesion, low residual stress, a high thermal and chemical resistance is also the requirement to endure the follow-up processes.

Based on the application, the adhesive materials can be divided into photosensitive and non-photosensitive types. The photosensitive materials are usually used as photoresist model to define the

* Corresponding author.
E-mail address: knchen@mail.nctu.edu.tw (K.-N. Chen).

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patterns. The non-photo ones are generally adopted for the passivation layer to protect circuits, or used to be the build-up layer. The bonding strengths of four different patternable materials (SU-8 from MicroChem Co., AZ-4620 from Shipley, SP-341 from Torray Co., and JSR-137N from Japan Synthesis Rubber Co.) have been thoroughly investigated by Pan et al. [4] with respect to bonding temperature and bonding force dependence. The bonding strength between identical materials exhibits the same behavior for all four materials. Fig. 1 shows the relationship between bonding strength and bonding temperature, which indicates the SU-8 has the maximum bonding strength of 20.6 MPa among the four materials, whereas the other three are all about 10 MPa. Other polymer materials such as benzocyclobutene (BCB) (Dow chemical), Polyimide (DuPont), Parylene, and several photoresists are also evaluated and compared [5,6]. The results illustrate the BCB has the highest bonding strength (>20 MPa) with very small void formation. Currently, BCB and SU-8 are the most common materials used for wafer-level adhesive bonding in 3D integration and applications.

As aforementioned, BCB is one of the adhesive wafer bonding materials that have been researched extensively for 3D IC platforms because of its outstanding wafer bonding capabilities, thermal resistance, bonding strength, chemical resistance, and wide acceptance in IC manufacturing environments. Researchers from RPI use CMOS silicon on insulator (SOI) wafers and BCB as the dielectric to develop 3D integration platforms by adhesive wafer bonding [7,8]. Fig. 2 shows a schematic 3D IC structure of RPI approach [7]. In this 3D integration platform, the pre-processed IC wafers are aligned and bonded with BCB adhesive by face-to-face wafer bonding scheme. One of the bonded wafers is thinned to an etch-stop layer, the buried oxide layer (BOX) in SOI wafer. Subsequently, vias are etched in the wafer stack, followed by the inter-wafer interconnects formation using Cu/barrier deposition and CMP. If required, a third wafer (or more) can be aligned, bonded, thinned and inter-wafer interconnected with the same process flow by face-to-back bonding method to achieve multi-layer 3D structures.

RTI develops the 3D integration platform for the infrared focal plane array detector (IR FPA device) application, using similar adhesive bonding and TSV approaches from RPI [9]. Fig. 3 demonstrates the cross section of the advanced 3D integrated IR FPA structure. The epoxy material is used as the bonding adhesive, and the via density in this structure is 65,536 cm^2 (256 × 256 vias). The signal conductive yield is over 99.9% with the successful demonstration of thermal image detection.

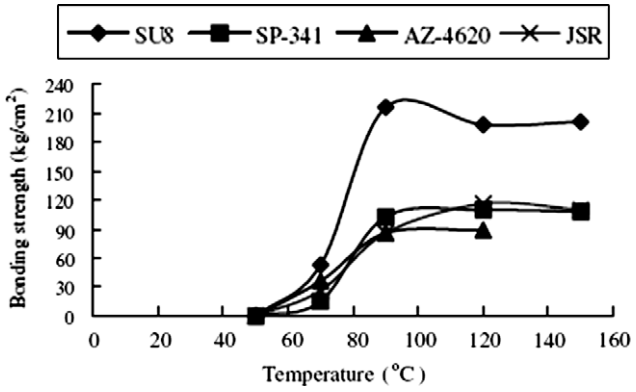

Fig. 1. The relationship between bonding strength and bonding temperature of the four adhesive materials [1].

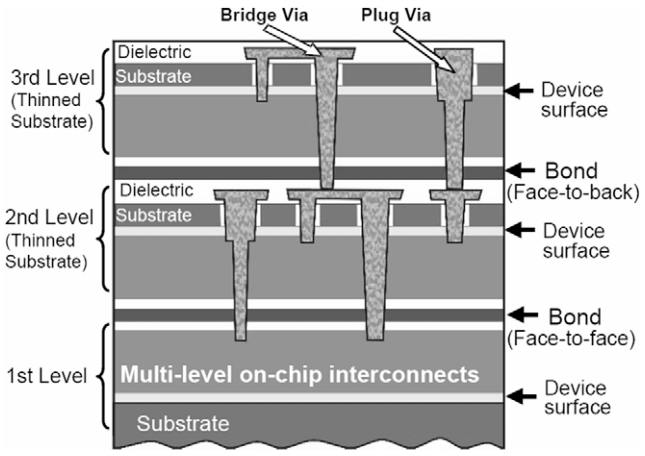

Fig. 2. Schematic representation of stacked bonding structure in the RPI 3D integration platform [7].

3. Metal diffusion bonding

The use of metal diffusion bonding (thermo-compression bonding) in 3D applications allows the mechanical and electrical connections to be made between two wafers in one step process. In this scheme, the metal pads are usually directly adopted for metal diffusion bonding. The common metal materials include Cu–Cu and Au–Au wafer bonds. Table 1 shows and compares the relative bonding conditions and bonding strength. In general, the Cu–Cu bonding temperature needs to be higher than 350 °C, and the bonding time larger than 30 min is also necessary. The research team of Professor Reif in MIT has done a series of extremely in-depth investigation on Cu–Cu bonding [10–12]. Fig. 4 demonstrates the morphology and strength map for copper wafer bonding under different bonding temperatures and conditions. Fig. 5 shows an example of the bonding interface comparison with and without annealing treatment [12]. Under this bonding condition, after annealing, no interface but Cu grain structure appears. Finally the bonding strength is increased and higher than 50 MPa.

For Au–Au wafer bonding, the general bonding temperature is about 300 °C with around 10 MPa bonding strength. However,

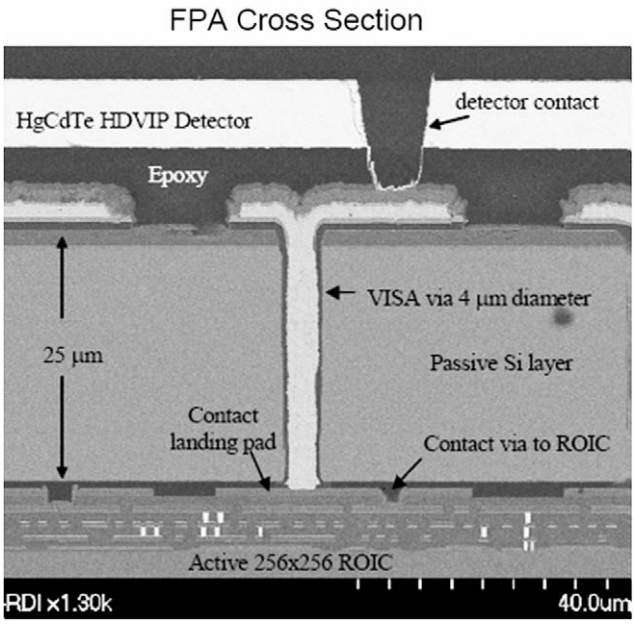

Fig. 3. The cross section of the advanced 3D integrated IR FPA structure developed in RTI [9].

Table 1
Comparison of different metal bonding conditions and strengths (the values inside bracket indicate specific conditions disclosed in few papers).

	Cu to Cu	Au to Au	Au to Au
Plasma treatment	N/A	N/A	Ar or N_2, >150 W, 10 min
Bonding temperature (°C)	350–400	~300 (298)	150–200
Bonding pressure (mbar)	140–8000	>10,000 (5000)	8000 (4000)
Bonding time	>30 min	45 min	10 min (30 min)
Tensile bonding strength (MPa)	~50	>10	30–50
Annealing	350–400 °C, 60 min	N/A	200 °C, 30 min or not

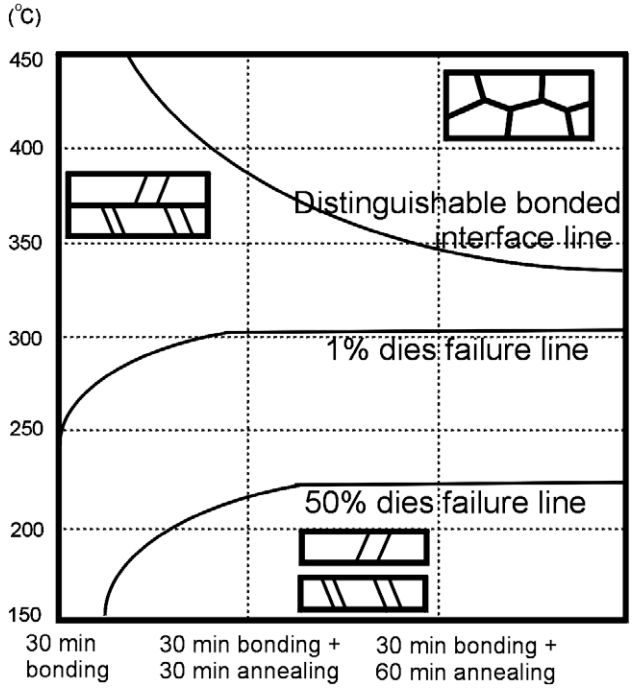

Fig. 4. Morphology and strength map for copper wafer bonding under different bonding temperatures and conditions [12].

the bonding process requires a high bonding pressure (generally >10,000 mbar except a few show 5000 mbar) [13]. According to the research from ITRI, if Ar or N_2 plasma treatment is performed to clean and activate the metal surface before bonding, the bonding

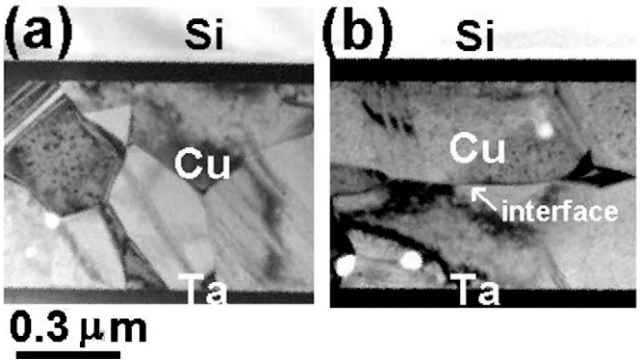

Fig. 5. TEM morphologies of (a) "grain" (bonded at 350 °C for 30 min followed by N2 annealing for 60 min) and (b) "interface" (bonded at 350 °C for 30 min) [12].

Table 2
The bonding technology comparison (Ref: EVG).

Bonding technology	Cu–Cu thermo-comp	Polymer (BCB)	Direct oxide
Bond accuracy (μm)	1.8–2	1.8–2	1.3–1.5
Future bond accuracy (μm)	1.2	1.2	<0.5
Process time per wafer (min)	60–120	30–60	3–6
Process chambers	4	4	1
Throughput (wafers/h/chamber)	2–4	4–8	10–20

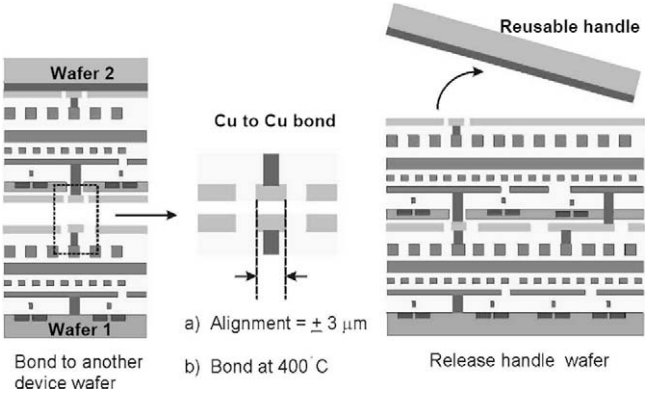

Fig. 6. The 3D integration scheme using Cu–Cu wafer bonding in MIT [16].

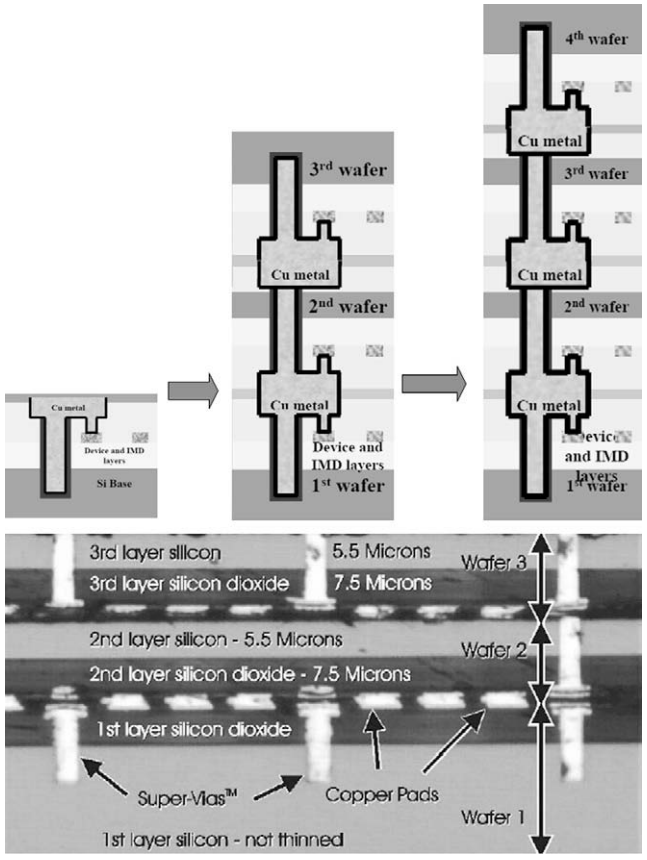

Fig. 7. The stacked scheme and cross section structure in the Tezzaron 3D integration platform [18].

temperature can be effectively dropped to 150 °C or lower, and the bonding pressure can be reduced under 1 MPa as well. The tensile test results also indicate that the bonding strength is increased to 30–50 MPa. With annealing after bonding, the strength can be further raised about 20% [14].

With outstanding electrical properties, compatible with current IC processes, and lower cost than gold, copper diffusion bonding is still the mainstream for 3D applications, though Au–Au bonding method has the superiority of lower bonding temperature than Cu–Cu bonding. Table 2 shows the bonding technology comparison from EVG. The long process time and small throughput are still the issues in Cu–Cu diffusion bonding technology. Considering mass production for 3D IC applications, Cu–Cu bonding with high yield and throughput will be the must requirement and important target in the future.

The 3D integration scheme developed in MIT is shown in Fig. 6 [15,16]. Two FEOL active device wafers are stacked in a back-to-face fashion and bonded together by means of Cu–Cu diffusion bonding method. To start with, the front side of the top layer on SOI wafer is attached to a handle wafer. The SOI wafer is then thinned back, created the Cu vias and pads, aligned, and bonded to the bottom device layer. The bonding temperature is 400 °C, followed by post-bonding annealing step for further inter-diffusion at the Cu–Cu interface to promote grain growth. After the handle wafer is released, the 3D structure is complete as shown in Fig. 6.

Tezzaron has used Cu–Cu stacked bonding technology to fabricate fully functional devices, including a variety of standalone memories, CMOS sensor, 3D FPGA, mixed signal ASIC, and processor/memory stack [17]. The stacking method uses (a) wafer-level, (b) via-first, (c) face-to-face first followed by face-to-back stacked fashion, and (d) Cu–Cu diffusion bonding. Fig. 7 illustrates this 3D stacked scheme and cross-sectional structure using copper metal bonding higher than 300 °C [18]. The total height of the stack with several layers increases only by about 15 μm per wafer. Therefore, even a stack of many layers can be housed in the normal packaging. After the stack is completed, the substrate of the bottom wafer can be thinned and finished with standard wire bonding or flip chip assembly.

4. Eutectic bonding

Eutectic wafer bonding is another option for advanced MEMS packaging and 3D integration. Since the eutectic temperature of two metals is lower than their melting points, the wafer bonding with the binary (or more) metal system under their eutectic point can be achieved at low temperature. A unique feature of eutectic metals is the melting of the solder-like alloys that facilitate surface planarization and provides a tolerance of surface topography and particles. At present, the commonly used materials include Cu–Sn, Au–Sn, Au–Si, and Sn–Pb. For Cu–Sn case, the bonding temperature is 150–250 °C. A post aging process, 250–300 °C for 5 min, is necessary to let the unstable Cu_6Sn_5 IMC completely transfer to the stable Cu_3Sn phase. However, the electromigration (EM) intrinsic reliability issue of the Cu–Sn microconnections has to be addressed because of the increased demand for higher interconnect densities and reduced bump size [19]. The eutectic bonding temperatures for Au–Sn and Au–Si are 290 °C and 363 °C, respectively [20]. The temperature for Sn–Pb is 183 °C, which is a mature and low temperature electrical bonding method. However, this approach is

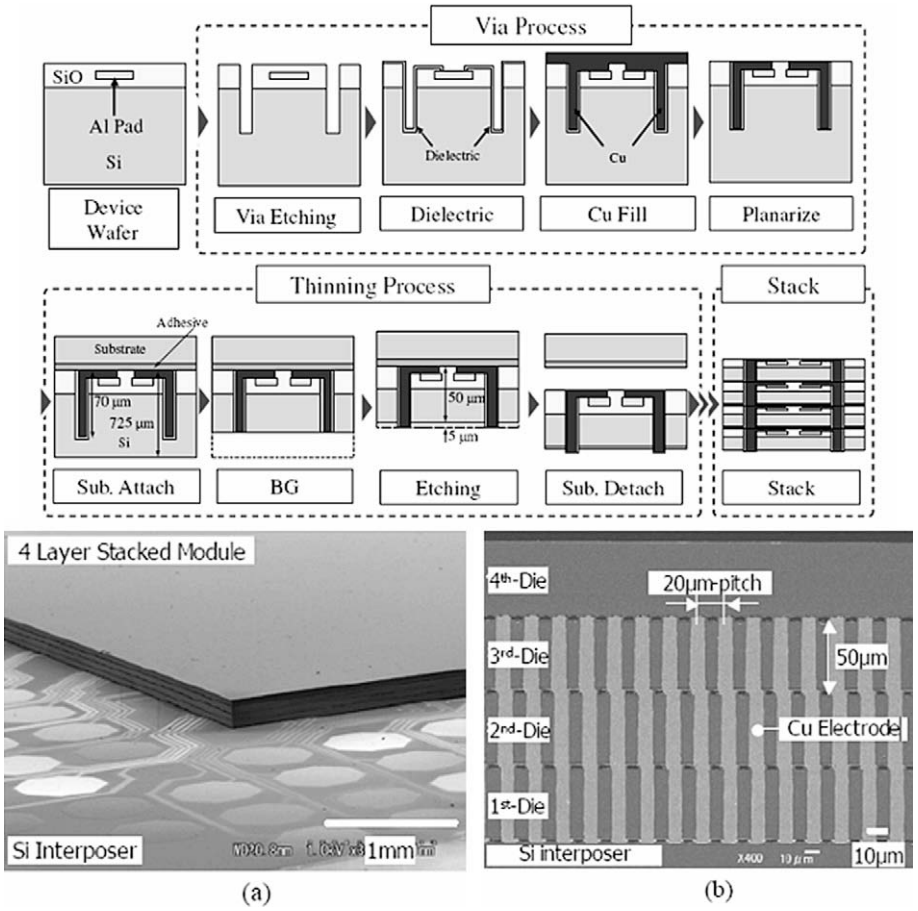

Fig. 8. The process flow and finished four layer stacked module developed in ASET [18].

not preferred due to the lead-free tendency for all electronic products.

ASET has developed Cu–Sn connection technique in stacking integration for micro-pitch connection and stacking connection of thin chips [21,22]. Fig. 8 shows the process flow and finished four layer stacked module developed in ASET. The via-first process is used, followed by thinning process to protrude the TSV stick for Cu–Sn stacked bonding. Here tin is deposited by electroless plating method, and finally forms the Cu_3Sn IMC with copper after eutectic bonding. Four layer stacked module on Si interposer is achieved with 20 μm pitch TSV and 50 μm each chip thickness, as shown in Fig. 8.

In IZM, the so called ICV-SLID technology [23] is optimized for chip-to-wafer stacking and provides a very high vertical interconnect density (>10^5 cm^{-2}) based on inter-chip vias (ICV) between metallization levels of stacked dice. Both the mechanical and vertical electrical connections are realized by solid–liquid-inter-diffusion (SLID) of thin electroplated and structured copper/tin layers [24]. Fig. 9 shows the 3D integration structure developed with ICV-SLID technology. The thinned chips with tungsten- or copper-filled inter-chip vias are connected to the bottom device wafer by the SLID system (Cu, Cu_3Sn, Cu). Here the wafer thickness is down to 10 μm with ICV size 2 μm only. Thermal bonding conditions (260–300 °C and 5 bar) are used to compose the stable Cu_3Sn alloy. The fully modular concept allows the formation of multiple device stacks.

ITRI's research mainly focuses on the integration of low cost Laser-drilled Through Silicon Interconnect (LTSI) technology [25–27]. There are four major processes in the LTSI process flowchart, including wafer thinning, direct laser drilling/patterning, insulation layer formation and PCB compatible via filling/wet etching. This provides more advantages than other competing technologies not only in the compatibility with low cost silicon-through processes but also in the flexibility to the inter-chips or inter-wafers assembly of connecting different components. The feature of this structure is the through-hole copper interconnect with polymeric material insulation. In addition, Cu–Sn eutectic bonding is studied for chip-to-wafer silicon-through vertical interconnect of 3D stacking packaging. The average value of contact resistance ranges from 0.74 mΩ to 1.5 mΩ, and the reliability test also shows good results on the 3D chip stacking structure. Fig. 10 demonstrates the 20-chip stacking performed with LTSI and Cu–Sn bonding technologies [28]. The corresponding X-ray image is shown to realize the well 3D interconnection and integration on the stacked chips.

5. Silicon direct bonding

Silicon direct bonding, also as known as fusion bonding, is the spontaneous adhesion of two wafers placed in direct contact. The Si-to-Si and SiO_2-to-SiO_2 wafer bonding are the major targets. This method describes the room temperature bond between wafers with or without dielectric layers, followed by a wet chemical or plasma activation step. The wafer surface needs to be very smooth with small total thickness variation (TTV). In bonding process, two-step technique is performed with room temperature contact followed by a high temperature anneal, typically, 1000 °C, to let the interface change from hydrogen bonds to strong covalent bonds (Si–O–Si). It offers a high bonding strength in combination with stress free and hermetic sealed bonded structures. However, the high anneal temperature is higher than thermal budgets of some applications, and the method is very sensitive to particle contamination. It has been reported that a particle with a diameter of 1 μm can cause a 1 cm in diameter void when bonding an 8-in wafer [29].

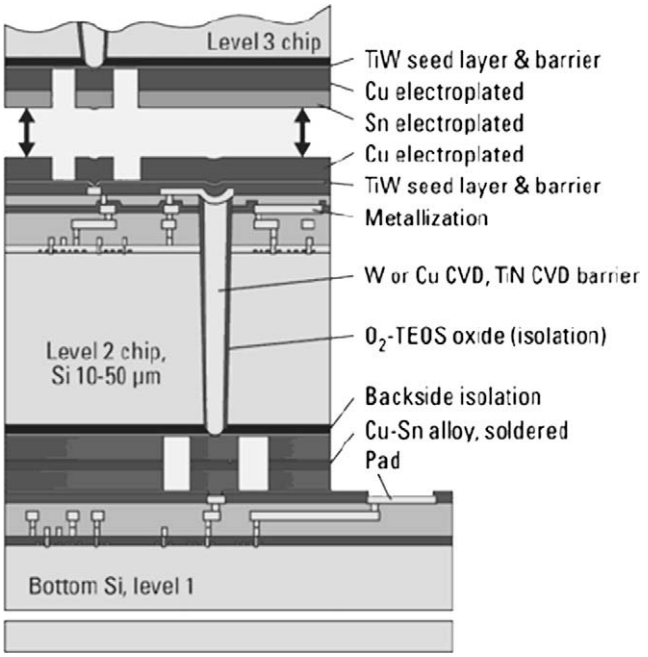

Fig. 9. The 3D integration platform developed with ICV-SLID technology in IZM [24].

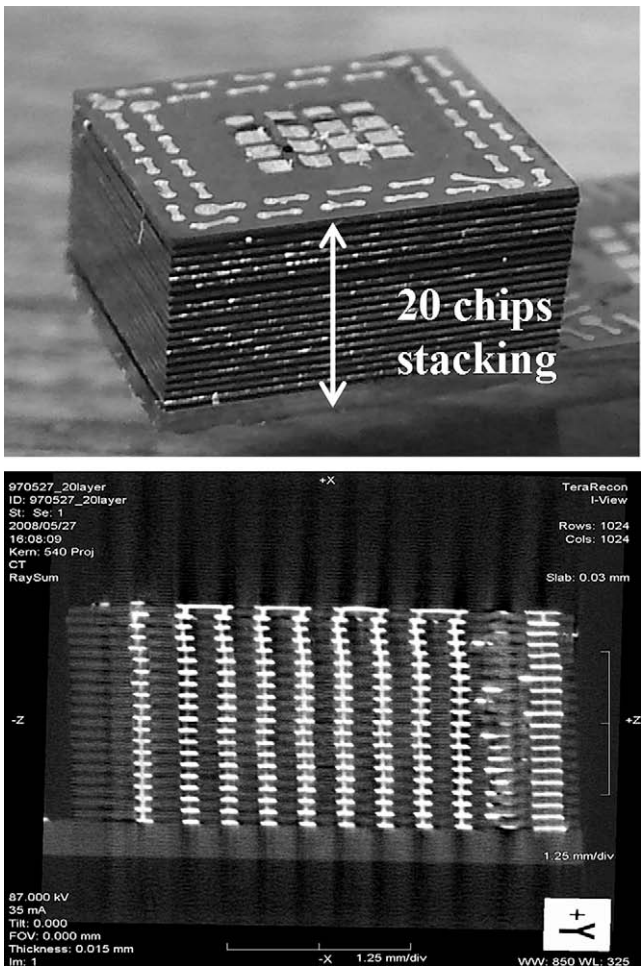

Fig. 10. 20-Chips stacking performed with LTSI and Cu–Sn bonding technologies in the ITRI 3D platform, and the corresponding X-ray image [28].

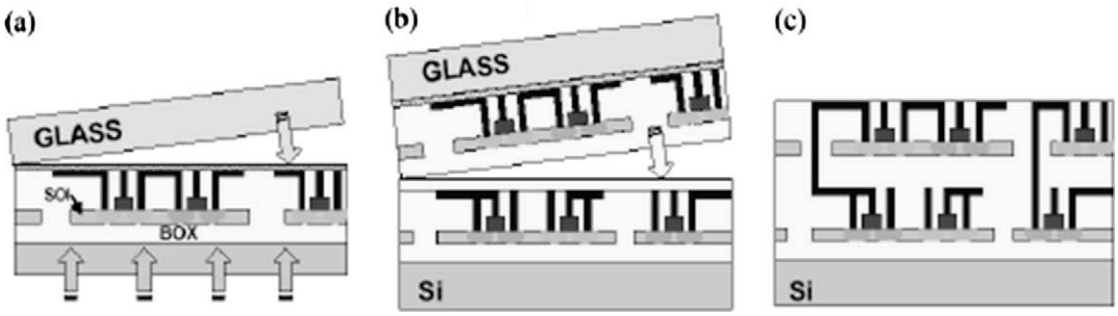

Fig. 11. Schematic representation of layer transfer and silicon direct bonding technologies in the IBM 3D integration platform [8].

One method of IBM 3D integration platforms uses silicon direct bonding approach for the permanent wafer bond [30]. As shown in Fig. 11, the front side of device SOI wafer is temporary bonded first to a glass handling wafer by organic adhesive. The device SOI wafer is then thinned to an etch-stop layer, the oxide layer (BOX) in SOI wafer, sequentially aligned and bonded to a second pre-processed device Si wafer using wafer bonding with inorganic dielectric layers (SiO_2). The wafer bonding process is chemically or plasma activated oxide-to-oxide fusion bonding, which is compatible with BEOL wafers. After the temporary glass handle wafer release, the inter-wafer vias are fabricated using Cu damascene process. The via size is 0.2 μm only with 2 μm depth around, which means each stacked layer is about 2 μm increase in total thickness, and the via density reaches to a high number of 10^8 cm^{-2}. If required, a third wafer (or more) can be further added to achieve multi-layer 3D structures. Another approach for comparison is the integration where SiO_2 direct bonding takes place without a handling substrate, which means the bulk lower wafer and SOI upper wafer are fabricated and bonded face-to-face, and then TSVs are formed after backside thinning to the BOX of SOI wafer [31].

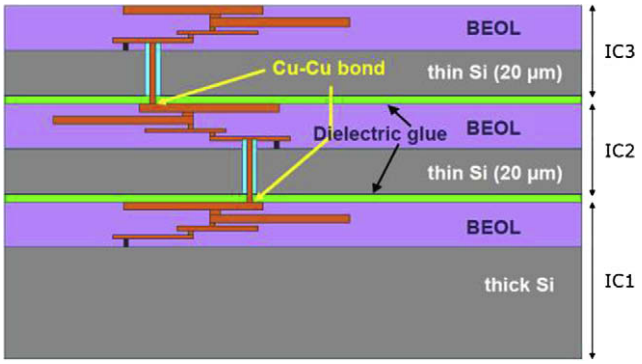

Fig. 12. Illustration of the 3D-SIC concept in IMEC: dies are separated by a thin dielectric glue layer, and interconnected through silicon Cu vias (TSVs) [34].

6. Hybrid bonding

Hybrid bonding is one emerging approach for wafer-level 3D integration [32–36]. It combines metal-to-metal bonding and wafer bonding with organic adhesives (ex. BCB) or inorganic dielectrics (ex. oxide), which can achieve intrinsic metal interconnection with adhesive serving reinforcement of the mechanical stability between stacked ICs. Because the adhesives or dielectrics can simultaneously act the roles of bonding material and underfill, they effectively increase the bonding strength and raise the device reliability. Moreover, because the electrical interconnect and micro-gap filling can be fabricated at the same time, it simplifies the process flow and avoids the micro-gap filling challenge, and therefore increases the throughput and yield.

IMEC is developing the simultaneous Cu–Cu and compliant dielectric bonding for 3D stacking, named collective hybrid bonding [34,36]. It combines fixation of a thin wafer or die by means of dielectric adhesives with the formation of metal interconnects. Fig. 12 shows the illustration of the 3D-SIC (3D-Stacked IC) concept with the hybrid bonding concept by IMEC. The introduction of a tacky polymer as an intermediate glue layer in the direct bonding scheme offers the possibility for die-to-wafer throughput optimization. The method includes pick-and-place of die and then bonding operations, as shown in Fig. 13. First, the TSV-dies are aligned and placed onto a landing wafer on which the polymer glue layer has been previously processed and patterned. This patterned tacky dielectric weakly bonds the stacked dies and fixes them during further handling. The operation is performed ideally at low temperature with the pick-and-place process repeated until the full wafer is populated. In second step, the fully populated wafer is moved to a wafer-level bonding tool where pressure and heat are applied to all stacked dies at once. Thus, the dielectric layer reflows and the metallic interconnect bonding is performed for all stacked dies simultaneously. BCB is one of the candidates as the glue material in this approach. After collective hybrid bonding of TSV-dies to a landing wafer, electrical measurements of daisy chains show a comparable and reproducible yield of 80% with working chains up to 1000 TSVs.

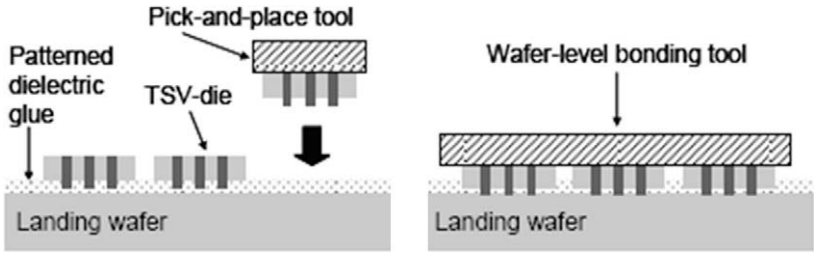

Fig. 13. Illustration of the die pick-and-place and the collective hybrid bonding process [36].

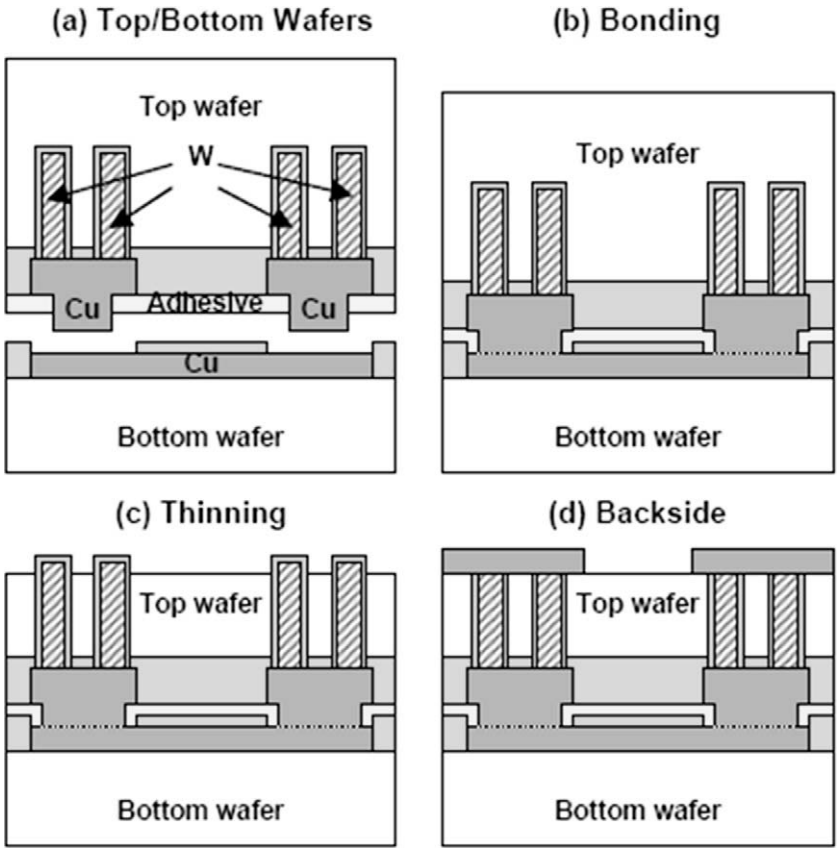

Fig. 14. Schematic diagram of 3D process flow developed in IBM [35].

In IBM, a 300 mm wafer-level three-dimensional integration (3DI) process using tungsten TSVs and hybrid Cu/adhesive wafer bonding is demonstrated [33,35]. The process flow for 3DI technology is shown in Fig. 14. The W TSVs have fine pitch (5 μm), small critical dimension (1.5 μm), and high aspect ratio (17:1). Lower CTE mismatch with surrounding Si and associated thermo-mechanical reliability benefits are included by using W TSV fill. However, because CVD W deposition results in very high stress film during deposition and is difficult to deposit more than about 1 μm thickness, design of W vias is suggested as less than 2 μm diameter with tight pitch. After W TSV formation, oxide insulation and Cu studs are formed on the top wafer. The bottom wafer utilizes Cu pads with recessed polymer adhesive openings. The wafers are then aligned and bonded in vacuum using hybrid Cu/adhesive bonding approach, also called transfer-join (TJ) method. After bonding, the top wafer is thinned to 20 μm in feature, and backside Cu metallization is patterned. The image of a completed 300 mm 3DI wafer after depositing and patterning of the backside Cu BEOL metallization is shown in Fig. 15. The electrical and physical properties of the TSVs and bonded interconnects are presented. RLC values show that both the power delivery and high-speed signaling requirements are satisfied for high-performance 3D systems.

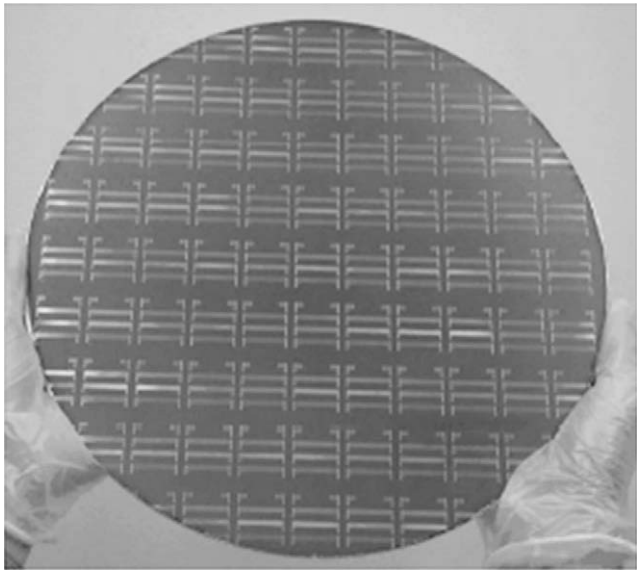

Fig. 15. Photograph of a completed 300 mm 3DI wafer [35].

7. Conclusions

This review paper summarizes wafer-level bonding technologies for 3D integration. Corresponding 3D integration technologies and platforms developed in world-wide companies or institutes are also introduced. Advantages and disadvantages of each bonding technology are discussed. Adhesive bonding has better particle contamination tolerance on wafer surface. However, this technology has potential contamination concerns on devices and fabrication tools. Metal diffusion and eutectic bonding provides direct interconnection, but un-bonded area with air gap may result in reliability issues. Silicon direct bonding provides high via density and better alignment, but the requirements of clean surface and bonding environment are very significant. Hybrid bonding, combines metal and adhesive/oxide bonding, can simultaneously achieve interconnect with adhesive serving reinforcement of the mechanical stability between stacked ICs. With high yield and

reliability superiority, hybrid bonding has become an emerging approach for 3D integration.

Acknowledgements

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