Fabrication and Packaging of Microbump Interconnections for 3D TSV

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Abstract

Memory bandwidth has become a bottleneck to processor performance for tera-scale computing needs. To reduce this obstacle, a revolution in package technologies is required for tera-scale computing requirements. 3D TSV (Through Silicon Via) stacking is believed to be one of the technologies that can meet those requirements. In advanced 3D stacking technologies, one of the important steps is to develop and assemble fine pitch, high density solder microbumps. This type of solder microbump in flip chip interconnection provides a high wiring density in silicon die with a high-performance signal and power connection. There is a growing interest in the development and study of this new type of chip stacking and bonding approach for both existing and future devices.

This paper will highlight the developments of ultra fine pitch and high density solder microbumps for advanced 3D stacking technologies. A Cu/SnAg solder microbump with 50/40 µm in pitch was fabricated at the silicon wafer level by an electroplating method. The total thickness of the plated Cu and SnAg microbump was 20um. The under bump metallurgy (UBM) layer on the Si carrier used thin film based metal layers. The assembly of the Si chip and the Si carrier was conducted with the thermocompression flip chip bonder at different temperatures, times and pressures and the optimized bonding conditions were obtained. After assembly, the underfill process was carried out to fill the gap and achieve a void free underfilling using a material with a fine filler size. Finally, various reliability tests were carried out for mechanical characterization of microbump interconnections.

I. INTRODUCTION

One of the hottest topics in the semiconductor industry today is 3D Packaging using Through Silicon Via (TSV) technology. While many research programs have been underway for years, no commercial product has been realized yet. Driven by the need for improved performance and the reduction of timing delays, methods to use short vertical interconnects have been developed to replace the long interconnects found in 2D. The industry is moving past the feasibility (R&D) phase for TSV technology into the commercialization phase, where economic realities will determine the technologies that can be adopted. Low-cost, high aspect ratio, reliable via formation and via filling technologies is need of the hour[1]. Nowadays, memory bandwidth becomes a bottleneck to ASIC/processor performance for tera-scale computing needs. Therefore, revolution in package technologies is required for tera-scale computing requirements [2].

Three-dimensional (3D) stacking is believed to be one of the technologies that can meet these requirements. In advanced 3D stacking technologies, one of the important steps is to develop and assembly fine pitch and high density solder microbumps. Solder microbumps for flip-chip interconnections allow high wiring density in the Si-carrier, as compared to organic or ceramic substrates, and also enable high-performance signal and power connections [3].

The demand for high density and multifunctional microelectronics leads to the development of 3D and wafer level packaging, which provides an optimal solution for the shortened interconnects, increased performance and functionality, miniaturization in size and weight, integration of hetero-generous technologies and complex multi-chip systems as well as reduced power consumption. [4]

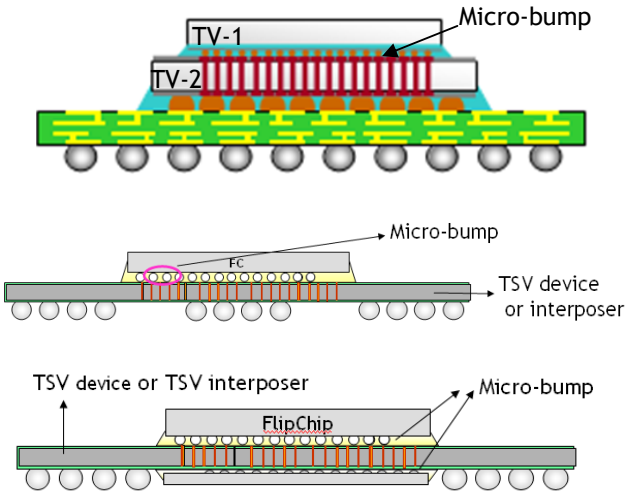

Figure 1. Various package types of the Si chip of microbump and TSV in flipchip packaging

Solder bumps are widely used to form electrical interconnect in flip chip technology for IC packaging. Currently, solder bumping techniques for bump pitch of 100 to 200 micrometers are available in industry. As packaging

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size is scaling down continuously with increasing demands for high I/O density, cost-effective fine-pitch solder microbumps are highly demanded for high-density, high-performance, and miniaturized 3D IC packaging.

Micro bumping technology where bump pitches are less than 50 micrometers using solder is explored extensively in the industry for realization of miniaturized 3D IC integration. Different solder and under bump metallurgy (UBM) material systems, fabrication process of solder microbumps as well as assembly process with those solder microbumps have been studied with the objective to develop reliable fine pitch solder micro joints at low cost. Fig.1 shows the schematics of 3D TSV stack packaging with TSV and microbump technology.

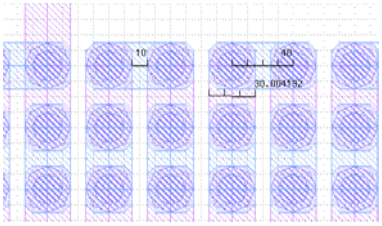
The fine pitch solder microbumps can be applied to chip-to-chip or chip-to-wafer assembly. This is an important step to realize microbumping technology for miniaturized 3D stacked packaging.

In this paper, microbump test vehicle fabrication, Chip-to-Wafer (CTW) bonding assembly process and its reliability test as well as characterization are discussed.

II. TEST VEHICLE FABRICATION

To evaluate how TSV packaging/assembly works with microbump, test vehicles (TV-1, TV-2) were fabricated on 8 inch size wafer. A test chip TV-1 of 5 X 5 mm2 size is designed with 10000/6000 off-chip interconnects at 40 / 50 μm pitch in fully populated rows using Re-distribution layer (RDL) to evaluate the CTW bonding test, as shown in Fig.2 (a). Si substrate TV-2 was also designed for daisychain connection as shown in Fig 2(b). The substrate is designed according to the present test chip design. The test chip comprises of daisy-chain structures for interconnects resistance continuity measurements.

(a)



(b)

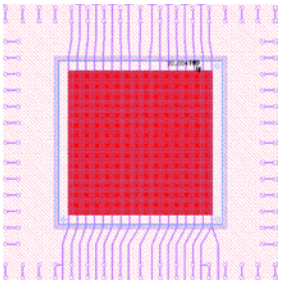


Figure 2. Test Vehicle Design; (a) TV-1 and (b) TV-2

Test vehicle fabrication is based on photolithography and electroplating processes, which is compatible with conventional IC fabrication. The fabrication process of wafer level process starts with bare Si wafer using Ultra Violet (UV) light lithography of spin on dielectric material. Secondly, Redistribution line (RDL) layer plating to re-route the Al/Cu bond pads to microbump locations. Thirdly, passivation of RDL layer using spin on dielectric coating and UV lithography to open the RDL metal pads at the bump pads. Fourthly, deposition of Ti/Cu seed layer and patterning of thick photoresist film using lithography to define the UBM pads, followed by UBM or copper pillar plating and then solder plating. Fig. 3 shows the test vehicle fabrication process flow. Schematics of cross-section of test vehicles interconnections are shown in Fig.4. And SEM micrographs of microbump are shown in Fig.5 for both 40μm and 50μm pitch.

After test vehicle fabrication, the microbump height and diameter and other dimensions are measured and characterized.

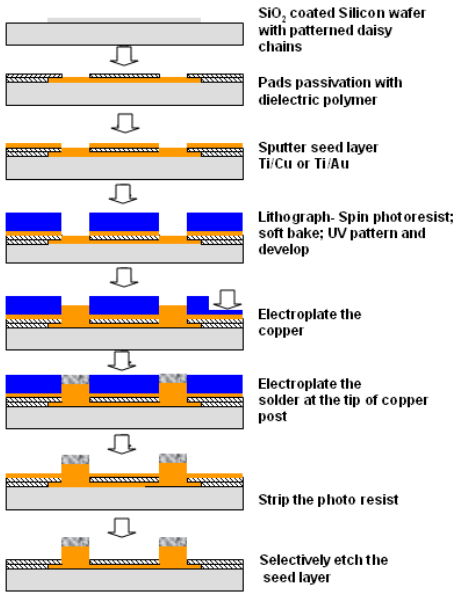


Figure 3. Test vehicle fabrication process flow

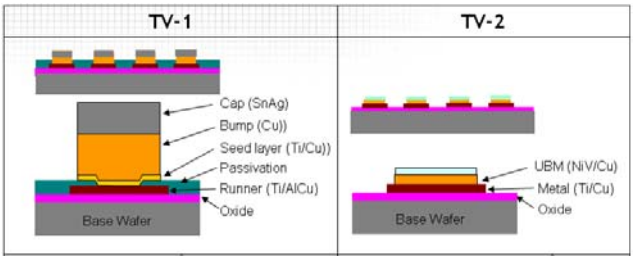


Figure 4. Schematics of cross-section of each test vehicle structure.

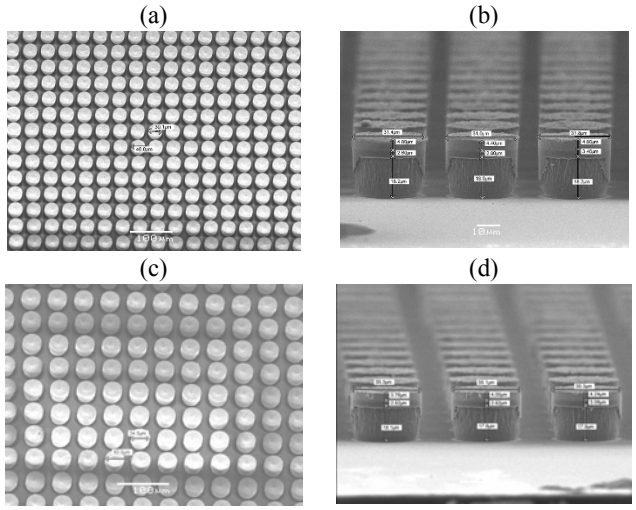
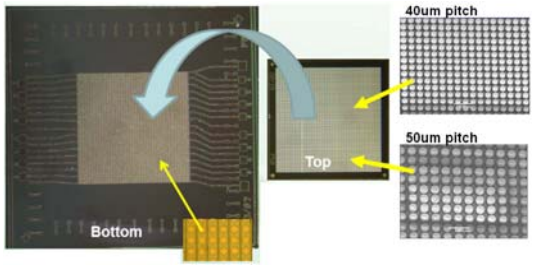


Figure 5. SEM micrographs of TV1 of top tilted view and side view of (a-b) 40µm pitch micro bump and (c-d) 50µm pitch micro bump.

III. ASSEMBLY AND PACKAGING

Flip chip package assembly was carried out to investigate the reliability with microbump flip chip. After flip chip die fabrication with bump, the die attachment was carried out with Thermo-compression flip chip bonders. One of optimized thermocompression bonding process with parameters is shown in Fig.6. Bonding head temperature with 300°C single step and flux was pre-deposited before bonding process. Bonder applied head height control with 3 steps.

(a)



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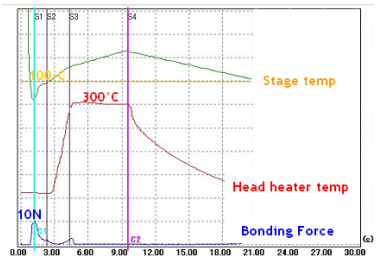

Figure 6. (a) CTW bonding of 40/50µm pitch microbump and (b) CTW bonding key parameters during thermo compression bonding process.

After bonding and assembly process, the resistance was measured to check the daisy chain interconnection. Details of reliability tests For microbump interconnects are described in Table 1.

Table 1. Reliability Test Conditions

Rel Test	Conditions	JEDEC
Preconditioning	MSL-3	J-STD-020
		JESD22-A113
HAST (Unbiased)	130°C, 85% RH	JESD22-A118
	(96hrs)	
Temp Cycling (TC)	-65°C/150°C	JESD22-A104
	(500x)	
High Temp Storage (HTS)	150°C	JESD22-A103
	(1000hrs)	

IV. RESULTS

A. CTW bonding

Different assembly conditions were evaluated to achieve a good joining bond including bonding temperature, time and pressure. Quick assessments by checking fractural surface and mechanical shear strength were conducted to select proper bonding conditions.

The joining quality between the chips was characterized and several DOEs were carried out. Fig. 8 and 9 shows the SEM micrographs of cross-section of the two chips joined for 40 and 50µm pitch microbumps. It can be seen that successful joining is achieved. The shear strength of the chips joined at this bonding condition was relatively high (10 Kgf). The shear strength was found to be further improved by increasing the bonding load. However, high bonding loading can damage the die itself, especially for thin die and if in case of low/ultra low-k material on the die. In further studies and development of optimization of the bonding conditions is the next study topic. A misalignment of about 3µm was observed between the Si chip and the Si carrier after assembly as shown in Fig. 8. This misalignment was a result of accuracy limitation of the bonder equipment. In order to resolve this issue, the size of the solder micro bumps may be designed smaller than that of the UBM pad and high melting solder will be better approach to prevent less collapse and bump shape control. Shear test was performed to evaluate the bump and joint strength of the assembly, shear strength measurements of the package samples were carried out by a commercially available shear tester (DAGE-SERIES-4000-T, Dage Precision Industries Ltd, Aylesbury, UK). After shear test, the failure surfaces of the Cu/SnAg solder microbumps on the Si chip and the UBM pads on the TV-2 are observed. It can be seen that after shear, the joints are separated along the interfacial IMC near UBM. The dominant failure is ductile failure of the bulk solder of the solder joint. Average adhesion strength was around 10Kgf in die shear test.

In conclusion, 40µm pitch microbump bonding was successfully achieved with UBM patterned Si test vehicle

substrate and electrical connection in Daisychain was confirmed with electrical resistance measurement.

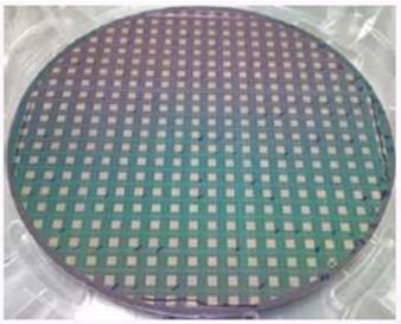

Figure 7. Picture of CTW bonding wafer

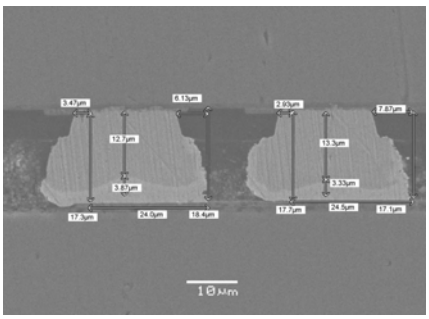

Figure 8. SEM micrographs of 40μm pitch microbump bonding.

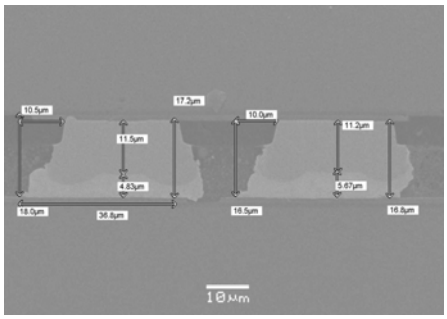

Figure 9. SEM micrographs of 50μm pitch microbump bonding.

B. Evaluation of underfill

In this work, the gap between the two jointed chips is about 15~20 μm; therefore it is important to evaluate the flow-ability of underfill and the void formation in underfill which contains silica-filler. Considering the fine CTW gap, fine filler size underfills were used to evaluate the underfill process. Scanning Acoustic Microscope (SAM) analysis was carried out to investigate the void formation or non-filled area by underfill. Through-SAM photograph of underfilled sample. It was observed that good filling without any void can be achieved with underfill resin containing very fine filler.

C. Reliability Test Results

40μm and 50μm microbump interconnects both were sent to reliability test. Reliability samples passed MSL-3 with 3x reflow process at Pb-free 260^{o}C peak temperature. All samples passed unbiased HAST and HTS reliability tests. There was no failure found after 500 T/C and 1000 T/C is still under testing. X-ray tool was used for observation of delamination of chip or pad as shown in Fig 10.

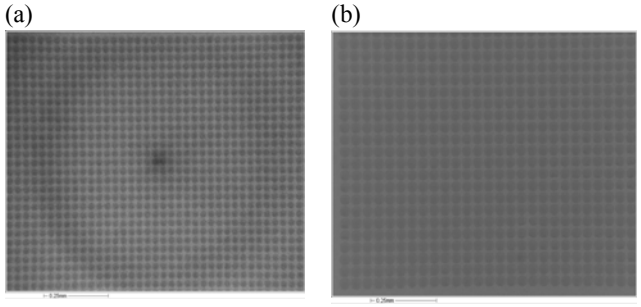

Figure 10. X-ray micrographs of (a) 40μm pitch and (b) 50μm pitch of CTW bonding.

V. CONCLUSION

The investigations of solder microbumps in 40μm and 50μm pitch and their assembly process are reported in this paper. The fine pitch solder microbumps can be used for F2F stacking of memory chip and microprocessor/ASIC chip as well as other 3D TSV systems in package. Some important results are summarized as

1. Cu/SnAg solder microbumps with 40μm and 50μm in pitch have been developed successfully. The ultra fine pitch and high density bump array can be used for face-to-face and 3D TSV flip chip stacking.
2. For Cu/SnAg solder microbumps in 40μm in pitch, the thickness of the SnAg solder cap should be thicker than 5μm and less than 10μm if the total bump height (Cu + SnAg) is kept to 20 μm.
3. Using current wafer level process, no technical issues were found in lithography and plating process. It is found that the design compensation and critical dimension control are the key issue in microbump fabrication.
4. As the gap between the two chips after assembly is about 15 ~ 20 μm, fine filler size underfill has used in this study and good filling without any void can be achieved.
5. With optimized bonding conditions (bottom temperature of 100^{o}C and upper temperature of 300^{o}C, 5 second, 20 MPa), good joining can be achieved between Cu/SnAg microbumps and UBM pads.
6. In this work, 40μm pitch microbump with Cu/SnAg successfully passed JEDEC standard reliability test.

7. There should be further study and development of assembly and packaging details, i.e. bump shape control, higher yield, improved CTW bonding UPH, solder-bump co-planarity, reliability tests (electromigration, diffusion etc.)

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