

From Technologies to Market

# 3DIC & 2.5D TSV Interconnect for Advanced Packaging Technologies & Market Trends

2016 - Business Update



Report sample



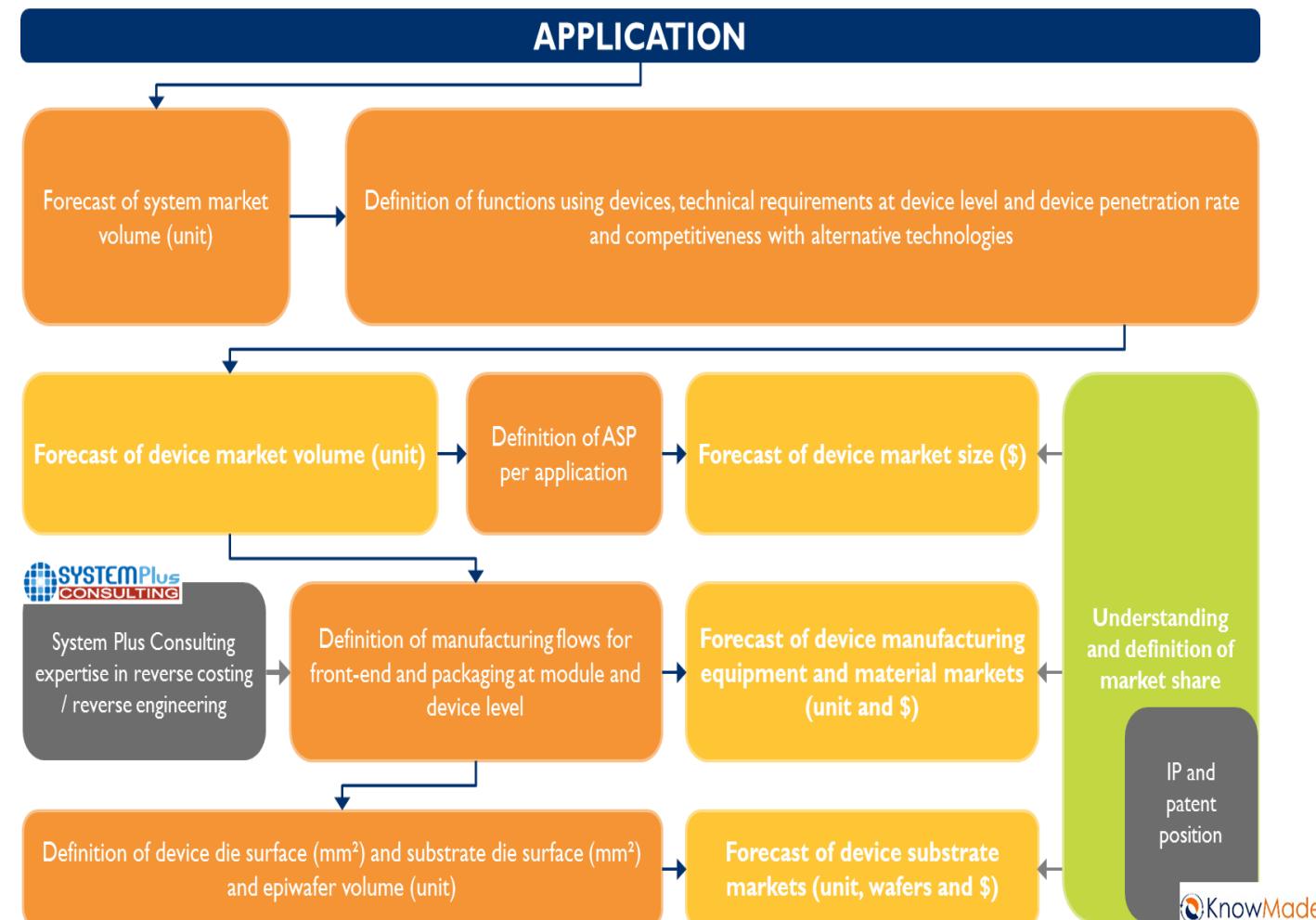
The objectives of this report are to provide:

- 3D/2.5D technology latest industry trends
- Wafer start forecast for different TSV application (Memories, MEMS, CIS, HBLEDs etc)
- Revenue & units forecast per TSV applications
- Detailed analysis of all TSV applications
- Commercialization status per product family
- Overview of TSV from different business models
- Key industrial market player's positioning: device makers, R&D centers, OSAT, foundries

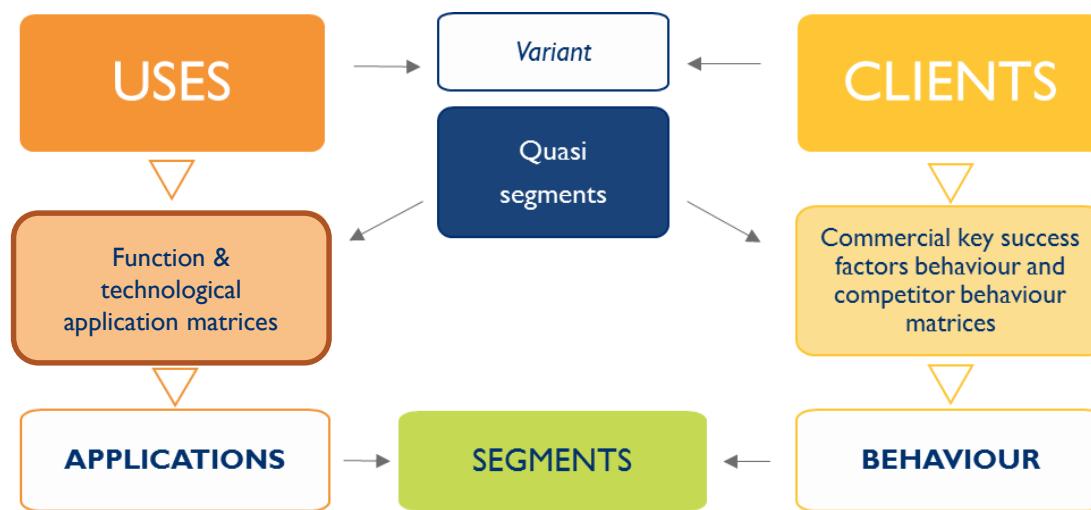
# REPORT METHODOLOGY (1/2)



## Market forecast methodology



## Market segmentation methodology



## Technology analysis methodology



## Information collection



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## Biography & contact



### Santosh Kumar

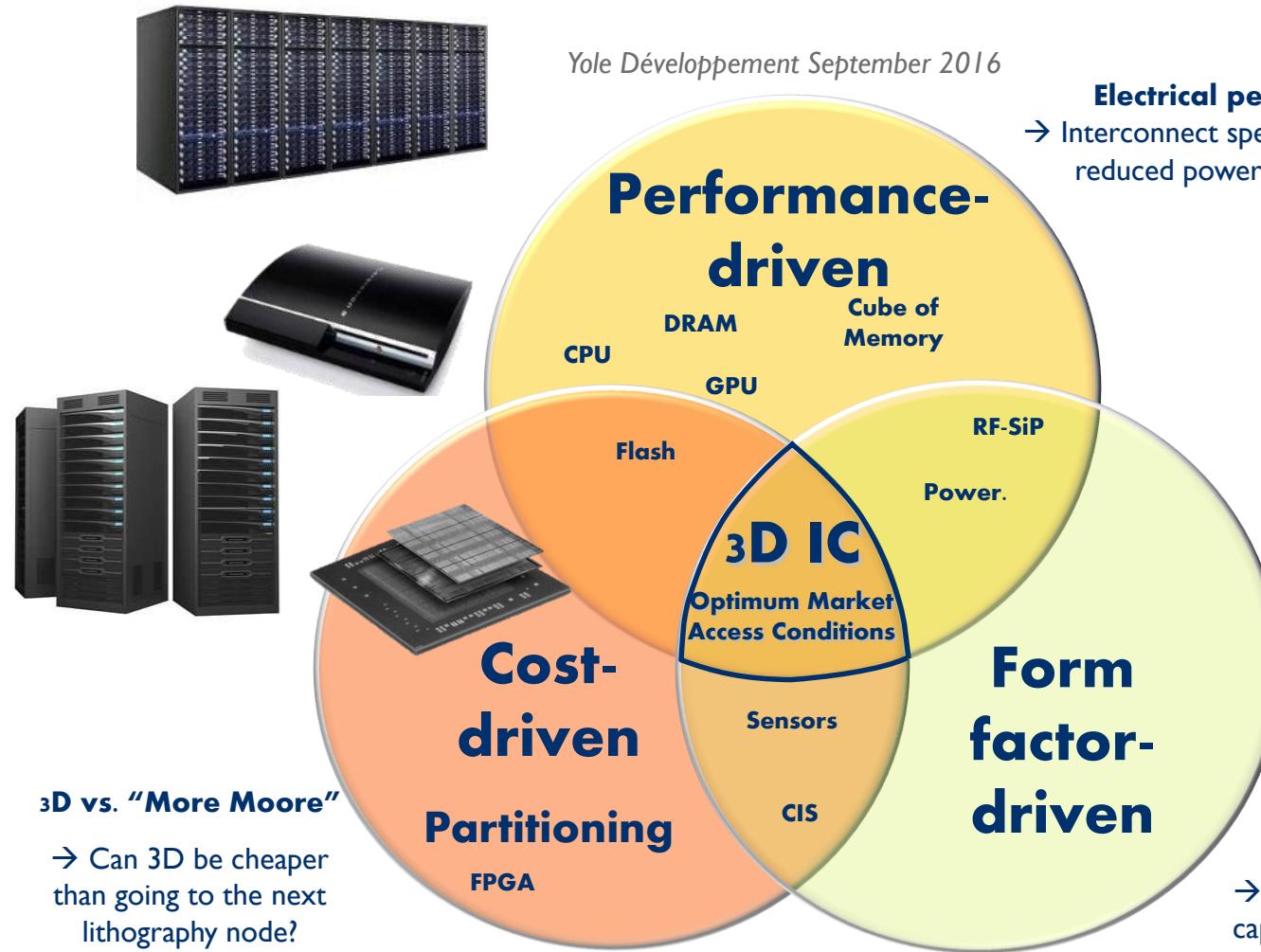
Santosh Kumar is currently working as Senior Technology & Market Research Analyst at Yole Développement, the "More than Moore" market research and strategy consulting company. He worked as senior R&D engineer at MK Electron Co. Ltd where he was engaged in the electronics packaging materials development and technical marketing. His main interest areas are advanced electronic packaging materials and technology including TSV and 3D packaging, modeling and simulation, reliability and material characterization, wire bonding and novel solder materials and process etc. He received the bachelor and master degree in engineering from the Indian Institute of Technology (IIT), Roorkee and University of Seoul respectively. He has published more than 20 papers in peer reviewed journals and has obtained 2 patents. He has presented and given talks at numerous conferences and technical symposiums related to advanced microelectronics packaging.

[kumar@yole.fr](mailto:kumar@yole.fr)



# Report sample

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**Electrical performance**  
→ Interconnect speed, bandwidth and reduced power consumption

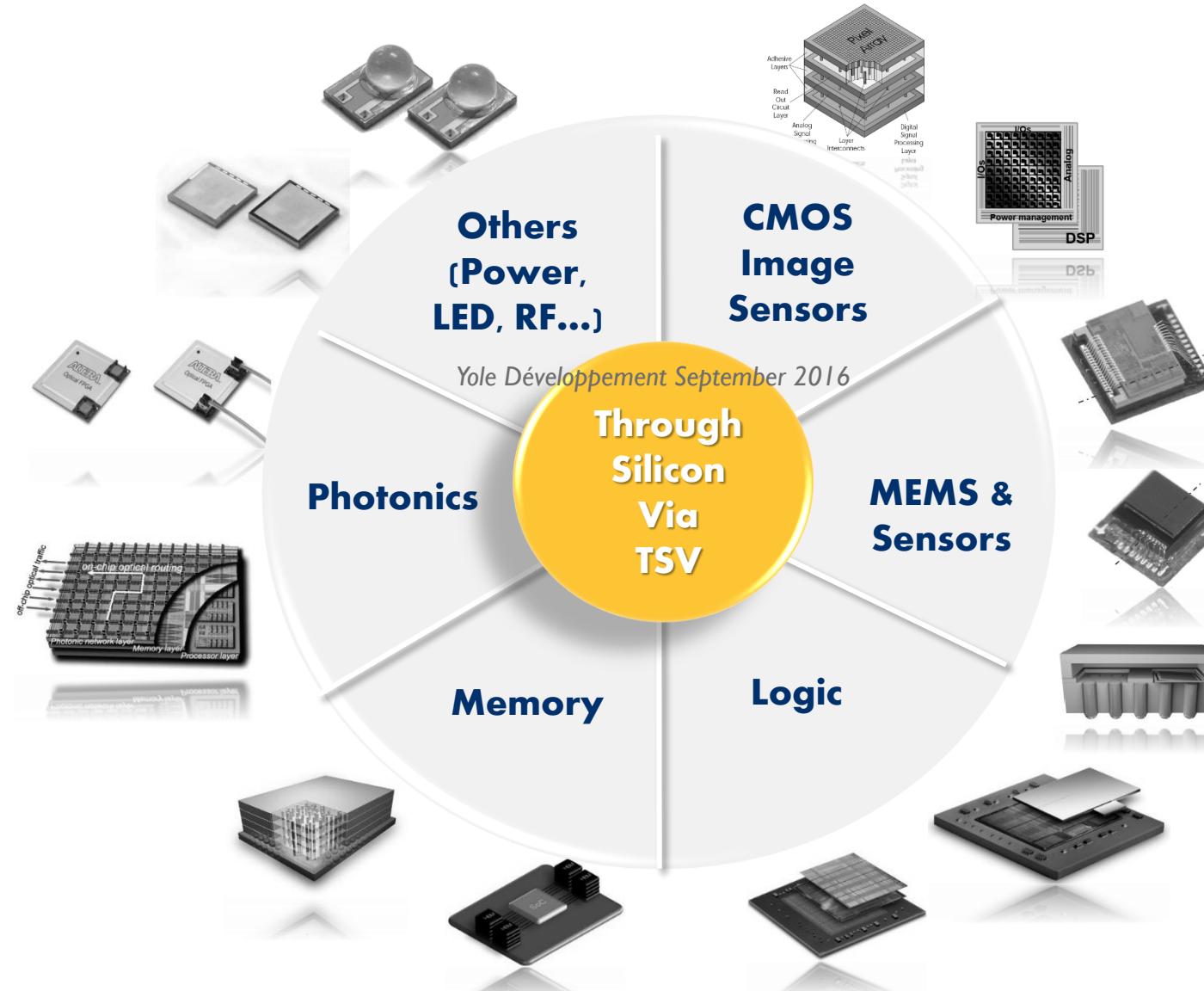
**"More than Moore"**  
**Heterogeneous integration**  
Co-integration of RF+logic+memory + sensors in a reduced space



**Density**  
→ Achieving the highest capacity / volume ratio



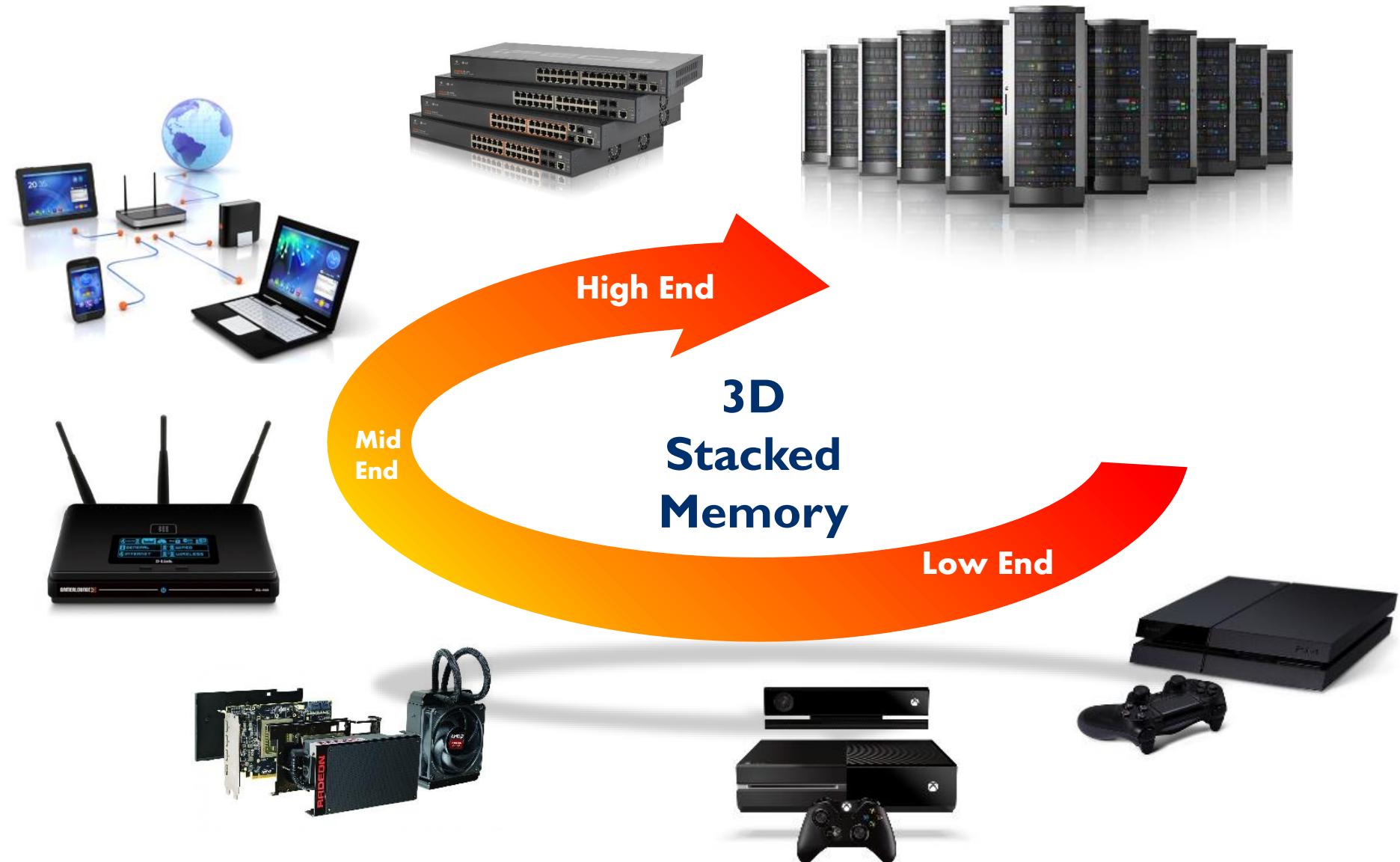
Broad range  
of application  
for 3D TSV!  
Keep growing!



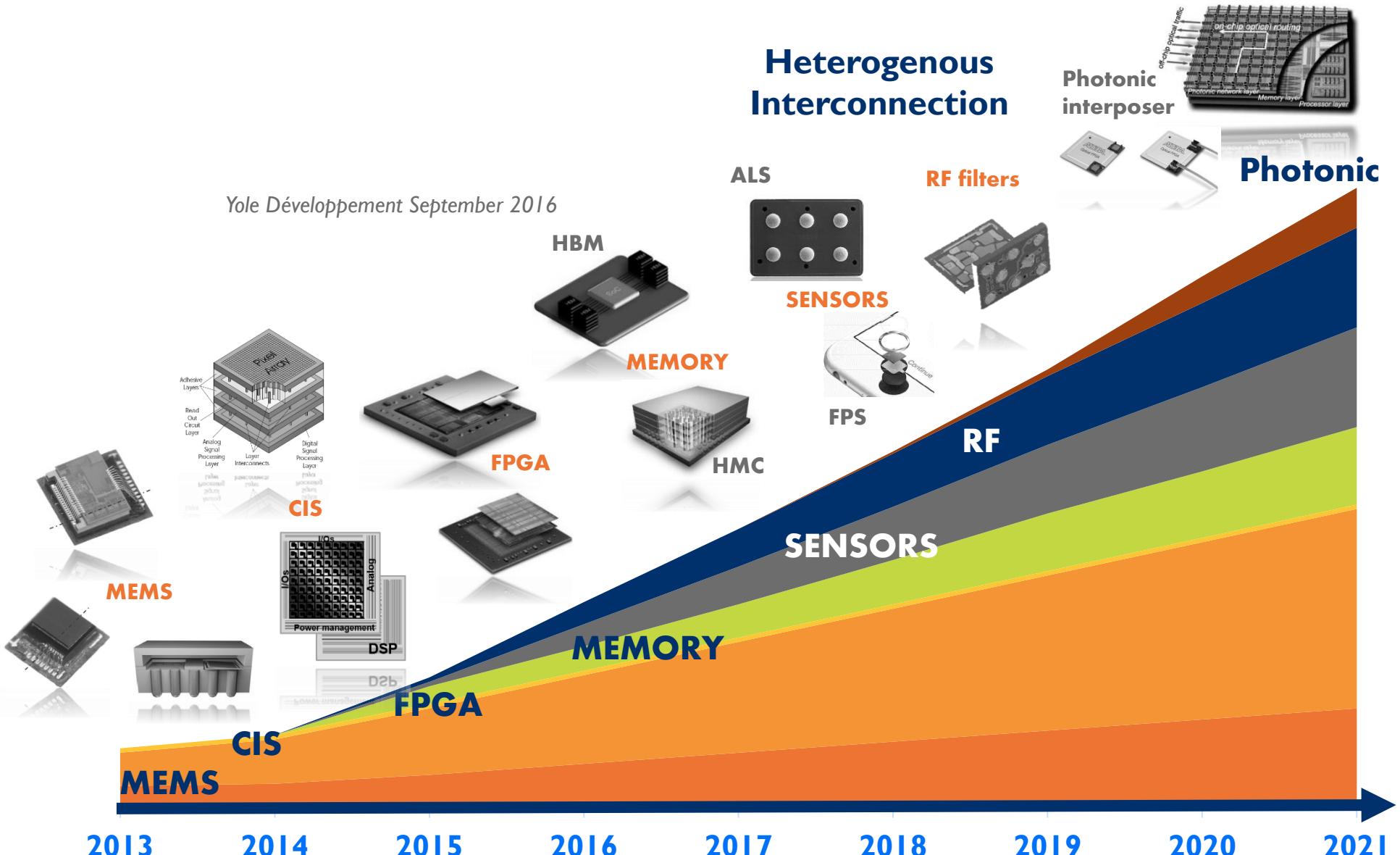
# MEMORY PRODUCTS WITH TSV – DRAM BASED



From game station to servers! 3D will have a broad scope of application

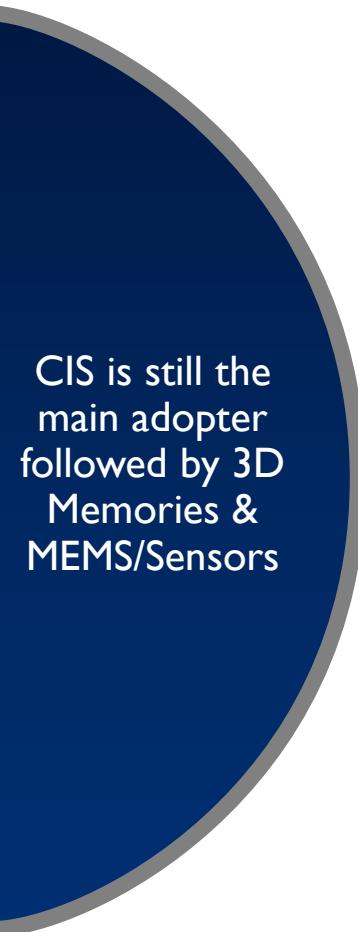


# TSV WAFER STARTS BREAKDOWN BY APPLICATION



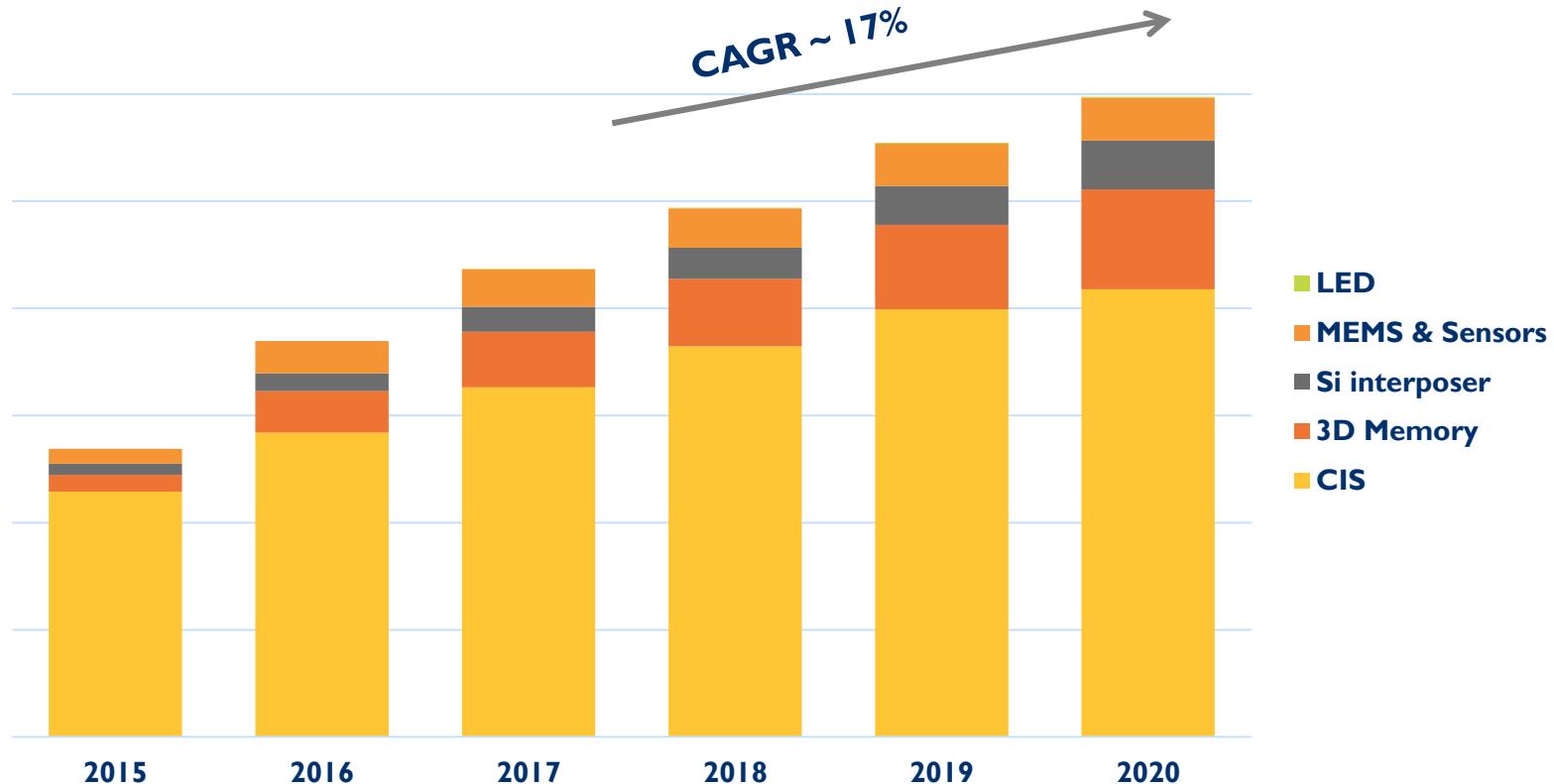
# TSV WAFER FORECAST (2015-2020)

## By application segment (12" eq )



- The wafer start for the TSV application is expected to reach ~ 3M wafers by 2020 at an CAGR of ~17%
- CIS was the earlier adopter of TSV technology & will continue to grow at an CAGR of ~13%
- For the TSV application, 3D memories will grow at the highest rate of CAGR of ~43% to reach around 0.5M wafer capacity by 2020
- The penetration of TSV technology for LED packaging will be slow and the volume will remain low

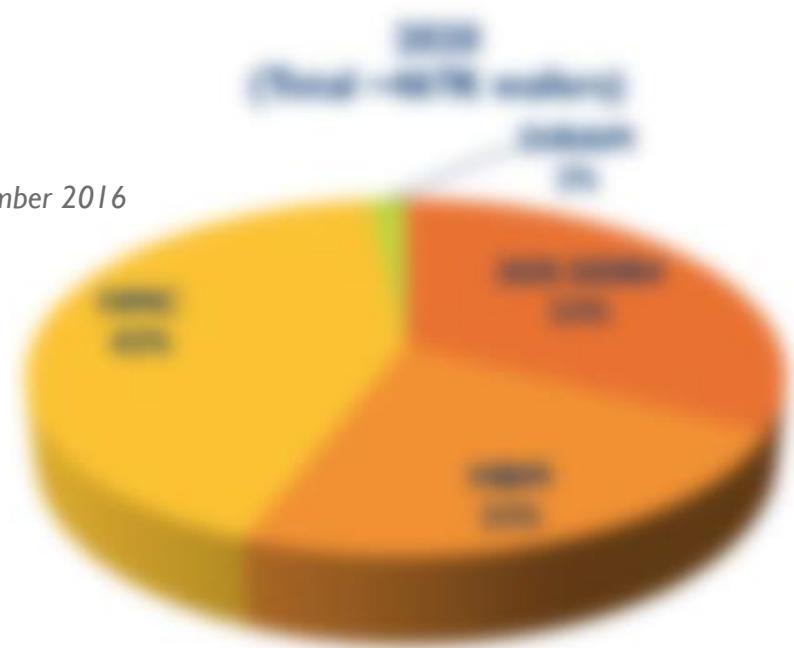
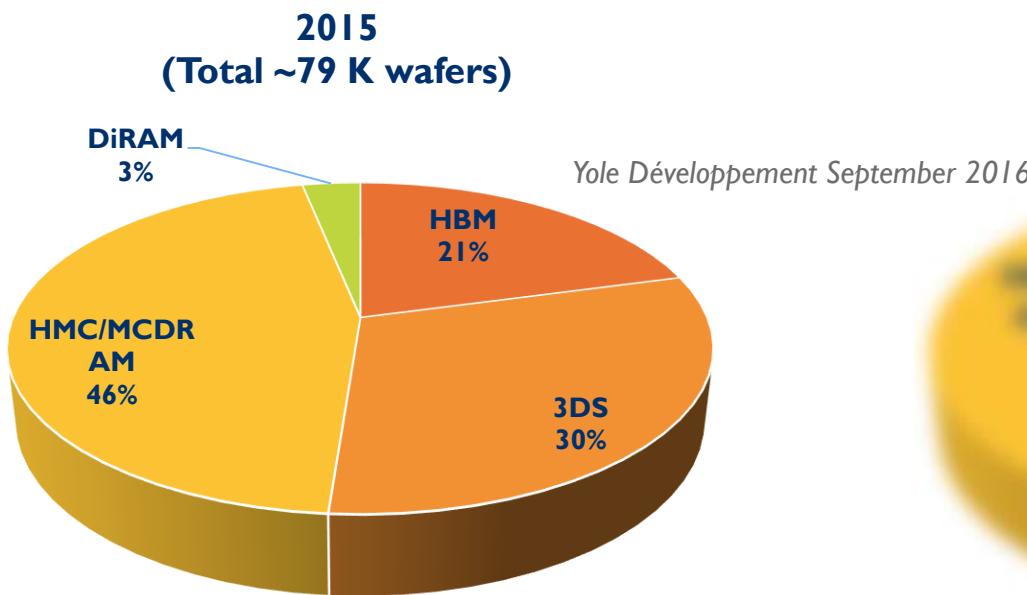
**Wafer forecast (2015-2020) for TSV application by segments**  
(in 12"eq wafers/yr)



# 3D TSV MEMORY MARKET SHARE BY WAFER START

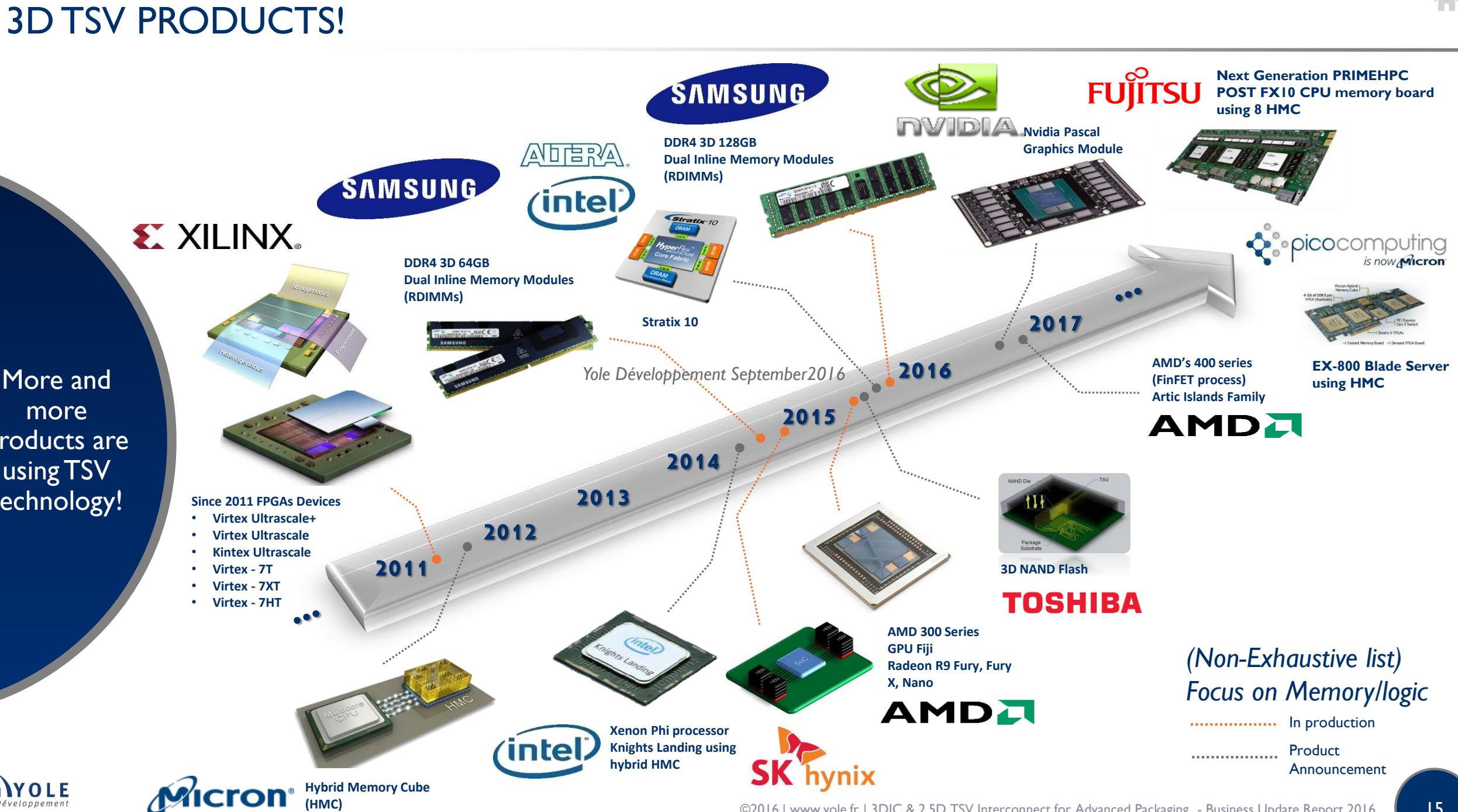


Breakdown by different memory architecture



# 3D TSV PRODUCTS!

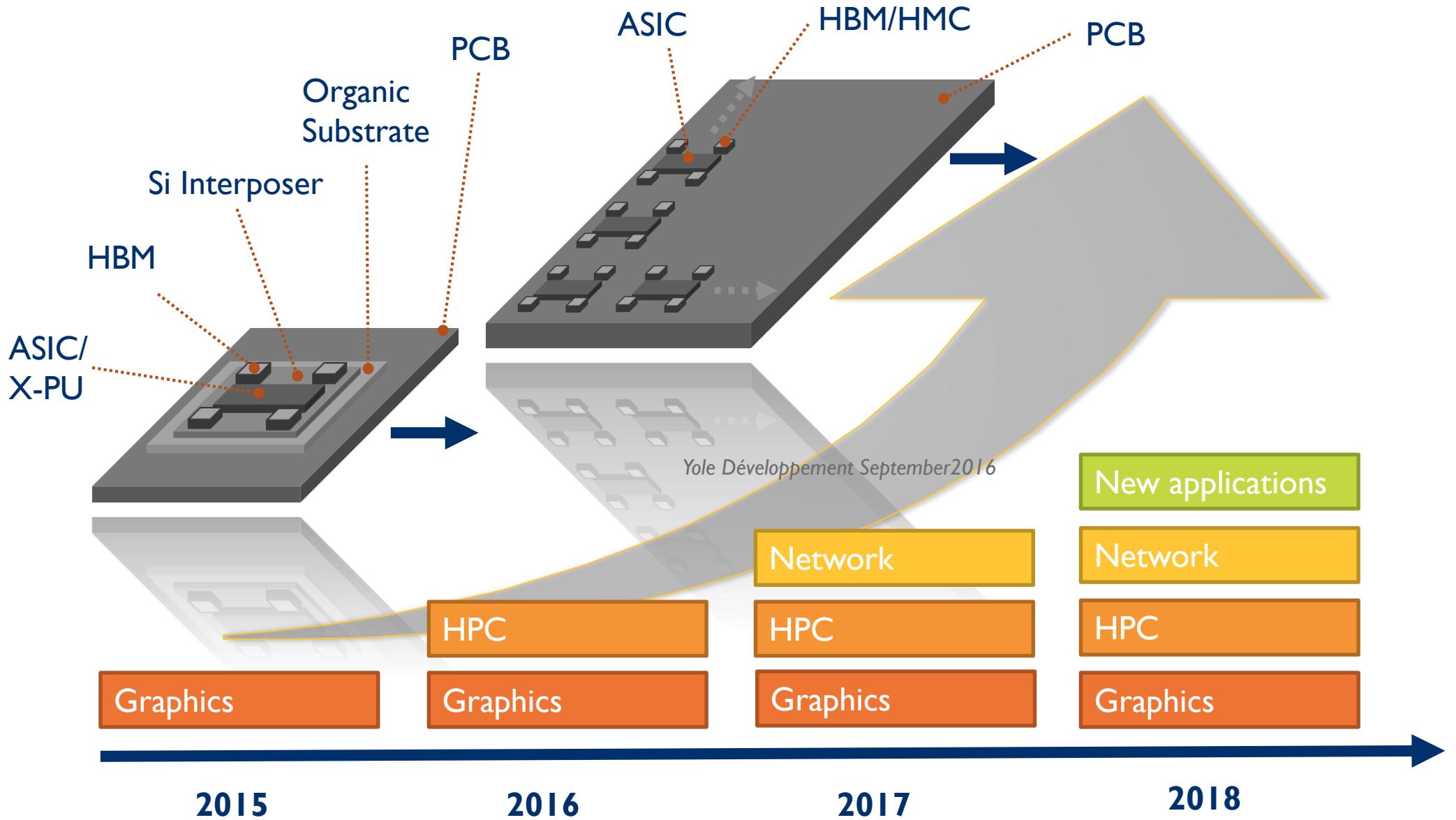
More and more products are using TSV technology!



# MEMORY STACKS – APPLICATION ROADMAP



OEMs are getting interest in stacked memories! More and more products to come!



2015

2016

2017

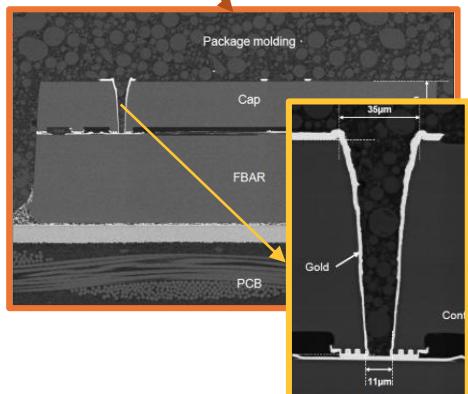
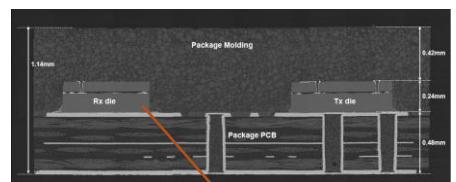
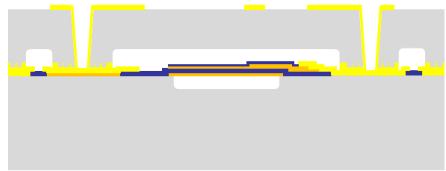
2018

# FILM BULK ACOUSTIC RESONATOR (FBAR) - BAW FILTER FROM AVAGO

## LGA package

- 2 MEMS
- 4 layers organic substrate

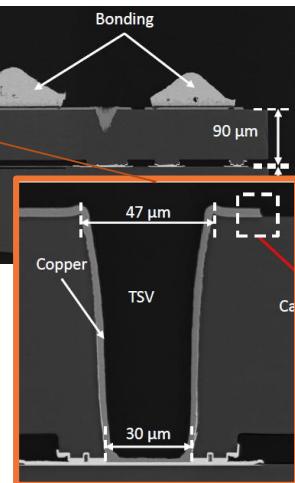
2013



## System in Package (SiP)

- Multi-dies (SAW, FBAR, Switch...)
- 7 layers coreless substrate
- **Extracted from iPhone 6S**

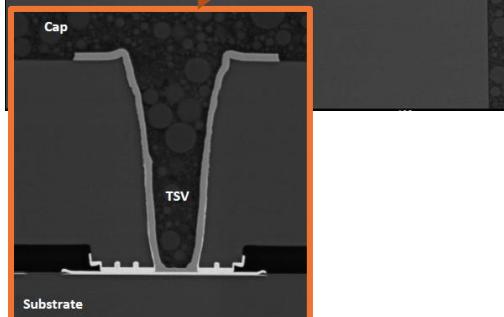
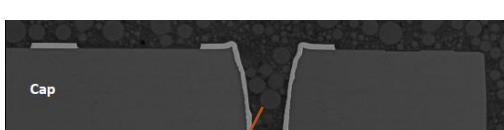
2015



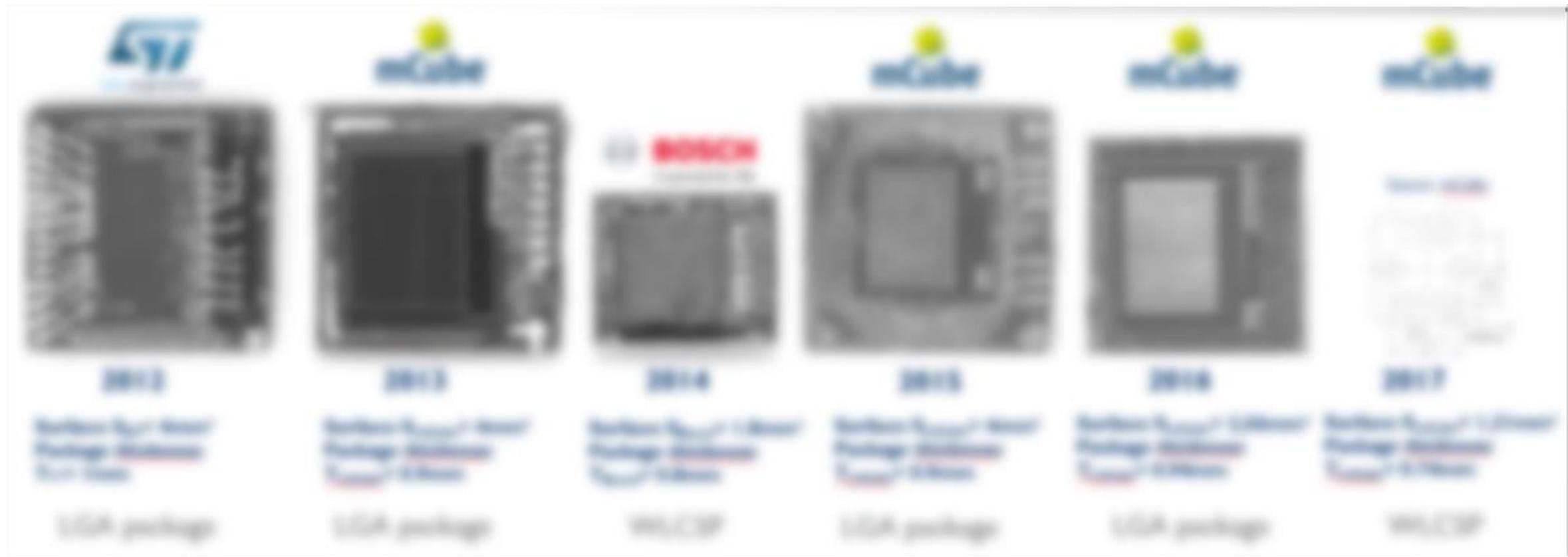
## System in Package (SiP)

- Multi-dies (BAW, Switches...)
- 7 layers coreless substrate
- **Extracted from Samsung S7**

2016



# 3-AXIS ACCELEROMETER PACKAGE SIZE COMPARISON – TSV INSIDE!



- Trends is clearly to reduce package surface to be able to ease MEMS integration in small devices. Package thickness is also key to achieve such small form factor.
- TSV integration combined with wafer level package enables very small form factor. mCube has announced the smallest packaged 3-Axis Accelerometer combining 3D heterogenous integration with Tungsten TSV achieving only 1,21mm<sup>2</sup> package surface!
- From standard LGA package from last past years, mCube will achieve **a reduction of 70% in package surface** using WLCSP with TSV!

# OTHER MEMS & SENSORS USING TSV !



And much more  
to come!

# HBM - JEDEC STANDARD

## Application segmentation!

(Non-Exhaustive list)



Graphic Cards



Networking Products,  
Servers and  
Supercomputers



Next generation  
Gaming Console



HBM1/2

End  
Customer

More information in the report

HBM key  
JEDEC  
standard for  
Memory!

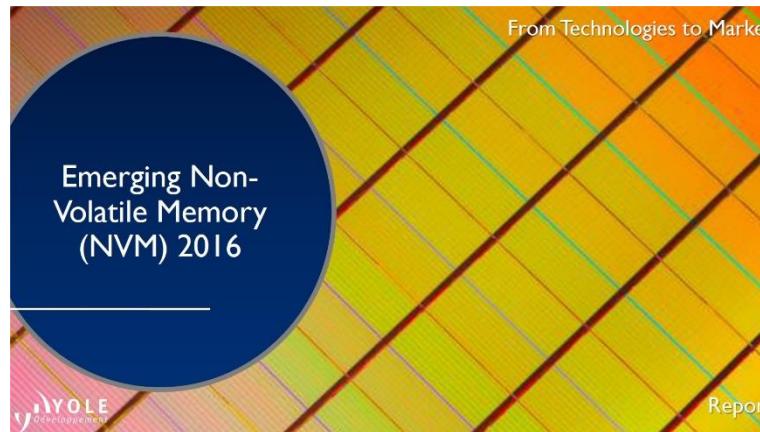
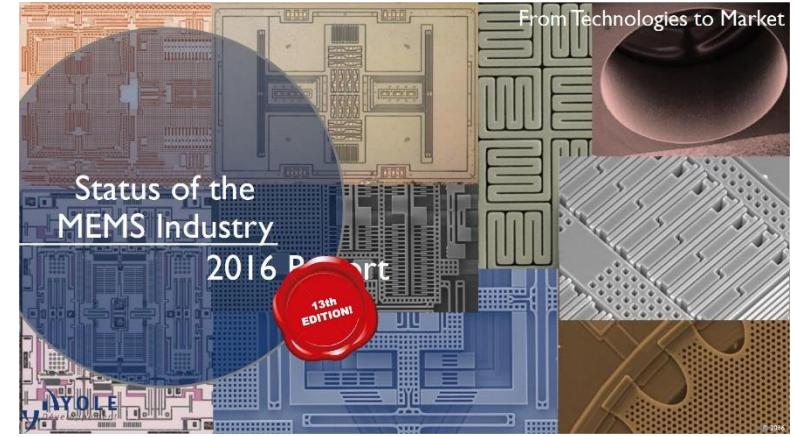
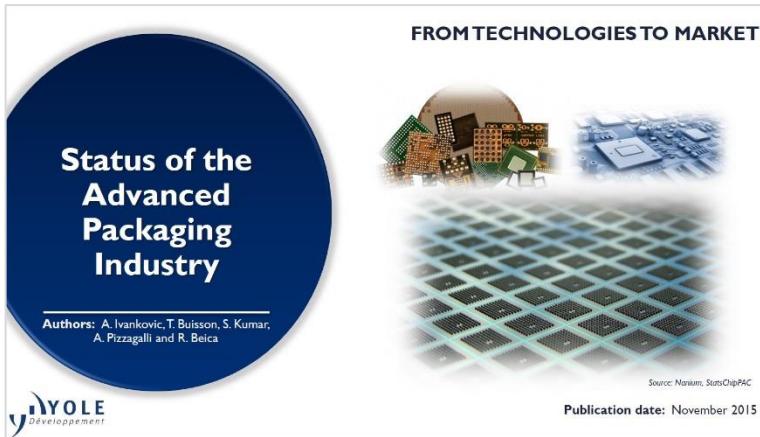


Detailed supply chain for key current and future products using  
3D TSV

# PLAYERS POSITIONING FOR DIFFERENT TSV APPLICATION

		Panel Packages				
		Memory	MEMS & Sensor	CIS	Si interposer	LED
Business models	OSATs	 	 			
	IDMs	More information in the report				
	Foundries					

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- North America: Steve Laferriere - [laferriere@yole.fr](mailto:laferriere@yole.fr)
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#### CONTACTS

For more information about :

- Consulting Services: Jean-Christophe Eloy ([eloy@yole.fr](mailto:eloy@yole.fr))
- Financial Services: Jean-Christophe Eloy ([eloy@yole.fr](mailto:eloy@yole.fr))
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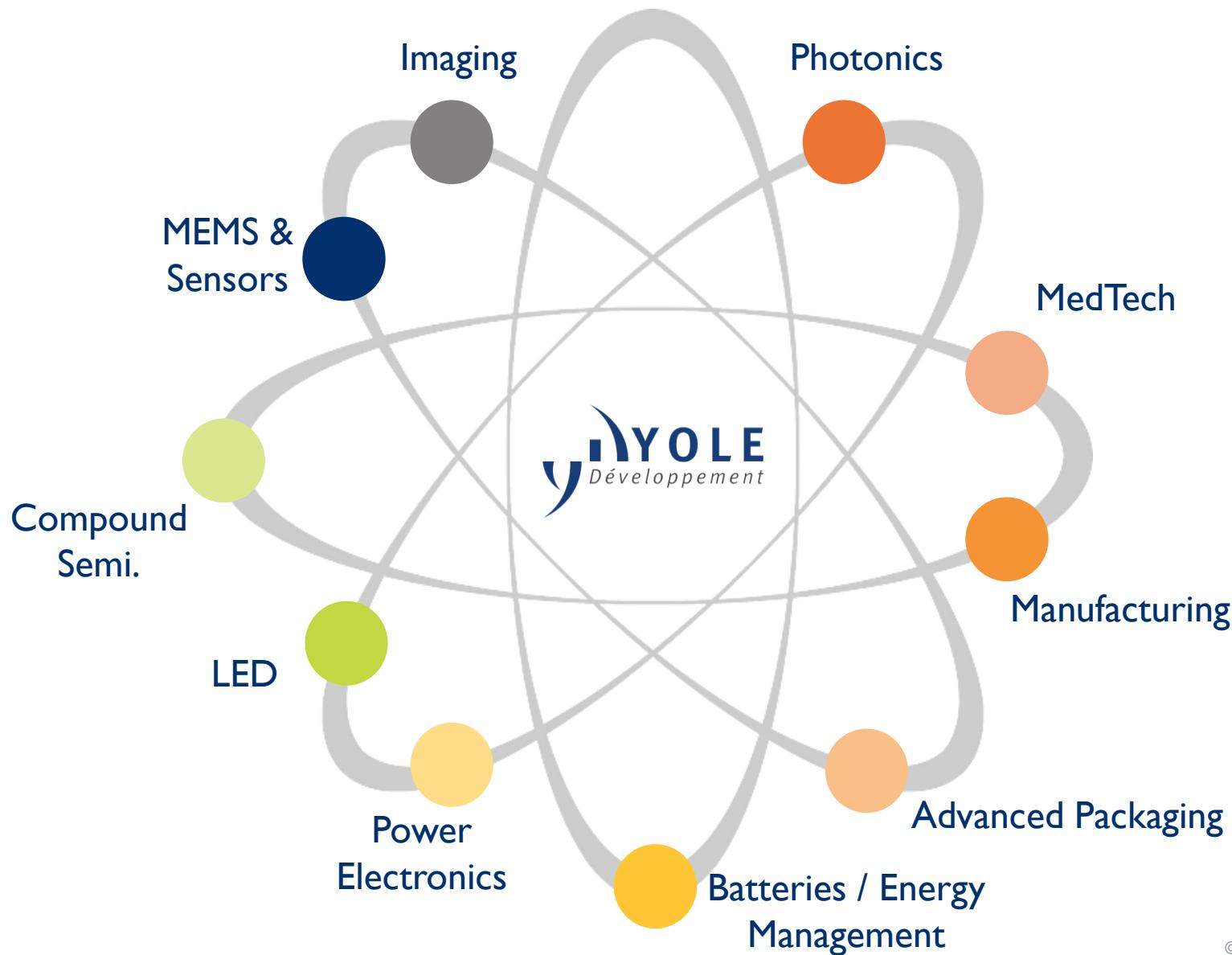
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*From Technologies to Market*

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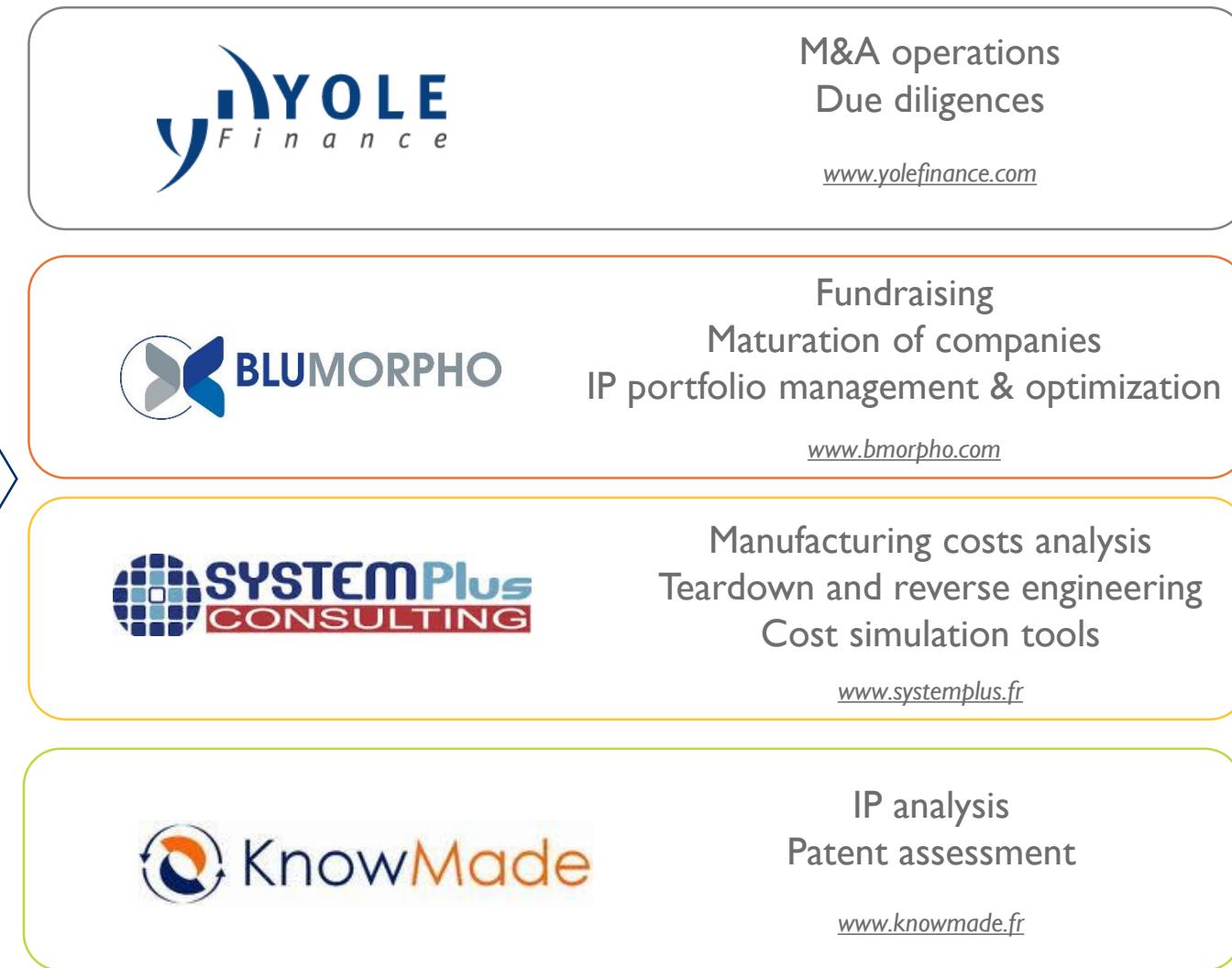
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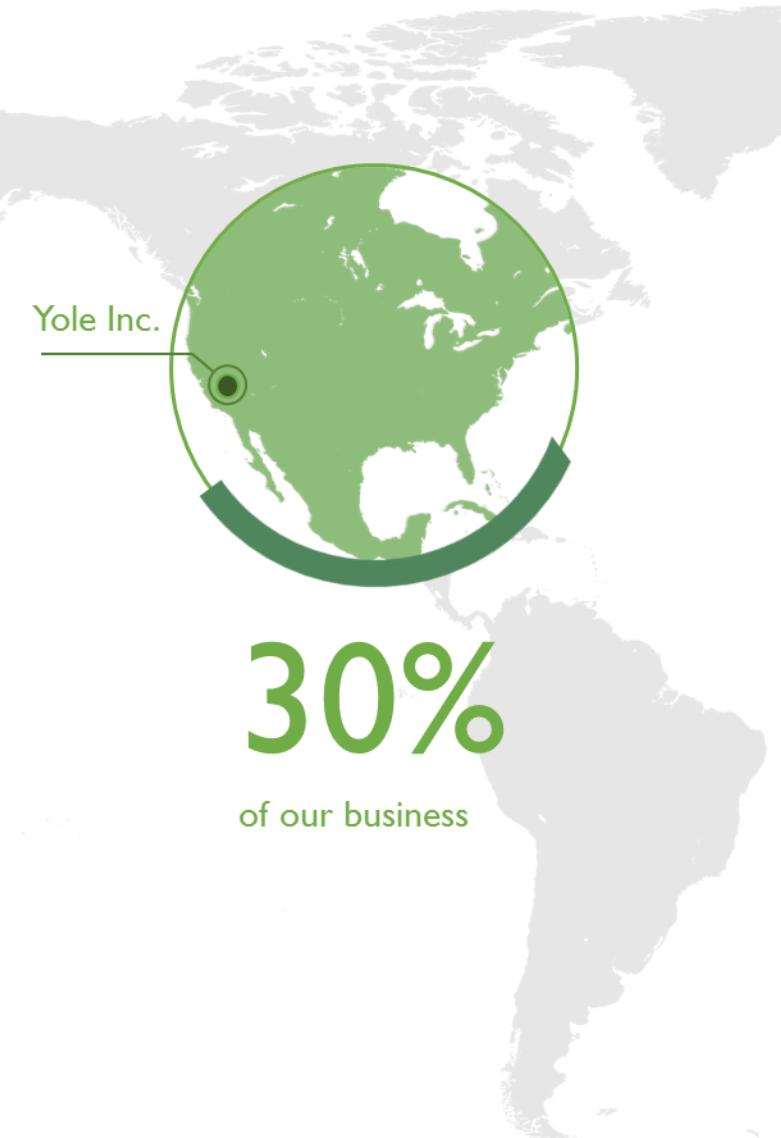
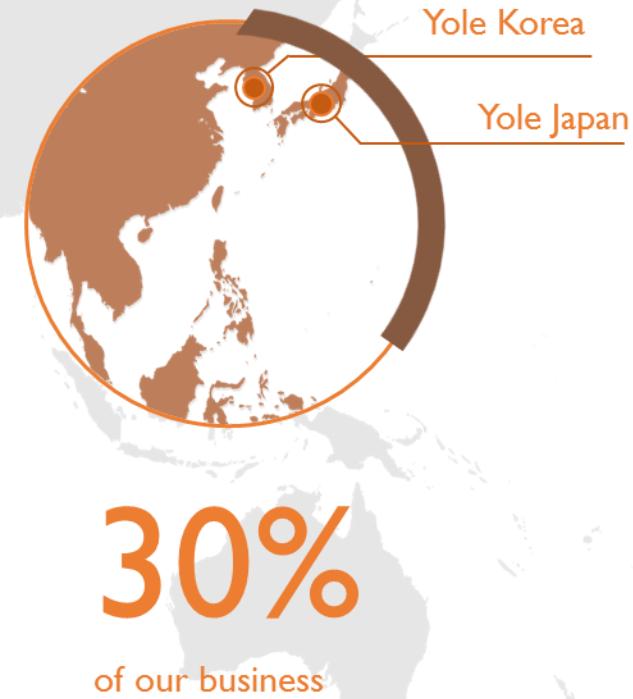
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# CONTACT INFORMATION

- Consulting and Specific Analysis
  - North America: **Steve LaFerriere**, Director of Northern America Business Development  
Email: laferriere@yole.fr
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