

Table 14 - Memory and Logic Technology Requirements									
<i>Year of First Product Shipment (Year)</i>									
1997 1998 1999 2001 2002 2003 2004 2005 2006 2007									
<i>Min. Logic Vdd (V) (absolute)</i>									
2.5-1.8 1.8-1.5 1.5-1.2 1.5-1.2 1.2-0.9 0.8-0.6 0.6-0.5									
<i>V_{DD} Variation</i>									
< 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10%									
<i>T_{on} (typical) (ns)</i>									
4-8 3-4 3-8 3-8 3-8 3-8 3-8 3-8 3-8 3-8									
<i>Extrinsic Maximum Field (mV/cm)</i>									
80 50 45 40 40 40 40 40 40 40									
<i>Min. L_g @ 25°C (λ_{th}) (nm)</i>									
600/290 600/290 600/280 600/280 600/280 600/280 600/280 600/280 600/280 600/280									
<i>Nominal L_g @ 25°C (λ_{th}) (nm)</i>									
600/290 600/290 600/280 600/280 600/280 600/280 600/280 600/280 600/280 600/280									
<i>Gate Length Metric (CV/II) (μm)</i>									
16-17 12-13 10-12 9-10 7 4-5 3-4 2-3 1-2 1-1									
<i>V_I (2σ Variation) (mV)</i>									
80 50 45 40 40 40 40 40 40 40									
<i>I_{off} (2σ Variation) (A/μm)</i>									
< 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10%									
<i>L_g (2σ Variation) (nm)</i>									
< 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10% < 10%									
<i>Drain Extension</i>									
Contact X (nm) 100-200 70-140 60-120 50-100 40-80 30-60 20-40 10-20 10-20 10-20									
X ₀ (channel) (nm) 50-100 36-72 30-48 26-52 20-40 16-32 10-20 10-20 10-20 10-20									
Silicide thickness (nm) 70 55 45 40 40 40 40 40 40 40									
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<i>Drain Extension</i>									

2.1 Introduction

2.2 Market demand for highly Integrated Circuits IC

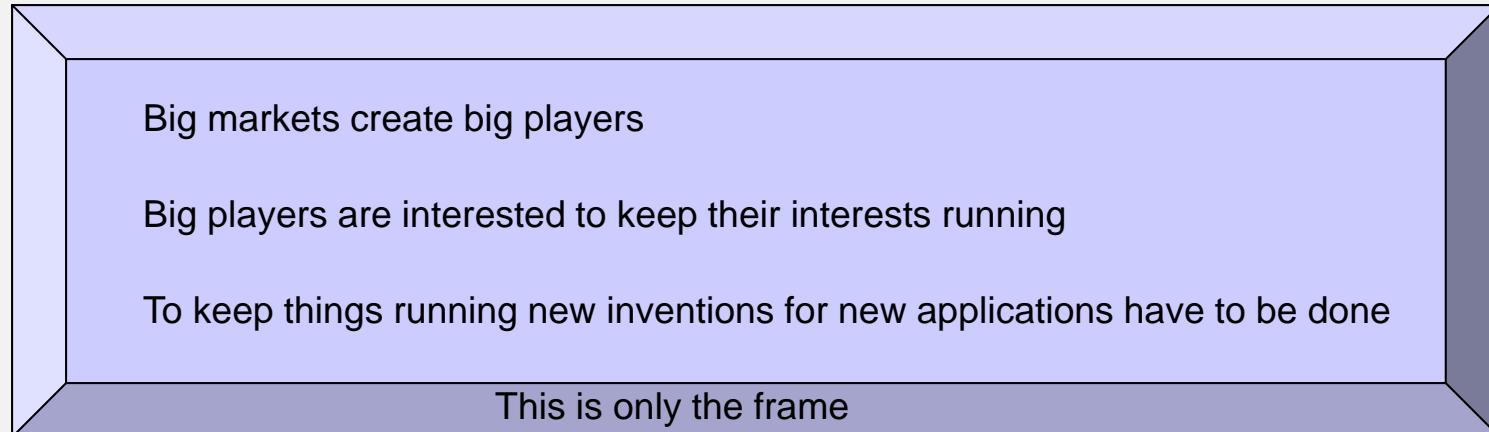
2.3 Shrinking: Making Money

2.4 Shrinking: Spending Money

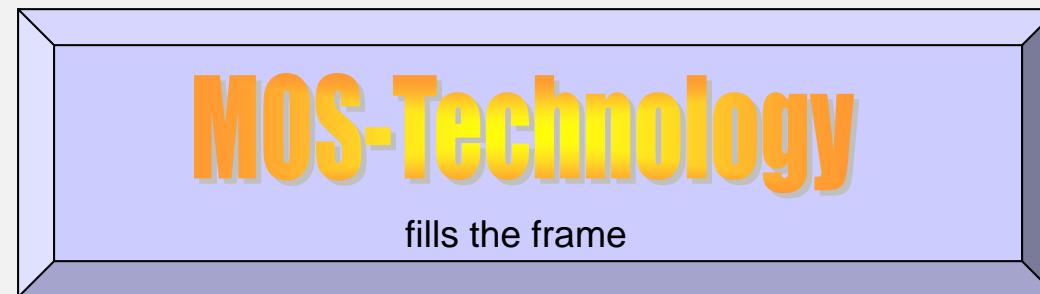
2.5 Calculation of Semiconductor Industry

2.6 Market Information on ICs

In chapter 1 (History) we have learned:



In this chapter 2 (Economics) we will see:

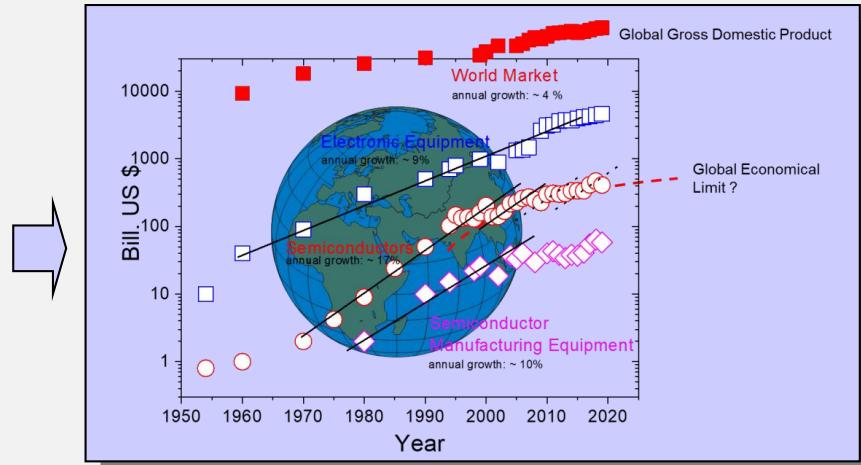


Only MOS-Technology enables the semiconductor industry
to **forecast** and to **calculate** its **income** as reliable as possible

1

Electronic Equipment is the world's largest market

A lot of
money

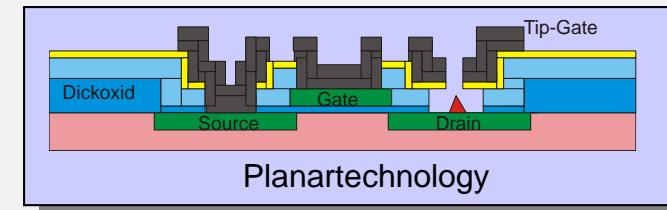


2

Planar technology

is the technological engine to keep the money running

As smaller the devices are, as cheaper they are

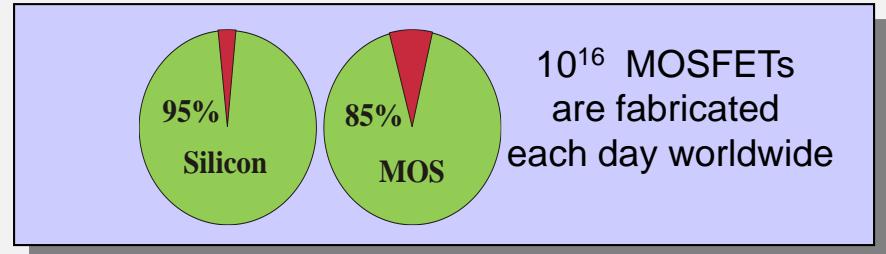


3

Silicon MOSFET devices

are:

- most easy to shrink
- are faster with shrink
- consume less power with shrink



CMOS is the far dominant device technology where the mainstream money is in

2.1 Introduction

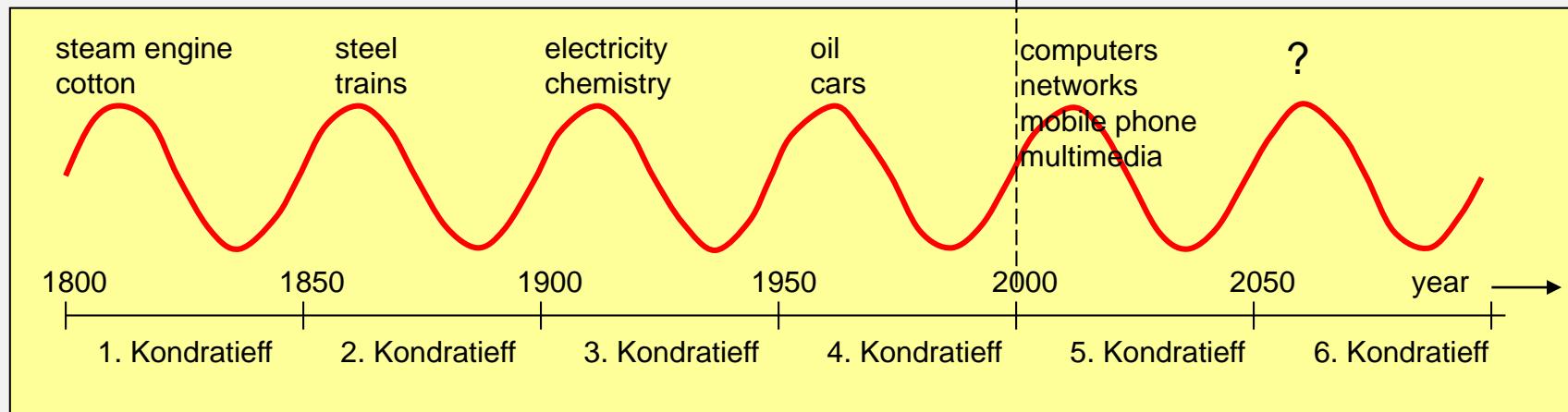
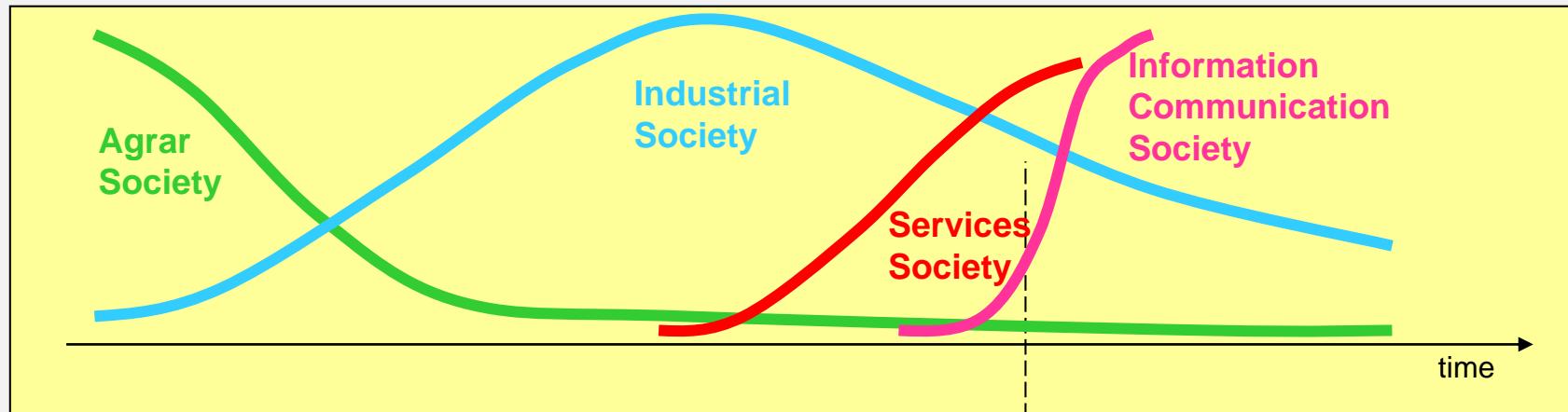
2.2 Market demand for highly Integrated Circuits IC

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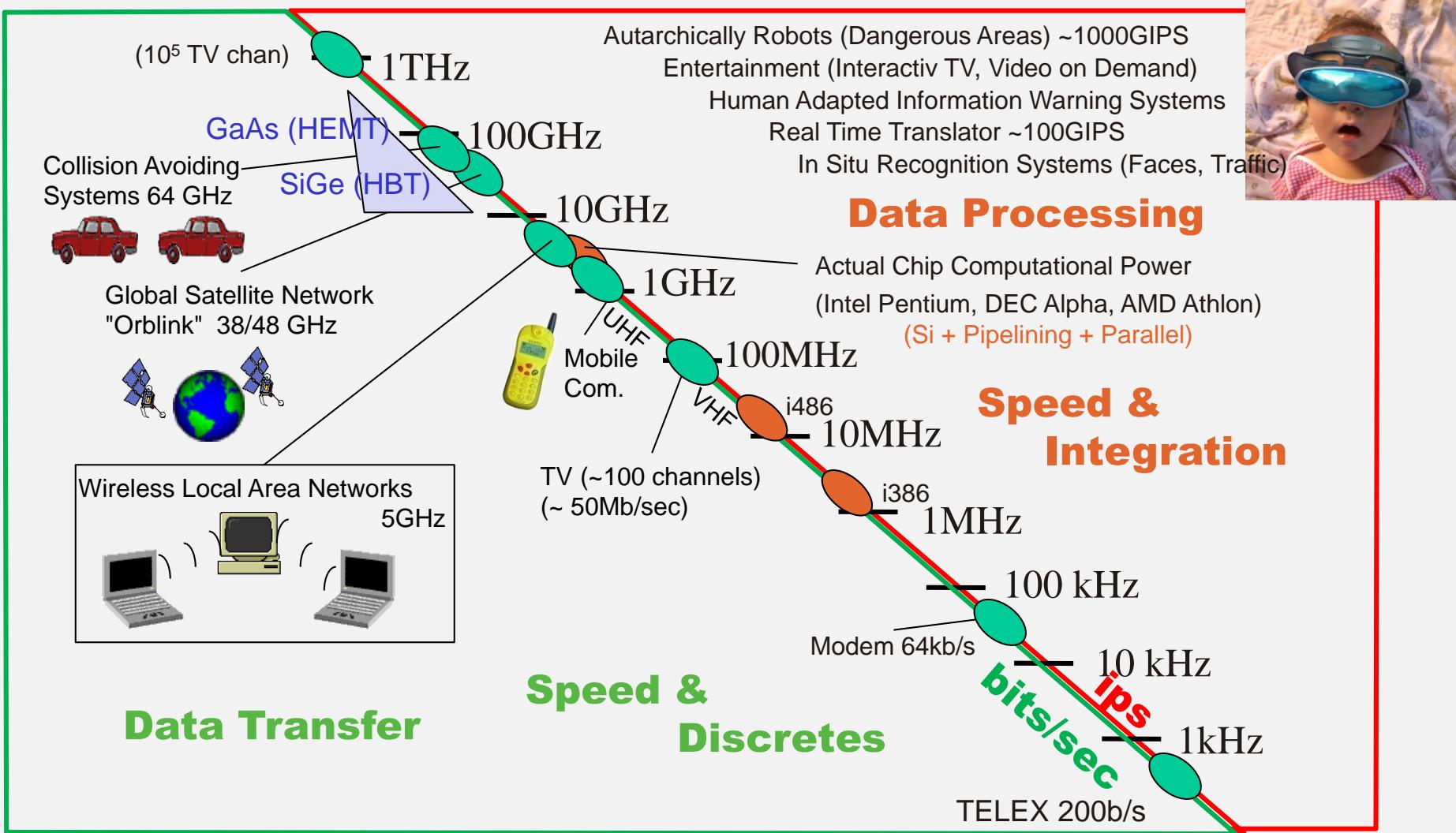
2.5 Calculation of Semiconductor Industry

2.6 Market Information on ICs



New inventions may change the society

The invention of the transistor and the IC enabled the mobile information- and communication society



 Data transfer is done by bipolar discrete devices, data processing is done by CMOS Integrated Circuits

We see:



Money is driving new applications



New applications are in need for

- more memory
- higher computational power (more logic circuits, higher speed)

Two possibilities:

1



Combine more conventional ICs

- increasing power consumption (4x more chips = 4x more power consumption)
- decreasing reliability of the system (4x more chips = $R_1 \cdot R_2 \cdot R_3 \cdot R_4$ reduced)
- linear increase in costs (4x more chips = 4x more costs + extra costs)
- technical limits of system realization (e.g. signal propagation between chips)

2



Development of higher integrated ICs with

- less increasing (better not increasing, best decreasing) power consumption
- higher yield and reliability of the system
- less increase of costs
- shifting technical limits of the system

History and semiconductor industry demonstrated, that:



Development of higher integrated ICs is the better alternative

Development of higher integrated ICs is based on:



Planar technology and MOSFETs

Economics: The opening of a big commercial market is based on reproducibility and reliability of the products

Semiconductor industry learned:

1. Reproducible and reliable devices can only be fabricated with a high purity, defect-free semiconductor crystal



1874: Braun Point rectifier -> 1948 Transistor

1926: MOSFET-Patent -> 1960 MOSFET Realization

2. Functional materials (semiconductor, insulator, metal) cannot be composed single-crystalline and defect-free

Technological realization:

we must perform:

1. Fabrication of a high-purity, defect-free semiconductor crystal
2. All device components and all devices must be fabricated within this semiconductor crystal

→ **Planar technology**

Future possibilities: extremely small devices (smaller than grain boundaries, smaller than lattice mismatch) plus material development (atomic monolayer processes, multi-component materials) may allow the fabrication of single-crystal devices and 3d-integration

still dreams

End of Planar technology ?

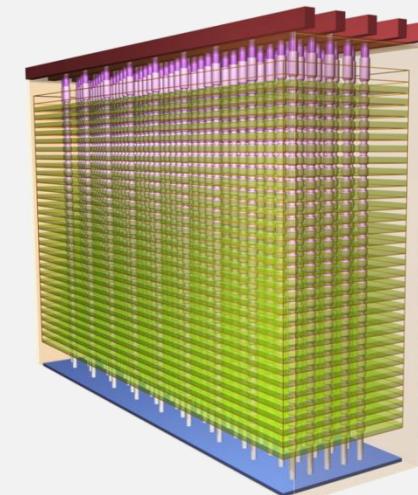
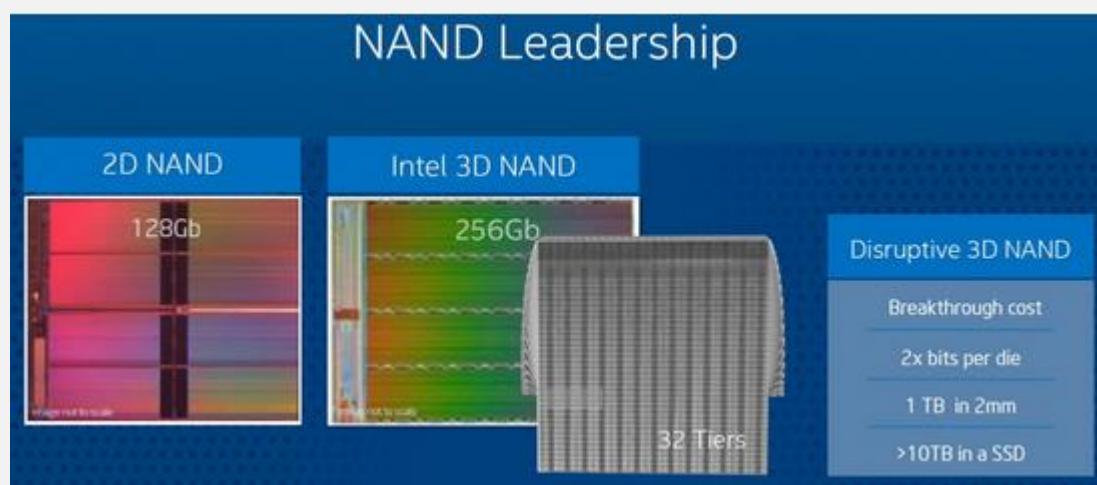
3d devices possible ?

Intel promises 10TB+ SSDs thanks to 3D Vertical NAND flash memory

November 21st, 2014 at 5:54 pm -Author Anton Shilov

At present solid-state drives with extreme capacities are very expensive and even the best of them cannot match high-capacity hard disk drives for nearline storage applications. However, thanks to the evolution of NAND flash memory in general, and 3D vertical NAND (3D V-NAND) in particular, the situation may change soon and SSDs with 10TB or higher capacities will become reality.

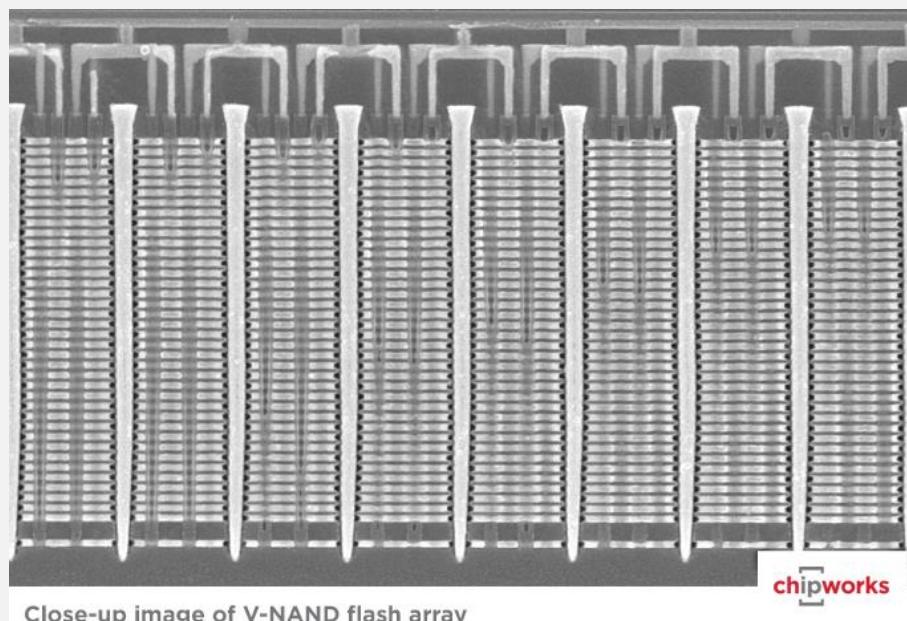
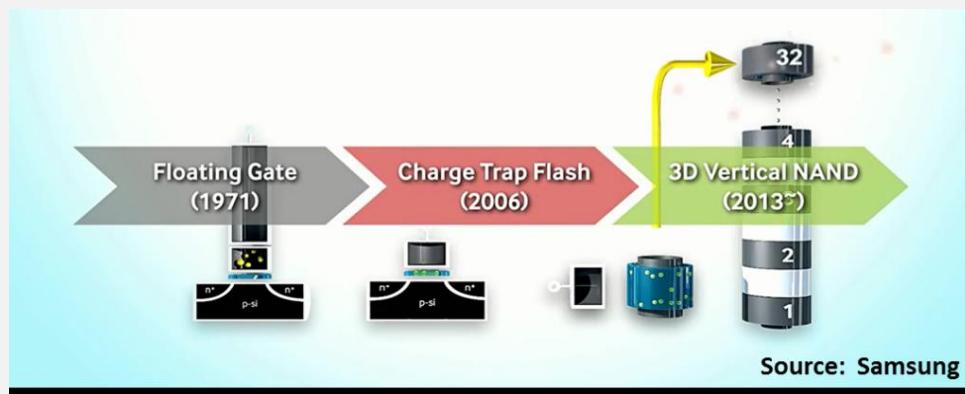
Intel Corp. revealed at its Investor Meeting 2014 event this week that in the second half of 2015 its joint venture with Micron Technology – Intel Micron Flash Technologies (IMFT) – will start mass production of 3D vertical NAND flash memory chips with up to 256Gb (multi-level cell, 2-bit-per cell) or 384Gb (triple-level cell, 3-bit-per cell) capacity. 3D V-NAND flash memory chips will feature 32-layer vertically stacked cell arrays that are “interconnected” using four billion through silicon vias (TSVs).



see details from SAMSUNG

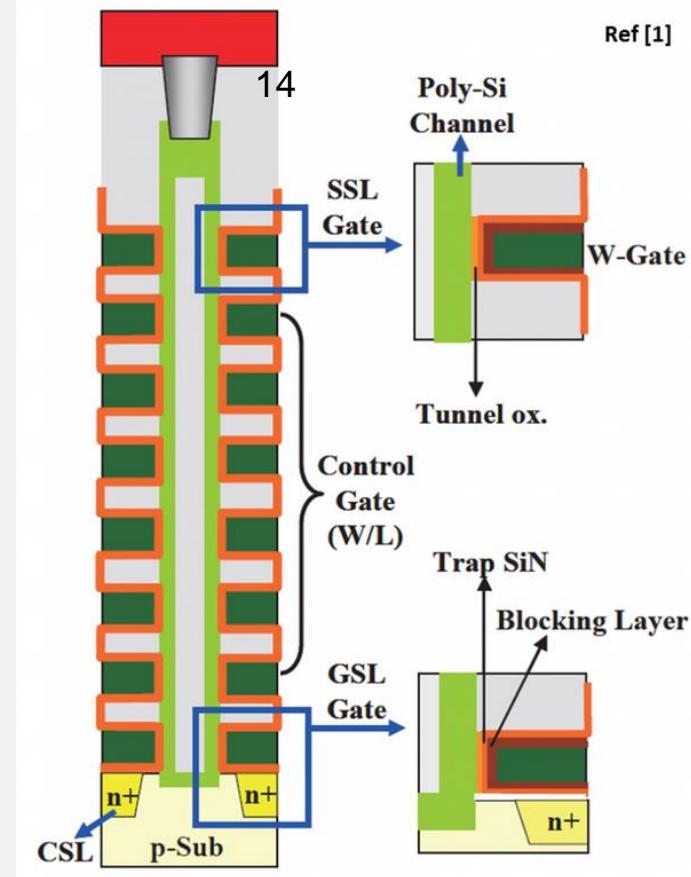
August 5, 2014

The Second Shoe Drops - Samsung V-NAND Flash



Close-up image of V-NAND flash array

Ref [1]



► Planar technology is overruled by 3D-Technology

► More details in chapter 6.9

der Bundeswehr

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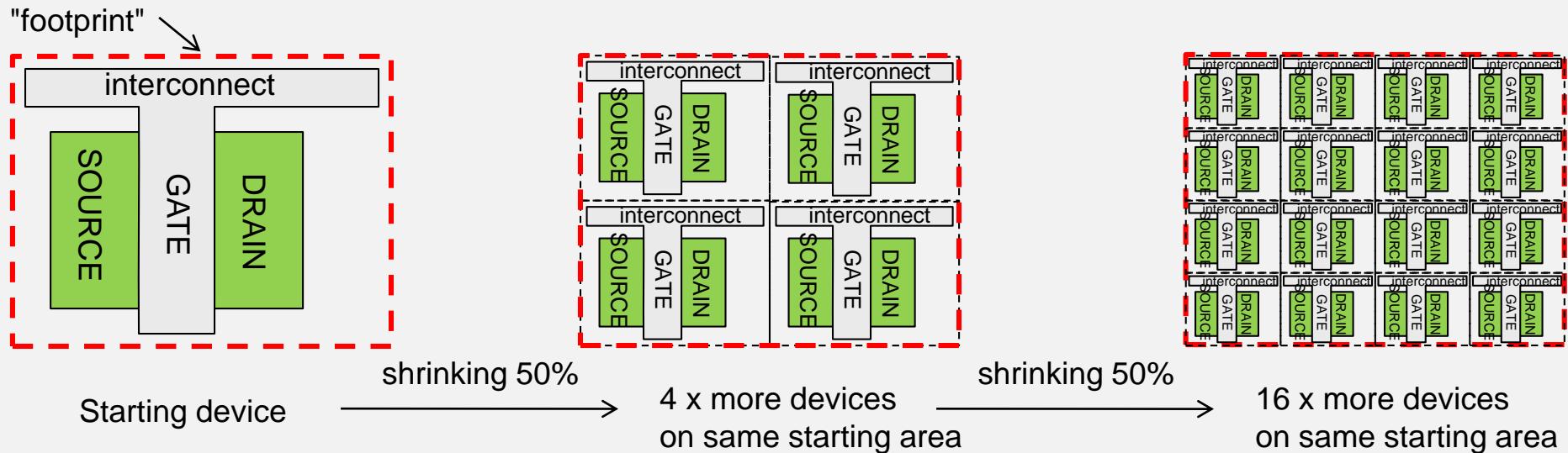
2.6 Market Information on ICs

In planar technology every device has a typical "footprint".

Increasing number of devices per chip means consuming area.

Increasing area per chip means higher costs per chip.

Cost reduction can be done by "Shrinking".



If shrinking can be done with the existing equipment (~ same process costs)
then number of devices increases -> cost per chip, cost per device, cost per function decreases



For the first view SHRINKING is a big economical advantage !

Higher Integration -> more devices per chip But several limitations for the number of devices per chip may exist:

Economical limitation:

Number of working chips

Modern devices are fabricated in up to 1000 process steps, each step may introduce defects and mistakes

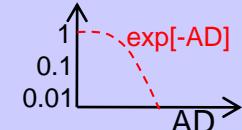
Since the probability to get a working chip is the product of all probabilities of all steps:

$$Y_{all} = Y_1 \cdot Y_2 \cdot Y_3 \cdot \dots \cdot Y_n$$

example:
0.9 x 0.9 x 0.9 = 0.73

and each yield Y is proportional to a critical device area $A \cdot D$

$$Y_{yield} = \exp[-A \cdot D]$$



Consequence: Therefore, increasing chip area by just adding more devices per chip is very critical

Shrinking devices will shrink critical device area and increasing yield

(see later in this chapter)

Physical limitation:

Power consumption + heat dissipation

Every device consumes power:

- no switching (leakage current, hold current) -> static power consumption
- when switching -> dynamic power consumption

Currents create ohmic heat, but the heat dissipation is limited for solids (and special geometries, special coolings)

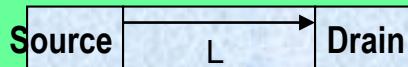
Power consumption per chip is limited -> will shrunked devices consume less power ?

Performance limitation:

Will the shrunked devices show better performance ???

Discretes

Gate



if: $v = 10^7 \text{ cm/sec}$
 $f = 1 \text{ THz}$
 $\rightarrow L < 100 \text{ nm}$

Integration

$$10 \text{ Gb} = 10^{10} \text{ dev/cm}^2$$

$$10^5 \text{ dev}$$



$$10^5 \text{ dev}$$

$$\rightarrow x < 100 \text{ nm}$$

Shrinking dimensions:

(by a factor S, details see ch. 4)



reduce device area

$$A = w \cdot L$$



$$A' = \frac{w}{S} \cdot \frac{L}{S}$$

$$A' = \frac{A}{S^2}$$



increase speed

$$\tau = \frac{L}{v}$$



$$\tau' = \frac{L}{S} / v$$

$$\tau' = \frac{\tau}{S}$$

reduce energy consumption
(power-delay)

$$P = V \cdot I \cdot \tau$$

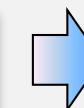


$$P' = \frac{V}{S} \cdot \frac{I}{S} \cdot \frac{\tau}{S}$$

$$P' = \frac{P}{S^3}$$

Shrinking dimensions induces:

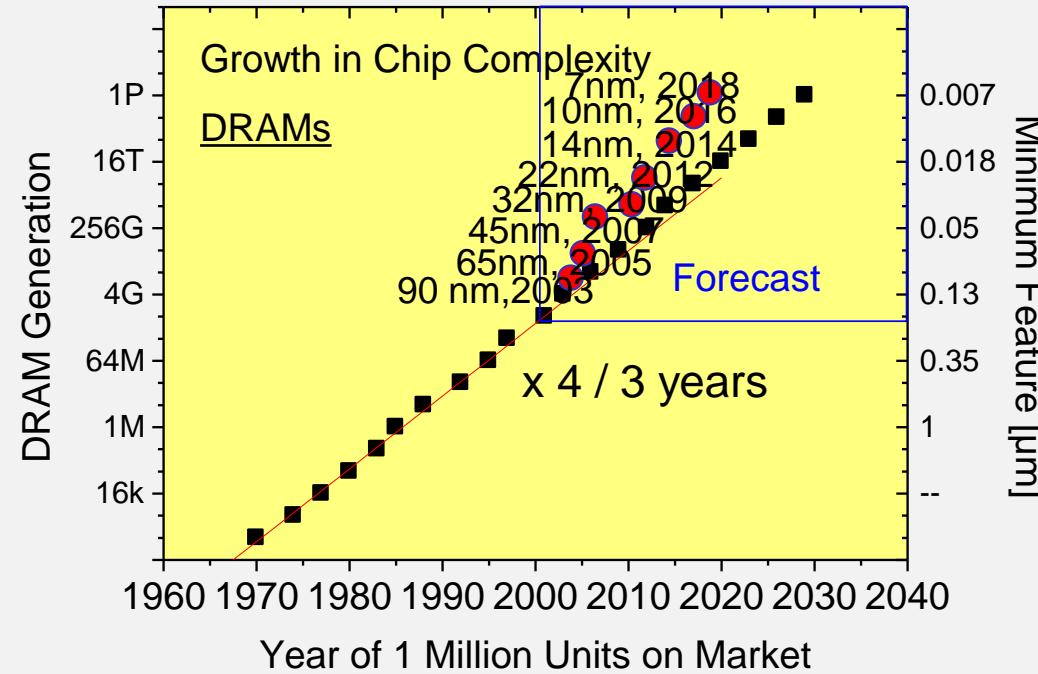
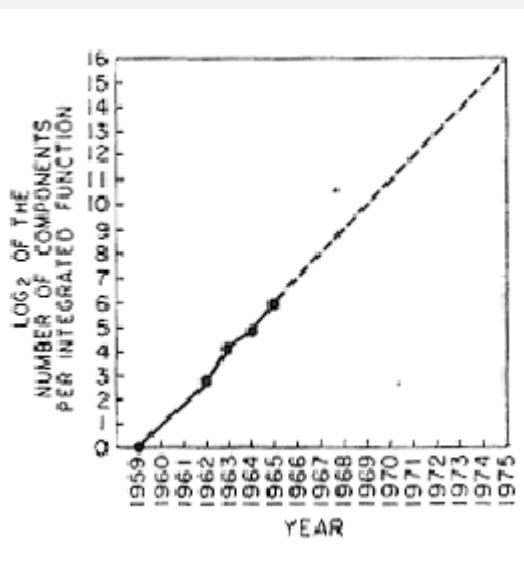
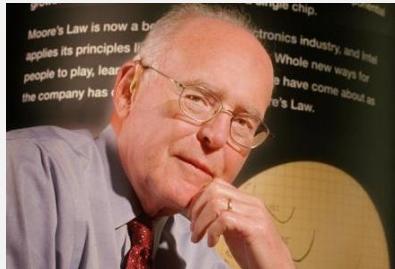
- + better devices (higher speed, lower power)
- + better economics (more devices per wafer)



so let's do shrinking



Increasing numbers of transistors (functions) on a chip due to shrinking is illustrated by the so-called "Moore's Law"



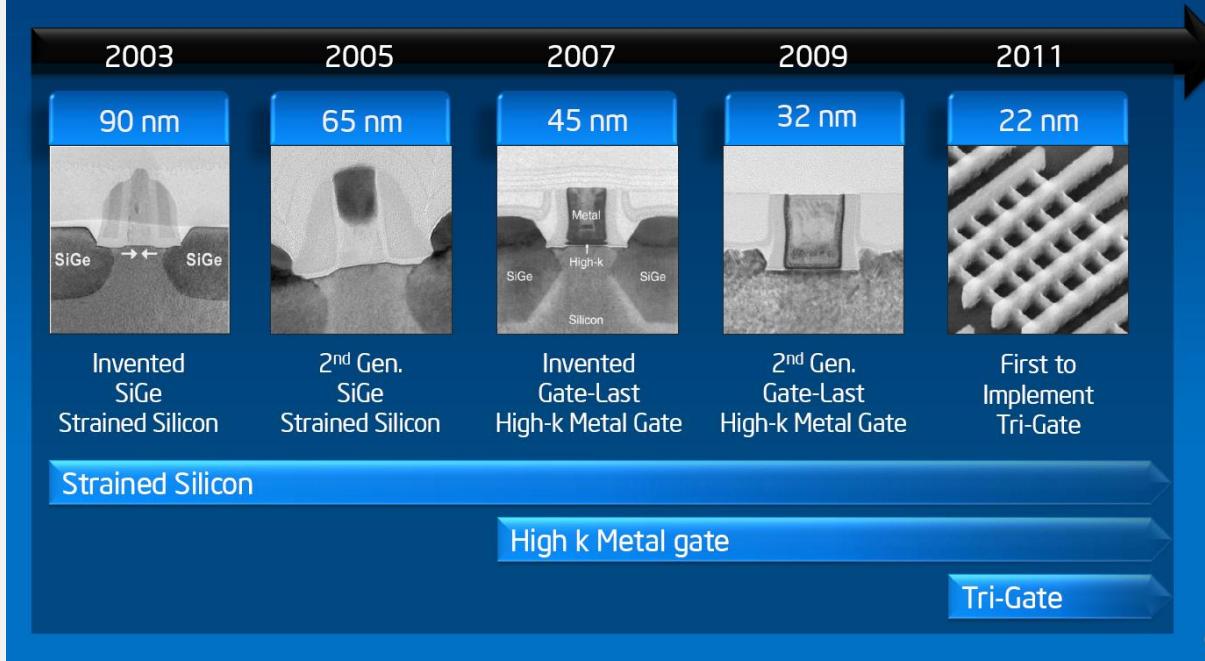
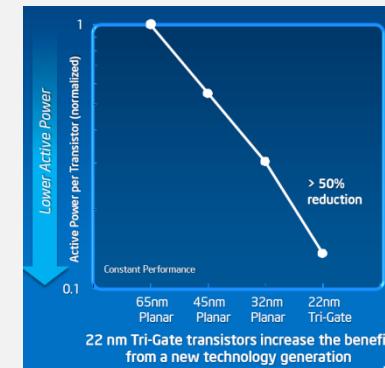
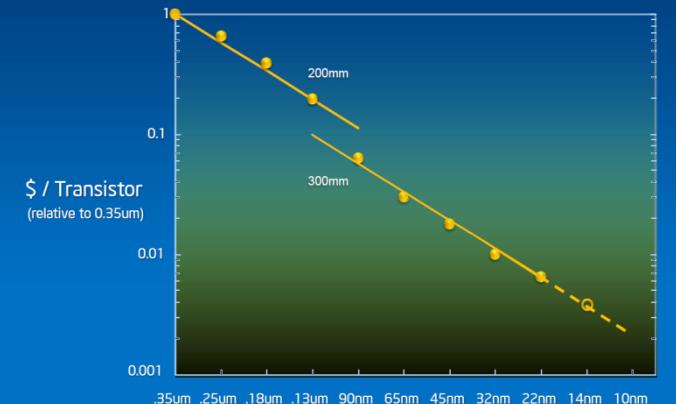
The prosperity of the semiconductor market (annual growth by ~17%) is mainly due to cost reduction by shrinking devices in planar technology (see next chapter)

In 1965 Gordon Moore presented a graphics which was proposing a doubling of transistors on a chip every 12 month. Due to upcoming technological difficulties the industry followed instead a doubling each 18 month. Anyhow, taking Moore's Law as a roadmap, a cost calculation guarantees the semiconductor industry an increase in income of about 17% year for year.

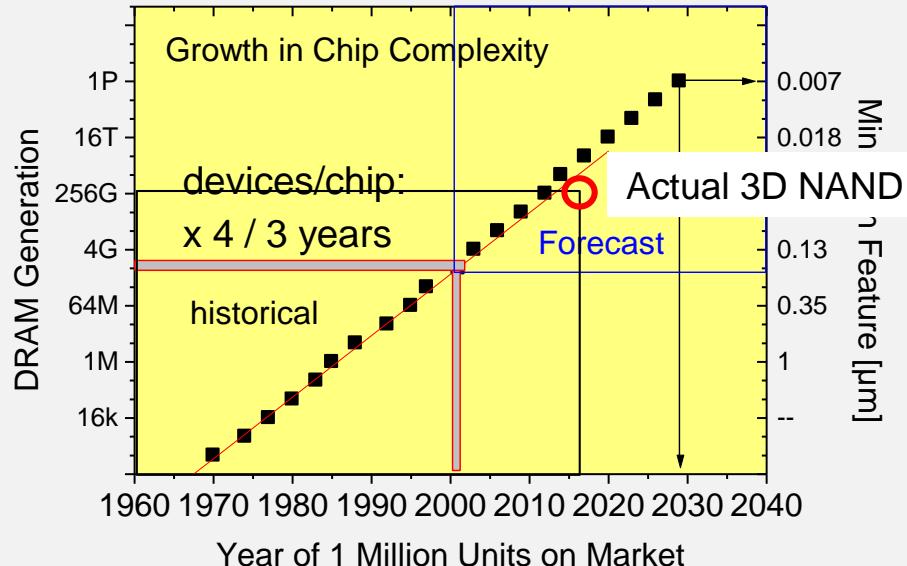
22nm Finfet May Extend Intel's Two Year Lead In Process.

By David Manners on July 22, 2011 1:36 AM

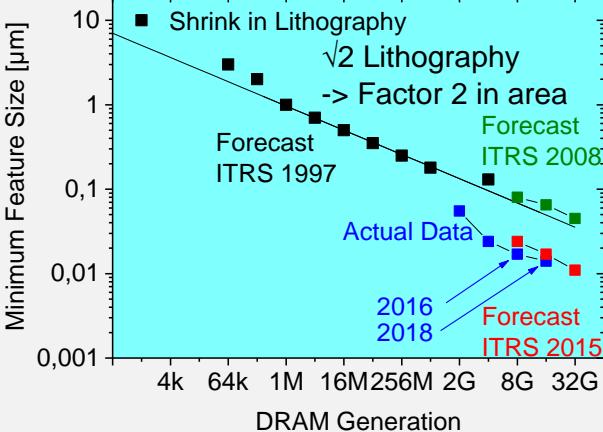
Intel has a two year lead in process technology over the rest of the semiconductor industry and could get further ahead if yields are satisfactory on its finfet-based 22nm process due for introduction later this year, said Mike Bryant, CTO of Future Horizons, at last week's IFS 2011.

Transistor Innovations Enable Technology Cadence**Transistor Innovations Enable Cost Benefits of Moore's Law to Continue**

see for example: <http://www.anandtech.com/show/4313/intel-announces-first-22nm-3d-trigate-transistors-shipping-in-2h-2011>

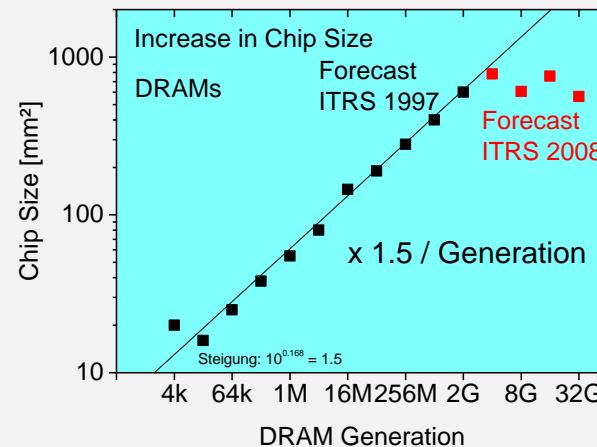


For shrinking dimensions a roadmap exists, which is called Moore's Law



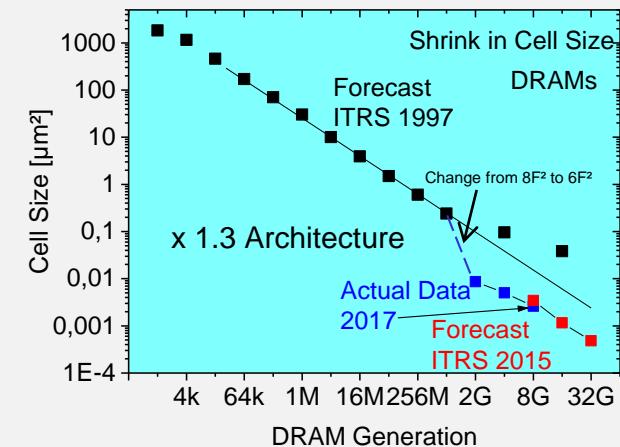
a factor $\sqrt{2}$ in dimension shrink

Saturation proposed



a factor 1.5 in chip size increase

Saturation due to yield aspects



a factor 1.3 in better design

Saturation due to $4F^2$

Roadmaps to continue Moore's Law 1997

Early roadmap from 1997:

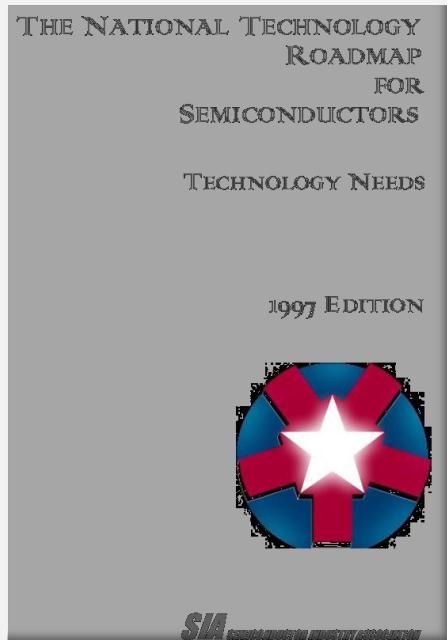


Table 14 Memory and Logic Technology Requirements

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Min. Logic V_{dd} (V) (desktop)	2.5-1.8	1.8-1.5	1.5-1.2	1.5-1.2	1.2-0.9	0.9-0.6	0.6-0.5
V_{dd} Variation	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$
T_{ox} Equivalent (nm)	4-5	3-4	2-3	2-3	1.5-2	< 1.5	< 1.0
Equivalent Maximum E-field (MV/cm)	4-5	5	5	5	> 5	> 5	> 5
Max I_{off} @ 25°C (nA/ μm) (For minimum L device)	1	1	3	3	3	10	10
Nominal I_{on} @ 25°C ($\mu A/\mu m$) (NMOS/PMOS)	600/280	600/280	600/280	600/280	600/280	600/280	600/280
Gate Delay Metric (CV/I) (ps)*	16-17	12-13	10-12	9-10	7	4-5	3-4
V_T 3σ Variation ($\pm mV$) (For minimum L device)	60	50	45	40	40	40	40
L_{gate} 3σ Variation (For nominal device)	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$
...							
S/D Extension Junction Depth, Nominal (nm)	50-100	36-72	30-60	26-52	20-40	15-30	10-20
Total Series Resistance of S/D (% of channel resistance)	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$	$\leq 10\%$
Gate Sheet Resistance (Ω/sq)	4-6	4-6	4-6	4-6	4-6	< 5	< 5
<hr/>							
Equivalent oxide thickness $T_{ox}(\text{nm})$	4-5	3-4	2-3	2-3	1.5-2	< 1.5	< 1.0
Thickness control (% 3σ)	± 4	± 4	± 4	$\pm 4-6$	$\pm 4-8$	$\pm 4-8$	$\pm 4-8$
<hr/>							
Drain structure	Drain Extension			+ Elev. S/D		Elev. Single Drain	
Contact X_J (nm)	100-200	70-140	60-120	50-100	40-80	15-30	10-20
X_J @ channel (nm)	50-100	36-72	30-60	26-52	20-40	15-30	10-20
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Drain extension conc. (cm^{-3})	1×10^{18}	1×10^{19}	1×10^{19}	1×10^{19}	1×10^{20}	1×10^{20}	1×10^{20}
Channel conc. for $W_{depletion} < 1/4L_{eff}$ (cm^{-3})	1×10^{18}	2×10^{18}	2.5×10^{18}	3×10^{18}	4×10^{18}	8×10^{18}	1.4×10^{19}
<hr/>							
DRAM 1st Year Electrical D _r @ 60% Yield/3rd Year @ 80% Yield (d/m^2)	2080 / 1390	1455 / 985	1310* / 875*	1040 / 695	735 / 490	520 / 350	370 / 250
MPU 1st Year Electrical D _r @ 60% Yield/3rd Year @ 80% Yield (d/m^2)	1940 / 1310	1710 / 1150	1510* / 1025*	1355 / 910	1120 / 760	940 / 640	775 / 525
<hr/>							
Solutions Exist		Solutions Being Pursued			No Known Solution		

- ➡ Year 2012 -> 50nm Generation
- ➡ Supply Voltage: (0.5 - 0.6) V
- ➡ $I_{off} < 10 \text{ nA}/\mu\text{m}$
- ➡ $I_{on} : 600 \mu\text{A}/\mu\text{m}$ } $\Delta I = 5 \text{ decades}$
- ➡ $\Delta V_G = 315 \text{ mV}$
(with ideal $S = 63 \text{ mV/dec}$)
- ➡ Equivalent oxide thickness for Long Channel Criterion
- ➡ S/D junction depth for Long Channel Criterion
- ➡ Channel doping for Long Channel Criterion
- ➡ Starting Yield: 60 %

Roadmaps are only a list of required device properties in time to ensure the prosperity of semiconductor industry

- Roadmaps are based on planar technology and shrinking
- for a lot of requirements today no realization possibility (red walls) exist

Roadmaps to continue Moore's Law 2018/2019

YEAR OF PRODUCTION	2018	2020	2022	2025	2028	2031	2034
G54M36	G48M30	G45M24	G42M21	G40M16	G40M16T2	G40M16T4	
Logic industry "Node Range" Labeling (nm)	"7"	"5"	"3"	"2.1"	"1.5"	"1.0 eq"	"0.7 eq"
IDM-Foundry node labeling	i10-f7	i7-f5	i5-f3	i3-f2.1	i2.1-f1.5	i1.5e-f1.0e	i1.0e-f0.7e
Logic device structure options	FinFET	finFET	finFET LGAA	LGAA	LGAA VGAA	LGAA-3D VGAA	LGAA-3D VGAA
Mainstream device for logic	finFET	finFET	finFET	LGAA	LGAA	LGAA-3D	LGAA-3D
DEVICE ELECTRICAL SPECS							
Mx pitch (nm)	40	36	32	24	20	16	16
M1 pitch (nm)	36	32	30	21	20	20	20
M0 pitch (nm)	36	30	24	21	16	16	16
Gate pitch (nm)	54	48	45	42	40	40	40
L _o : Gate Length - HP (nm)	20	18	16	14	12	12	12
L _g : Gate Length - HD (nm)	22	20	18	14	12	12	12
Power Supply Voltage - Vdd (V)	0.75	0.70	0.70	0.65	0.65	0.60	0.55
Subthreshold slope (mV/dec) - HP (mV/dec)	68	78	82	80	75	75	70
Subthreshold slope (mV/dec) - HD (mV/dec)	68	72	75	75	68	65	65
Inversion layer thickness (nm) [1]	1.10	1.10	1.00	1.00	0.90	0.90	0.90
V _{t,sat} at Ioff=10nA/um - HP (mV)	190	222	237	236	226	226	211
V _{t,sat} (mV) at Ioff=100pA/um - HD (mV) [2]/[3]	323	345	363	371	341	326	326
Effective mobility (cm ² V.s)	150	125	125	100	100	100	100
Rsd (Ohms.um) [4]	300	285	271	257	244	232	221
Ballisticity/Injection velocity (cm/s)	1.32E-07	1.39E-07	1.46E-07	1.46E-07	1.46E-07	1.46E-07	1.46E-07
V _{dsat} (V) - HP	0.141	0.160	0.149	0.163	0.140	0.140	0.140
V _{dsat} (V) - HD	0.155	0.177	0.168	0.163	0.140	0.140	0.140
Ion (uA/um) at Ioff=10nA/um - HP when Rsd=0 [5]	2027	1733	1950	1670	1975	1696	1501
Ion (uA/um) at Ioff=10nA/um - HP [6]	972	853	911	820	923	826	759
Ion (uA/device) at Ioff=100nA/um - HP [7]	86	91	157	157	144	132	91
Ion (uA/um) at Ioff=100pA/um - HD when Rsd=0 [5]	1447	1157	1271	991	1334	1139	859
Ion (uA/um) at Ioff=100pA/um - HD [6]	596	483	495	390	520	467	347
Ion (uA/device) at Ioff=100pA/um - HD [7]	52	52	75	75	81	75	42
Cch,total (fF/um ²) - HP/HD [8]	31.38	31.38	34.52	34.52	38.35	38.35	38.35
Gate height over fin (nm)	30	25	20	15	15	15	15
Spacer k value	4.5	4.0	3.5	3.5	3.0	3.0	3.0
Cch (fF/um) - HP [8]	0.50	0.45	0.44	0.39	0.37	0.37	0.37
Cch (fF/um) - HD [8]	0.55	0.50	0.50	0.39	0.37	0.37	0.37
CV/I (ps) - FO3 load, HP [9]	1.16	1.11	1.02	0.92	0.78	0.80	0.80
I/(CV) (1/ps) - FO3 load, HP [10]	---	---	---	---	1.00	1.25	1.25
Energy per switching [CV2] (fJ/switch) - FO3 /						0.40	0.33

Solutions Exist

Solutions Being Pursued

No Known Solution

Year 2028 -> 1.5nm Generation

Gate pitch: saturation at 40 nm

L: saturation at 12 nm

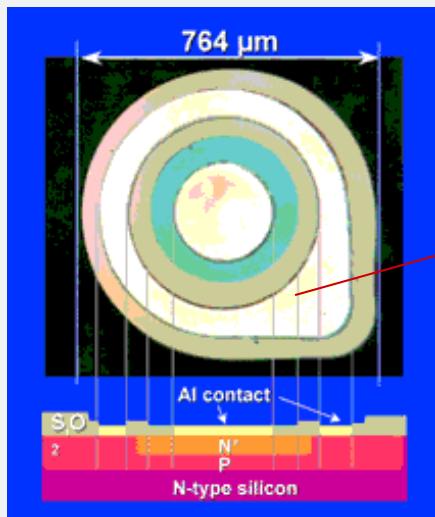
Supply Voltage: 0.65 V

S: 68 mV/dec

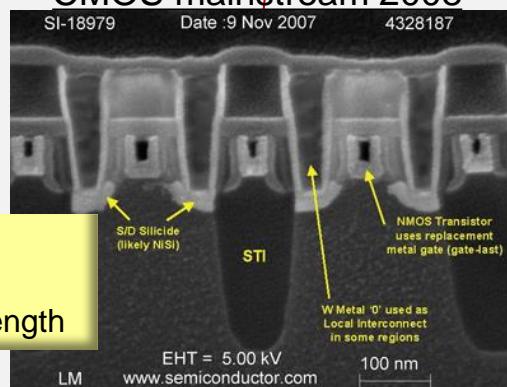
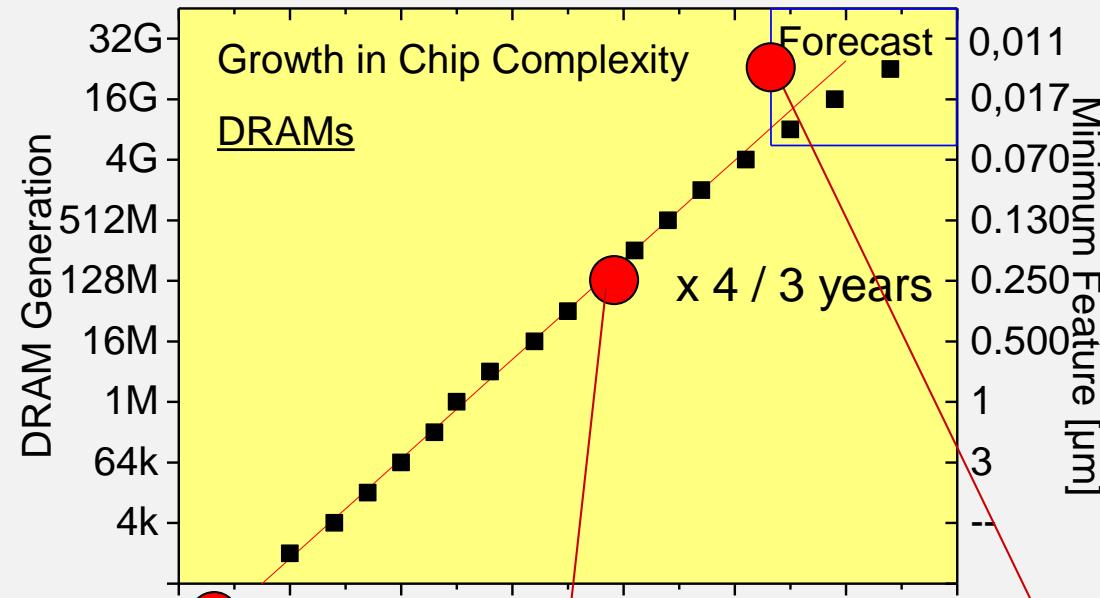
Parts of current are not longer drift-diffusion but other transport effects, like tunneling, hot electrons, avalanche.

Roadmaps are only a list of required device properties in time to ensure the prosperity of semiconductor industry

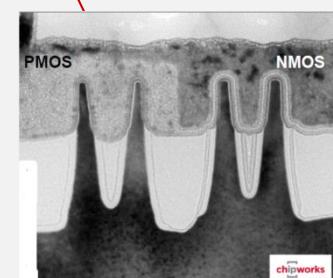
- > Roadmaps are based on planar technology and shrinking
- > for a lot of requirements today no realization possibility (red walls) exist



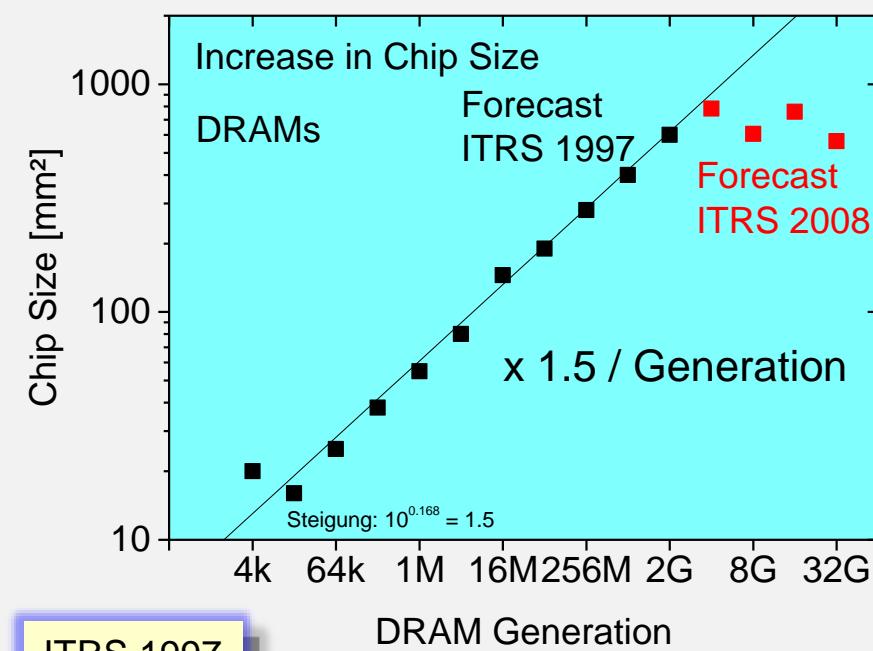
Hoerni (Fairchild) 1957
Si-Planartransistor 2N1613,
764 μm diameter



INTEL 2007
Penryn CPU,
45 nm Gate Length



INTEL 2014
14 nm Gate Length

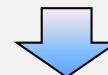


ITRS 1997

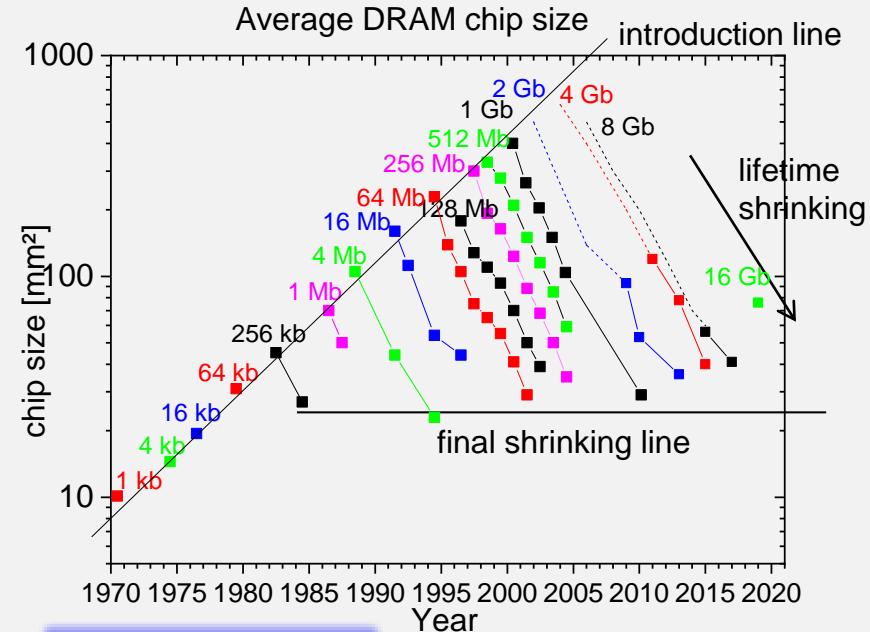
DRAM Generation

At introduction each chip is 1.5 larger than the antecessor chip at introduction

Due to continuous shrinking during chip fabrication time each chip finally ends at the same size



That's what Moore is saying:
each 3 years 4 time more transistors on the same chip



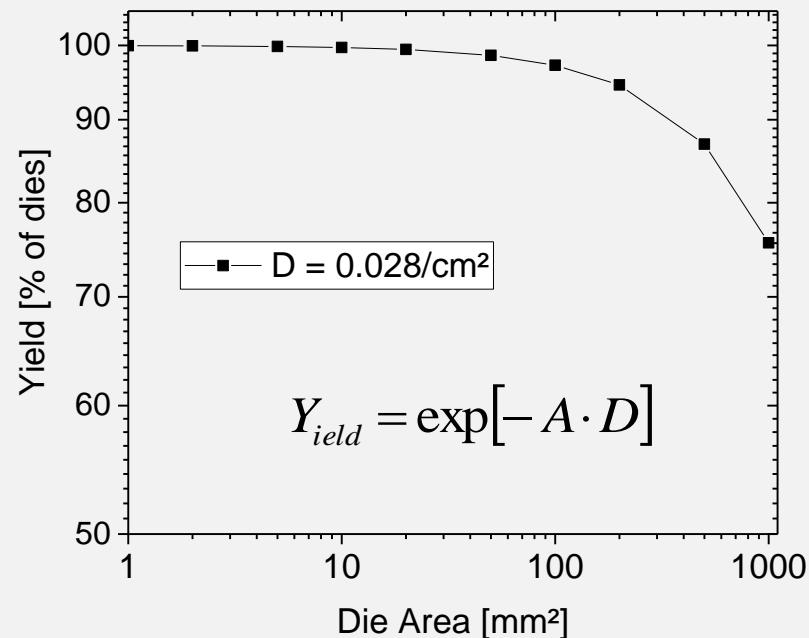
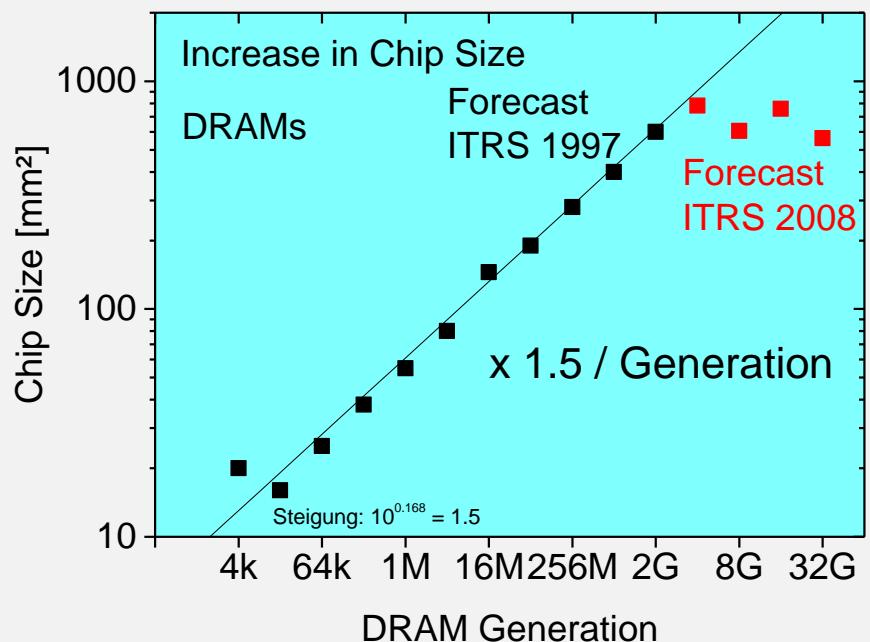
ITRS since 2008

ITRS 2015: 32 Gbit last DRAM

Maximum of chip size is ~ 700 mm²



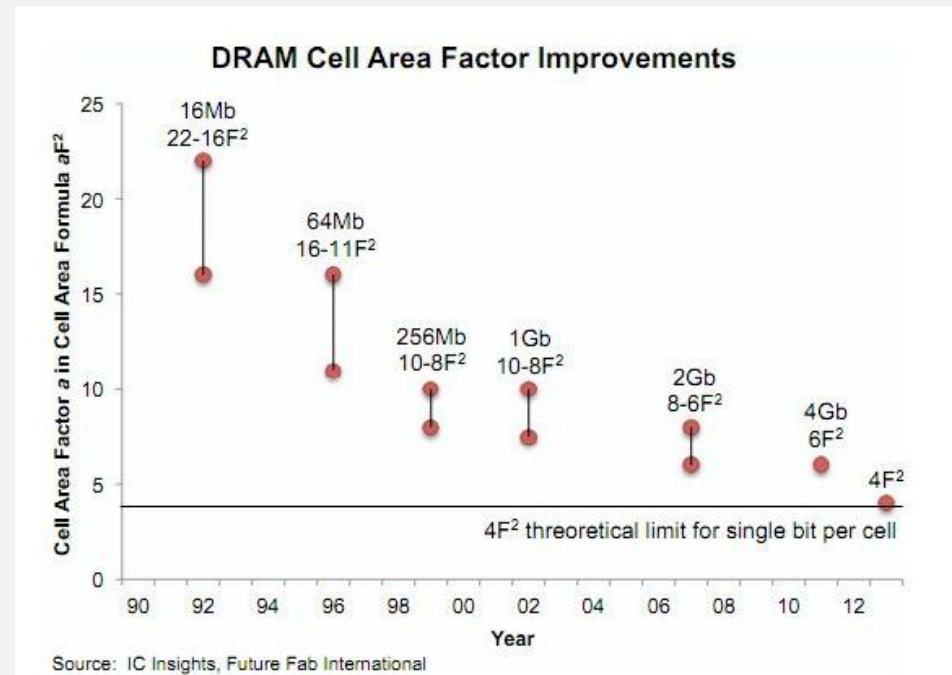
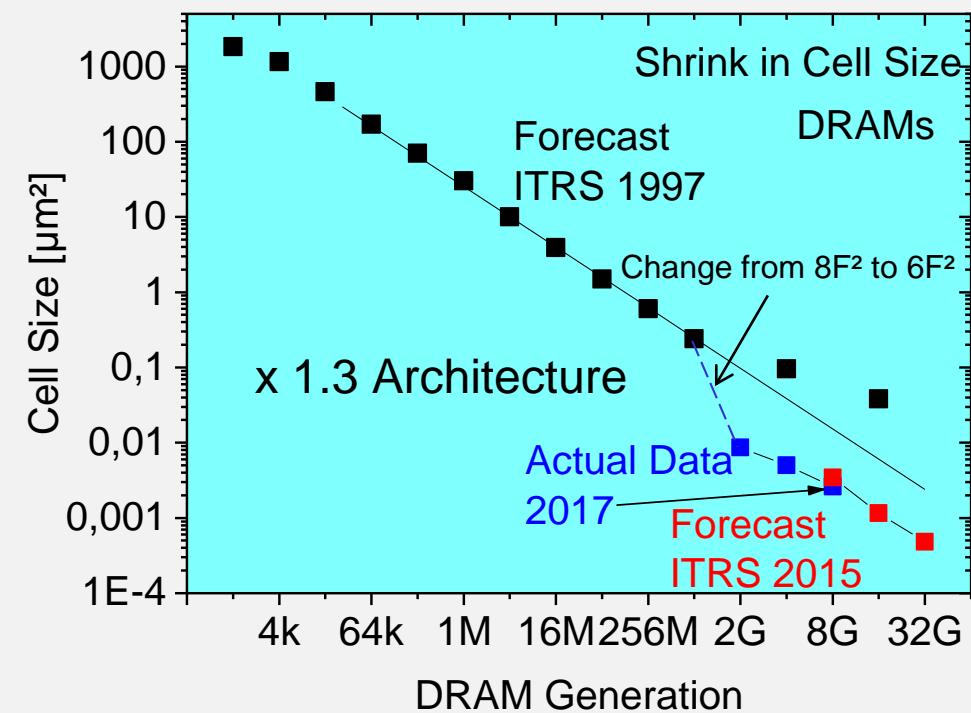
What is the reason that the chip size is not increasing?



The bigger the chip size is the smaller the yield

A bigger chip size then 700 mm² is not economical because the yield will be to small

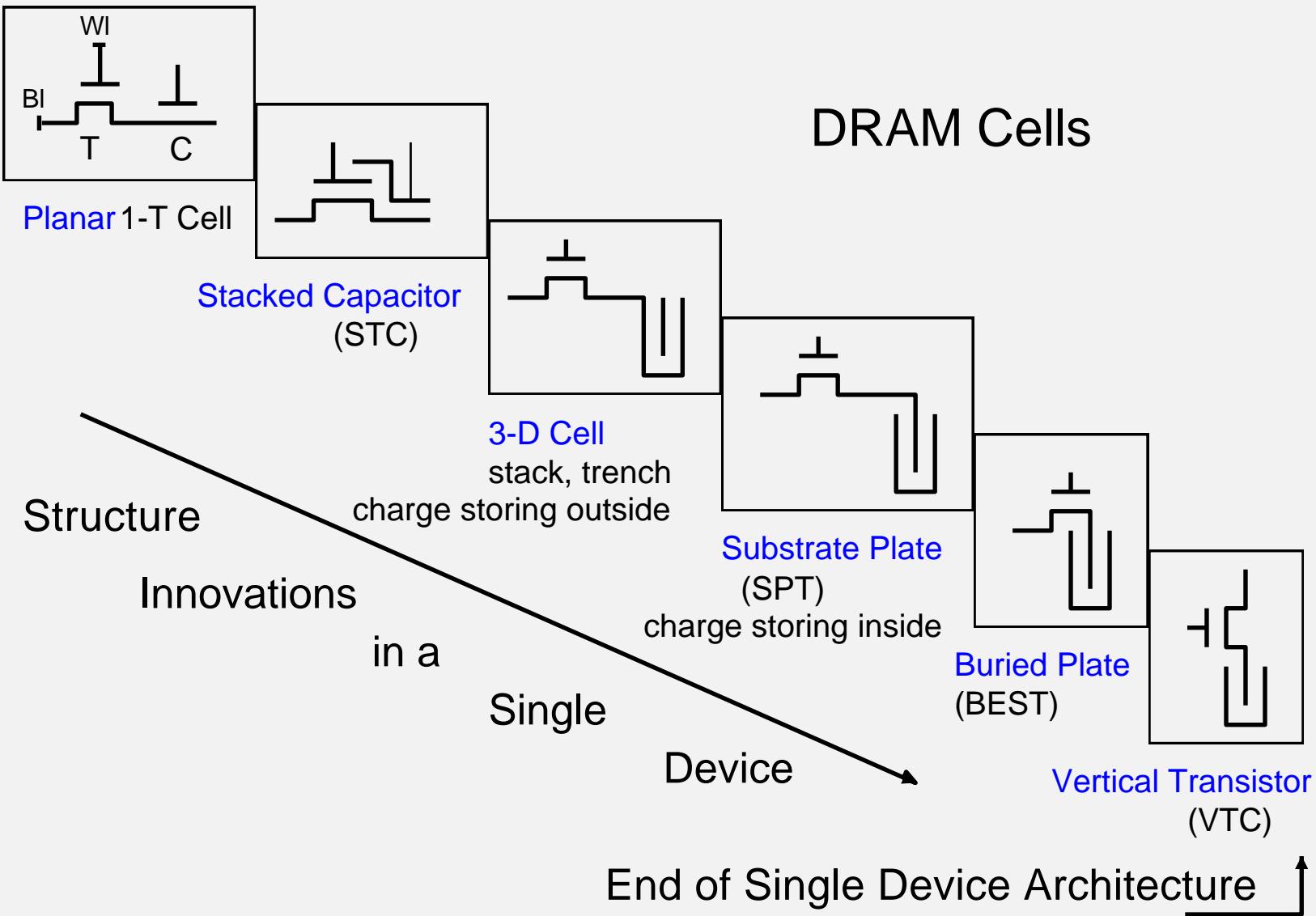
Moore's law is not taking the yield into account

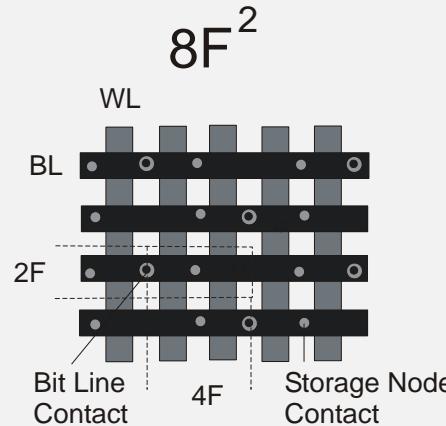


Actual Cell Size is smaller than the predicted by ITRS 1997

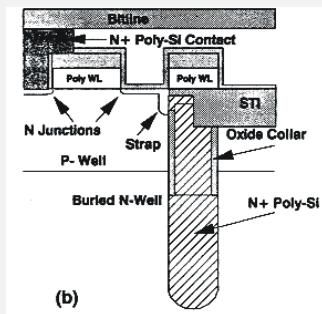
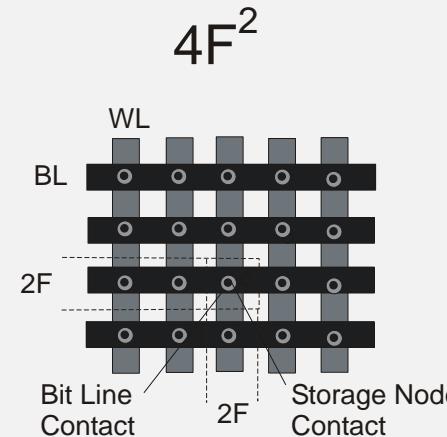


Actual Cell Size is in the range of the predicted by ITRS 2015

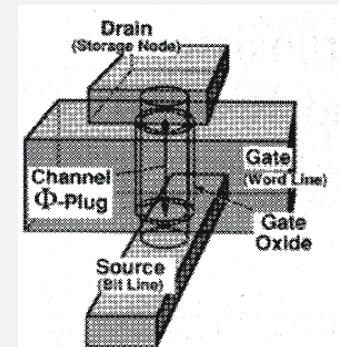
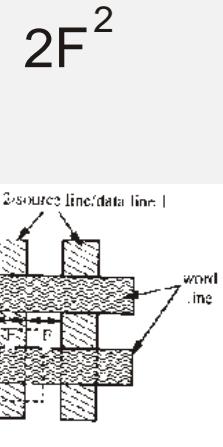


Area reduction of DRAM-cells:**BEST Cell**

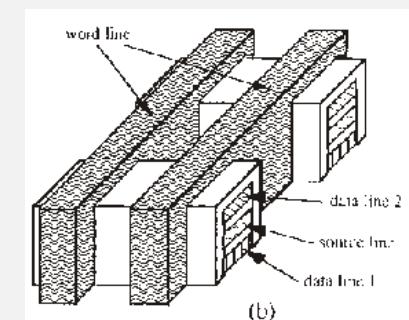
Planar MOSFET + vertical Capacitor

example: Nesbit et al., IEDM'93, 627
IBM/SIEMENS/TOSHIBA**Φ Cell**

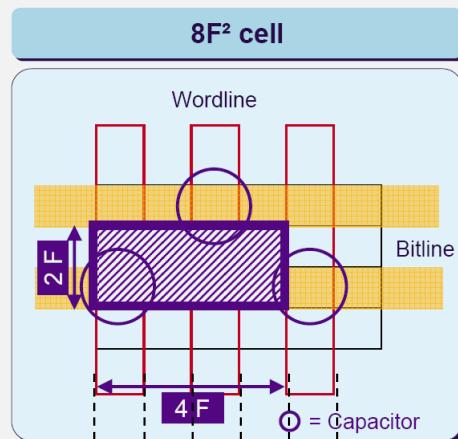
Vertical MOSFET + vertical Capacitor

example: Maeda et al., ED-42 (1995) 2117
MITSUBISHI**SEM Cell**

2 vertical SEM devices

example: Ishii et al., IEDM'97, 924
HITACHI

Examples of Architecture Improvement



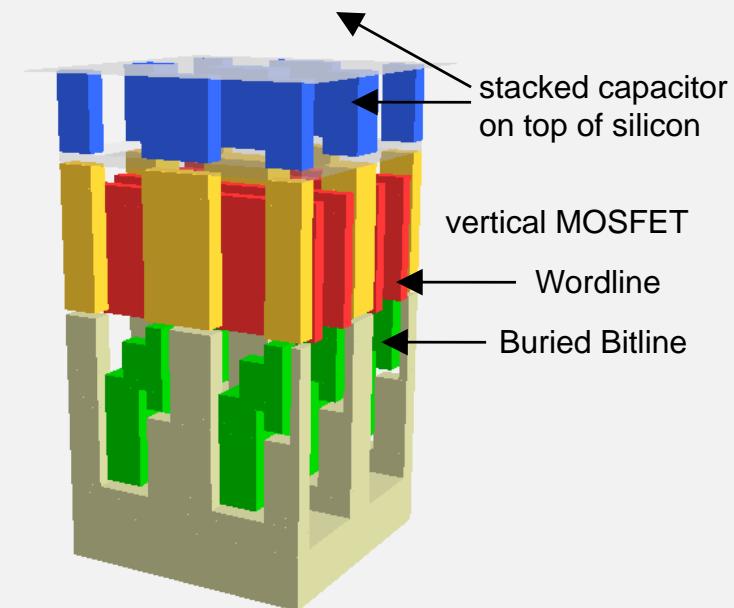
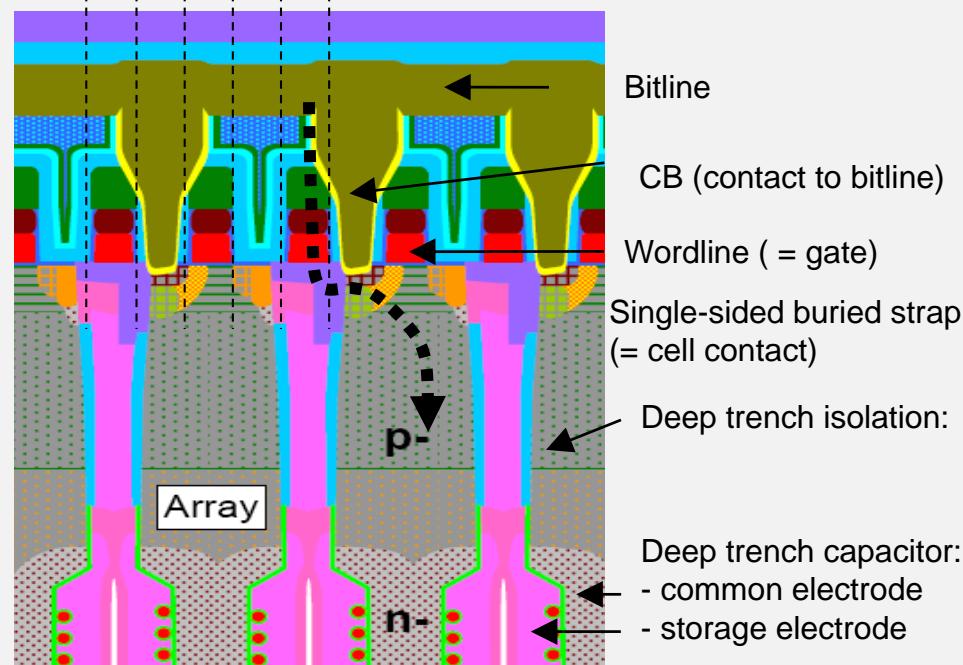
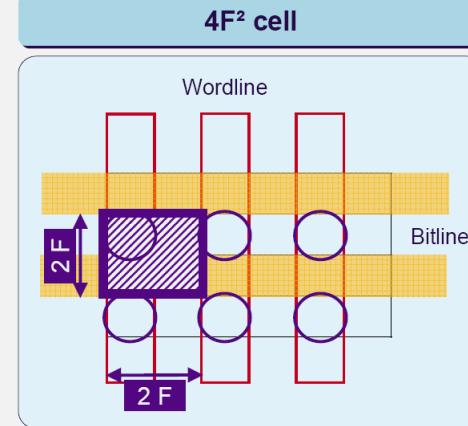
Area reduction of DRAM-cells:



Plans of Qimonda 2008

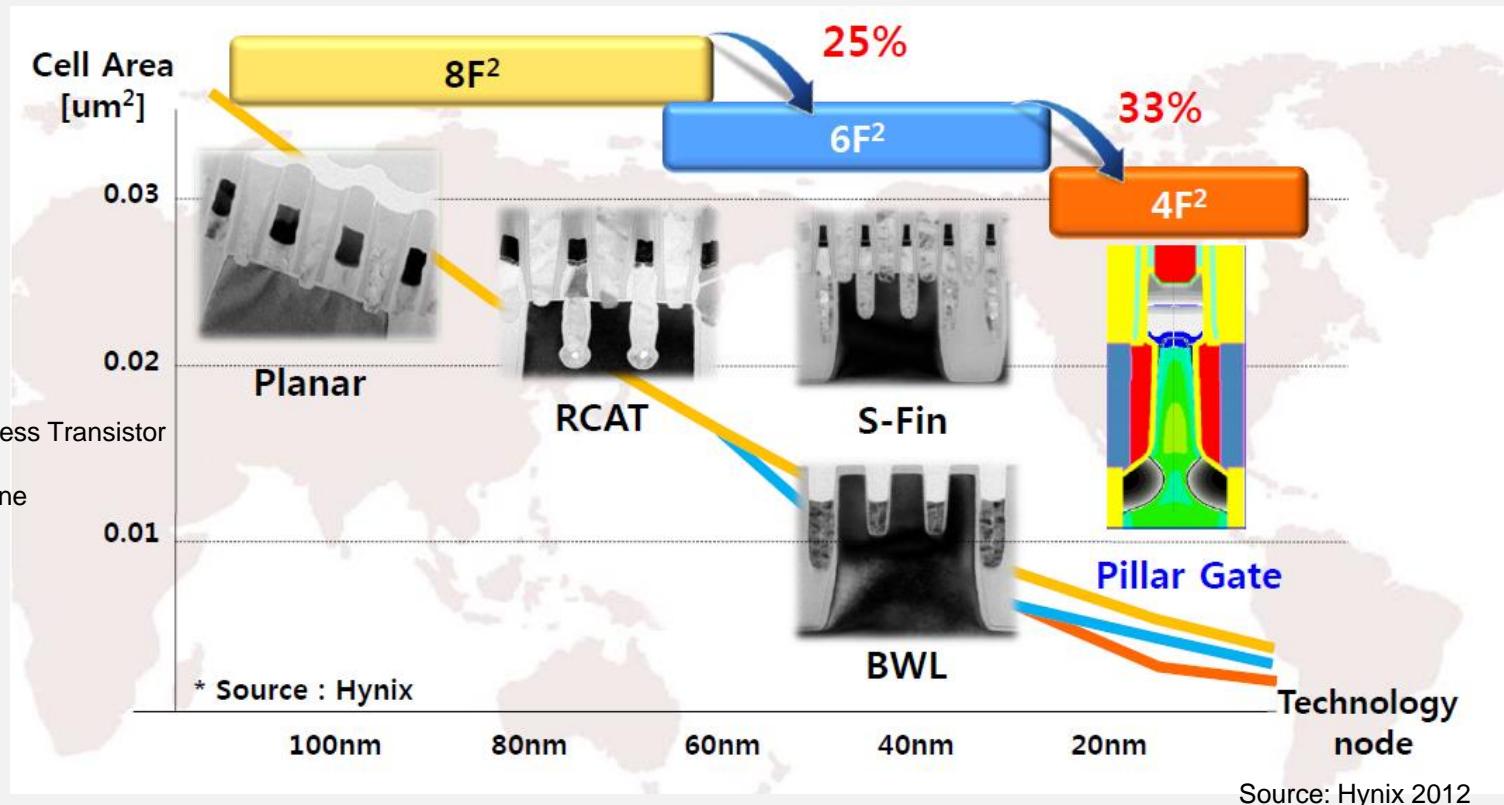
$8 F^2 \longrightarrow 4 F^2$

only architecture improvement



http://www.eetasia.com/ART_8800518931_499486_NP_c5145f4f.HTM

Today industry is talking about 10 nm class-node. The real technology node can vary from company to company (Status 2019).



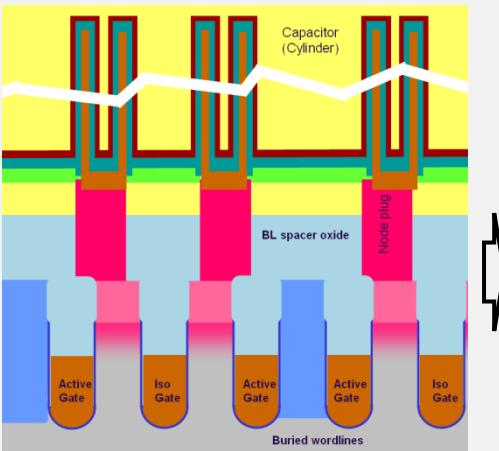
Till the 20 nm Technology Node 6F^2 as architecture is used

At 10 nm class-node (2017) there should have been the transition to 4F^2

Fabricated by mainstream CMOS-technology until the 30 nm technology node



presented by Qimonda



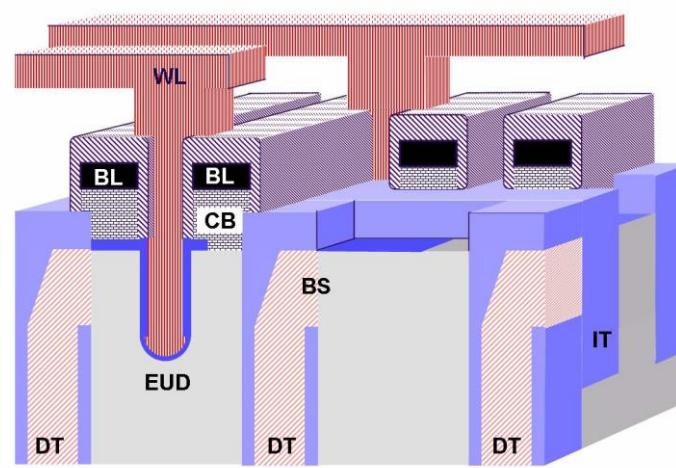
other DRAM companies like SAMSUNG, ... have similar devices in production

A novel cell arrangement enabling Trench DRAM scaling to 40nm and beyond

L. Heineck, W. Graf, M. Popp, D. Savignac*, H.-P. Moll, R. Tews, D. Temmler, G. Kar, J. Schmid, M. Rouhanian, I. Uhlig, M. Goldbach, E. Landgraf, L. Dreeskornfeld, M. Drubba, S. Lukas, D. Weinmann, W. Roesner*, W. Mueller
Qimonda Dresden GmbH & Co. OHG, Dresden, Germany; *Qimonda A.G., Munich, Germany

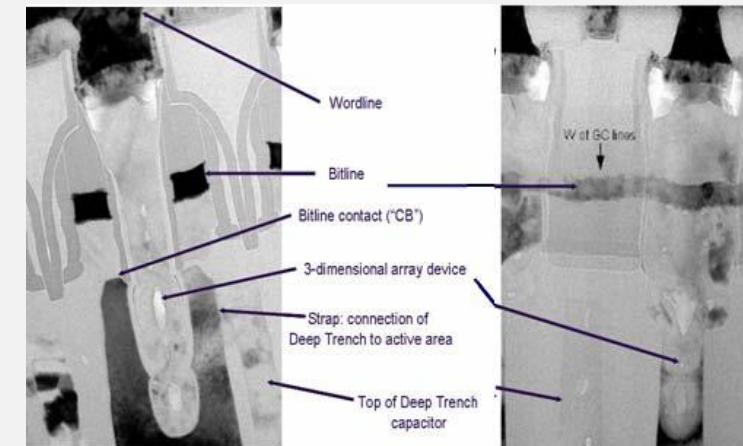
TABLE 1.
Main innovations for trench DRAM scaling - previous technologies taken from (4)

	90nm	75nm	58nm	48/40nm
Cell layout	CKB	CKB	CKB	WOB
Capacitor dielectric	NO	NO	AlSiO	HfSiON
Active area isolation	HDP	Selox/ HDP	SOG/ HDP	SOG/ HDP
Self-aligned features	1	1	1	3
Cell transistor	Planar	Planar	EUD	EUD
Support device/gate	WSix	W	W	W
Interlayer Dielectric	HDP	HDP	Low K	Low K

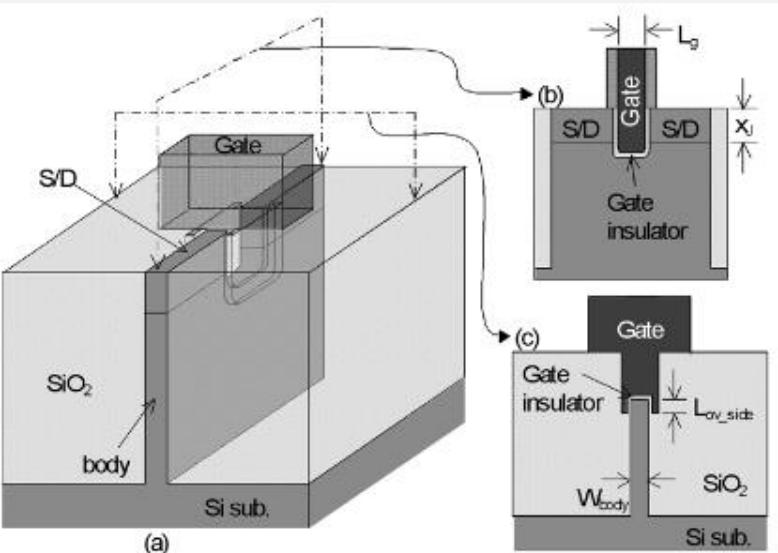


IEDM 2007:

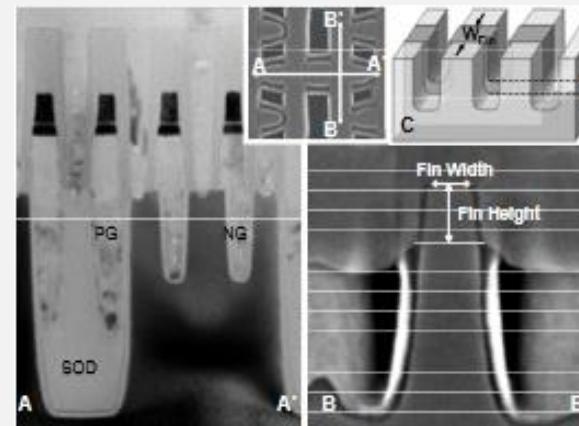
WOB = wordline over bitline



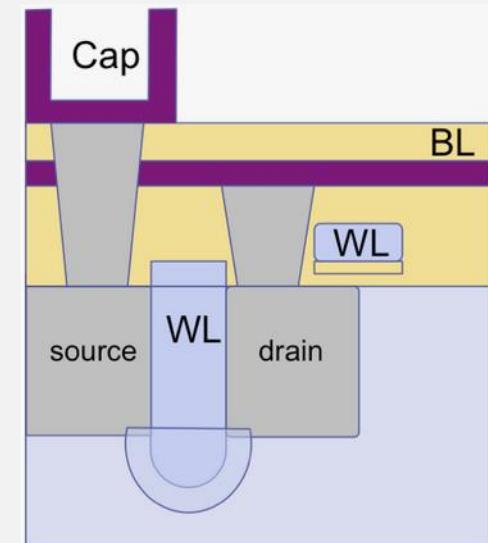
Fabricated by mainstream CMOS-technology until now



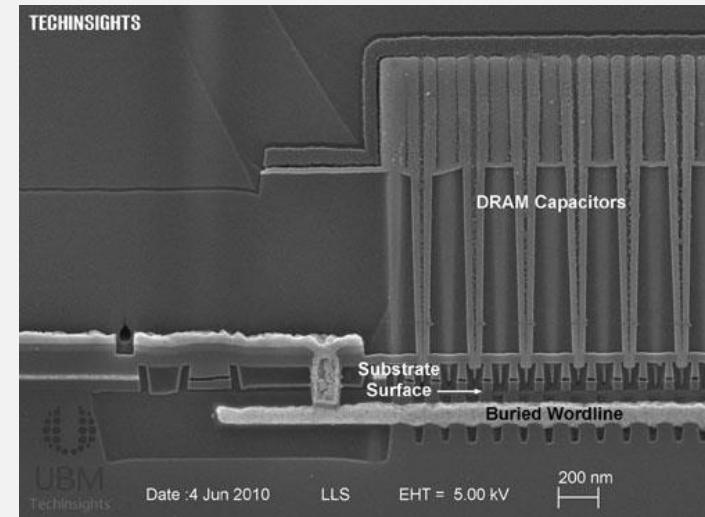
Ki-Heung Park, Kyoung-Rok Han, and Jong-Ho Lee, Highly Scalable Saddle MOSFET for High-Density and High-Performance DRAM, IEEE 2005



Hyunjin Lee et. all, Fully Integrated and Functioned 44nm DRAM Technology for 1GB DRAM , IEEE 2008



<http://semitracks.com/newsletters/november/2015-november-newsletter.php>

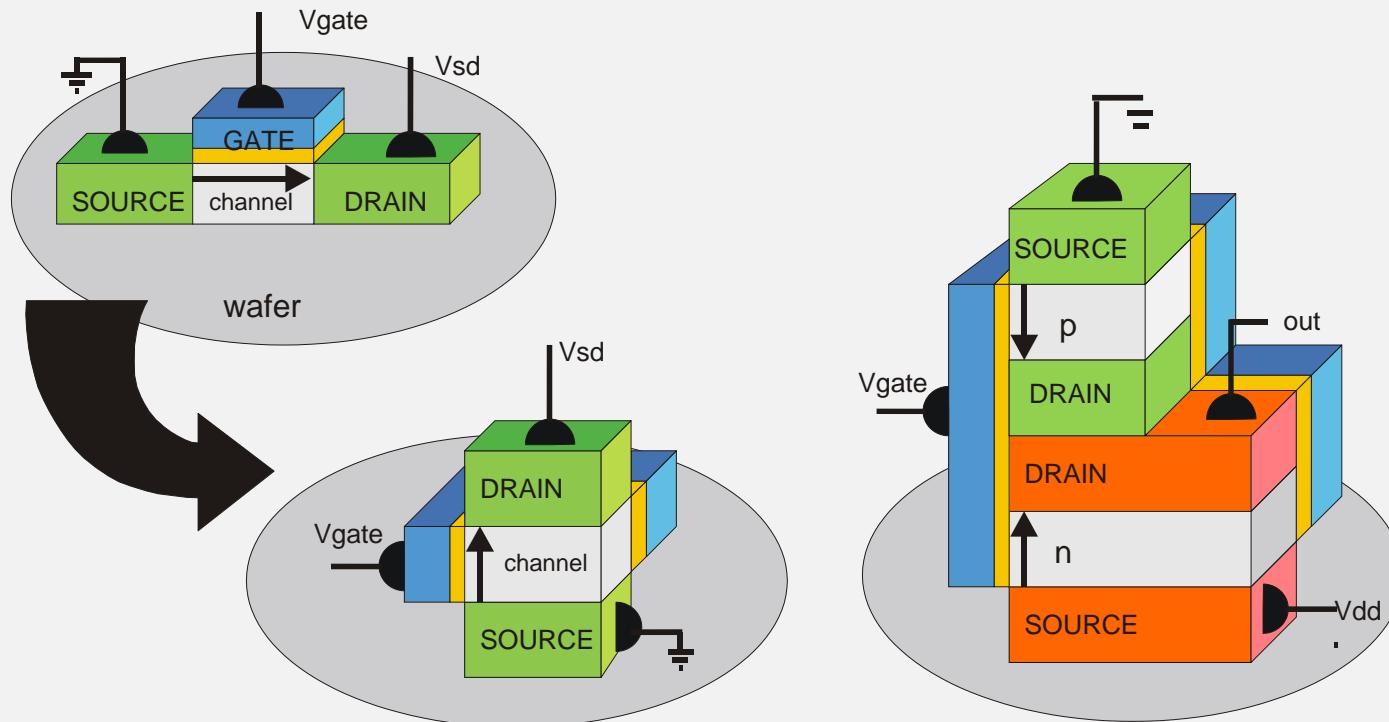


Mixture between RCAT and FinFET

Capacitor over transistor

Improved short-channel effects compared to RCAT

The concept of vertical MOSFETs



With vertical MOSFETs nm-channels can be fabricated far before planar roadmap

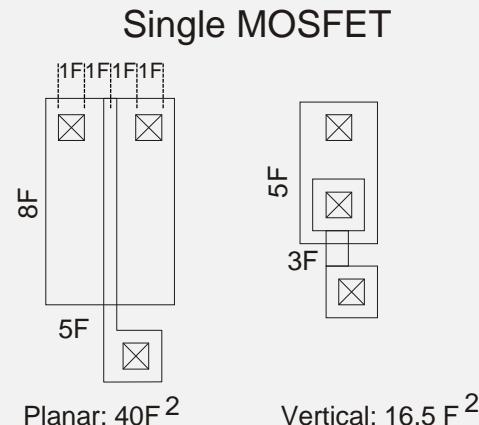
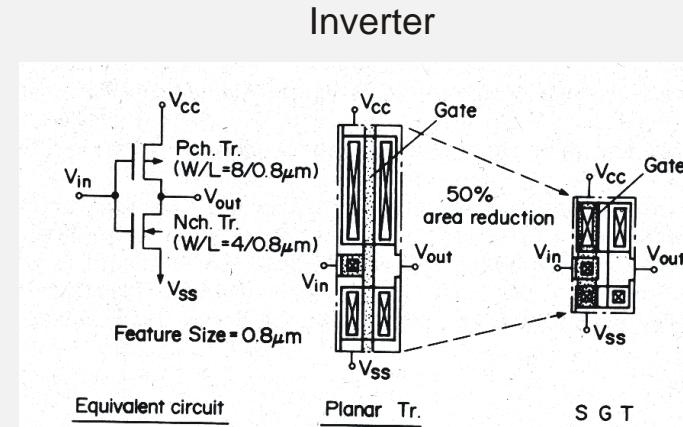
better devices



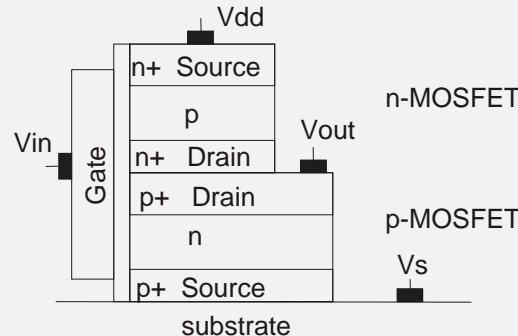
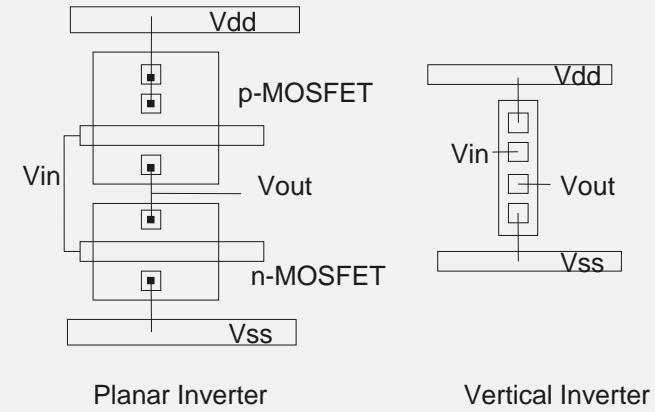
With vertical MOSFETs large area reduction can be achieved

cheaper devices

Conventional Reduction

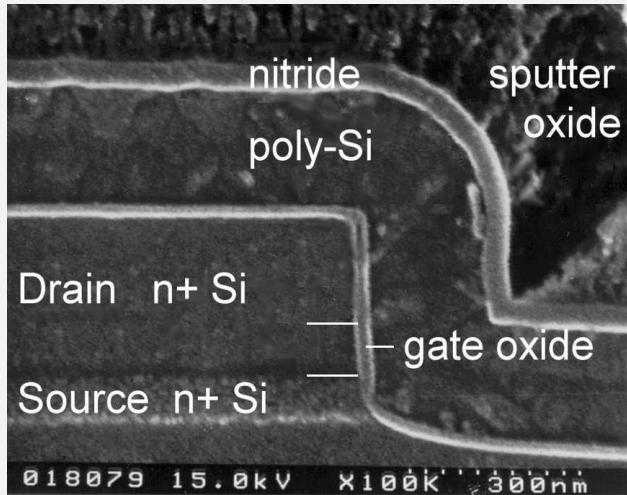
**Reduction by ~2****Reduction by ~2**

Innovative 3D Reduction

**Reduction by ~5**

With vertical MOSFETs large area reduction can be achieved





Goßner et al.: „Vertical MOSFET with Channel Lengths of 50 nm by Molecular Beam Epitaxy“
presented at SSDM'93, Jpn.J.Appl.Phys.33 (1994) 2423
Hansch et al.: ESSDERC'97
Rao et al.: IEDM'97

Early pioneer (1993) with 50nm channel length



it can be done !

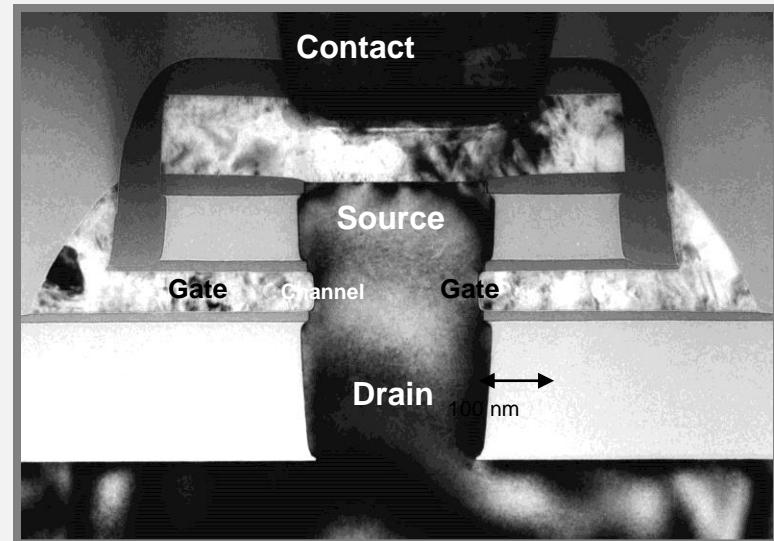
The Vertical Replacement-Gate (VRG) MOSFET:

Jack Hergenrother and Don Monroe
Bell Laboratories, Lucent Technologies
IEDM'1999

Fabricated by mainstream CMOS-technology



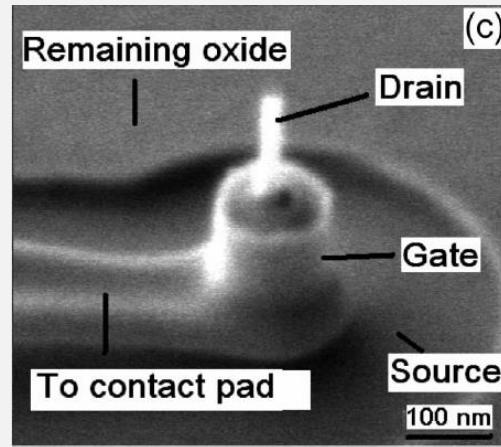
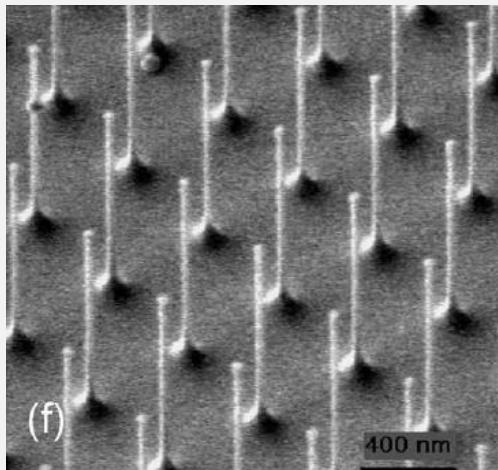
ready for industry (~2000)



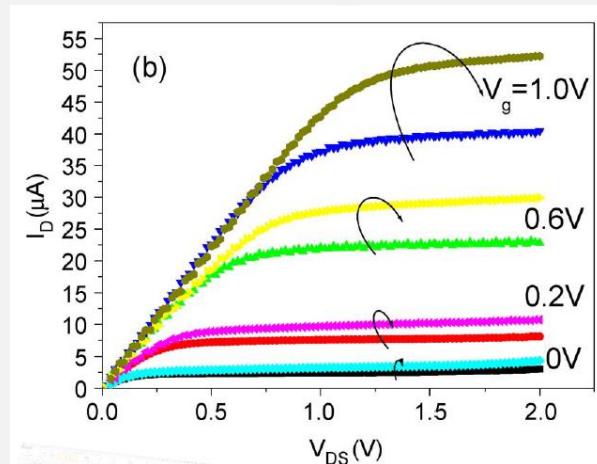
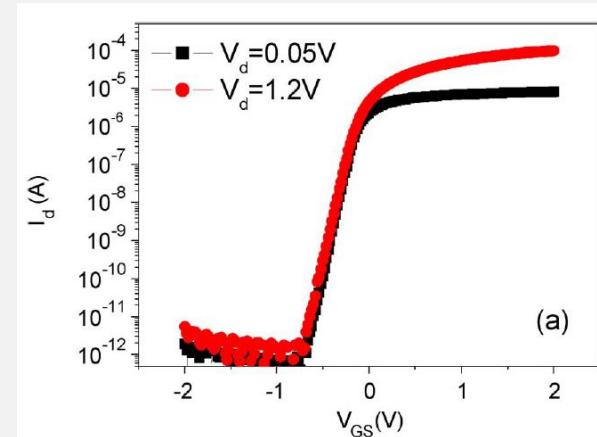
Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET

IEEE 2008

B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong



$L_G = 150 \text{ nm}$
 $D = 25 \text{ nm}$



Up to now no vertical MOSFETs are used in industry,
mainly because planar MOSFETs could fulfill Moore's Law

Anyhow vertical MOSFETs are still under investigation.

Details will be explained in chapter 6.8

ITRS 2015: 32 Gbit last DRAM

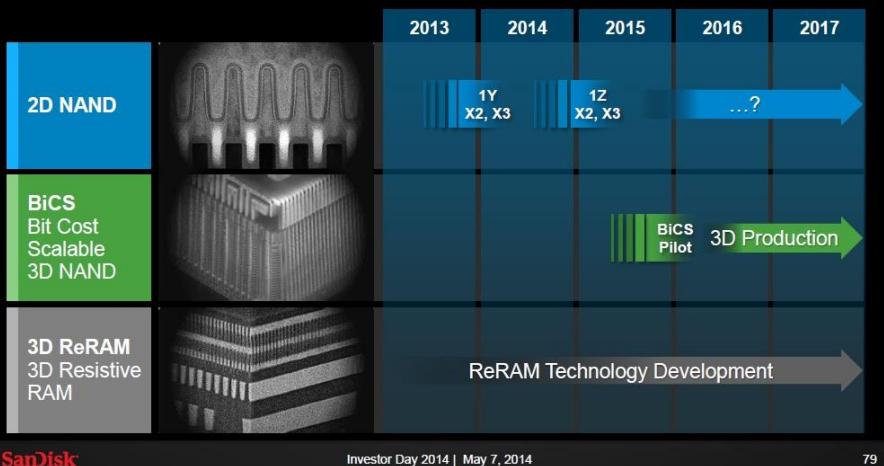
No better architecture than 4F² possible

Seems that the 10 nm technology node will be the last 2D-DRAM

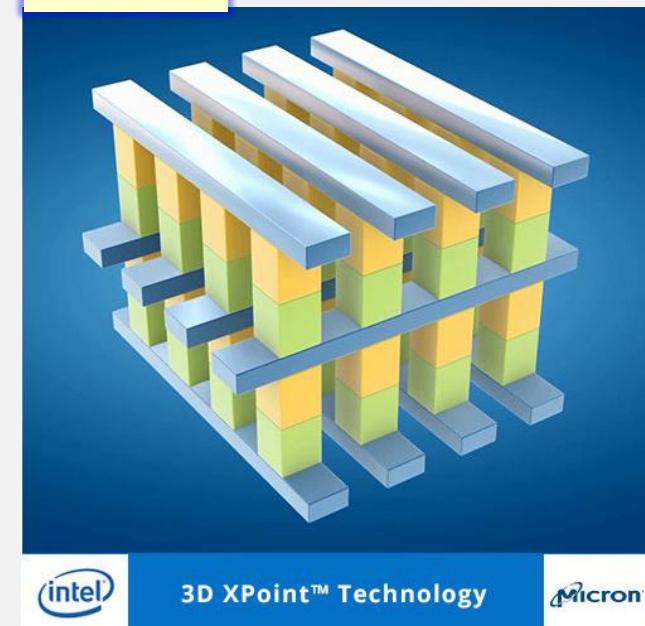
All big companies see the RERAM/RRAM (resistive RAM) as an alternative for DRAM and Flash NAND

2014 SanDisk

SanDisk Technology Roadmap



2016 Intel



Details will be explained in chapter 6.9

Following Moore's Law (only true for MOS-technology) with shrinking dimensions exhibits:

a performance advantage due to shrinking:

- faster devices
- reduction in power consumption
- more devices per chip
- higher storage capacity / higher computational power

Question 1: Why not to make the smallest devices now, instead of following Moore's Law ?

Long Answer 1:

- Developing smaller devices consumes development money
- Fabricating smaller devices needs many suitable equipment (which must be developed, qualified and available)
- Chip performance is embedded in many electronic systems which are fabricated by many companies
 - > to ensure a large market all users should be able / ready to use the advantage of better performance
(example: no use of 1GHz chip on a 33MHz motherboard, no use of 1Tb-DRAM in a consumer PC today)

Following the time scale given by Moore's Law choreographs the whole market for maximum efficiency and money

Short Answer 1: In a historical grown and highly complex system like semiconductor fabrication only small development steps can be done to keep things running. Revolutions usually break down established systems.

Question 2: How long will Moore's Law hold ?

Technological Answer: No one knows, there are red walls everywhere, but we trust in GOD (and history)

Economical Answer: As long as increasing cost for smaller devices are lower than the selling price

Let's have a closer look to the economical advantage of Moore's Law



as smaller the devices are

- as more chips are on a wafer
- as higher the yield (defect density) -> as more good chips are on a wafer
- as lower the fabrication costs per device (we will see how long)

2.1 Introduction

2.2 Market demand for highly Integrated Circuits IC

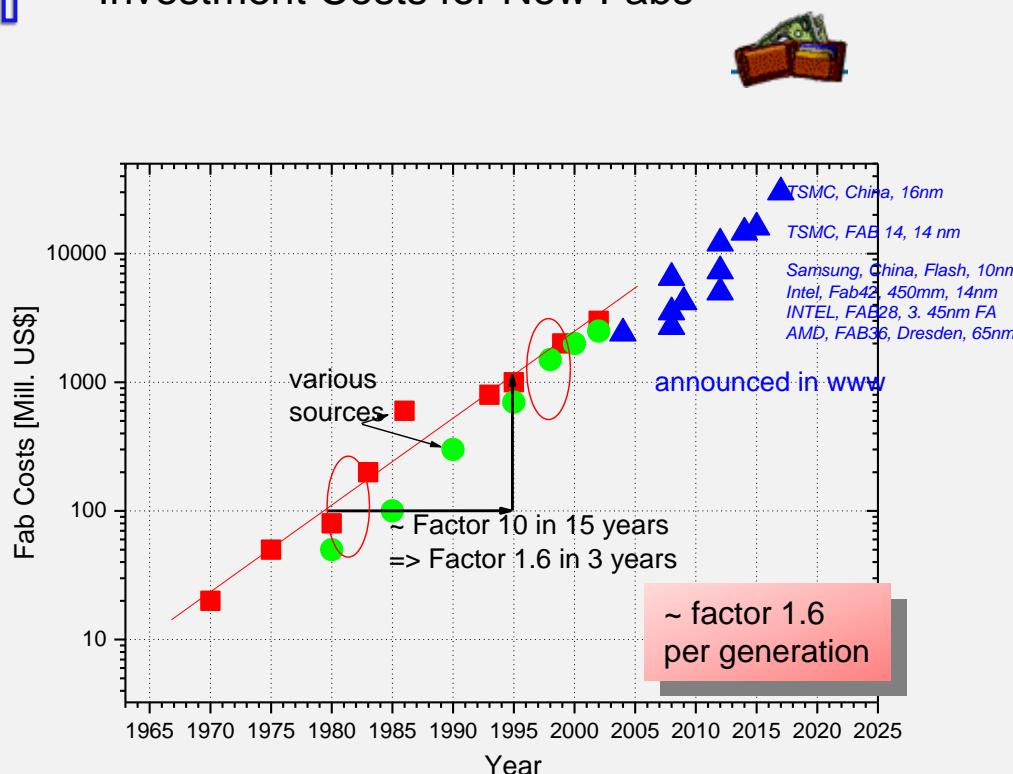
2.3 Shrinking: Making Money

2.4 Shrinking: Spending Money

2.5 Calculation of Semiconductor Industry

2.6 Market Information on ICs

1 Investment Costs for New Fabs



2 Increasing Process Complexity

(e.g. INTEL, source: *press publications*)

Intel CPUs	Number of Masks
386	10
486	12
Pentium	18
Pentium IV (2004)	25

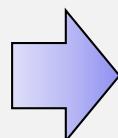


3 Increasing Production Costs / Generation

Equipment	+ 50 %
Pure Materials	+ 35 %
Process Steps	+ 25 %
Test	+ 20 %
Production Costs	+ (30-50) %

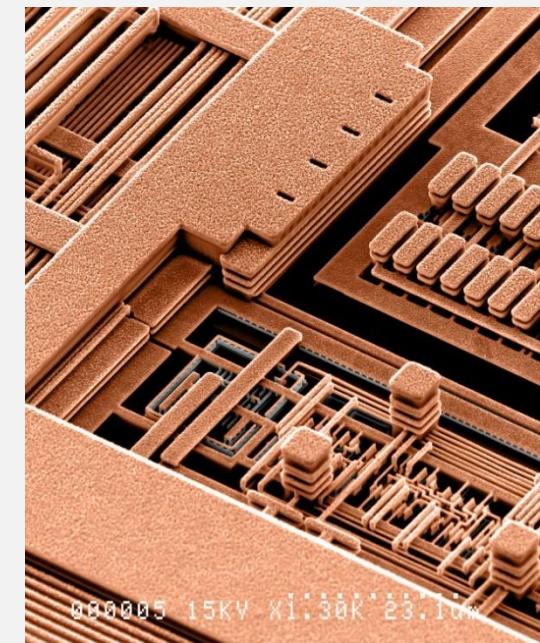
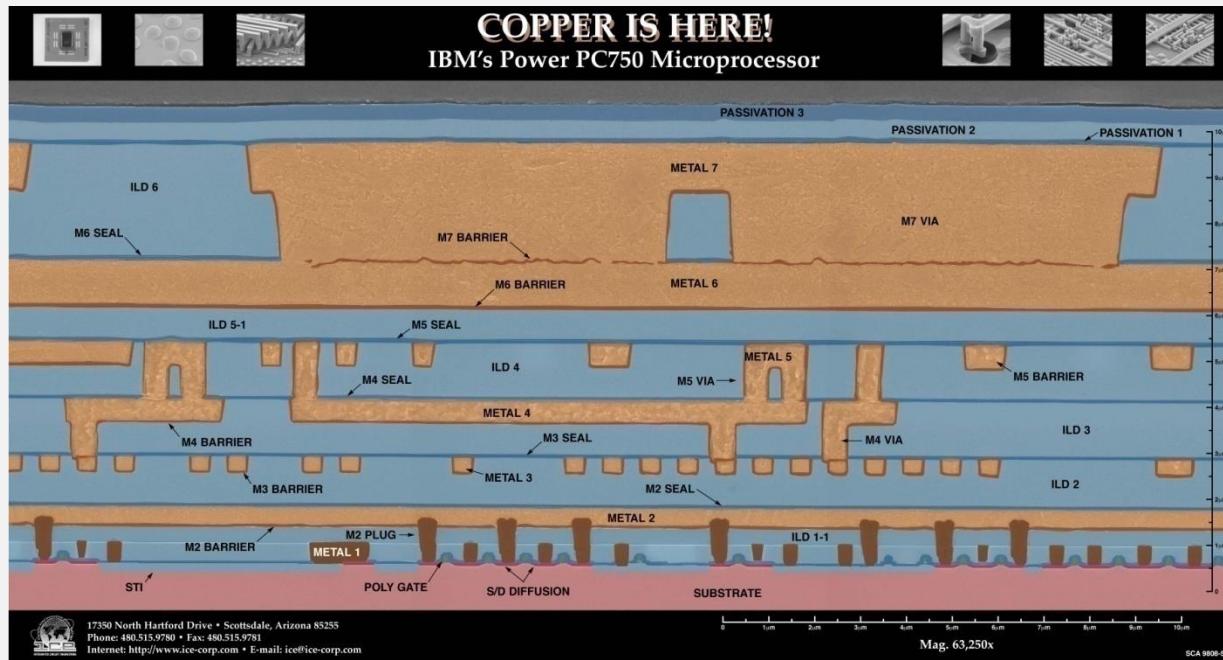


Cost Reducing Strategies



1. Around 2000 with 300mm wafer automation and Mini-Environments
2. Cooperation (Sharing costs, risks and time)

~ factor 1.5 per generation



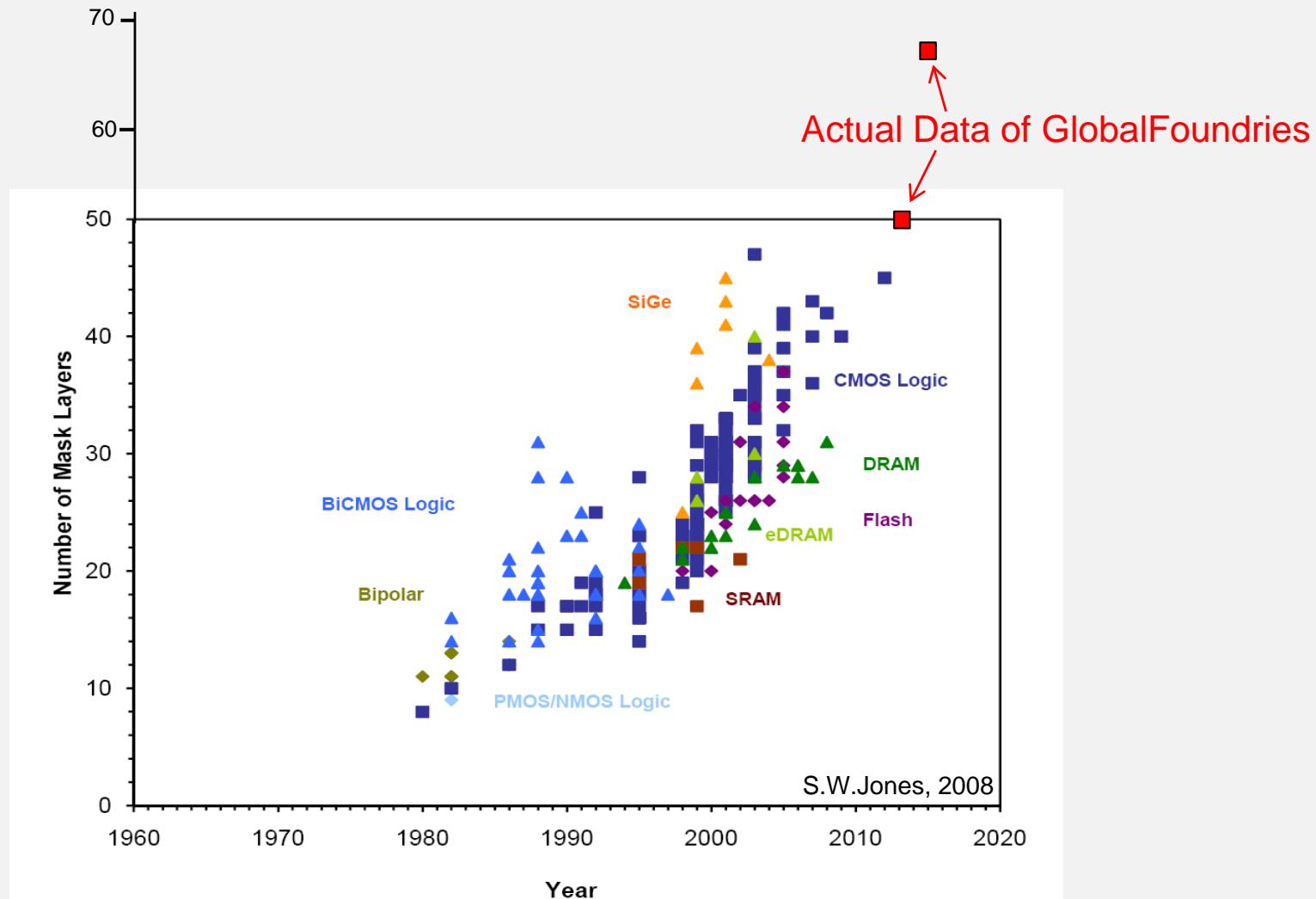
Higher fabrication costs due to more processes:

Due to shrinking geometries (-> increase in RC-delay times)
more and more metallization layers must be fabricated.

- 1970: 02-03 Metallization layers (poly-Si, Al)
- 2000: 06-07 Metallization layers (poly-Si, W, TiSi, CoSi, Cu)
- 2012: 10-12 Metallization layers (high-k, low-k, SiGe,)
- 2018: 10-13 Metallization layers (... , air-gaps, new workfunction layers)



Exponential increase in fabrication costs

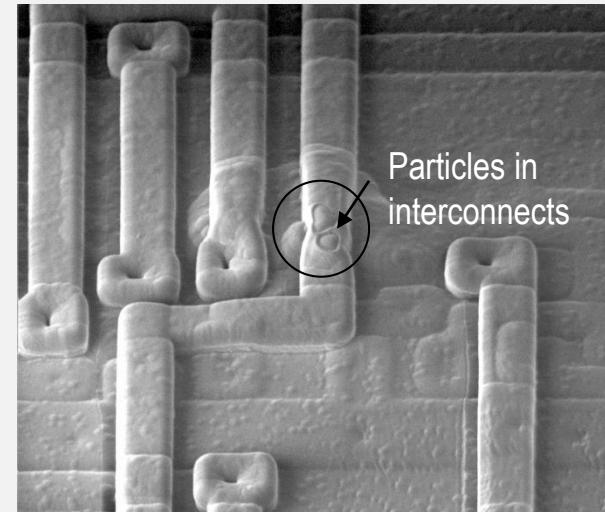
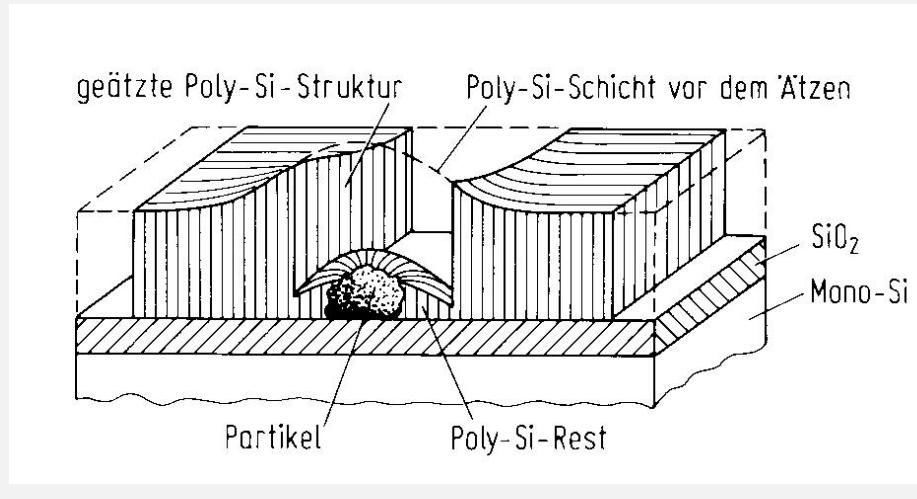


Circuit elements are formed in a repeated process of mask steps.

The number of steps differs by maker, but is normally 40~44 for 40nm DRAM and 35 for 30nm NAND

The number of steps for ~50 for 28nm logic, ~66 16/14nm logic, ~80 7nm logic (no EUV used).

Avoiding particles:



Experience

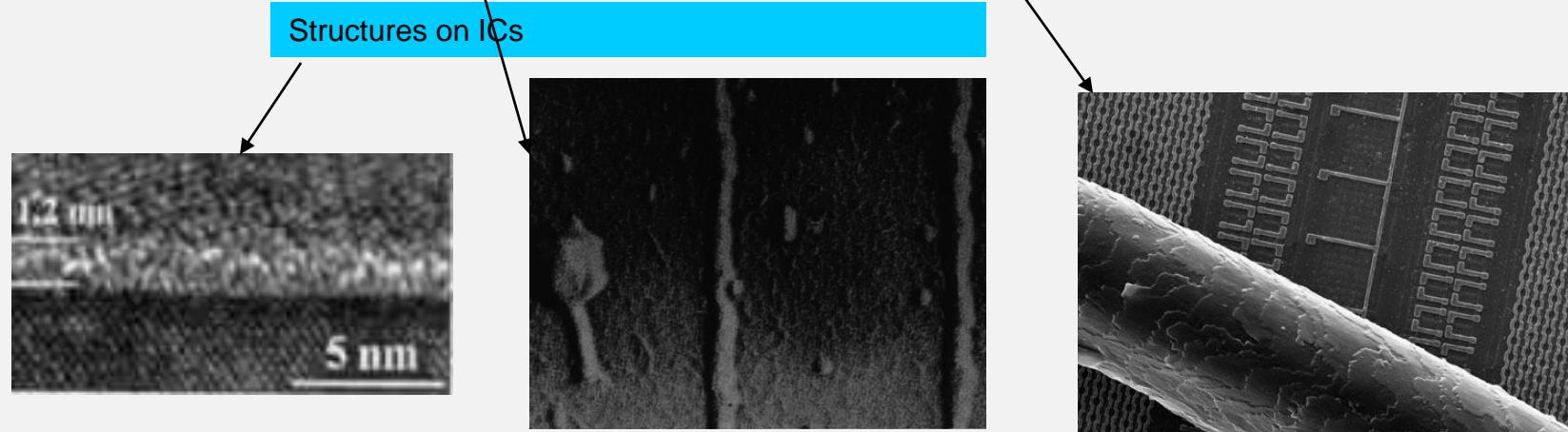
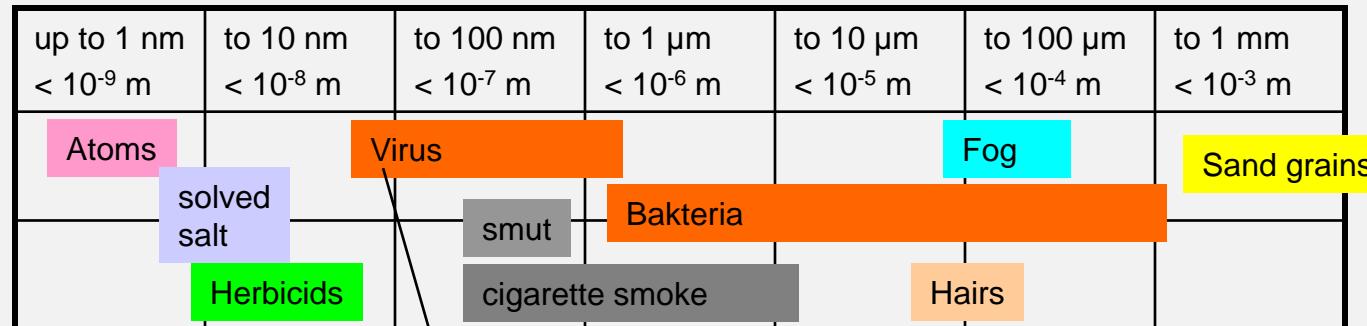
Particles, larger than half of the structure,
are killers !

An IC, consisting of 1 billion transistors (eg. 1 Gb- Processor, price ~ 500 €) may be destroyed
by one single ! particle

1) From vulcano eruptions, combustion engines and environment pollution reactive gas molecules like CO, NO, SO₂, O₃ ... are created, which act as nucleation center for additional molecules -> creation of ultra-fine particles (3-10)nm, ~ 100 – 10'000 / cm³

2) Larger particles are formed by salt dust over the oceans, virus, bakteria, pollen, vulcano eruption and erosion, ashes, dirt

Dimensions



Gate-Oxide: thickness 1.2nm
= 5 atoms

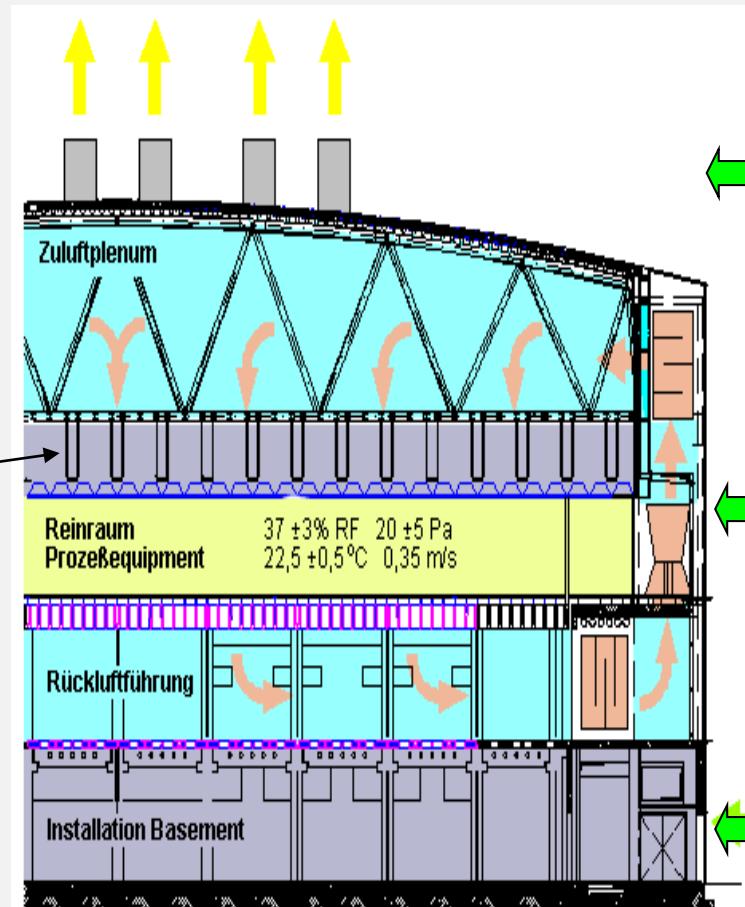
T-Phagen-Virus (~20nm) near e-beam PMMA-lines

Hair (~30µm) on 4-Mb DRAM



Most airborne particles equal the size of structures on ICs

Filter ceiling with approx. 5,000 aerosol particulate filters



5 process exhaust units, each with 105,000 m³ / h (with exhaust purification)

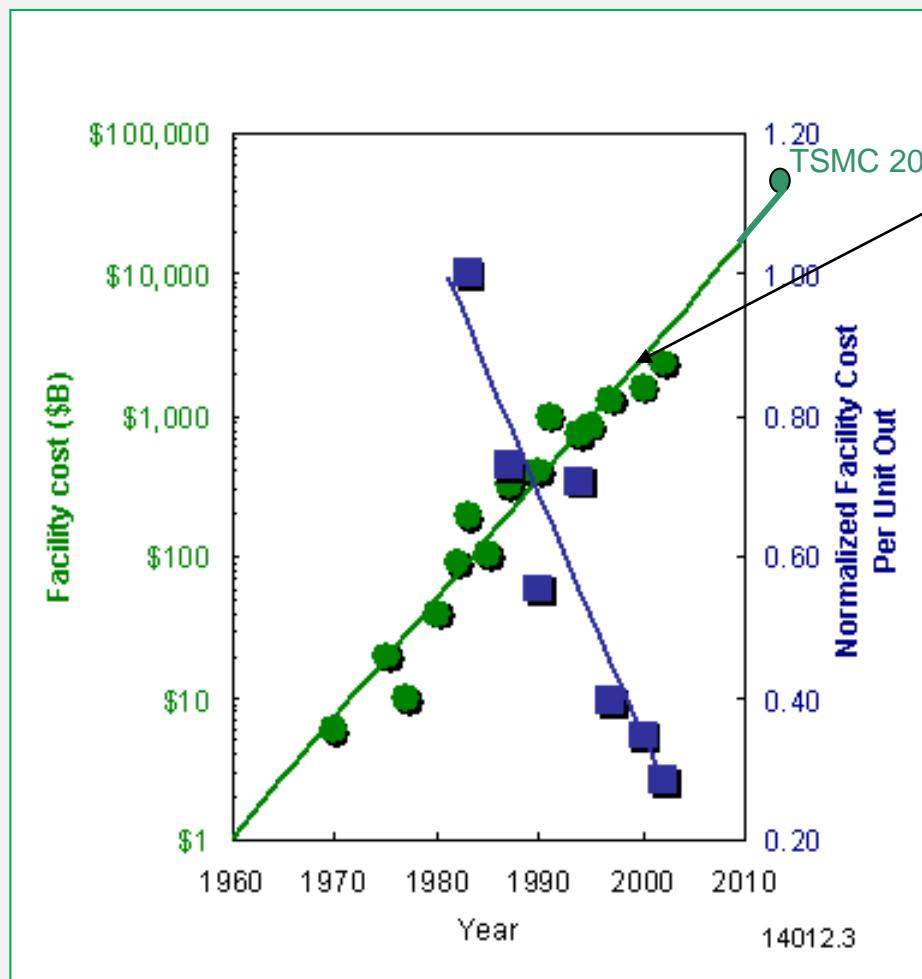
34 air circulation units, each with 165,000 m³ / h (air is filtered up to 363 x per hour using ultra-small filter sizes)

7 fresh-air make-up units of 60,000 m³ / h with pre-filtration, humidifier, fine filtration aerosol particulate filters (sufficient for airconditioning for 10,000 people)

Example:

The clean room of a modern 512 Mb-DRAM Fab (e.g. Infineon Dresden) has a foot print of about 5000 m² and is surrounded by 4 floors of air condition.

der Bundeswehr



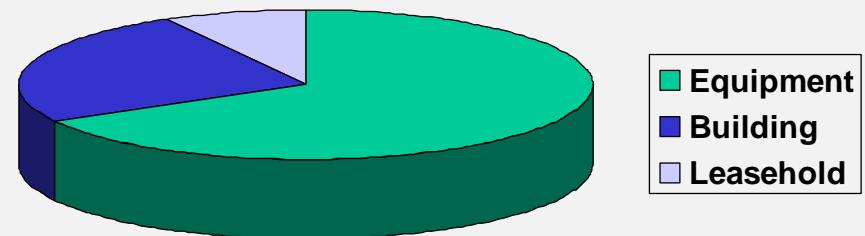
Year 2005:

Fab hardware costs: ~1'000 to 2'000 Mill. €

(lifetime ~ 3 generations ~10 years)



67% Equipment (50% rise per generation)
25% Building (mainly cleanroom)
8% Leasehold



Fabrication costs: ~ 1-2 Mill. \$US per day !



200 mm wafer, 1000 wafer/day

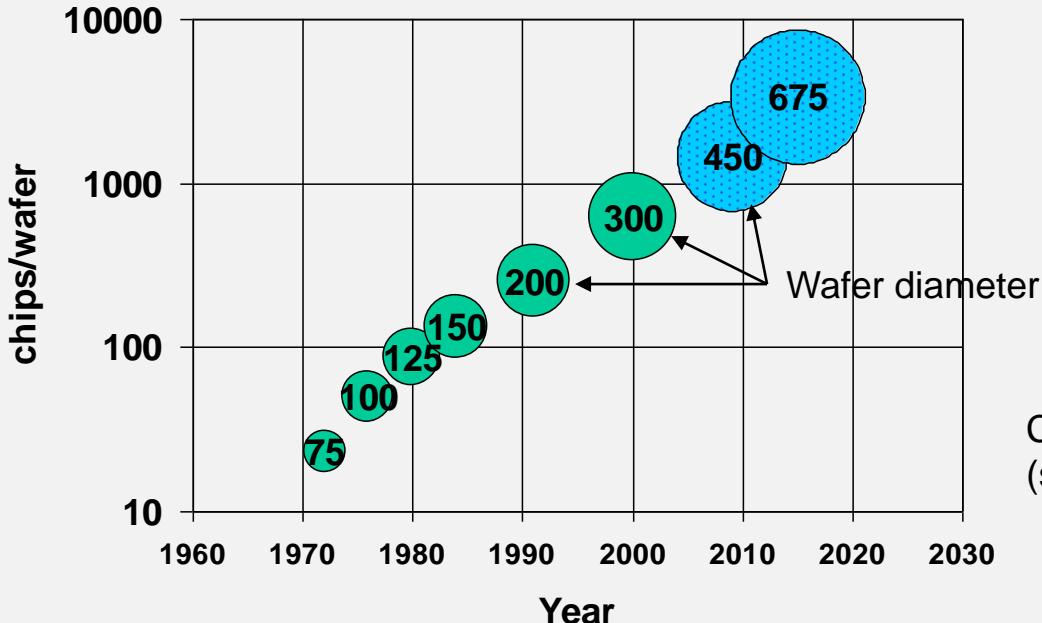
2005: from: http://www.icknowledge.com/economics/fab_costs.html

Shrinking causes:

Fabrication costs are rising exponential

Where is the economical advantage of shrinking ?

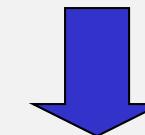
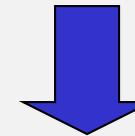
- 2.1 Introduction
- 2.2 Market demand for highly Integrated Circuits IC
- 2.3 Shrinking: Making Money
- 2.4 Shrinking: Spending Money
- 2.5 Calculation of Semiconductor Industry**
- 2.6 Market Information on ICs



Larger wafers will result in more chips

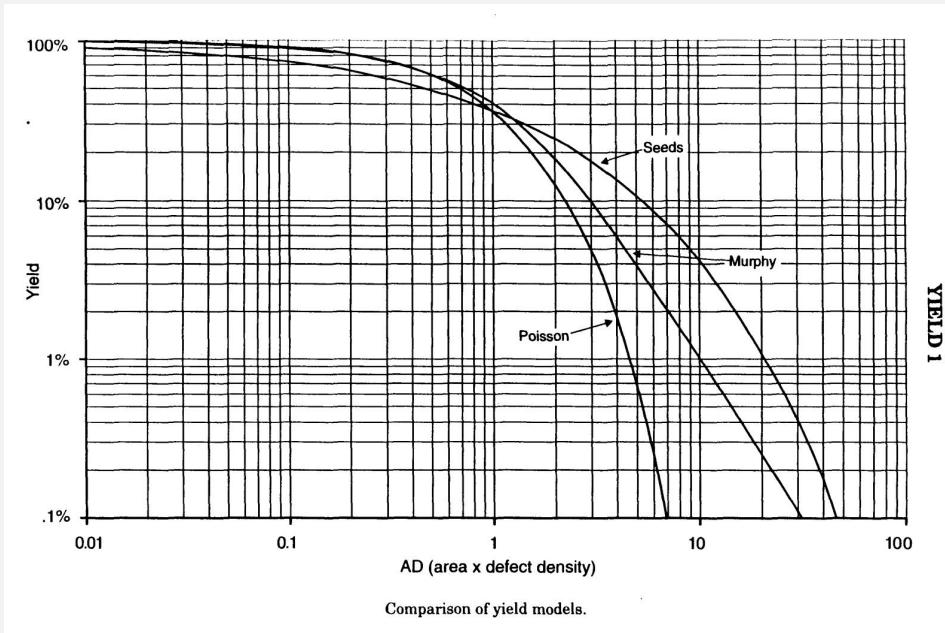


Calculation of number of chips vs. wafer size and chip size
(see exercises)



DRAM (in volume)	4kb	16kb	64kb	256kb	1Mb	4Mb	16Mb	64Mb	256Mb				1 Gb	
Year	1974	1976	1979	1982	1985	1988	1991	1994	1997	2001	2004	2007	2010	2013
wafer dia [mm]	75	100	100	125	150	150	200	200	200	300			300	
Number of 1cm ² -chips	21	50	50	86	132	132	~250	~250	~250	~600			~600	
Actual chip size [mm ²]	24	16	25	45	54	91	140	190	250	400			~30	
Number of actual chips	140	415	254	217	266	147	174	122	89	132			~2000	

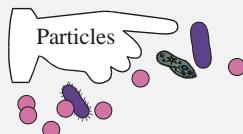
From the critical area A and the density of particles D [cm⁻²] on the chip the number of working ICs can be calculated:



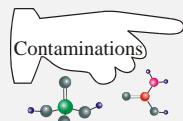
-homogeneously distributed, random particles:
-> Poisson-distribution

$$Y_{yield} = \exp[-A \cdot D]$$

Vice versa the number of allowed particles in the process air can be calculated with the projected yield (of course close to 100%) as a starting point:

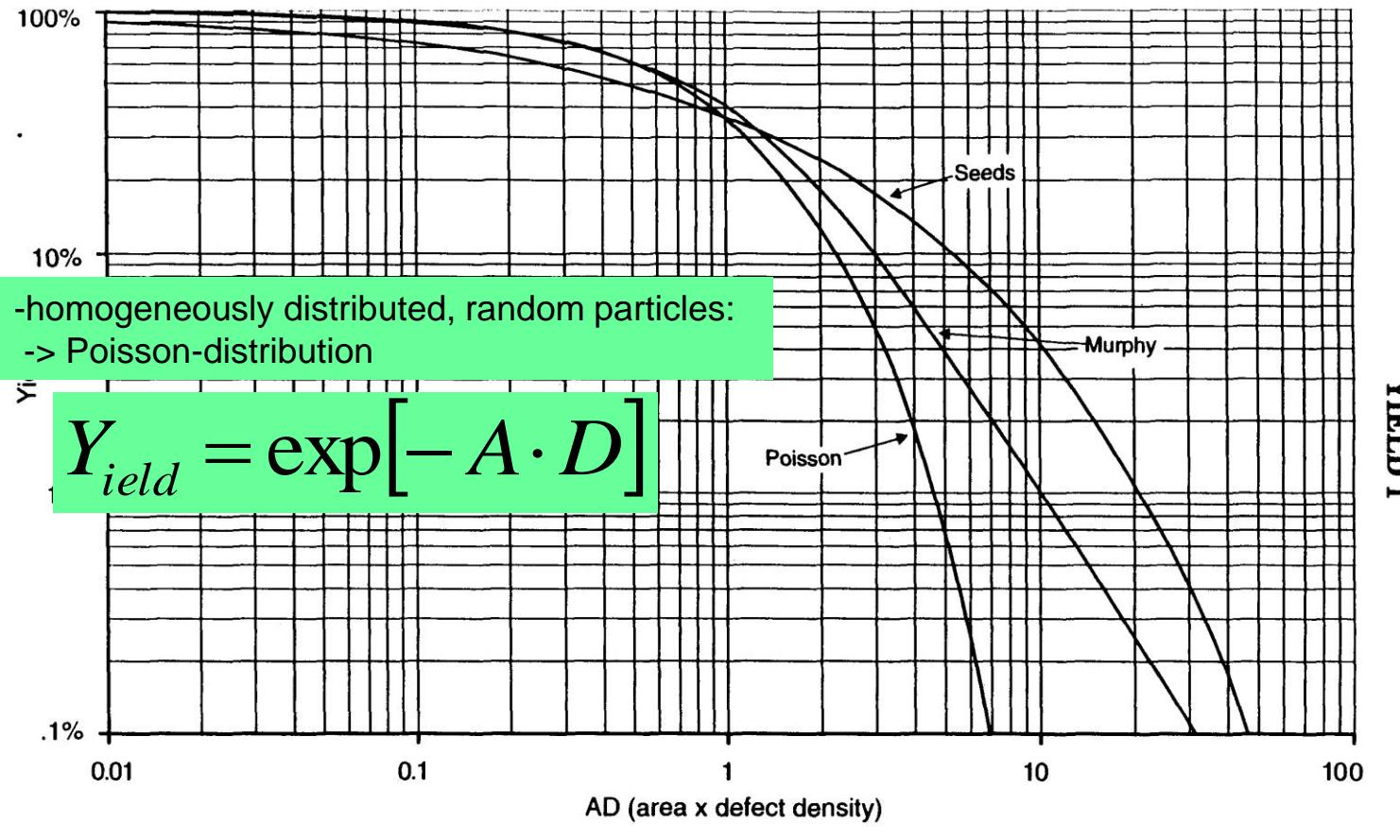


for 250 nm DRAM -> less than 27 particles/m³ > critical size (125nm) were requested
for todays 22 nm DRAM -> less than 1 particle/m³ > critical size (10nm) are requested



for 250 nm DRAM -> less than $2.5 \cdot 10^{10}$ at/cm² of critical metals were requested
for todays 22 nm DRAM -> less than $2.5 \cdot 10^9$ at/cm² of critical metals are requested

From the critical area A and the density of particles D [cm⁻²] on the chip the number of working ICs can be calculated:



Comparison of yield models.



As smaller the chips are as higher the yield (number of good chips) for a given defect density

Example: Fabrication costs per wafer

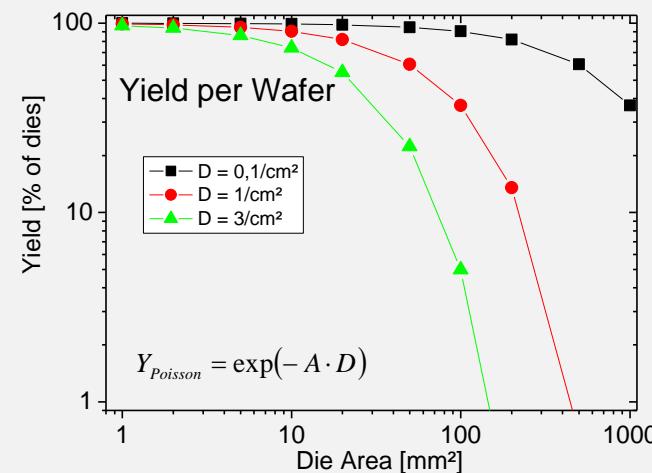
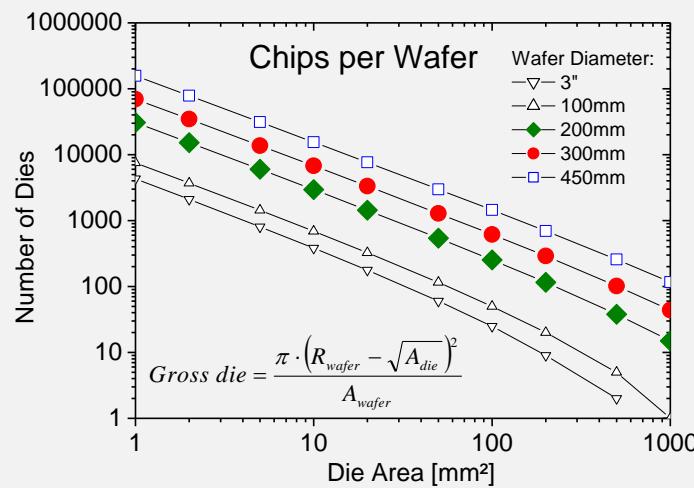
Technology (~1990)	Application	3"	100mm	150mm
NMOS (array) + CMOS	1 Mb DRAM	75 USD	90 USD	130 USD

with:
wafer size: 100 mm
die size: 9x9 mm²
defect density: 3 / cm²

Production Costs per working chip

6.92 \$

Redesign
Shrink by 15 %

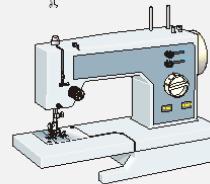


Production Costs per working chip

3.75 \$



Small shrinking in device dimensions reduces fabrication costs / device drastically



1973
1000 ICs of 1kb
~75'000 €

1977
64 Ics of 16kb
~ 5'000 €

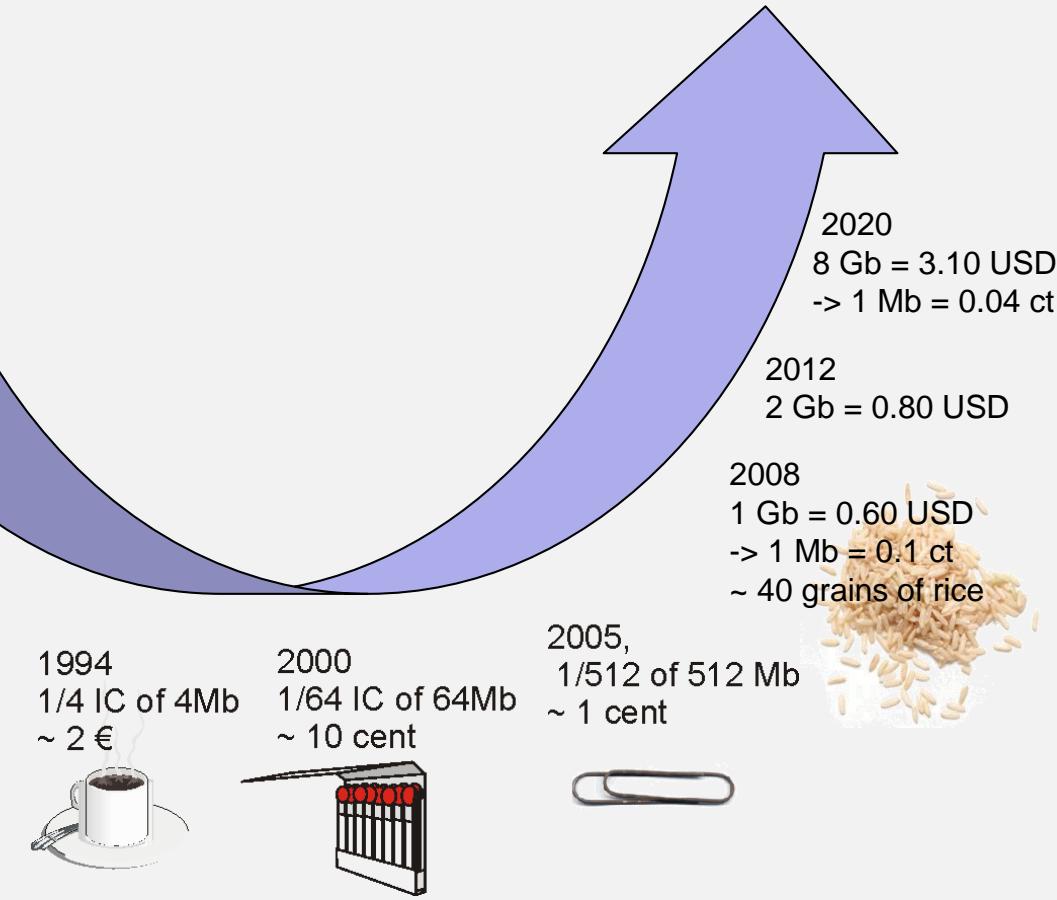
1981
16 ICs of 64kb
~ 400 €

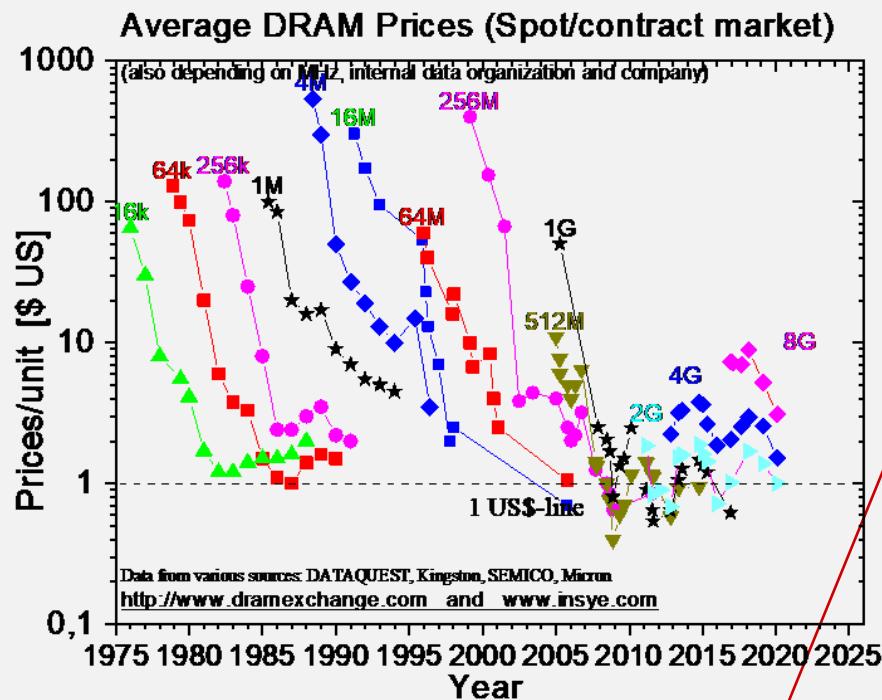
1984
4 ICs oft 256kb
~120 €



1990
1 IC of 1Mb
~ 5 €

The equivalent of 1Mb:



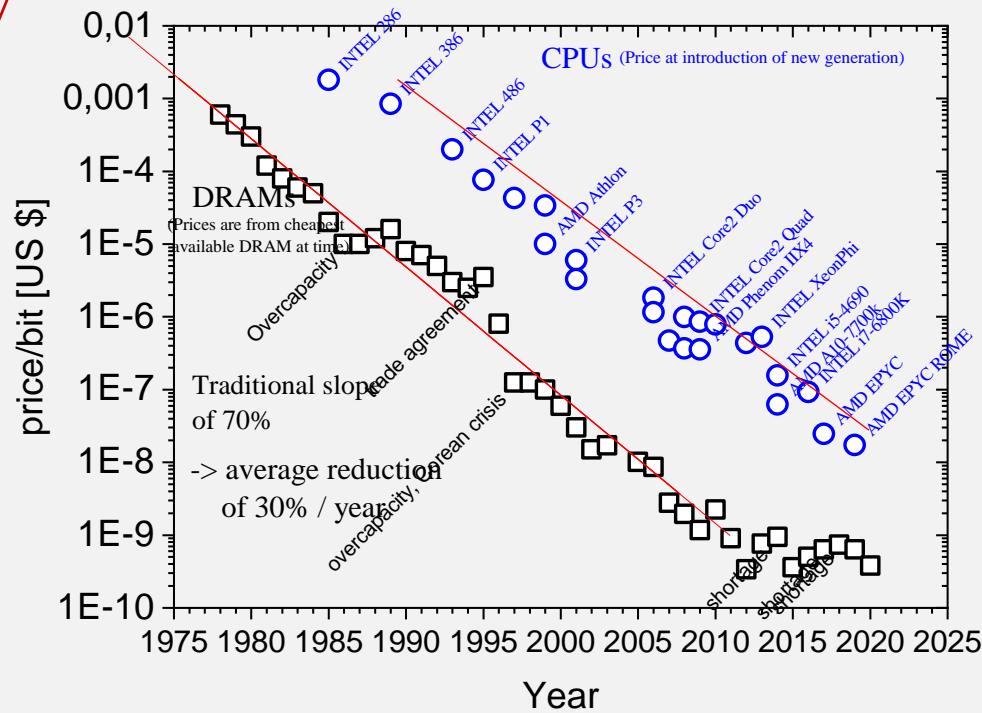


Finally every IC will end around 1 US \$

Fabrication costs are below 1 \$US per chip

(but well kept secret of every company !)

Price reduction of DRAMs creates a dramatical reduction in costs/function of about 30% per year and function



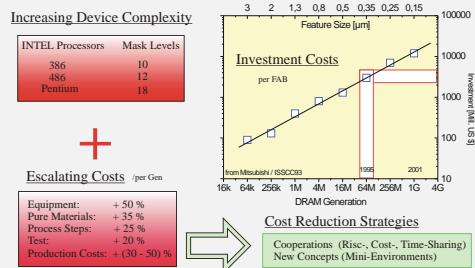
Selling prices decrease about 2 per bit and generation

Shrinking dimensions reduces fabrication costs per function ! drastically

BUT:

How can semiconductor industry survive ?

1

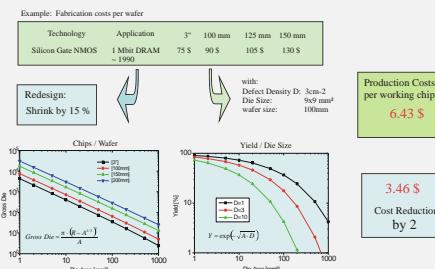


The Calculation of Semiconductor Industry

Fab-costs rise about a factor 1.6 / Generation
(1990: 4 Mb-DRAM: ~1 Billion US \$)

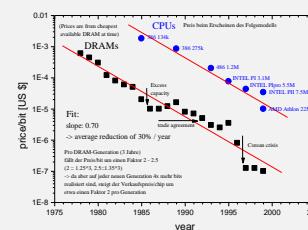
Fabrication costs rise about <1.5 / Generation

2



3

Fabrication costs: 1Mb-DRAM on 6"-wafers: ~130 US \$ / wafer



Calculation:

Equipment costs: FAB (1990) ~ 1Bill. US \$, life cycle about 10 years ~ 3 generations

Fabrication costs: input: 7000 wafer/week * 52 weeks * 10 years * 130 US\$/wafer = 470 Mill. US\$

Cost ratio: fabrication costs/ equipment ~ 1/2

Cost increase / gen. = 2 parts FAB * Factor 1.6 + 1 Part production * Factor 1.4 = 4.6 new parts / 3 old parts = 1.53



income: increased selling price per generation / cost rise per generation = 1.4 / 1.53 ~ 27 %

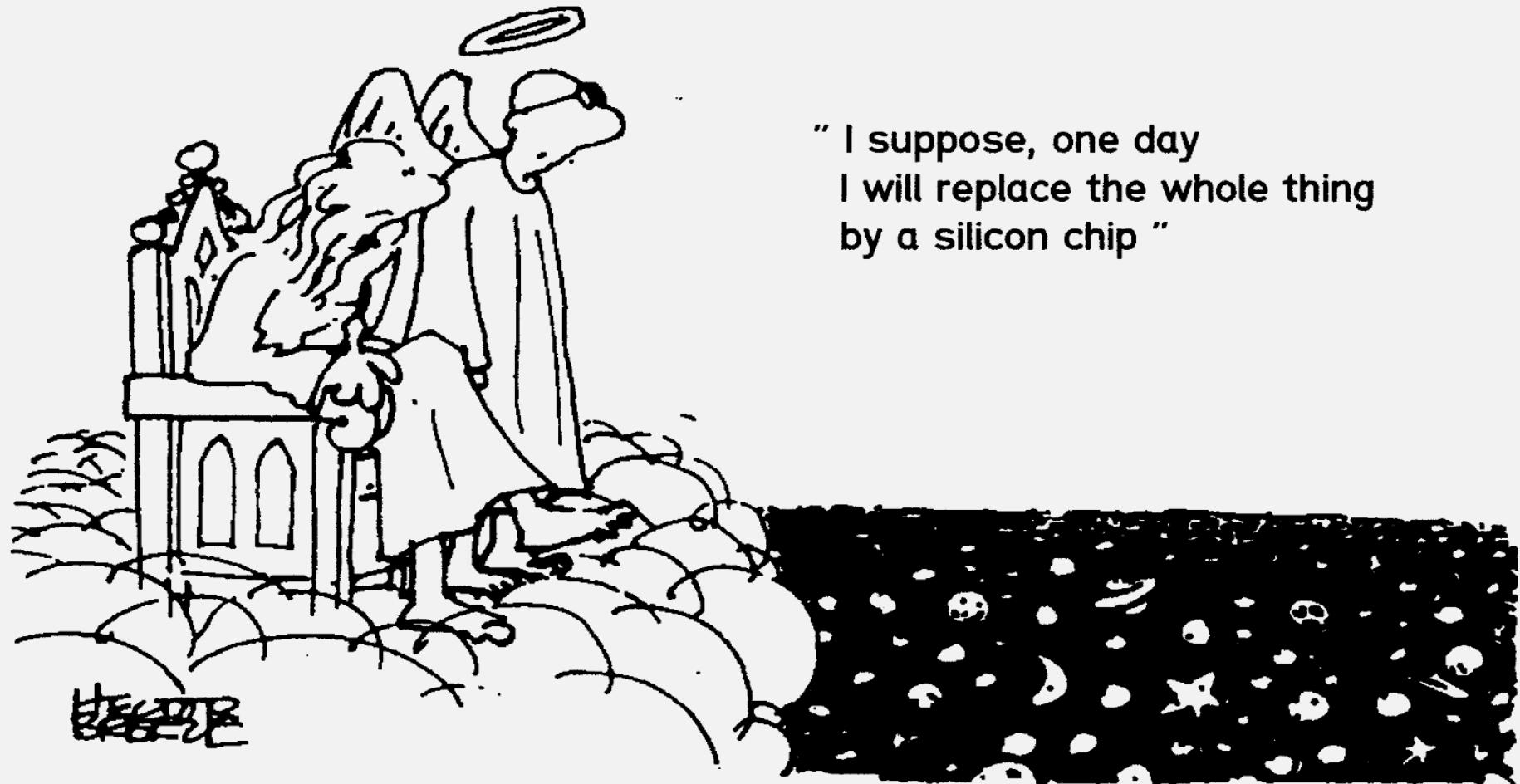
Semiconductor industry is working on a very sensitive, high level content of daily money

Each day 1-4 Mill. US\$ are consumed and earned in each semiconductor Fab

The average income margin of semiconductor industry is small (about 10% per year)

Increasing demand of chips result in a 17% average growth per year of the whole semiconductor industry

Since all calculations depend on power laws, little changes in production or market will result in earning a lot of money or losing a lot of money



“ I suppose, one day
I will replace the whole thing
by a silicon chip ”

2.1 Introduction

2.2 Market demand for highly Integrated Circuits IC

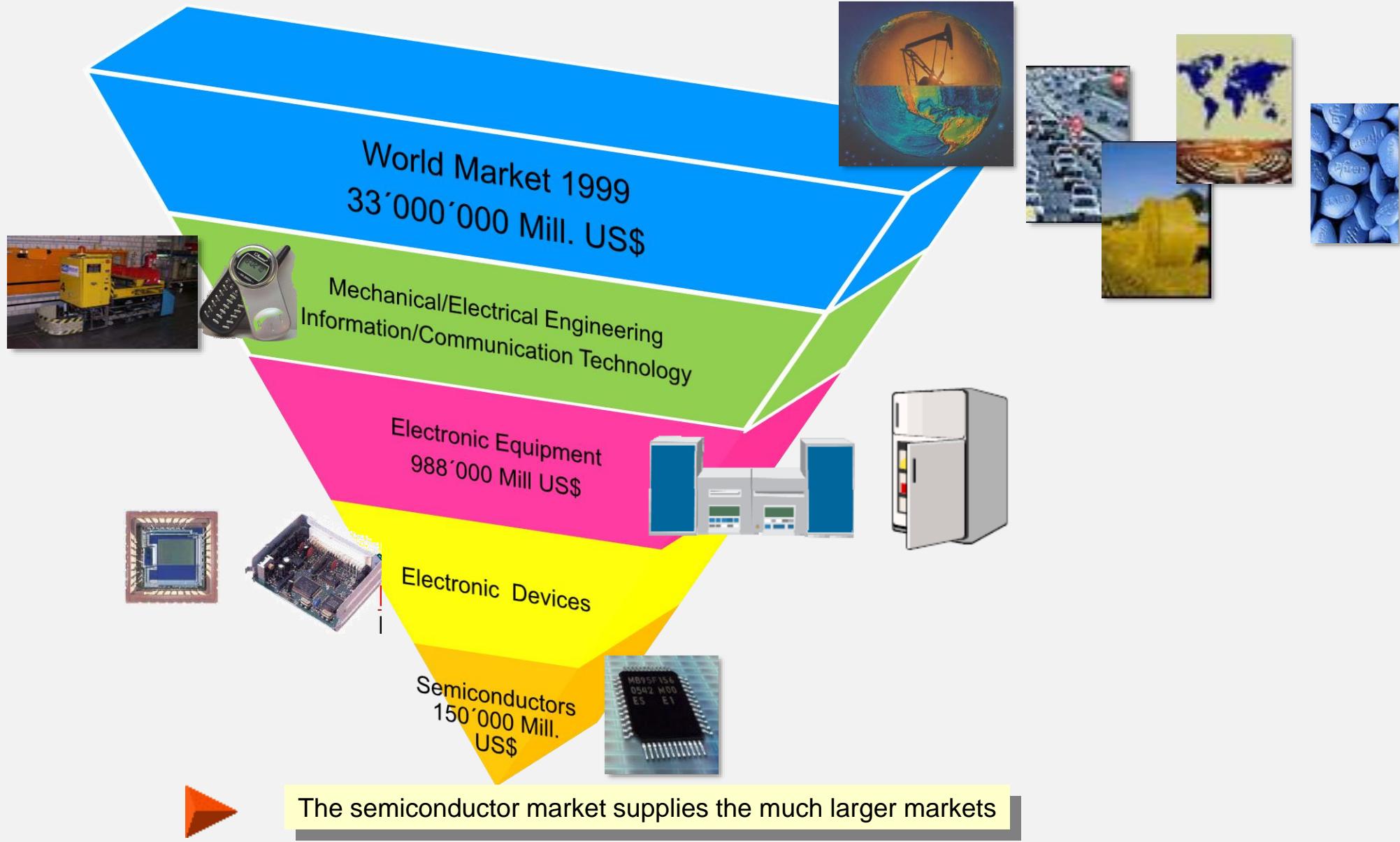
2.3 Shrinking: Making Money

2.4 Shrinking: Spending Money

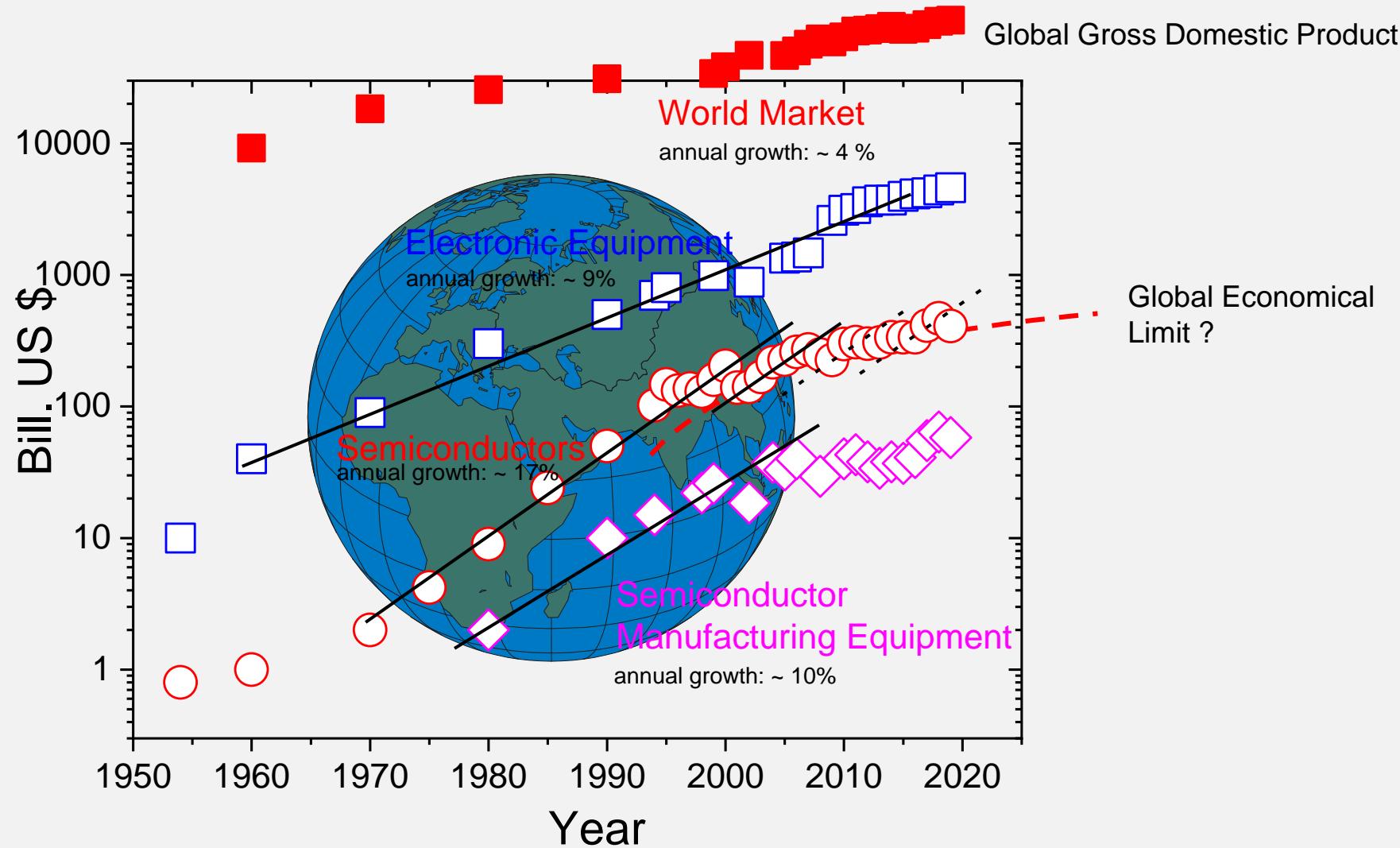
2.5 Calculation of Semiconductor Industry

2.6 Market Information on ICs

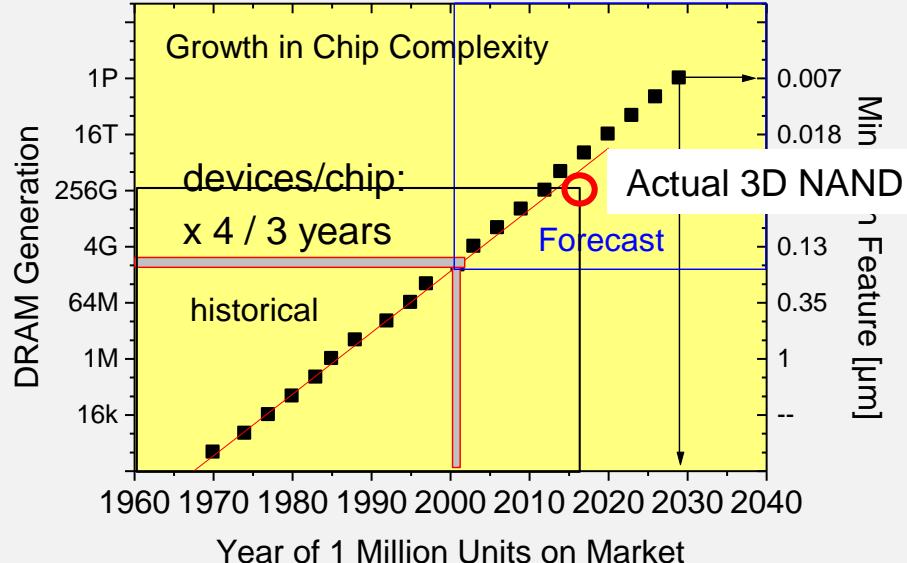
Leverage Effect of Semiconductor Industry



Semiconductor Drives the World Largest Market



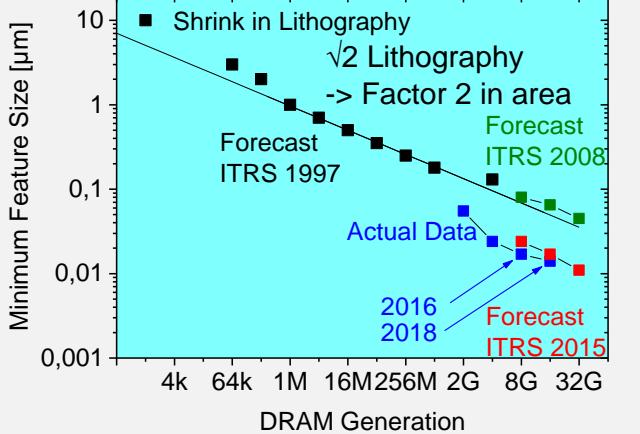
Moore's Law in Detail



For shrinking dimensions a roadmap exists, which is called Moore's Law

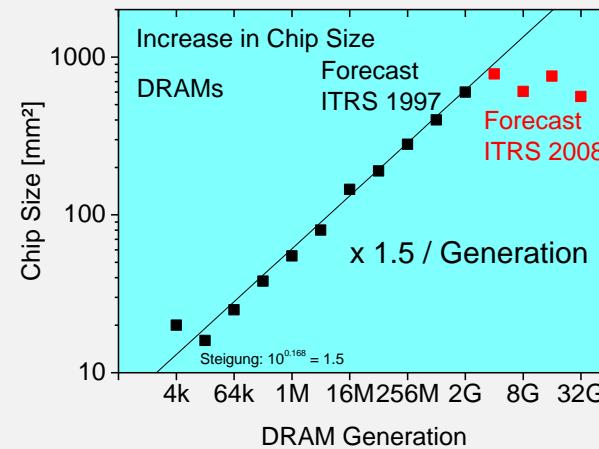
Moore's Law:
the number of devices/chip increases by a factor 4 every 3 years

Moore's law is achieved by:



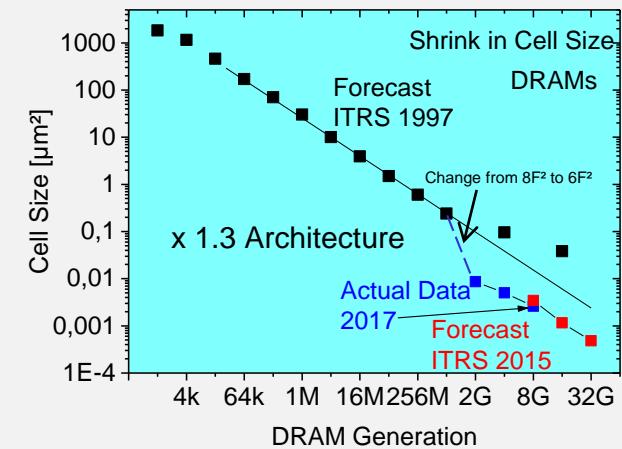
a factor $\sqrt{2}$ in dimension shrink

Saturation proposed



a factor 1.5 in chip size increase

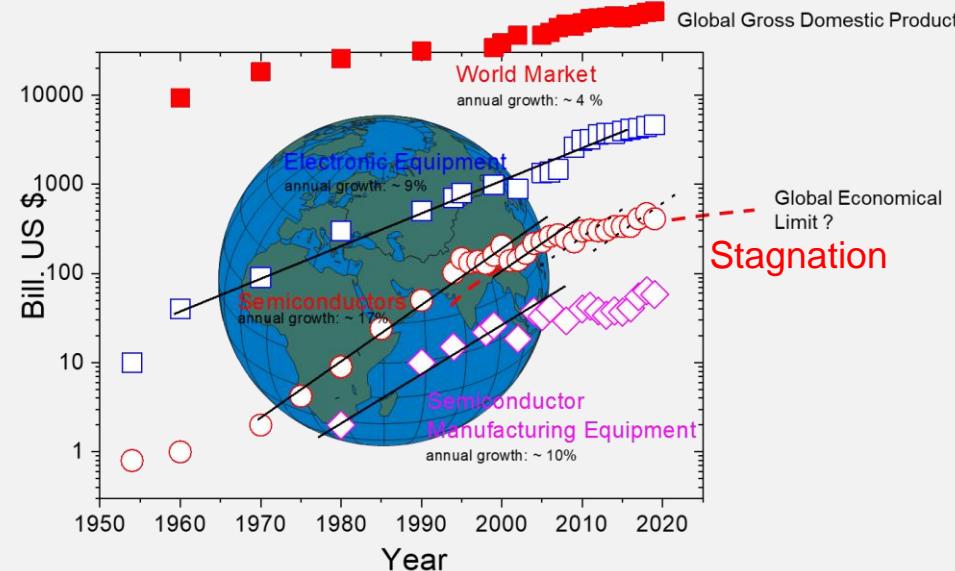
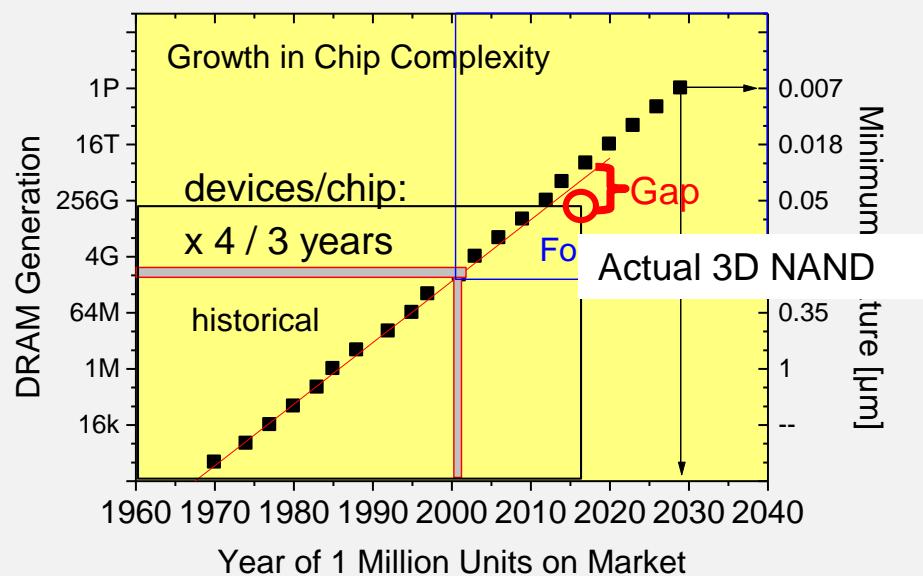
Saturation due to yield aspects



a factor 1.3 in better design

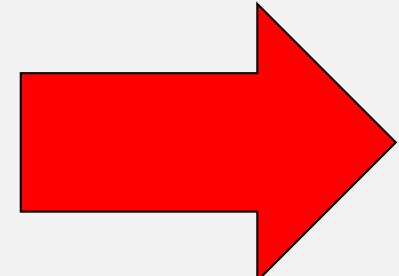
Saturation due to 4F²

Stagnation of Semiconductor Market (2016)



If this gap is true, it shows that Moore's Law, making only technological improvements, cannot be fulfilled. This means that semiconductor industry cannot follow the historical 17% growth per year (stagnation).

Other mechanisms or actions are needed



The semiconductor market is stagnating and also the revenue of the companies. So what are the companies doing?

HARDWARE : REPORT

Intel Drops Tick-Tock Strategy Once and For All – Now Aims at Process, Architecture and Optimization, 3 Year Cadence



By Hassan Mujtaba

81
SHARES

SHARE

TWEET

SUBMIT

Posted Mar 23, 2016

Intel has seemingly dropped their Tick-Tock strategy which is the process of offering a new node (Tick) followed by a new architecture (Tock) during a two year time frame. The Tick-Tock strategy is based on the fundamentals of Moore's Law which was devised by Intel's industry veteran, Gordon Moore, back in 1965 and revolves around the process of a CPU incorporating double the number of transistors in a certain period of time (2 Years).

[News Release](#)

July 28, 2015

Share this Article



Contact Intel PR

INTEL AND MICRON PRODUCE BREAKTHROUGH MEMORY TECHNOLOGY

New Class of Memory Unleashes the Performance of PCs, Data Centers and More

NEWS HIGHLIGHTS

- Intel and Micron begin production on new class of non-volatile memory, creating the first new memory category in more than 25 years.
- New 3D XPoint™ technology brings non-volatile memory speeds up to 1,000 times faster¹ than NAND, the most popular non-volatile memory in the marketplace today.

Intel will fab ARM chips for LG on upcoming 10nm foundry node

By Joel Hruska on August 17, 2016 at 9:10 am | 14 Comments

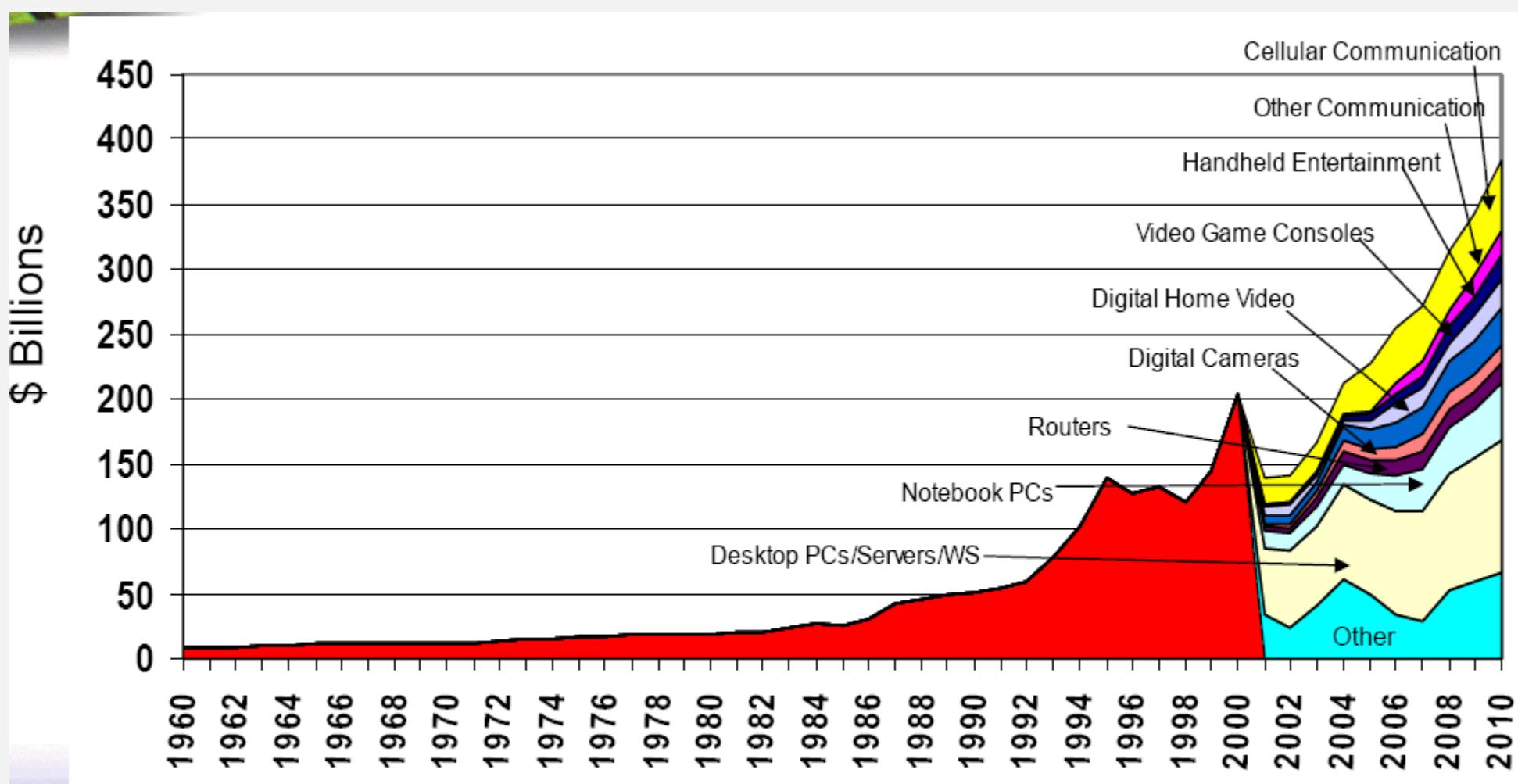
294
shares



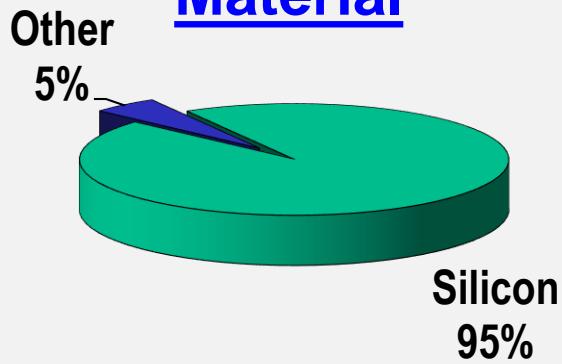
When Intel announced that it was canceling its tablet and smartphone products and effectively exiting the Android-x86 market, it was generally seen as a sign that the company had given up on attempting to compete against low-power ARM products manufactured by Samsung, TSMC, and GlobalFoundries. Now Intel announced that it would begin building 10nm hardware for companies that want to license standard ARM cores.

To achieve growth companies over take smaller companies, open foundries or make new technologies

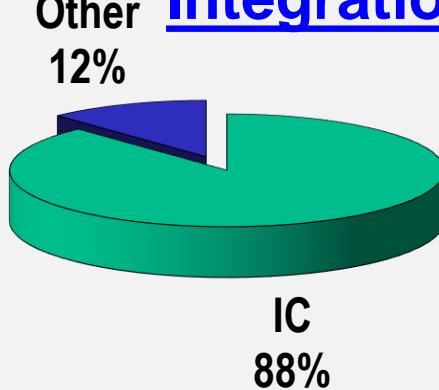
Use of Semiconductor Components



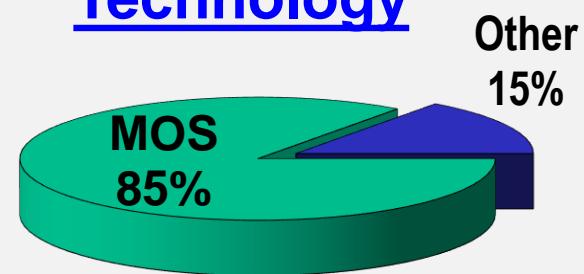
Material



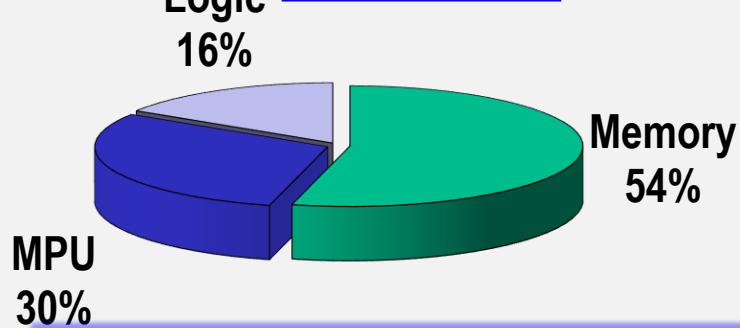
Integration



Technology



Logic MOSFETs



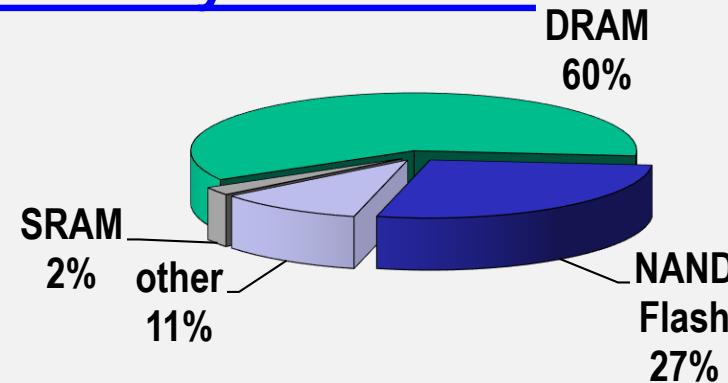
► Silicon is the dominant semiconductor material (95 %)

► 88% of all semiconductors are in ICs

► MOS is the far dominant technology (85%)

► DRAM is still the most important product (~25% of all semiconductor money),
but Flash is speeding up.

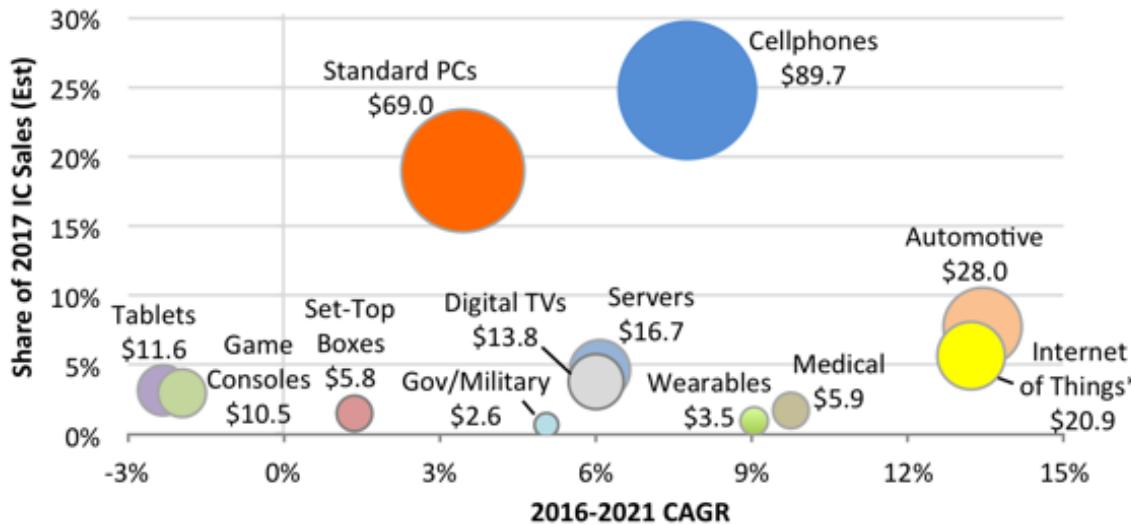
Memory 2009-2017



All values are financial values, not numbers

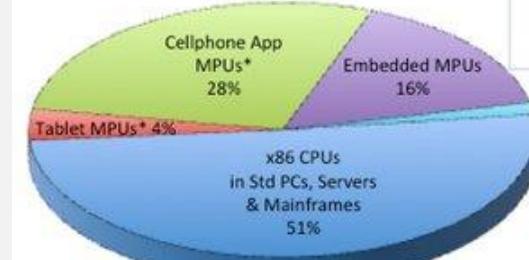
Forecast 2017

IC End-Use Markets (\$B) and Growth Rates



Forecast 2018

2018 MPU Sales by Application (Fcst, \$74.5B)



Embedded Microprocessors = 16%
Network Processors = 3.8%
Computers & Peripherals = 1.8%
Industrial/Medical = 4.1%
Consumer = 2.6%
Automotive = 2.2%
Other = 1.3%

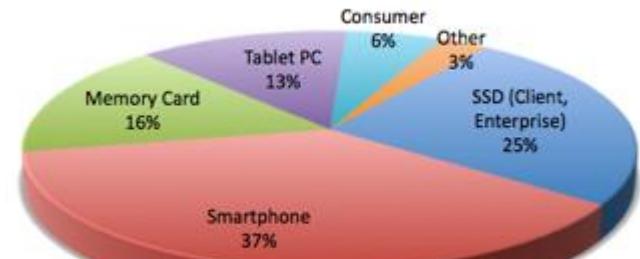
*Includes ARM-based and x86 processors. **Includes ARM-based and other RISC processors.
Source: IC Insights

Status 2017

Smartphone/Automotive market is growing the last years

More and more chips are going to Smartphone/Automotive

2018F NAND Bit Demand Profile



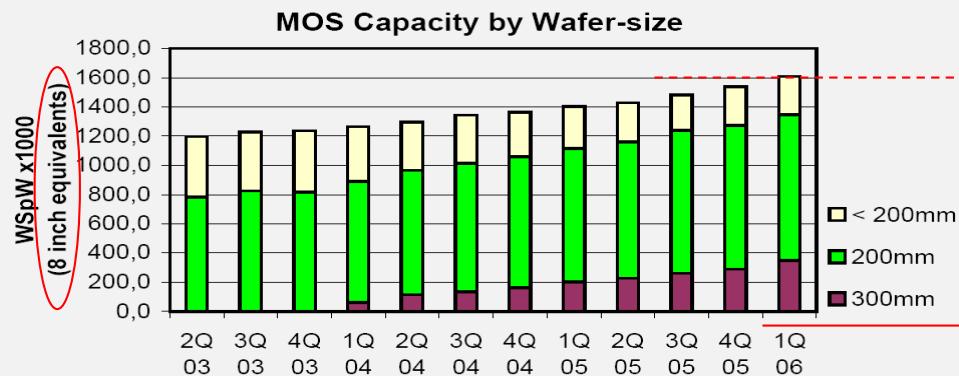
Source: IC Insights

Status 2017

Dr.-Ing. J.Biba
AdMOS, 2-66

Historical Increase of MOS Devices

The following graphs show the capacity of the major SC manufacturers who together represent the majority (~90%) of the world's SC production



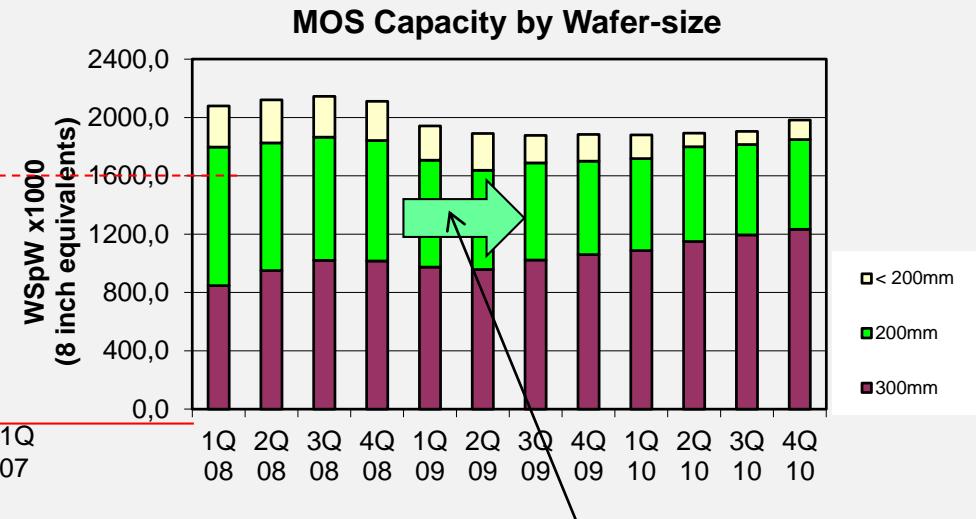
WSpW = Wafer-Starts per Week.

In older Fabs still 6"-wafer (150mm) are manufactured. The majority of Fabs are now working with 300mm-wafers.
For the market the number of fabricated chips is important. Due to historic development the capacity of chips is normalized to the old standard of 200mm-wafers.

Conversion of areas:

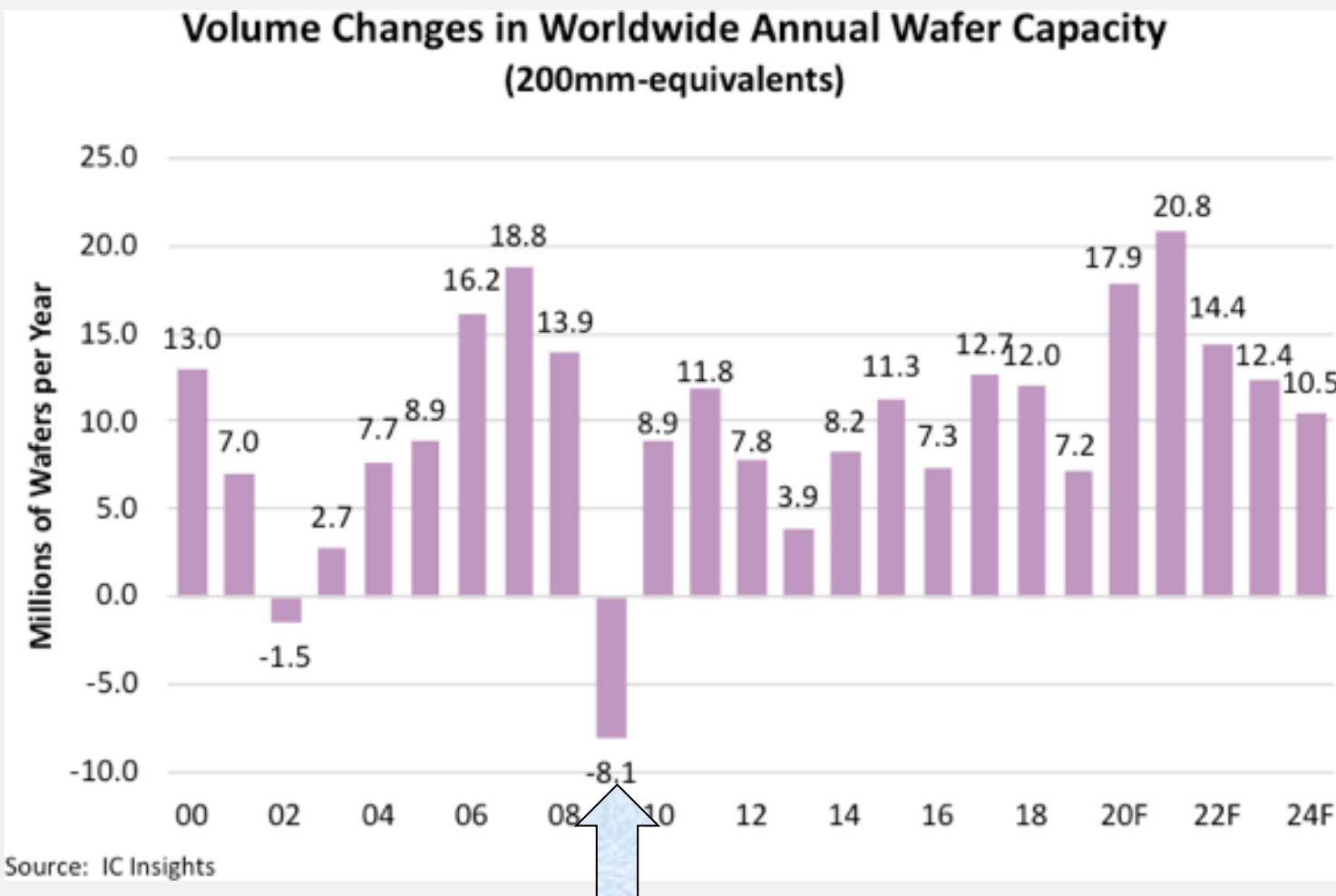
$$150\text{mm} \rightarrow 200\text{mm} = 0.563$$

$$300\text{mm} \rightarrow 200\text{mm} = 2.25$$



With 2009 economic depression Fabs with smaller wafer size (<200mm and 200mm) were closed (bars getting smaller) and 300mm increased

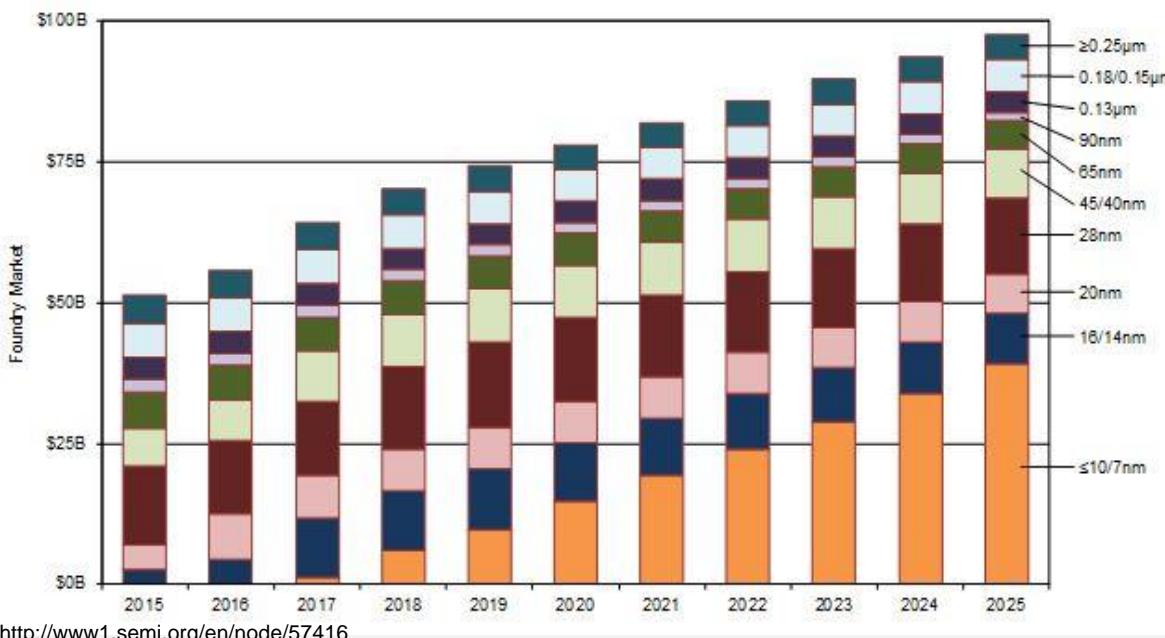
Historical Increase of MOS Devices



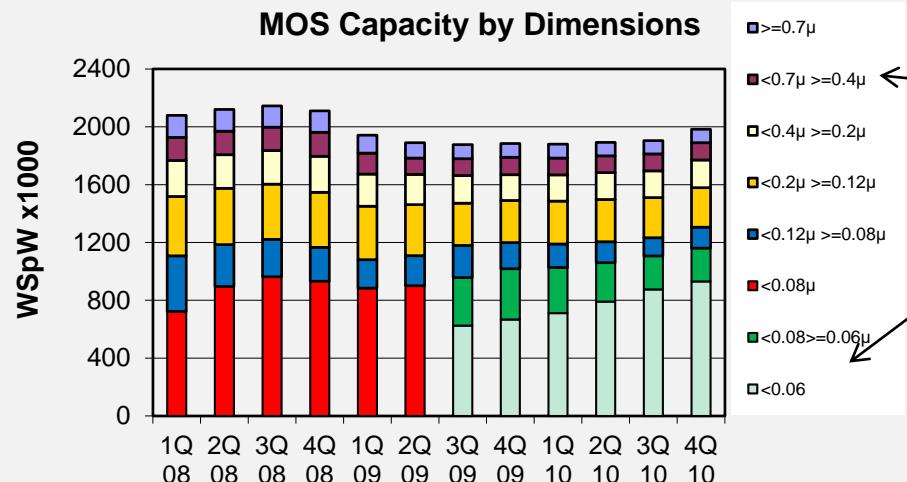
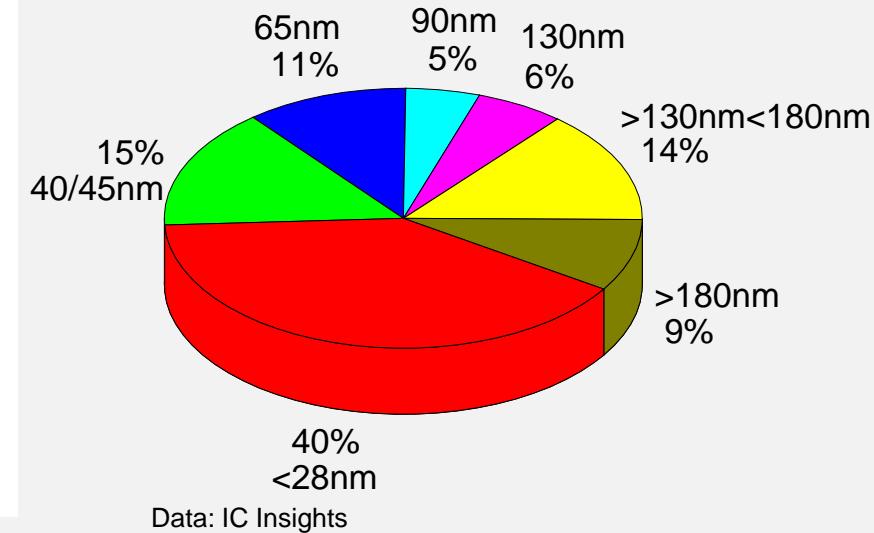
2008 global financial crisis

-> some fabs closed

Historical Increase of MOS Devices

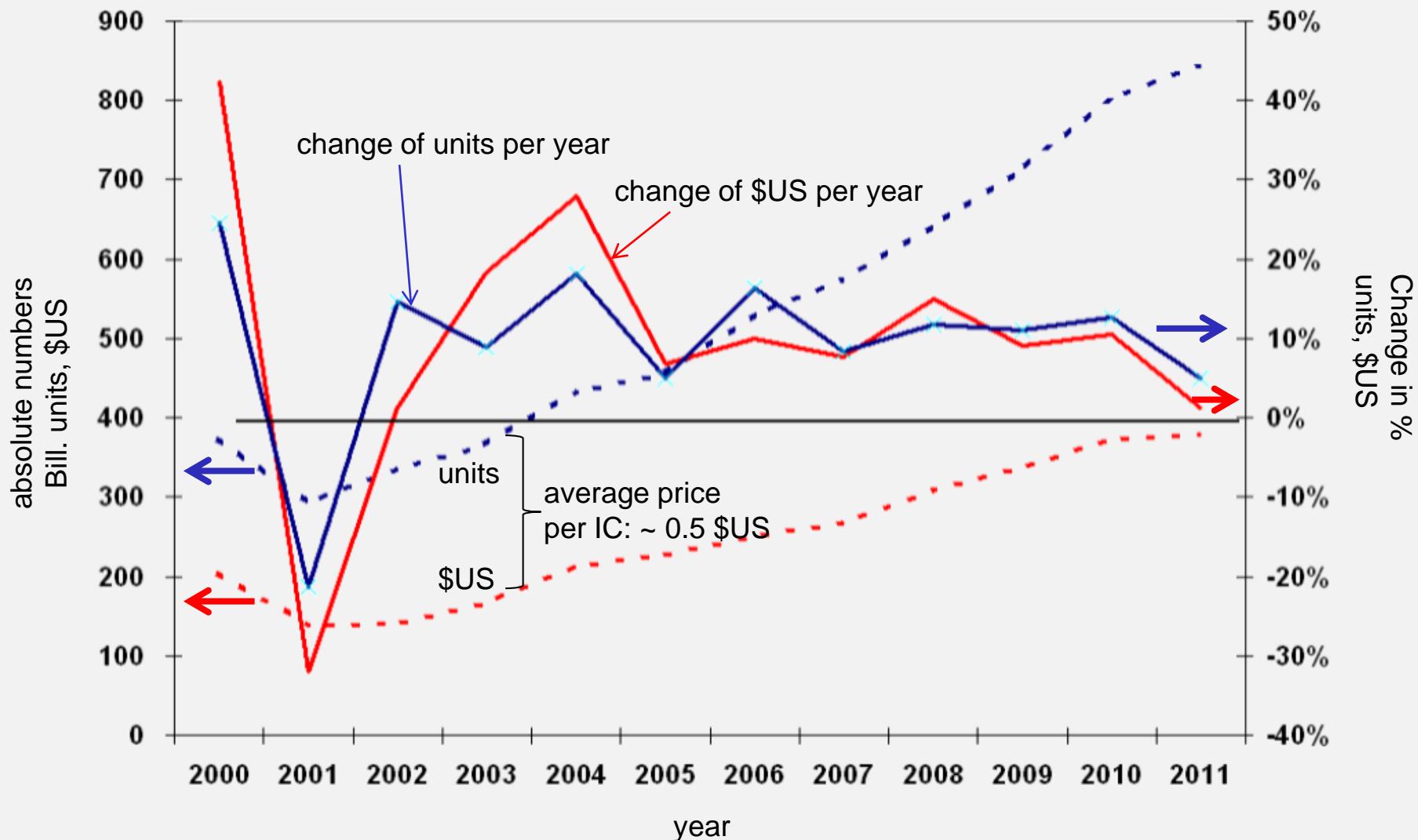


Sales by Feature Size 2016



In older Fabs still large devices are fabricated.

The increase in number of chips is carried by new Fabs: if older Fabs are closed, only a few chips with large technology are canceled, but with new Fabs many more chips due to smaller technology are coming on the market.



The Top Ten of Semiconductor Manufacturer

Rank 2011	Rank 2010	Company	Country of origin	Revenue (million \$ USD)	2011/2010 changes	Market share
1	1	Intel Corporation(1)	USA	49 685	+23.0%	15.9%
2	2	Samsung Electronics	South Korea	29 242	+3.0%	9.3%
3	4	Texas Instruments(2)	USA	14 081	+8.4%	4.5%
4	3	Toshiba Semiconductor	Japan	13 362	+2.7%	4.3%
5	5	Renesas Electronics	Japan	11 153	-6.2%	3.6%
6	9	Qualcomm(3)	USA	10 080	+39.9%	3.2%
7	7	STMicroelectronics	France Italy	9 792	-5.4%	3.1%
8	6	Hynix	South Korea	8 911	-14.2%	2.8%
9	8	Micron Technology	USA	7 344	-17.3%	2.3%
10	10	Broadcom	USA	7 153	+7.0%	2.3%
11	12	Advanced Micro Devices	USA	6 483	+2.2%	2.1%
12	13	Infineon Technologies	Germany	5 403	-14.5%	1.7%
13	14	Sony	Japan	5 153	-1.4%	1.6%
14	16	Freescale Semiconductor	USA	4 465	+2.5%	1.4%
15	11	Elpida Memory	Japan	3 854	-40.2%	1.2%
16	17	NXP	Netherlands	3 838	-4.7%	1.2%
17	20	NVIDIA	USA	3 672	+14.9%	1.2%
18	18	Marvell Technology Group	USA	3 448	-4.4%	1.1%
19	26	ON Semiconductor(4)	USA	3 423	+49.4%	1.1%
20	15	Panasonic Corporation	Japan	3 365	-32.0%	1.1%
Top 20				203 907	3.5%	65.2%
All Other companies				108 882	-1.1%	34.8%
TOTAL				312 789	1.9%	100.0%

Note:

Total Market 2011:
312 Bill. US \$

Top Ten Share: 160 Bill. USD
only ~50 %

the trend of the last years (since 2006) is, that big players try to increase productivity by overtaking smaller or weaker competitors

2019F Top 15 Semiconductor Sales Leaders (\$M, Including Foundries)

2019F Rank	2018 Rank	Company	Headquarters	2018 Total IC	2018 Total O-S-D	2018 Total Semi	2019F Total IC	2019F Total O-S-D	2019F Total Semi	2019/2018 % Change
1	2	Intel	U.S.	69,880	0	69,880	69,832	0	69,832	0%
2	1	Samsung	South Korea	75,698	2,843	78,541	51,750	3,860	55,610	-29%
3	4	TSMC (1)	Taiwan	34,208	0	34,208	34,503	0	34,503	1%
4	3	SK Hynix	South Korea	36,200	567	36,767	22,291	595	22,886	-38%
5	5	Micron	U.S.	30,930	0	30,930	19,960	0	19,960	-35%
6	6	Broadcom Inc. (2)	U.S.	16,454	1,735	18,189	15,917	1,789	17,706	-3%
7	7	Qualcomm (2)	U.S.	16,385	0	16,385	14,300	0	14,300	-13%
8	8	TI	U.S.	13,908	946	14,854	12,705	842	13,547	-9%
9	9	Toshiba/Kioxia (3)	Japan	12,293	1,508	13,801	9,839	1,437	11,276	-18%
10	10	Nvidia (2)	U.S.	11,951	0	11,951	10,514	0	10,514	-12%
11	15	Sony	Japan	627	7,088	7,715	878	8,674	9,552	24%
12	11	ST	Europe	6,628	2,991	9,619	7,241	2,215	9,456	-2%
13	13	Infineon	Europe	5,465	3,745	9,210	5,366	3,580	8,946	-3%
14	12	NXP	Europe	8,429	978	9,407	7,969	888	8,857	-6%
15	14	MediaTek (2)	Taiwan	7,891	0	7,891	7,948	0	7,948	1%
--- Top-15 Total				346,947	22,401	369,348	291,013	23,880	314,893	-15%

(1) Foundry (2) Fabless (3) Formerly Toshiba Memory

Source: Company reports, IC Insights' Strategic Reviews database

	Market Value 2019 [billion \$]	Revenue 2019 [billion \$]
Facebook	567	71
Alphabet	842	155
Intel	273	72
Samsung	326	230

The Top Ten of Semiconductor Manufacturers

Semiconductor Sales Leaders

Rank	1990	1995	2000	2006	2014	2015F
1	NEC	4.8	Intel	13.6	Intel	29.7
2	Toshiba	4.8	NEC	12.2	Toshiba	11.0
3	Hitachi	3.9	Toshiba	10.6	NEC	10.9
4	Intel	3.7	Hitachi	9.8	Samsung	10.6
5	Motorola	3.0	Motorola	8.6	TI	9.6
6	Fujitsu	2.8	Samsung	8.4	Motorola	7.9
7	Mitsubishi	2.6	TI	7.9	ST	7.9
8	TI	2.5	IBM	5.7	Hitachi	7.4
9	Philips	1.9	Mitsubishi	5.1	Infinion	6.8
10	Matsushita	1.8	Hyundai	4.4	Philips	6.3
Top 10 Total (\$B)		31.8	86.3	108.1	118.2	187.7
Semi Market (\$B)		54.3	154	218.6	265.5	354.8
Top 10 % of Total Semi		59%	56%	49%	45%	53%

Source: IC Insights

*Not including foundries

**Fabless

Rank	Company	Sales (\$B)	2016			2017			2018			2019F		
			Company	Sales (\$B)	Change	Company	Sales (\$B)	Change	Company	Sales (\$B)	Change	Company	Sales (\$B)	Change
1	Intel	\$57.0	Samsung	\$65.9	48.8%	Samsung	\$78.5	19.2%	Intel	\$70.6	1.0%			
2	Samsung	\$44.3	Intel	\$61.7	8.2%	Intel	\$69.9	13.2%	Samsung	\$63.1	-19.7%			
3	TSMC (2)	\$29.5	TSMC (2)	\$32.2	9.1%	SK Hynix	\$36.8	37.6%						
4	Qualcomm (1)	\$15.4	SK Hynix	\$26.7	79.5%	TSMC (2)	\$34.2	6.4%						
5	Broadcom (1)	\$15.2	Micron	\$23.9	76.7%	Micron	\$31.0	29.6%						
6	SK Hynix	\$14.9	Broadcom (1)	\$17.8	16.9%	Broadcom (1)	\$18.5	3.7%						
7	Micron	\$13.5	Qualcomm (1)	\$17.0	10.5%	Qualcomm (1)	\$16.4	-3.8%						
8	TI	\$12.5	TI	\$13.9	11.3%	Toshiba*	\$14.9	12.1%						
9	Toshiba	\$10.9	Toshiba	\$13.3	21.9%	TI	\$14.9	6.8%						
10	NXP	\$9.5	Nvidia (1)	\$9.4	36.1%	Nvidia (1)	\$12.0	27.1%						
Top 10 Total (\$B)		\$222.8	—	\$281.9	26.5%	—	\$327.0	16.0%						
Semi Market (\$B)		\$364.0	—	\$445.2	22.3%	—	\$504.1	13.2%	—	\$468.9	-7.0%			

Source: IC Insights (1) Fabless (2) Pure-Play foundry

*Includes Toshiba Memory

Fabless

2017E Top 10 Fabless/System IC Companies (\$M)

2017E Rank	Company	Headquarters	2016 Tot IC	2017E Tot IC	2017/2016 % Change
1	Qualcomm	U.S.	15,414	17,078	11%
2	Broadcom Ltd.	Singapore	13,846	16,065	16%
3	Nvidia	U.S.	6,389	9,228	44%
4	MediaTek	Taiwan	8,809	7,875	-11%
5	Apple*	U.S.	6,493	6,660	3%
6	AMD	U.S.	4,272	5,249	23%
7	HiSilicon	China	3,910	4,715	21%
8	Xilinx	U.S.	2,311	2,475	7%
9	Marvell	U.S.	2,407	2,390	-1%
10	Unigroup**	China	1,880	2,050	9%
Top 10 Total		—	65,731	73,785	12%
Other		—	24,694	26,825	9%
Total Fabless/System		—	90,425	100,610	11%

*Custom ICs provided by foundries for internal use.

**Includes Spreadtrum and RDA

Source: Company reports, IC Insights' Strategic Reviews database

Foundries

Major 2017 Foundries (Pure-Play and IDM)

2017 Rank	2016 Rank	Company	Foundry Type	Location	2015 Sales (\$M)	2016 Sales (\$M)	2016/2015 Change (%)	2017 Sales (\$M)	2017/2016 Change (%)
1	1	TSMC	Pure-Play	Taiwan	26,574	29,488	11%	32,163	9%
2	2	GlobalFoundries	Pure-Play	U.S.	5,019	5,495	9%	6,060	10%
3	3	UMC	Pure-Play	Taiwan	4,464	4,582	3%	4,898	7%
4	4	Samsung	IDM	South Korea	2,670	4,410	65%	4,600	4%
5	5	SMIC	Pure-Play	China	2,236	2,914	30%	3,101	6%
6	6	Powerchip	Pure-Play	Taiwan	1,268	1,275	1%	1,498	17%
7	8	Huahong Group*	Pure-Play	China	971	1,184	22%	1,395	18%
8	7	TowerJazz	Pure-Play	Israel	961	1,250	30%	1,388	11%
Top 8 Total		—	—	—	44,163	50,598	15%	55,103	9%
Top 8 Share		—	—	—	87%	88%	—	88%	—
Other Foundry		—	—	—	6,597	7,112	8%	7,207	1%
Total Foundry		—	—	—	50,760	57,710	14%	62,310	8%

*Includes Huahong Grace and Shanghai Huali.

Source: IC Insights, company reports

There is INTEL - and the Others



NEC Electronics Joins Fishkill Alliance

NEC Electronics has joined the IBM-led Fishkill Alliance, with a goal of implementing NEC's automotive microcontrollers and other products on the high-k/metal gate process at 32 nm design rules.

David Lammers, News Editor -- Semiconductor International,
9/11/2008

Demonstrating continued momentum for its partnership model, IBM Corp. (Armonk, N.Y.) announced that NEC Electronics (Tokyo) has joined the Fishkill Alliance, with a mutual goal of implementing the 32 nm high-k/metal gate process on NEC's chip-level products. NEC becomes the eighth company to participate in the bulk CMOS development alliance, which includes Chartered Semiconductor Manufacturing Ltd. (Singapore), Freescale Semiconductor Inc. (Austin, Texas), Infineon Technologies AG (Neubiberg, Germany), Samsung Electronics Co. (Seoul, South Korea), STMicroelectronics NV (Geneva) and Toshiba Corp. (Tokyo).

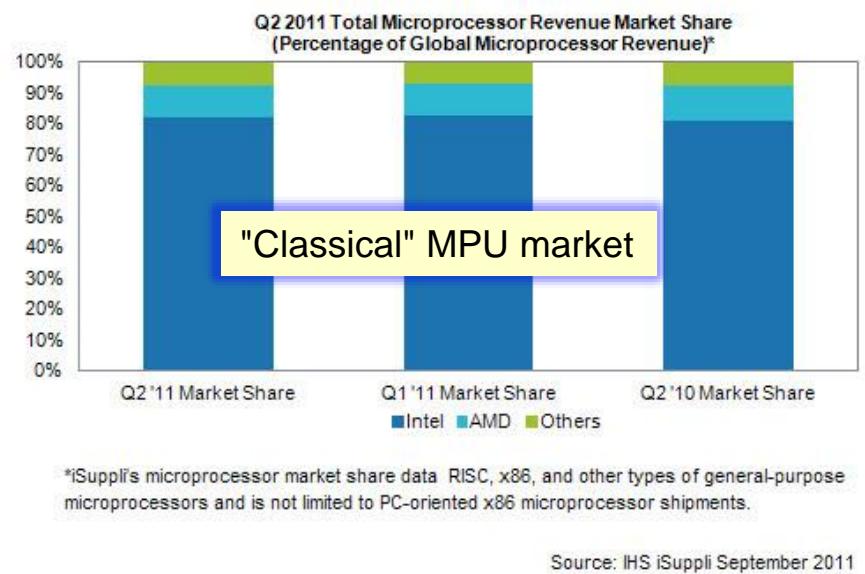
Gary Patton, vice president of the IBM Semiconductor Research & Development Center, said the alliance is focused on the 32 nm generation, where high-k/metal gate technology will provide an advantage over foundries such as Taiwan Semiconductor Manufacturing Co. Ltd. (TSMC, Hsinchu, Taiwan). "Spurred by the success we've had in the high-k program, NEC wanted to get involved directly, as well as in the early research work in Albany," he said. "If you look at adoption of the new technology, the rate of people moving into 45 has slowed down. Design teams are challenged to keep on a two-year cycle. There are a number of customers skipping the 45/40 node and going straight to 32 nm to get the big density improvement and power/performance advantage of high-k/metal gate."

NEC and IBM engineers are beginning discussions this week about how the low-power and general-purpose bulk 32 nm processes will align with NEC's product strategy, which includes automotive-use microcontrollers and other system-on-a-chip (SoC) products.

NEC Electronics will move IP to the Fishkill multi-project wafer (MPW) shuttle to test out 32 nm designs. Patton said the alliance's goal is to have the low-power version of the 32 nm process in early production by the fourth quarter of 2009, with the general-purpose version coming in the first quarter of 2010.

Also, the two companies agreed that NEC will participate in the IBM-led research alliance, which is focused on 22 nm and beyond technologies, including extreme ultraviolet (EUV) lithography, 3-D interconnects, and other topics. The research alliance conducts much of its work at the College of Nanoscale Science and Engineering (CNSE) of the University at Albany, with additional research based at IBM's Watson Research Lab (Yorktown, N.Y.) and the IBM Almaden lab (San Jose).

Any alliance partner has the option of taking its designs to the foundry partners within the Common Platform, including Chartered and the foundry operations of IBM and Samsung. The Common Platform will hold a technology event Sept. 30 in Santa Clara, Calif., where Patton said the focus will be on "32 nm technology and what it buys customers in terms of yields, performance and design ease. We also will be talking about what is coming down the pike for 15 nm and 22 nm."

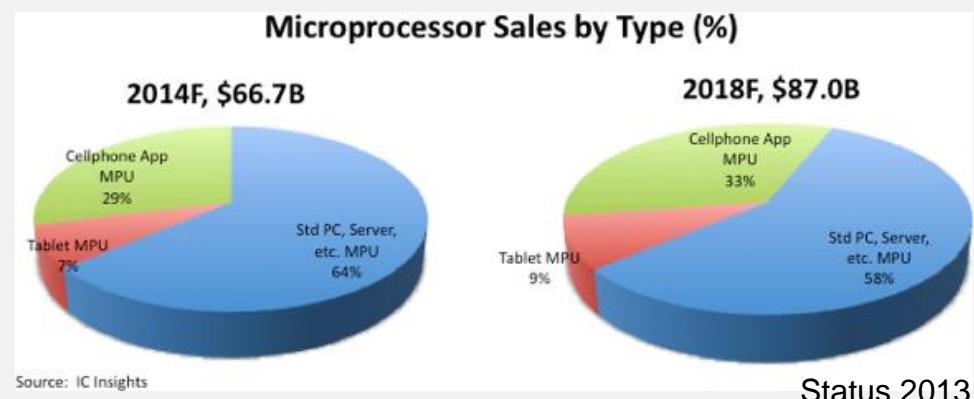
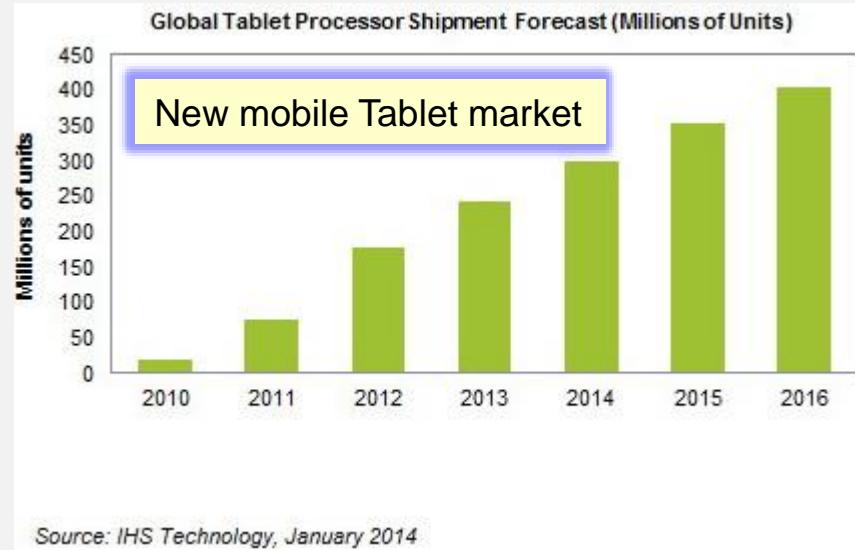


The classical MPU market (for PC) is carried by 2 players:
Intel ~ 80 % and AMD ~ 15%

Some special MPUs (e.g. IBM) are playing a tiny economical part



but since ~ 2012 the classical MPU market is replaced by the mobile MPU market (tablets, smartphones, ...)
-> new players arise

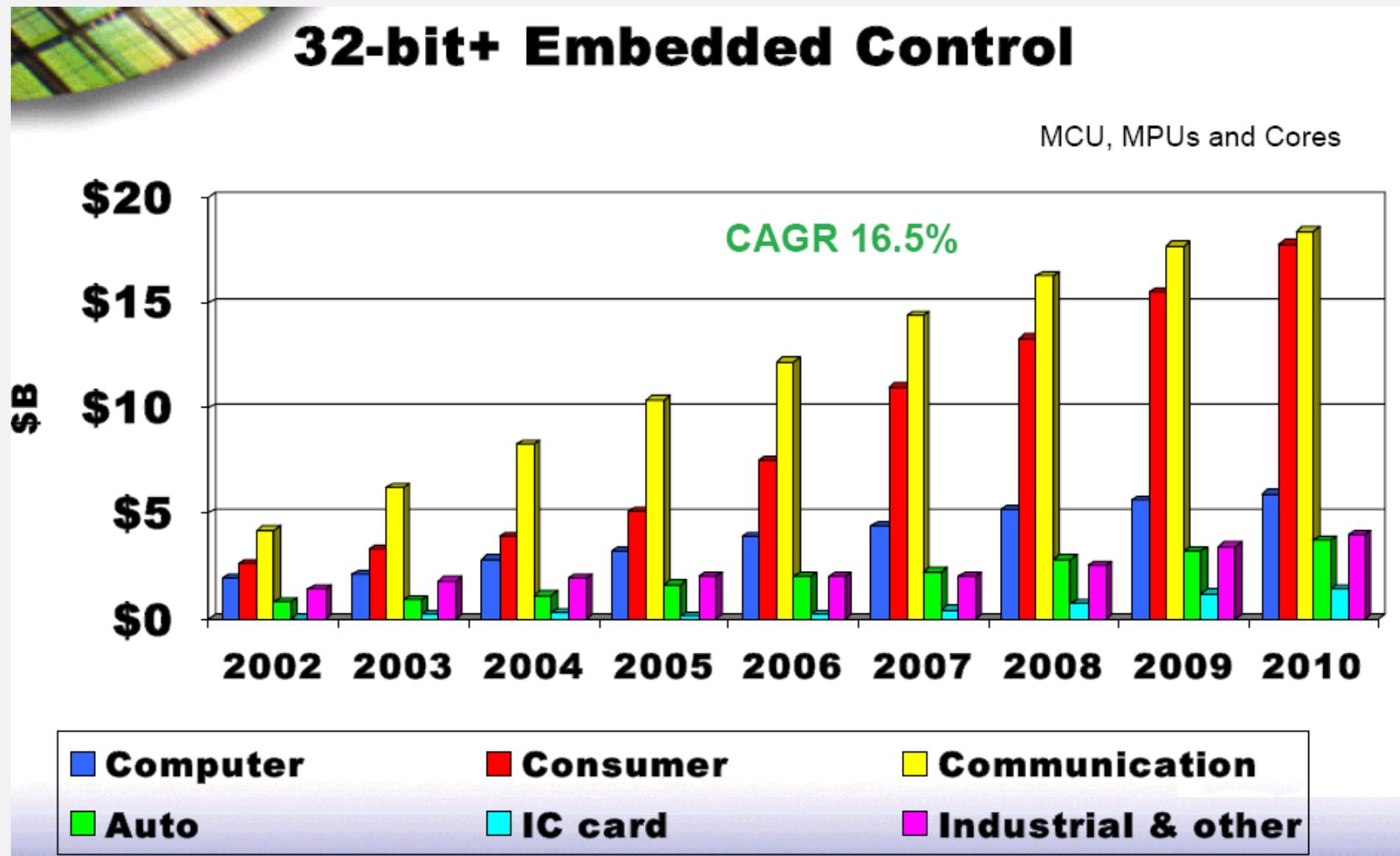


The screenshot shows the ARM website's 'big.LITTLE Technology' page. The header includes the ARM logo, navigation links for Products, Support, Community, Markets, About, and Careers, and a search bar. The main content features a large image illustrating the big.LITTLE architecture with two CPU cores: a 'BIG CPU' and a 'LITTLE CPU'. The BIG CPU is associated with 'HD GAMING', while the LITTLE CPU handles tasks like 'CAMERA', 'MAPS DIRECTIONS', and 'NEWS APP'. Below this, a section titled 'DELIVER AN IMPROVED USER EXPERIENCE AT HIGHER LEVELS OF POWER EFFICIENCY' is presented. A detailed text explains the technology's benefits, mentioning power optimization, performance, and battery life. To the right, there's a graphic showing the 'big.LITTLE' logo, which consists of two overlapping circles labeled 'big' and 'LITTLE'.

Entry Market: low cost MPUs from mainly China
(Allwinner, Amlogic, Mediatek or Rockchip)

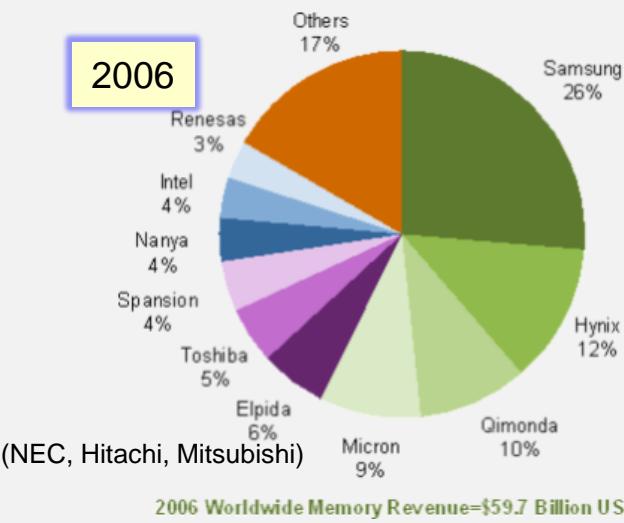
High-End market: Samsung, Qualcomm,..
Intel is fighting with their MPUs called
Bay Trail, Cherry Trail and Willow Trail

Processor design: ARM is designing processors with integrated grafic unit (GPU) with SoC with extreme low power and giving licences to basically all players (Apple, Samsung, Qualcomm, ...)

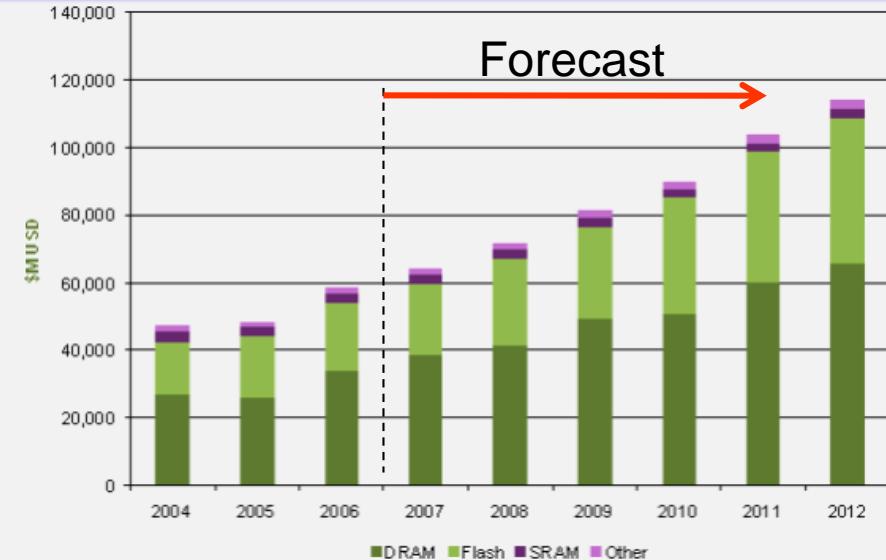


Communication and Consumer are the top key markets for logic ICs (MPU, MCU)

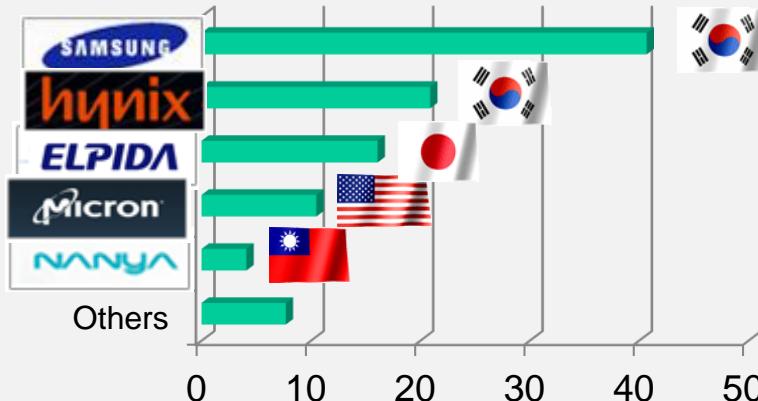
Worldwide Memory Supplier Market Share



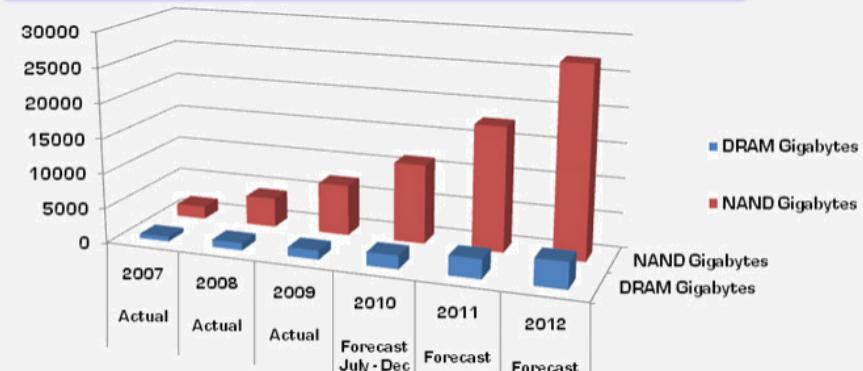
Worldwide Memory Revenue Forecast by Product Category



2010 Acquisition cleans the market

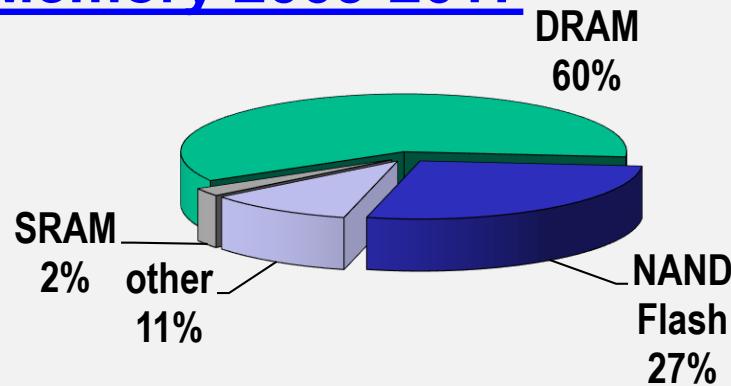


Worldwide Memory Shipments in GBytes

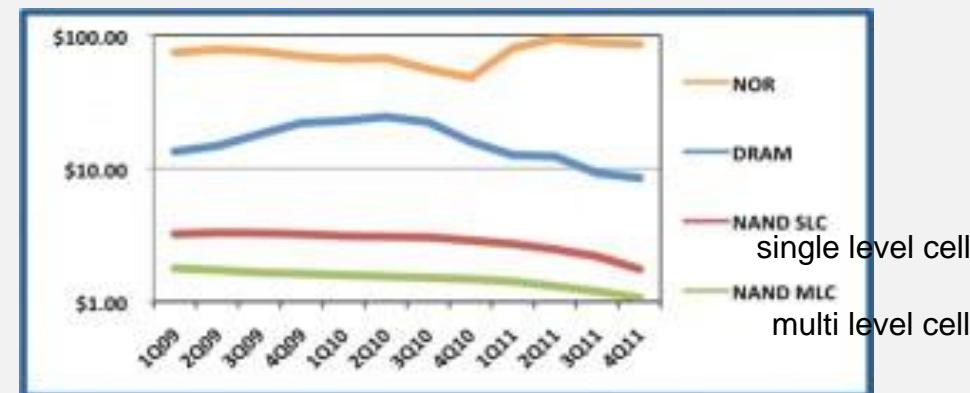


Far-East (Korea, Japan, Taiwan) dominates the Memory-Market with ~ 90% share

Memory 2009-2017

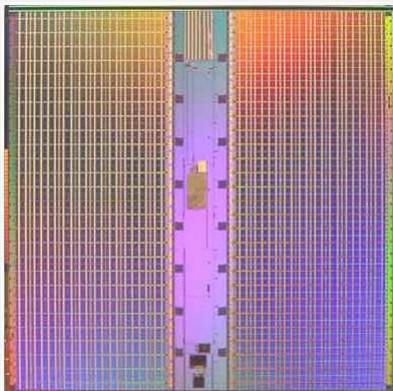


Costs per GByte

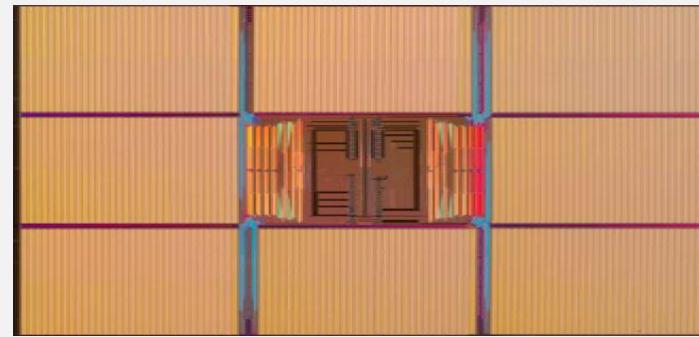


<http://www.reram-forum.com/2012/07/10/are-we-there-yet-is-new-memory-costbit-equal-to-dram-yet/>

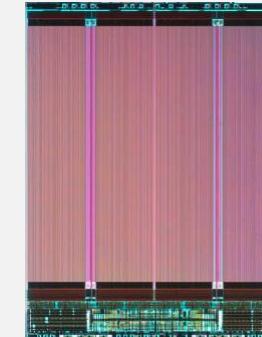
source: convergent semiconductors



70 Mb SRAM, INTEL

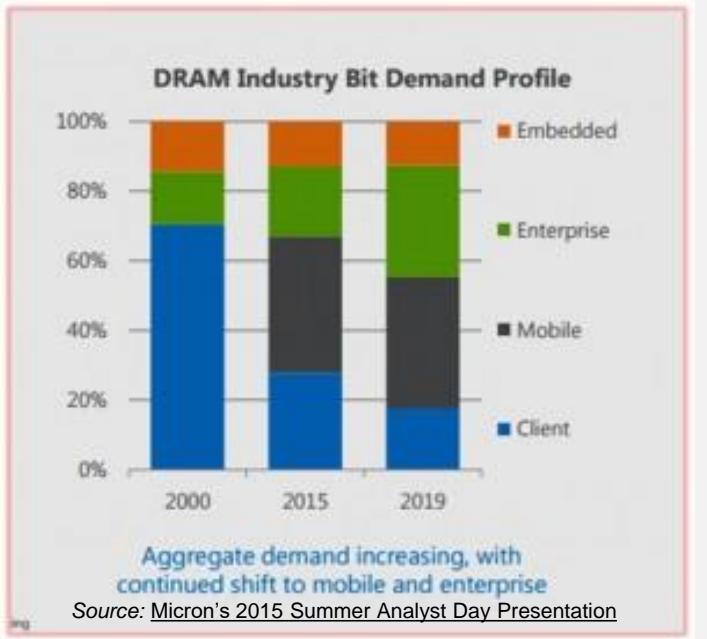


2 Gb DRAM, SAMSUNG



8 Gb NAND, SAMSUNG

Slicing-up the Semiconductor Market (DRAM)



2017

Table: 3Q17 Global Revenue Ranking of Branded DRAM Manufacturers (Unit: USD Million)

Ranking	Company	Revenue			Market Share	
		3Q17	2Q17	QoQ	3Q17	2Q17
1	Samsung	8,790	7,633	15.2%	45.8%	46.2%
2	SK Hynix	5,514	4,501	22.5%	28.7%	27.3%
3	Micron Group	4,023	3,559	13.0%	21.0%	21.6%
4	Nanya	439	417	5.3%	2.3%	2.5%
5	Winbond	177	163	8.7%	0.9%	1.0%
6	Powerchip	103	107	-3.6%	0.5%	0.6%
	Others	135	133	1.2%	0.7%	0.8%
	Total	19,181	16,514	16.2%	100.0%	100.0%

Note 1: 2Q17 USD\$1:KRW\$1,130; USD\$1:TWD\$30.25

Note 2: 3Q17 USD\$1:KRW\$1,131; USD\$1:TWD\$30.25

Source: DRAMeXchange, Nov., 2017

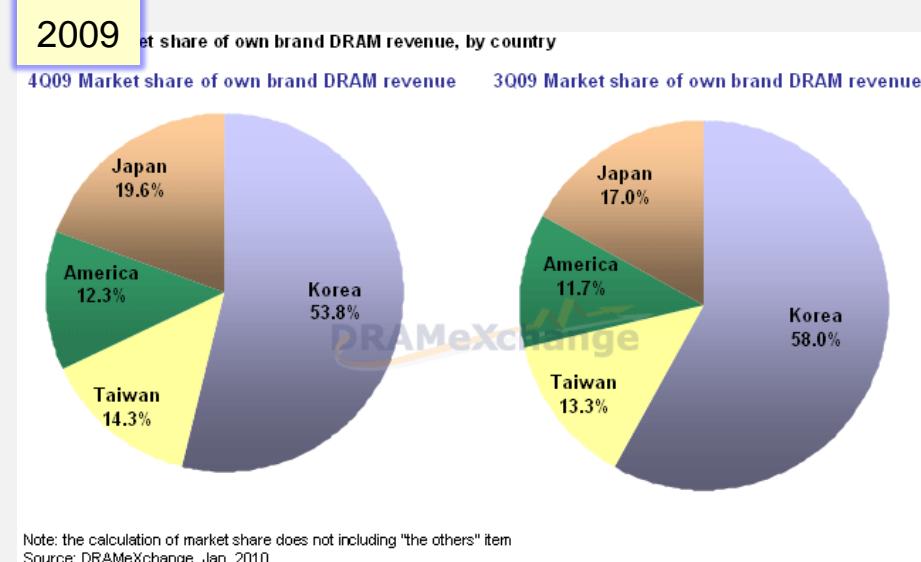


Figure: Branded DRAM Market Share by Region

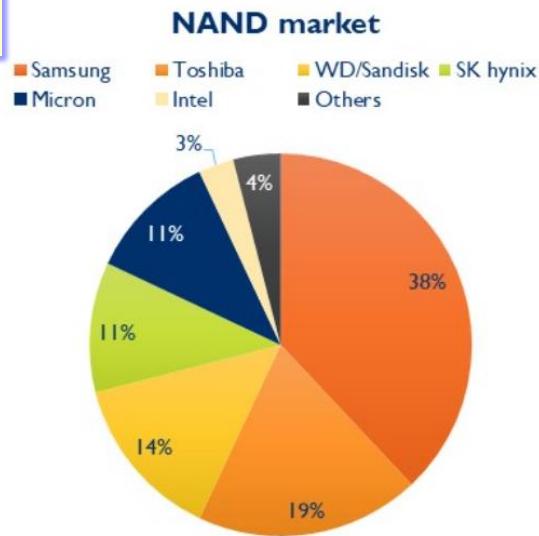


Note: Market share calculation does not include "Others" category.

Source: DRAMeXchange, Nov., 2017

Worldwide NAND Supplier Market Share

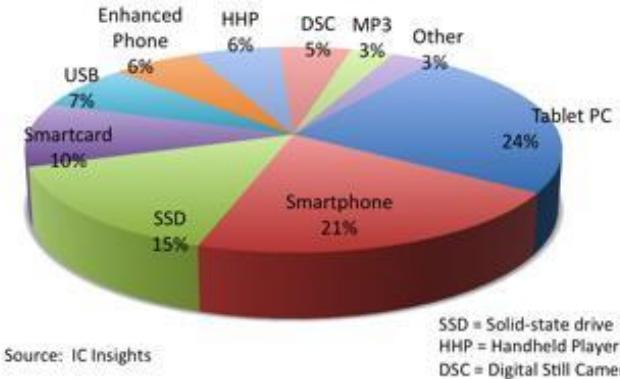
2018



Source: Yole Développement.

NAND Applications Forecast 2015

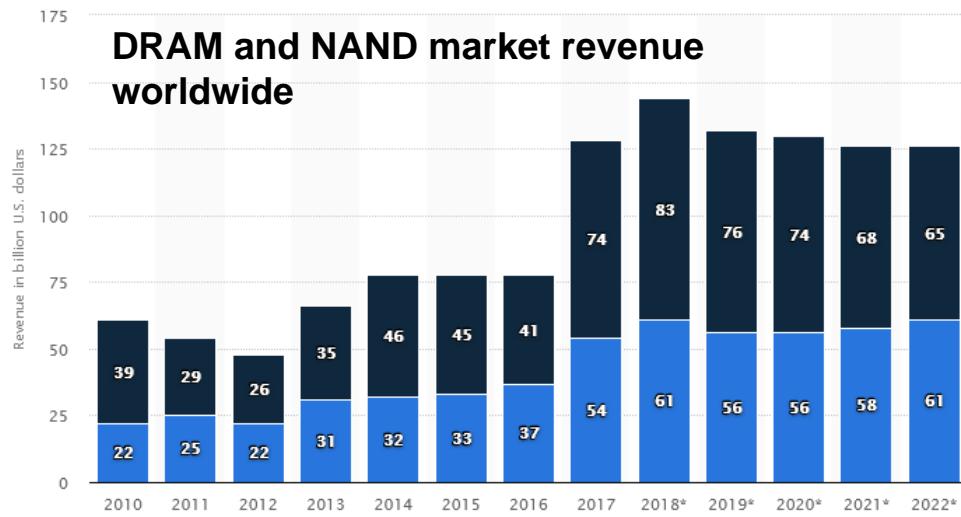
2015F NAND Market by Application (\$27.2B)



Source: IC Insights

SSD = Solid-state drive
HHP = Handheld Player
DSC = Digital Still Camera

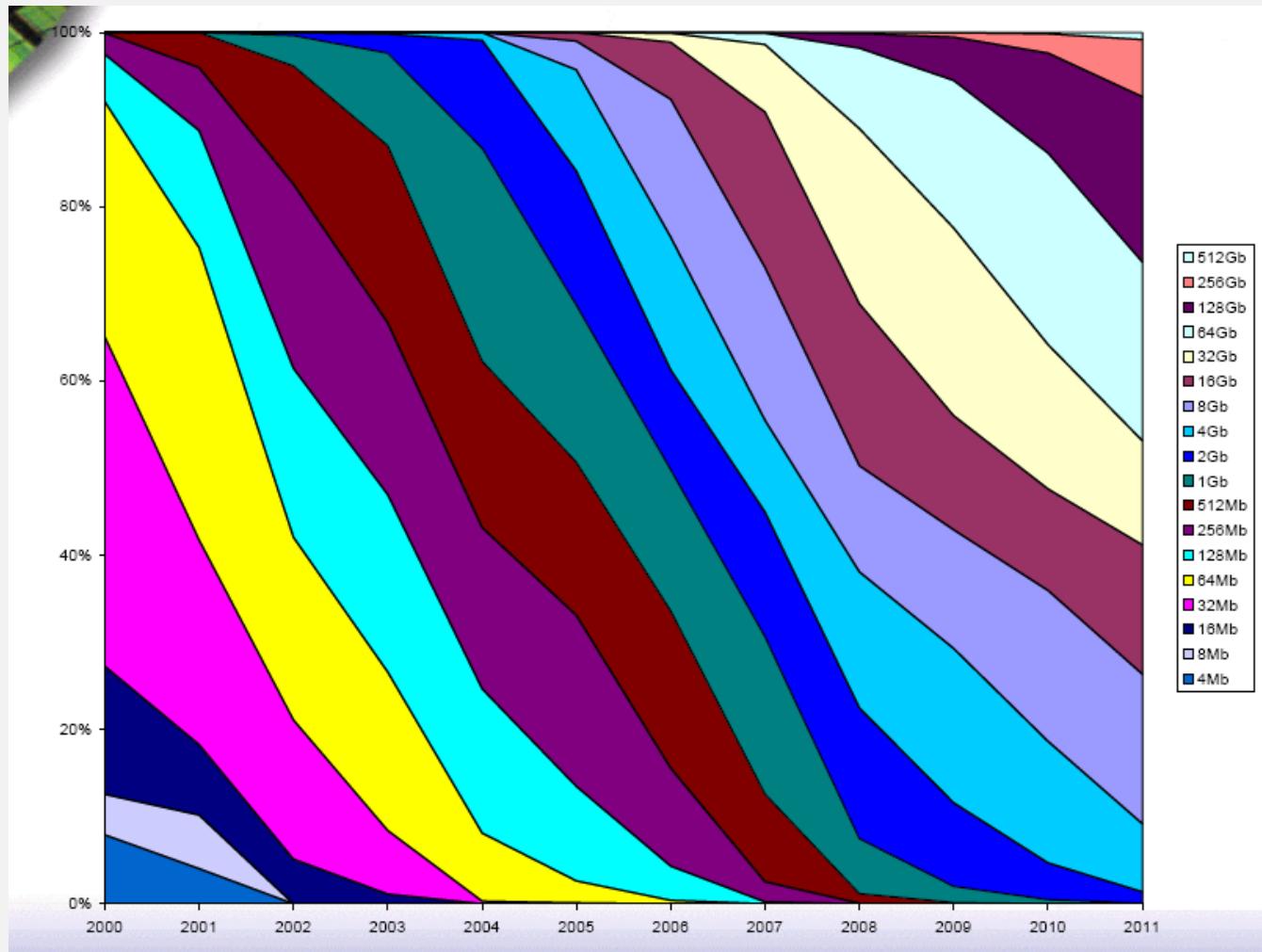
DRAM and NAND market revenue worldwide



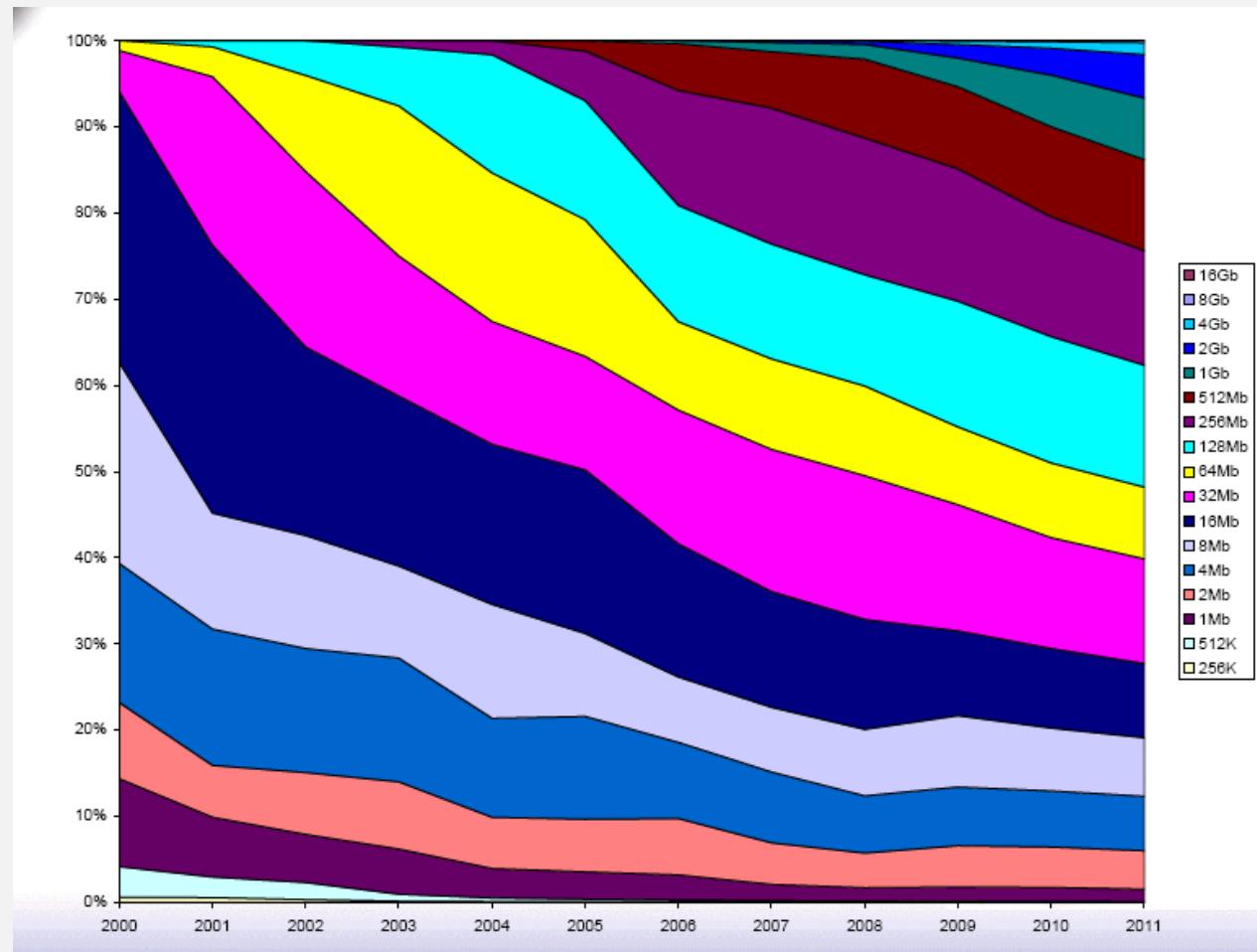
Details: Worldwide; Statista estimates; IHS; 2010 to 2017

© Statista 2020

der Bundeswehr

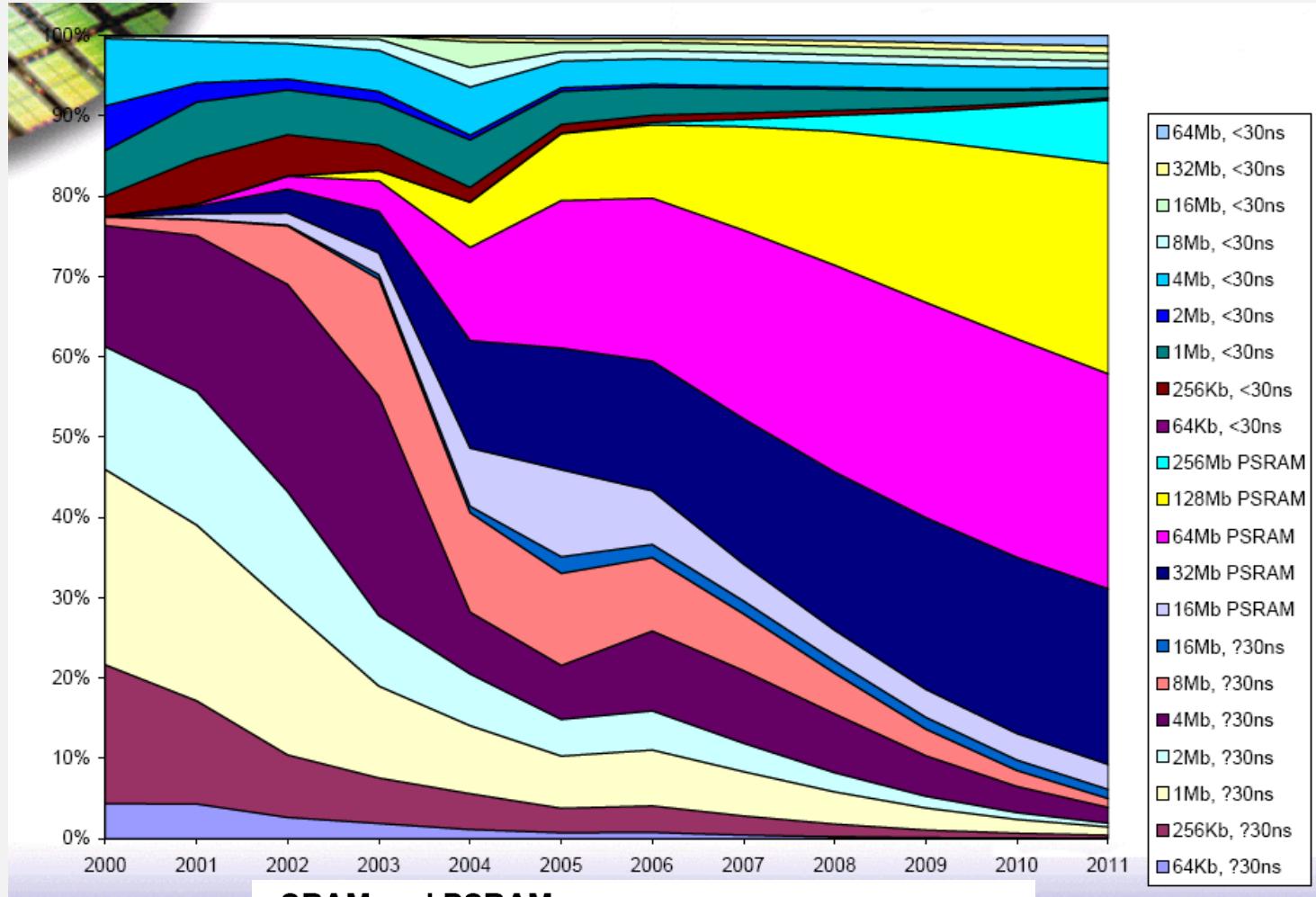


- ◆ NAND – primarily data storage
 - Digital cameras, cell ph, USB drive, MP3, etc.
 - Densities introduced quickly with short life cycle



- ◆ NOR – code storage, some data storage
 - Major market – cell phones
 - focus is on cost per part, long life cycle

Development of SRAM and PSRAM



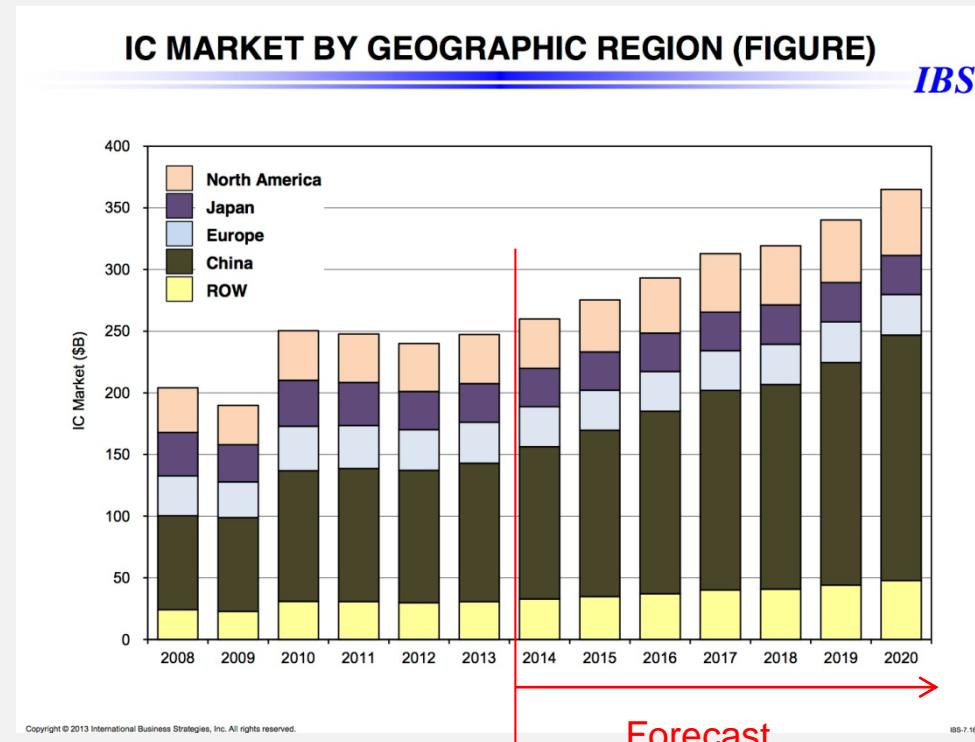
SRAM and PSRAM

- PSRAM and Synch SRAM are high growth
- PSRAM mainly for cell phones
- Synch SRAM expensive, networking equipment and telecom
- focus is on cost per part, long life cycle**

SRAM: Static RAM

PSRAM: Pseudo Static RAM

Where do all the Dies Go ?



Forecast

China becomes the world's largest regional IC market due to producing low price consumer electronics

But China missed to create an own semiconductor industry, so 95% of all needed ICs must be imported

Fab city in India is good news for Infineon

By David Manners -- Electronics Weekly, 4/12/2007

The India-Infineon deal to set up a ten fab, 'Fab City', looks a very good one both for India and for Infineon.

The Indian government recently announced a support scheme for semiconductor manufacturing under which the government pays up to 20 per cent of a project cost through equity participation, tax breaks or other financial incentives.

The reason why the Indian government is so keen on the semiconductor industry is because it expects domestic sales (of **electronic goods**) to increase by 10 times in the next ten years, **reaching \$363 billion by 2015**, for which the **semiconductor content will be worth \$36 billion**.

Either these goods can be bought from overseas or they can be made in India using Indian-built semiconductors.

"We have a burgeoning market **demand in the communications industry, automotives, security cards, defense**, etc and this will help in meeting the needs of the market," said Shenoy. Having a series of fabs, starting with mature, cheap, 0.13-micron technology and escalating to leading edge, will give India the capability to perform all the main value-added stuff locally.

Clearly it's better for India to do everything locally, rather than go through the China syndrome of having a vast local production capacity for electronic goods which is either unprofitable, or barely profitable because around 95 percent of the ICs going into them have to be imported.

By going in with the Hindustan Semiconductor Manufacturing Company to provide its process technology and fab-building expertise to the setting up of ten fabs in India, Infineon will be in pole position to see its products designed into the new generation of India-produced, inexpensive, electronic goods. Others involved in the huge project are Siemens, MW Zander, the clean-room specialists, and US Liquids.

Infineon's contribution will be the provision of process technology, chip design capabilities and expertise in setting up new fabs.

"Fab City will have everything in terms of infrastructure, power, water and chemicals which the semiconductor industry needs," an Infineon spokesman told Electronics Weekly. "**One reason they have chosen Infineon is because we set an industry benchmark with our fab in Malaysia where we went from cornerstone to first wafer out in a year, another reason is that our process fits with the requirements of the Indian market.**"

The first fab Infineon will help build will be a 200-mm 130-nm fab costing about \$800 million to be running by 2009.

The second fab will be a 300-mm 90-nm fab. "The other eight fabs will be announced later," said the spokesman. All will be announced by 2010.

When Fab City expands, and the fabs become leading edge, then Infineon will no doubt have the opportunity to cut an advantageous foundry deal.

That will be a particularly good thing for Infineon because it has said it won't build another fab after the current 65-nm process generation.

So it seems that Infineon has solved a number of challenges with its deal in India.

Challenge number one: How to get fab after its current fab stable obsoletes? Challenge number two: How to get into new markets?

Challenge number three: How to expand its manufacturing capability?

In the meantime, India has secured its semiconductor manufacturing future.

Feb 2008 Chartered to Acquire Eight-Inch Wafer Fab Operation in Singapore

Additional Capacity to Support Mature Technology Offerings as Chartered Faces Limits in Internal Capacity Enhancement SINGAPORE--(Business Wire)--
Chartered Semiconductor Manufacturing Ltd. (Nasdaq:CHRT) (SGX-ST:CHARTERED), one of the world's top dedicated semiconductor foundries, today announced that it has entered into an agreement with Hitachi, Ltd and Hitachi Asia, Ltd to purchase 100 percent of the shares in Hitachi Semiconductor Singapore Pte Ltd ("HNS"), which owns and operates an eight-inch wafer fabrication facility located in Singapore, for a total consideration of approximately US\$233 million in cash. This additional facility will augment the capacity of four eight-inch fabs Chartered currently operates. The incremental capacity resulting from this transaction will enable Chartered to meet some of the additional requirements of existing customers, capture new business opportunities and further diversify its customer base. The transaction also includes a manufacturing agreement with Renesas Technology Corp, an existing customer of HNS, to provide approximately US\$250 million to US\$300 million worth of future wafer fabrication services. The transaction, which is scheduled to be completed at the end of first quarter 2008, is expected to be funded through a combination of existing cash balance, cash flow from operations and credit facilities and is subject to certain customary closing conditions. The transaction is expected to be neutral to Chartered's earnings in 2008.

The facility is located on a 90,000 square-meter campus with building space of 28,000 square meters, including approximately 12,000 square meters of clean-room space. The bulk CMOS logic wafer fabrication facility is currently capable of producing approximately 24,000 eight-inch wafers per month at the 0.15-micron to 0.25-micron technology nodes. Based on the purchase consideration, the investment translates to approximately US\$7.0 million per 1,000 wafers output per month capacity, after excluding the carrying value of the building and other current assets and liabilities acquired as part of this transaction.

"Chartered remains committed to providing a full suite of foundry services to customers, enabling them to deliver market-leading solutions not only in advanced technologies but also in mature technologies. This announcement reflects the progress we have made so far with our value-added technology offerings and allows us to capitalize the investments we have already made in that area by adding immediately available capacity near our existing campus with a trained employee base of approximately 800 people," said Chia Song Hwee, president & CEO of Chartered.

Chartered's 2008 cash-flow based capital expenditures are now expected to be US\$590 million, US\$40 million lower than what was communicated earlier, primarily due to lower capital expenditure requirements in existing eight-inch fabs, as a result of this acquisition. This figure does not include the cost of the acquisition. Chartered Semiconductor Manufacturing Ltd. (Nasdaq:CHRT) (SGX-ST:CHARTERED), one of the world's top dedicated semiconductor foundries, offers leading-edge technologies down to 65 nanometer (nm), enabling today's system-on-chip designs. The company further serves its customers' needs through a collaborative, joint development approach on a technology roadmap that extends to 32nm. Chartered's strategy is based on open and comprehensive design enablement solutions, manufacturing enhancement strategies, and a commitment to flexible sourcing. In Singapore, the company operates a 300mm fabrication facility and four 200mm facilities. Information about Chartered can be found at www.charteredsemi.com.

DRAM Maker Qimonda Files for Insolvency

01.23.09 FRANKFURT/[SEOUL](#) (Reuters) -

German memory chip maker Qimonda filed for insolvency on Friday and South Korea's Samsung Electronics posted its first-ever quarterly loss, in the latest signs of recession hitting the technology sector.

Qimonda said it filed an application to open insolvency proceedings, aiming to reorganize operations as part of an ongoing restructuring program—just nine days after a similar move by Canadian telecoms gear maker Nortel Networks. Bereits im Oktober hat Qimonda ein globales Restrukturierungs- und Kostensenkungsprogramm eingeleitet, um das Unternehmen neu zu positionieren. Im Fokus steht dabei die Konzentration auf die Kernkompetenzen wie die innovative Buried Wordline-Technologie sowie Infrastruktur- und Grafikprodukte. Der Verkauf der Beteiligung an Inotera im November 2008 war ein weiterer wichtiger Schritt, weil dadurch die Abhängigkeit vom PC-Markt und der damit verbundene Mittelabfluss reduziert werden. Die Schließung der 200-mm-Fertigung in Richmond, USA und der Backend-Fertigung für Komponenten und Module in Dresden laufen planmäßig. Zusätzlich hat das Unternehmen seine Produktentwicklung in München und Xi'an konsolidiert sowie die Mitarbeiterzahlen und Kosten in der Verwaltung reduziert.

Qimonda's parent company, Infineon, said it expected to make provisions in the hundreds of millions of euros.

South Korea's Samsung said oversupply and uncertain demand on the chip market would continue, while it posted its first-ever quarterly loss, joining a host of technology companies including Microsoft and Nokia suffering from diving prices and slumping consumer demand.

Consumer demand for computers, phones, TVs and other gadgets has slumped as the global financial crisis becomes a broad recession engulfing the United States and much of Europe, and dampening demand in once-resilient emerging markets.

Samsung, the world's top maker of memory chips and LCD screens, posted a fourth-quarter 4Q08 operating loss of 937 billion won (\$682 million), more than double the loss analysts polled by Reuters had expected.

In Tokyo, shares in Japan's **Sony Corp** tumbled 7 percent after the maker of Bravia [flat](#) TVs, Cyber-shot digital cameras and PlayStation games machines said it would post a bigger-than-expected \$2.9 billion operating loss this business year.

On Thursday, **Microsoft Corp** surprised Wall Street with a profit miss and plans to slash up to 5,000 jobs. It stopped offering quantitative guidance, except to say profit and revenue would almost certainly drop in the next two quarters.

The world's top software maker blamed PC market weakness and the popularity of low-cost netbook computers. Its shares fell 11.7 percent to an 11-year low.

Intel to Roll Out 32 nm MPUs This Year

Staff -- Semiconductor International, 2/10/2009 8:05:00 AM

Intel said it will begin making 32 nm "Westmere" processors later this year. In a speech this morning, Intel CEO Paul Otellini said the company will spend ~\$7B over the next two years to upgrade existing sites in Oregon, Arizona and New Mexico for 32 nm production. At the Intel Developer Forum in San Francisco today, the company is expected to demonstrate working 32 nm processors. Intel's planned investments will be made at existing manufacturing sites in Oregon, Arizona and New Mexico, and will support ~7000 jobs at those locations. Intel has a total workforce of >45,000 in the United States. The company said >75% of its sales are outside the United States, and ~75% of its manufacturing and R&D is done within the United States. In recent weeks, Intel has said it will close older fabs and packaging facilities in the United States and throughout Asia, impacting ~6000 workers.

The initial Intel Westmere processors built with the 32 nm process will be used in desktop and "mobile mainstream" systems. Westmere combines Intel's Nehalem micro-architecture with integrated graphics, which Intel said will provide increased performance while simplifying system manufacturing.

TSMC and Nanjing Sign 12-inch Fab Investment Agreement

Issued by: TSMC

Issued on: 2016/03/28

Hsinchu, Taiwan, R.O.C. – March 28, 2016 - TSMC (TWSE: 2330, NYSE: TSM) today announced that the Company and the municipal government of Nanjing, China have signed an investment agreement. This agreement affirms that TSMC will make an investment in Nanjing valued at US\$3 billion to establish TSMC (Nanjing) Co. Ltd., a wholly-owned subsidiary managing a 12-inch wafer fab and a design service center.

TSMC's 12-inch fab site in Nanjing will be located in the Pukou Economic Development Zone. Planned capacity is 20,000 12-inch wafers per month, and the facility is scheduled to commence production of 16nm process technology in the second half of 2018.

As a technology leader, TSMC began volume production of 16nm process technology for customers in 2015, and accounted for more than half of the global foundry market for production of 14/16nm technology wafers in that year. Further significant increases in global foundry market share of the 14/16nm technology production is forecast for 2016. TSMC also holds the largest foundry market segment share in China with more than 100 Chinese customers.

"With our 12-inch fab and our design service center in Nanjing, we aim to provide closer support to customers as well as expand our business opportunities in China in step with the rapid growth of the Chinese semiconductor market over the last several years," said TSMC Chairman Dr. Morris Chang. "We look forward to stronger collaboration with our customers to further expand our market share in China." and Nokia suffering from diving prices and slumping consumer demand.

SMIC Shenzhen Launches Construction of the First 12-Inch IC Production Line in South China

Issued by: SMIC

Issued on: 2016/11/03

SHENZHEN, China, Nov. 3, 2016 /PRNewswire/ -- Semiconductor Manufacturing International Corporation ("SMIC"; NYSE: SMI; SEHK: 981), one of the leading semiconductor foundries in the world, and the largest and most advanced foundry in Mainland China, announces the official launch of a 12-inch integrated circuit (IC) production line at SMIC's Shenzhen facility. It will be the very first 12-inch fab in South China.

In order to meet the large demand for IC chips in the IoT era, SMIC Shenzhen is building the new 12-inch IC production line in an existing building. The new line will manufacture mainstream mature technology. Construction is planned to start by the end of 2016. Some second-hand equipment for the new line has already been secured. The early production is expected to begin by the end of 2017. The total designed capacity is 40,000 12-inch wafers per month; capacity ramp will be based on customer needs.

Located in Pingshan New District, Shenzhen, SMIC Shenzhen opened the first 8-inch IC production line in South China in December 2014. Its capacity is currently 30,000 wafers per month, and it will continue to expand based on market demand.

Investments for fab technology and product upgrades, as well as for additional capacity, will grow as the emergence of numerous new fabs significantly increases equipment demand, the forecast shows. The World Fab Forecast Report currently tracks **78 new fabs and lines that have or will start construction between 2017 to 2020** (with various probabilities) and will eventually require more US\$220 billion in fab equipment (Figure 1). Construction spending for these fabs and lines is expected to reach US\$53 billion during this period.

Fully 60 percent of these fabs will serve the Memory sector (the lion's share will be 3D NAND), and a third will go to Foundry.



SK Hynix to build new DRAM fab in Icheon (Gyeonggi Province), Korea – The construction, to be completed by the end of 2020, will adopt 1znm node (probably EUV). Total investment is estimated to exceed \$13 billion.

Shanghai Jita Semiconductor/Huada Semiconductor – Shanghai Jita Semiconductor, a subsidiary of Huada Semiconductor and China Electronics Corporation (CEC), announced plans earlier this month to build both 200 mm and 300 mm semiconductor fabs for analog and power semiconductors in Shanghai. The combined fab investment will total \$5.18 billion.

Murata to invest into 150mm expansion – Murata announced a 5 billion Yen investment (US\$44.6 million) in a new fab extension in Vantaa, Finland.

Bosch 300mm fab in Dresden, Germany – Bosch held a groundbreaking ceremony on April 24. Equipment installation is expected in 2H19.

<https://electroiq.com/2018/09/semi-fabview-update-more-investments-in-semiconductor-fabs/>

2.1 Introduction

2.2 Market demand for highly Integrated Circuits IC

2.3 Shrinking: Making Money

2.4 Shrinking: Spending Money

2.5 Calculation of Semiconductor Industry

2.6 Market Information on ICs

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Chapter 2