



## Master Course

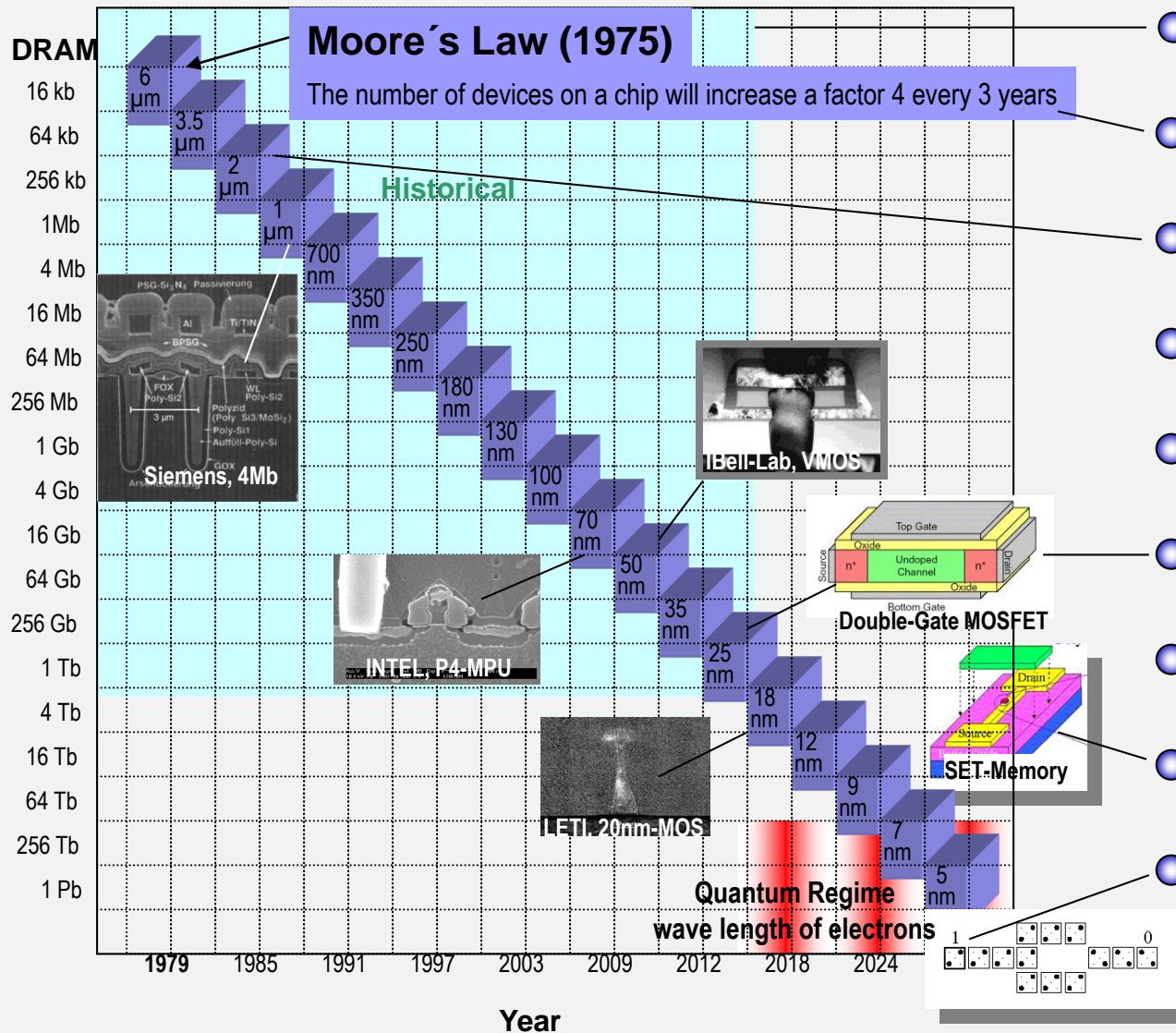
# Advanced MOSFETs and Novel Devices

A Look at the Future Development of Industrial Semiconductor Devices

**Dr. Josef Biba (UniBw Munich)**



German Institute of Science and Technology  
Cooperation of  
Nanyang Technological University and Technical University Munich



- **1 History**  
Planar technology, Transistors, ICs
- **2 Economics**  
Future Applications, Markets, Semiconductors
- **3 Long-channel MOSFETs**  
Basic Behavior, High-Field Effects
- **4 Short-channel MOSFETs**  
Short-Channel Effects, Scaling
- **5 Carrier Transport**  
Theory, Simulation, Experiment
- **6 Advanced MOSFETs**  
SiGe, high-k, vertical MOS, Double-Gate
- **7 Hot Electron Transistors**  
PDB-FET, IMOS, Spin-Valve-Transistor
- **8 Tunneling Transistors**  
Tunneling-FET, Single-Electron Transistor
- **9 Quantum-Coherence Transistors**  
Spin-Resonance Transistor, Quantum Computing

0.1 Remarks on Lecturer

0.2 GIST - TUM-Asia

0.3 Singapore - a Global Semiconductor Hub

0.4 Overview of Lecture

## Curriculum Vitae



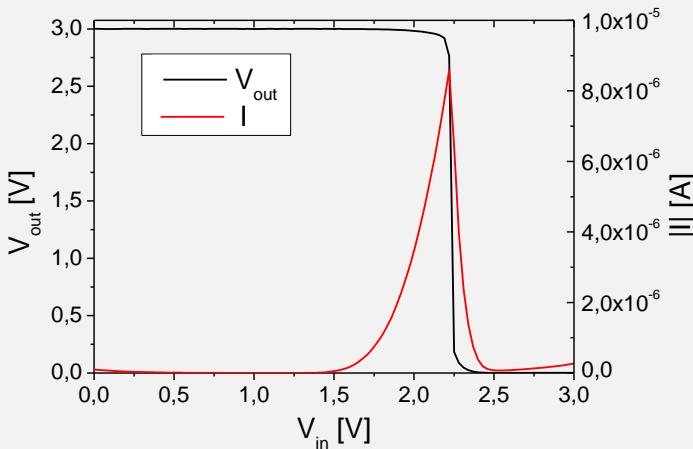
Dr.-Ing. Josef Biba

since 2013 Senior Engineer at the Institute of Physics at the Universität der Bundeswehr  
Scientific Laboratory Supervisor  
2009 – 2012 Assistant at the Institute of Physics at the Universität der Bundeswehr  
Ph.D. Thesis: High-k Metal-Gate CMOS Transistors  
2008 – 2009 Assistant at the Institute Semiconductor Manufacturing Technology (TUM)  
2002 – 2008 Studies of electrical engineering at the Technical University München (TUM)

## Aktual Working Field

CMOS Technology  
Future Devices  
Security on Chip  
Measurement Systems

Homepage: <https://www.unibw.de/physik>  
Email: [Josef.Biba@unibw.de](mailto:Josef.Biba@unibw.de)  
Phone: 0049 / 89 / 6004 - 4041

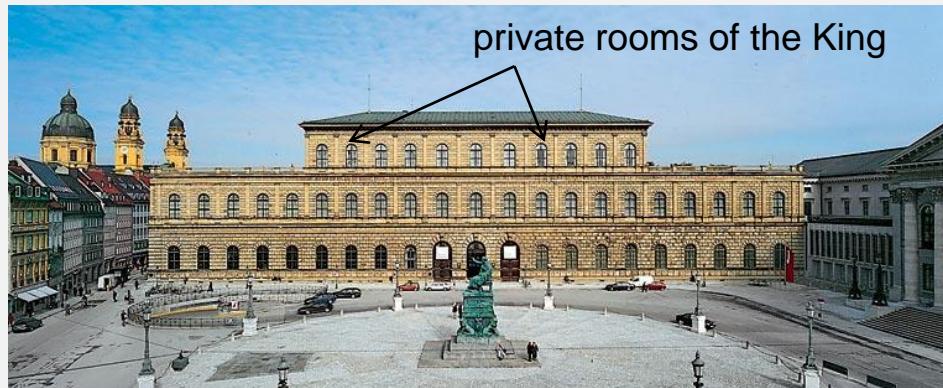




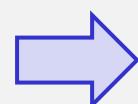
About 1.2 Mill. people are living in Munich.

Munich is the home of :

- 10 universities with about 80.000 students
- 45 museums and galleries and 58 theatres.

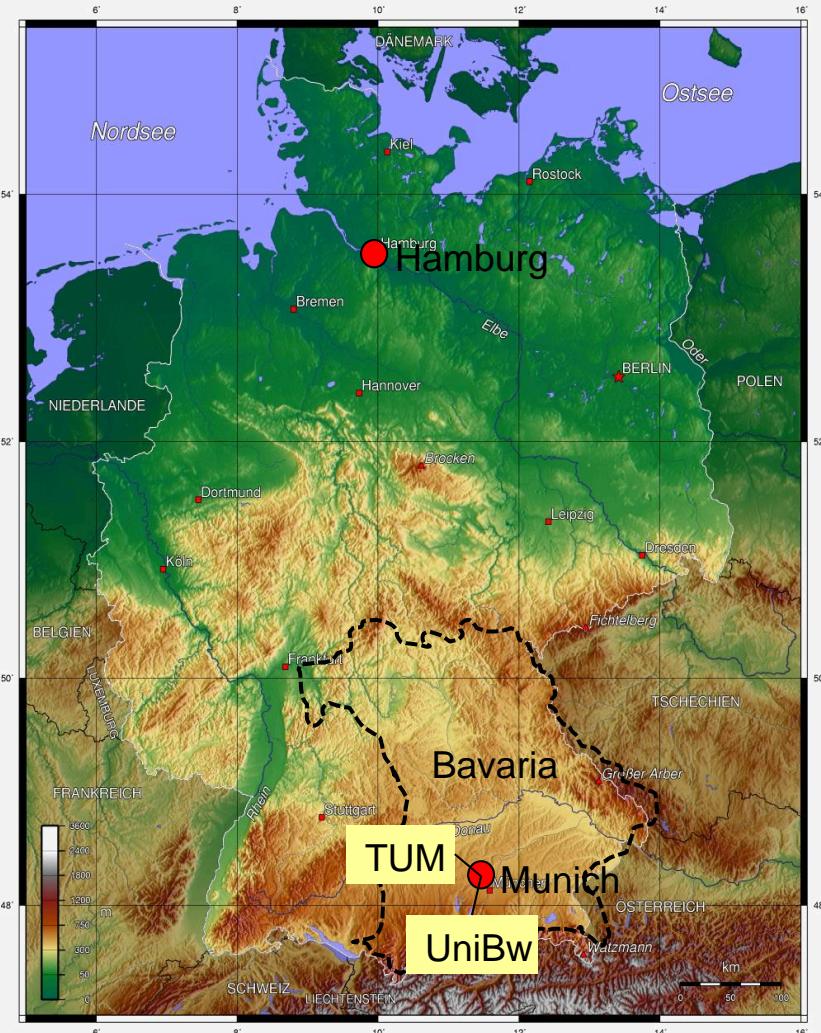


200 years ago the Bavarian King Ludwig I ordered, that it is not allowed in Munich to build houses, which are higher than his residence



Munich is a city fabricated in "planartechnology"





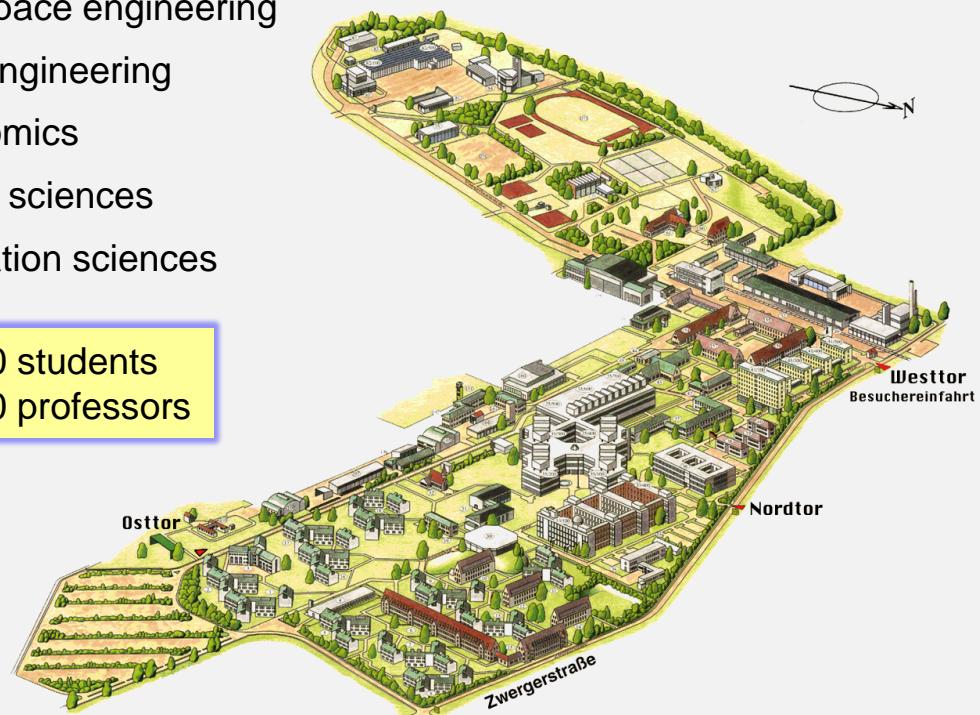
In 1973 the German Government founded two universities to ensure a high-quality, fast academic education of their commanding officers.

Universität der Bundeswehr München:

7 faculties:

- Computer and information sciences
- Electrical engineering and information technology
- Aerospace engineering
- Civil engineering
- Economics
- Social sciences
- Education sciences

~ 3500 students  
~ 170 professors





Prof. Dr. Walter Hansch  
Chair for Micro Systems Technology



Prof. Dr. Georg Düsberg  
(Director Institute of Physics)  
Chair for Sensor Technology



Prof. Dr. Christoph Kutter  
Chair for Smart System Electronics  
in cooperation with Fraunhofer Institute Munich  
+ Director of EMFT-Fraunhofer Institute



Prof. Dr. Ignaz Eisele (exc. Em.)  
Head of Division of EMFT-Fraunhofer Institute

## Laboratories

### 2 Cleanrooms

- Class 1, 400 m<sup>2</sup>
- CMOS, 4", 6", 8"



### Associated Labs

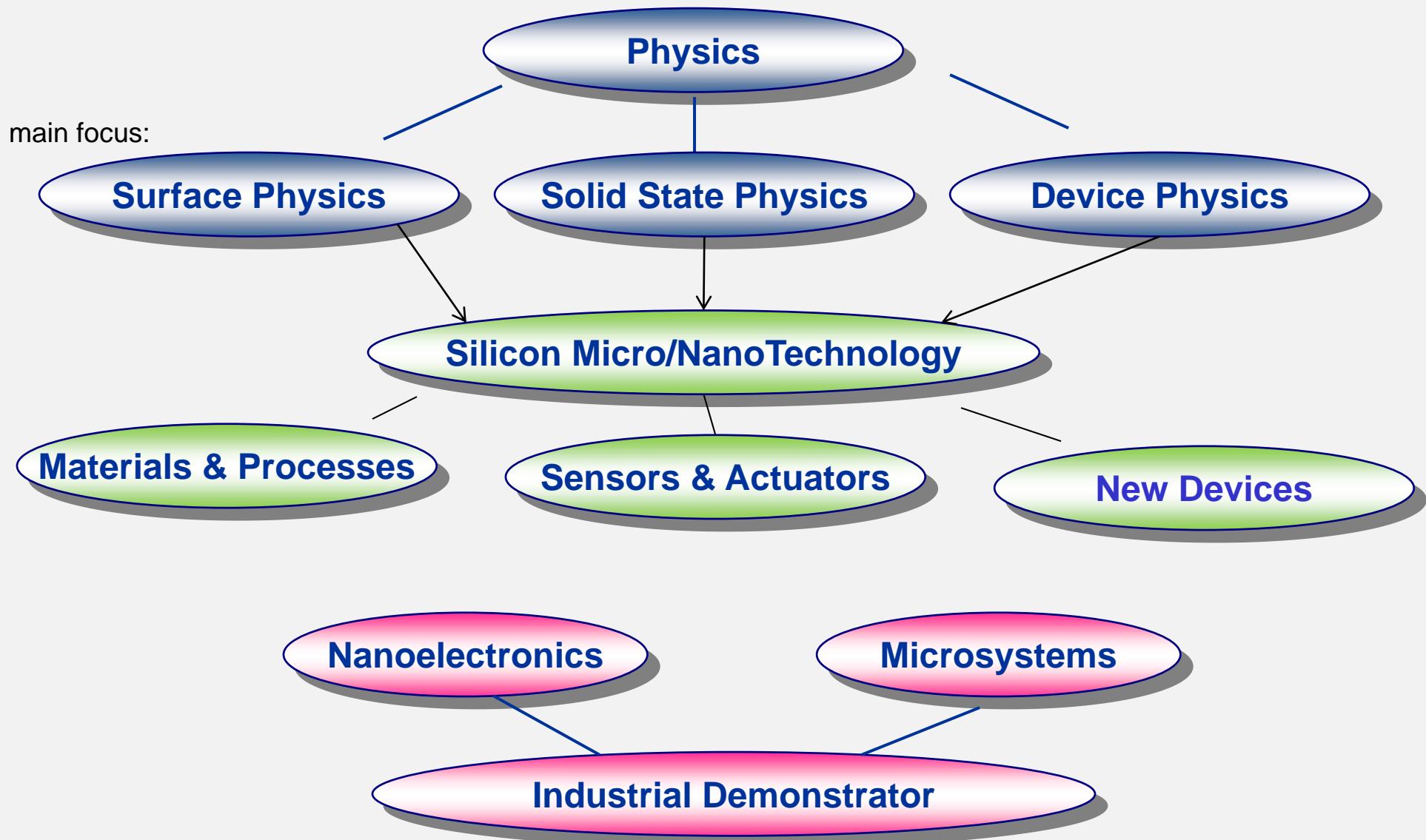
- 400 m<sup>2</sup>
- MBE, Sensors, Packaging

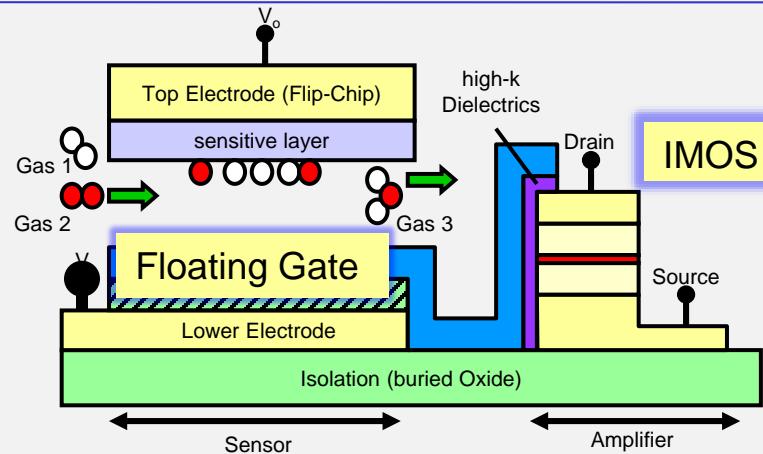
### Analytic Labs

- 200 m<sup>2</sup>
- SIMS, AFM, STM, LEED, AES, XPS
- Electrical characterization

### Staff

- 10 permanents
- 10-15 scientific staff (most Ph.D. students)



Typical Example

Industrial Demonstrator

in cooperation with: SIEMENS

Microsystems

(sensor &amp; amplifier)

Nanoelectronics

(layers with nanometer thickness)

Materials &amp; Processes

(new sensor materials)

Sensors &amp; Actuators

(new sensor Floating Gate -FET)

New Devices

(Impact Ionization FET)

Silicon Micro/NanoTechnology

Surface Physics

- \* reaction kinetics
- \* work function engineering

Solid State Physics

- \* mechanism of impact ionization
- \* carrier mobility due to strain

Device Physics

- \* steep slope switch-on due to impact
- \* high-temperature operation due to high doping

## The Periodical System:

Hydrogen: 1 Proton

	I	II	IIIb	IVb	Vb	VIb	VIIb	VIIIb	Ib	IIb	III	IV	V	VI	VII	VIII		
1	H 1.007														He 4.002			
2	Li 6.941	Be 9.012																
3	Na 22.98	Mg 24.30																
4	K 39.09	Ca 40.07	Sc 44.95	Ti 47.88	V 50.94	Cr 51.99	Mn 54.93	Fe 55.84	Co 56.93	Ni 58.93	Cu 58.69	Zn 63.54						
5	Rb 85.46	Sr 87.62	Y 88.90	Zr 91.22	Nb 92.90	Mo 95.94	Tc 98.90	Ru 101.0	Rh 102.9	Pd 106.4	Ag 107.8	Cd 112.4						
6	Cs 132.9	Ba 137.3		Hf 178.4	Ta 180.9	W 183.8	Re 186.2	Os 190.2	Ir 192.2	Pt 195.0	Au 196.9	Hg 200.5						
7	Fr 223.0	Ra 226.0		104	105	106	107	108	109	110	111	112	Dy 162.5	Ho 164.9	Er 167.2	Tm 168.9	Yb 173.0	Lu 174.9
				Rf 261.1	Db 262.1	Sg 263.1	Bh 262.1	Pr 265	Hs 266	Mt 269	Uun 272	Uub 277						
				La 138.9	Ce 140.1	Pr 140.9	Nd 144.2	Sm 146.9	Eu 150.3	Gd 151.9	Tb 157.2							
				Ac 227.0	Th 232.0	Pa 231.0	U 238.0	Np 237.0	Pu 244.0	Am 243.0	Cm 247.0	Bk 247.0	Cf 251.0	Es 252.0	Fm 257.0	Md 258.0	No 259.1	Lr 260.1

There are 2 important elements:

Carbon

the element of life



Silicon

the element of electronics



There exist almost no electrical equipment without semiconductors

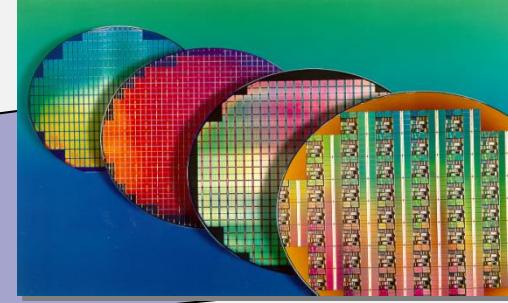
A huge market for innovations



$10^0$   
= 1m  
some flowers



$10^9$   
= 1 Billion Meter  
earth with moon



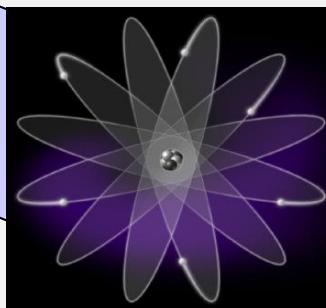
$10^{16}$

CMOS transistors  
are fabricated every day;  
arranged in one line they reach  
from earth to moon every day

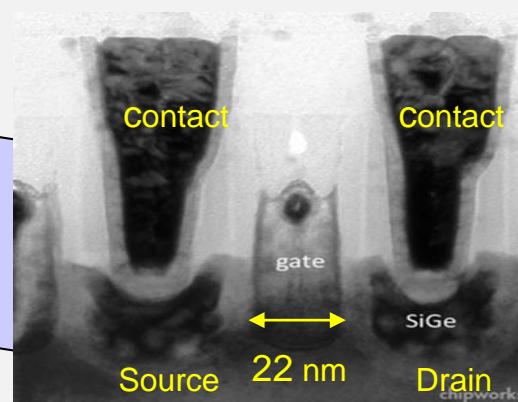


$10^{47}$

Silicon atoms in solid ground  
Si is the second frequent element



$10^{-9}$   
= 1 ppb  
= 1 nanometer  
diameter of single atoms



Source      22 nm      Drain

Contact  
gate  
SiGe  
chipworks

Nanometer dimensions  
dimensions of an INTEL IvyBridge 2012  
smallest lateral dimension: < 22nm  
**= 100 atoms !**



5 nm

Nanometer dimensions  
actual dimensions of a gate oxide  
vertical dimensions: 1.2 nm  
**= 5 atoms !**

**2 Cleanrooms**

- Class 1, 400 m<sup>2</sup>
- CMOS, 4", 6", 8"

**Associated Labs**

- 400 m<sup>2</sup>
- MBE, Sensors, Packaging

**Staff**

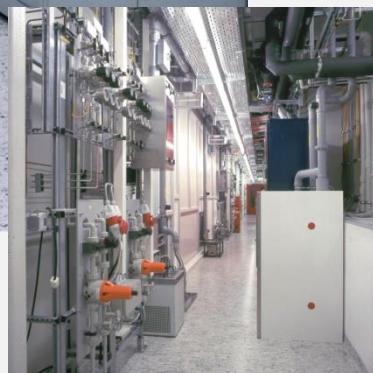
- 10 permanents
- 10-15 scientific staff (most Ph.D. students)

**Equipment**

- \* Wet benches (cleaning, etch)
- \* Evaporation (thermal, e-gun)
- \* Sputtering: metals, dielectrics
- \* LPCVD: Si, SiO<sub>2</sub>, Si<sub>3</sub>N<sub>4</sub>
- \* Anisotropic Dry Etch RIE
- \* Furnace processes: diffusion, oxidation
- \* Rapid Thermal Processing: diffusion, oxidation
- \* Photolithography (2μm)
- \* Backend: dicing, bonding

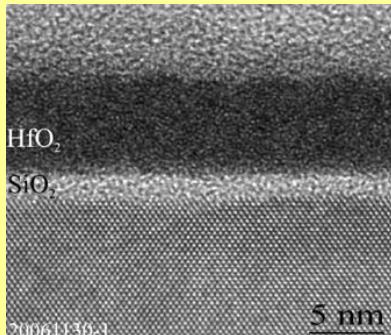
**Analytic Labs**

- 200 m<sup>2</sup>
- SIMS, Nano-IR AFM, STM, LEED, AES, XPS, Raman
- Electrical characterization IV, CV, GV, Stress, LHe

**Quality Management:**

- \* Tool Capability
- \* Design of Experiments
- \* Statistical Process Control
- \* Device Control
  - > Reproducibility
  - > Yield
  - > Reliability

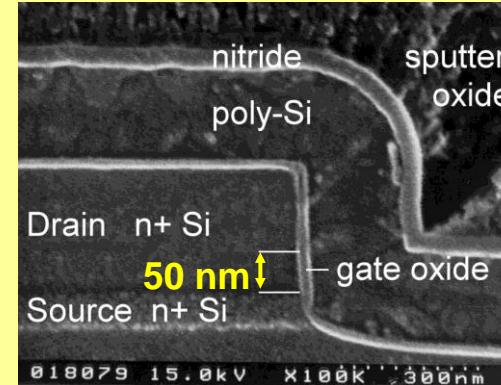
## New Materials and Processes



### High-k Dielectrics deposited by Atomic Layer Deposition

- \* own investigations in institute cleanroom
- \* Cooperation with semiconductor industry

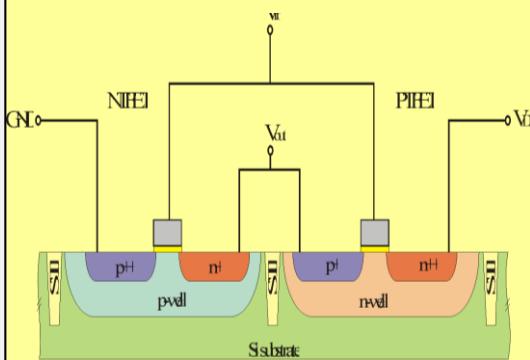
## New CMOS-Structures



### Vertical Silicon on Nothing-FET

- \* own investigations in institute cleanroom
- \* Cooperation with semiconductor industry

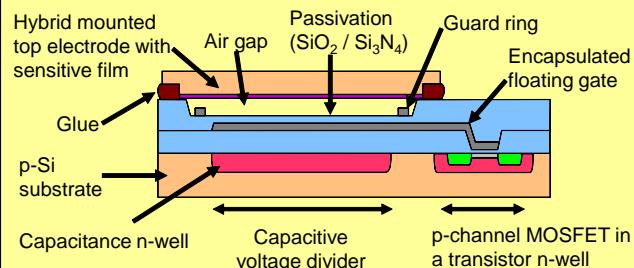
## New Devices



### Complementary Tunneling-FETs

- \* own inventions
- \* own investigations in institute cleanroom
- \* Cooperation for circuits with semiconductor industry

## New Applications



### Micro Systems

- \* own fabrication in institute cleanroom
- \* Cooperation with industry



**Technology**

Physics, Material, Processes, Device, Microchip  
der Bundeswehr  
*Universität München*

KETEK

**Packaging**

**System**

**Application**

Electronics + Tool

**Technology**

Physics, Material, Processes, Device, Microchip  
der Bundeswehr  
*Universität München*

EPCOS

**System**

**Application**

Advanced MOSFETs and Novel Devices



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The Free Encyclopedia

Main page  
Contents  
Featured content  
Current events  
Random article

Article

Talk

Read

Edit

## Opportunity (rover)

From Wikipedia, the free encyclopedia

**Opportunity**, also known as **MER-B** (**Mars Exploration Rover – B**) or **MER-1**, is a robotic **rover** active on the planet **Mars** since 2004.<sup>[1]</sup> Launched on July 7, 2003, *Opportunity* landed on Mars' **Meridiani Planum** on January 25, 2004 at 05:05 **Ground UTC** (about 13:15 **Mars local time**), three weeks after its twin *Spirit* (MER-A), also part of **NASA's Mars Exploration Rover Mission**, touched down on the other side of the planet.<sup>[6]</sup> With a planned 90 **sol** (Martian days) duration of activity, *Spirit* functioned until getting stuck in 2009 and ceased communications in 2010, while *Opportunity* remains active as of 2014, having already exceeded its operating plan by 10 years, 127 days (in Earth time). *Opportunity* has continued to move, gather scientific observations, and report back to Earth for over 40 times its designed lifespan. On July 28, 2014, NASA

News » Product and Company News

## NEWS

### KETEK LANDS ON MARS



Quelle: Nasa / JPL-Caltech

On board of Mars rover Curiosity and as part of a X-ray spectrometer, KETEK's Silicon Drift Detectors have arrived on the Red Planet. The X-ray instrument, again part of an onboard science laboratory, irradiates a rock or soil target with X-rays. The irradiation results in the target giving off own characteristic X-ray radiation, which is collected and understood by KETEK's Silicon Drift Detector at the spectrometer head. Quality and quantity of chemical elements in the target are revealed. A significant improvement to Curiosity's X-ray instrument compared to those of previous Mars rover X-ray spectrometers is the Silicon Drift Detector's cooling system. Instruments of previous Mars laboratories could only measure during the night when temperatures are low. The advanced cooling also allows measurements at day.

### NEWS

- ▶ Product and Company News
- ▶ Conferences and Events
- ▶ News Archive



KETEK cooperates for research and development with the Institute of Physics since 2002. Most processes of the X-ray detector chips were fabricated at the Institute of Physics.



**KETEK**  
Creative Detector Solutions



# Examples of R&D with Industry



2000-2004  
Atomic Layer Deposition



since 2002  
X-ray Detectors



2004-2008  
Selective SiGe-Epitaxy



1999-2009  
Manufacturing Engineering



since 2015-2018  
Reliability Automobile Electronics



2000-2004  
Microcoils  
2006-2011  
Metallization for  
SAW-Filter



2010-2017  
Plasma-Etching-Technique



2008-2014  
Gas Sensors



2013-2017  
- Robustness of Smart Systems  
- Chip Security



2011-2014  
Glass Lenses for  
Automobile



2010-2014  
Solar Cells



2004-2008  
High Temperature Sensors  
2009-2011  
SIMS-Analytics

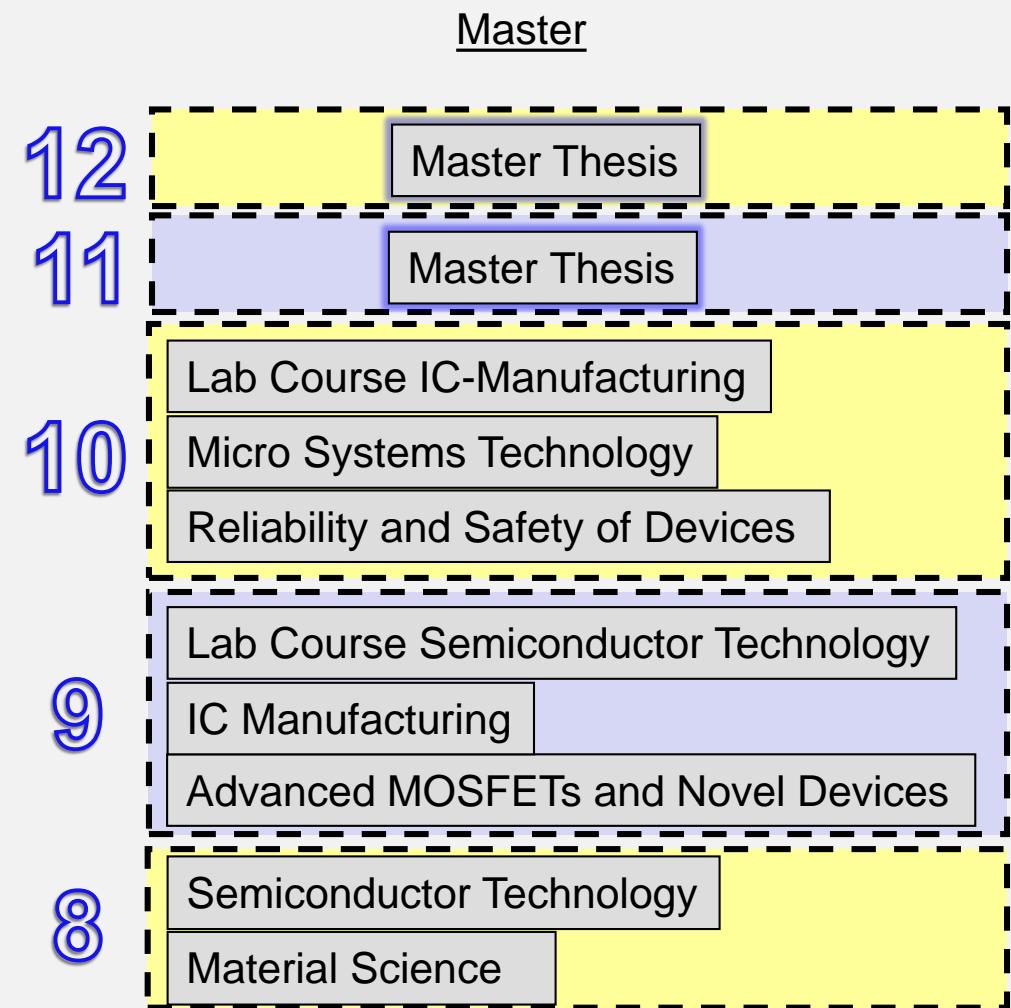
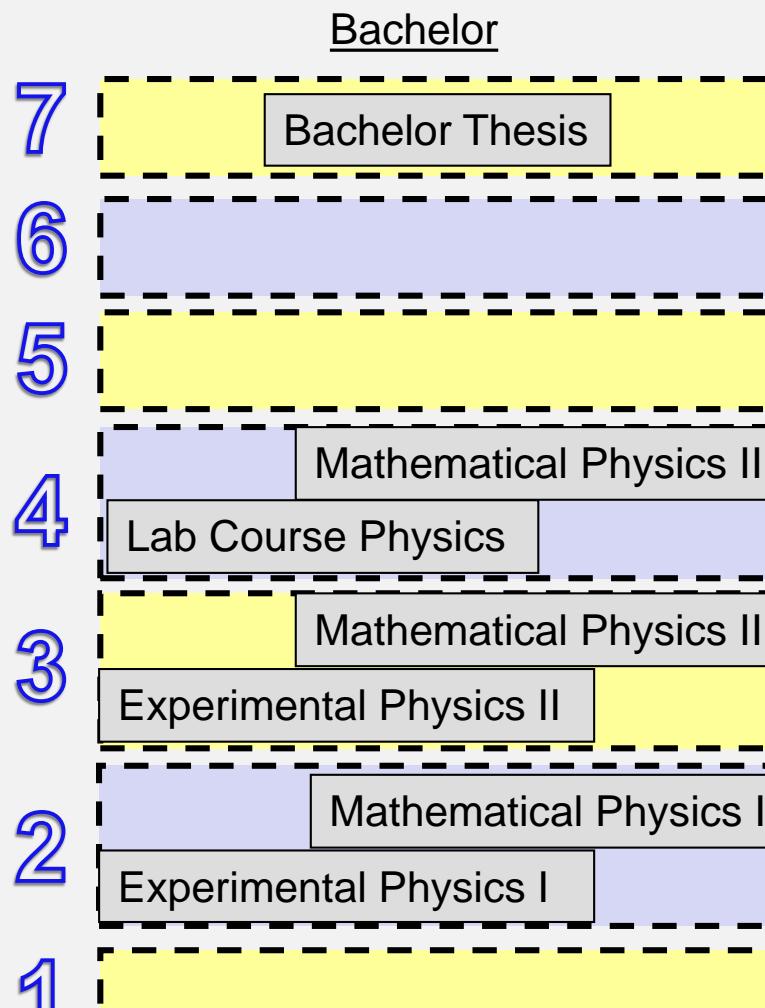
AMAT (Tools, Process)  
ATV (Tools, Process)  
BMW (Position-Sensors)  
EADS (Gas-Sensors)  
EPCOS (Passive Components)  
Freescale (Process)  
Infineon (Device Reliability)  
INTEL (Novel Devices)  
Ketek (Radiation Detector)  
Mattson (Coating Processes)  
Micronas (Gas-Sensors)  
Siemens (Analytics)  
Siemens (Microsystems)  
Tepla (Plasma Technique)  
TUI Laser (Process)



2000-2004  
Laser Etching



since 2011  
Amorphous Silicon-CVD



## What about TUM-Asia ?



● German Institute of Science and Technology  
**The First German University Abroad in Operation**

\* In February 2003 TUM was the first German university to establish a privately organized affiliation abroad, the German Institute of Science and Technology (GIST).



The start-up funds were provided by the German Academic Exchange Service – Deutscher Akademischer Austauschdienst (DAAD) – and the Singapore government. In future the privately organized university will finance itself exclusively by means of tuition fees. Scholarships are available for suitable candidates.

In Singapore GIST is competing with already established affiliations of renowned universities such as the Massachusetts Institute of Technology(MIT), the Georgia Institute of Technology and the John Hopkins University.

## What about TUM-Asia ?

Singapore: Best Practice from Munich

**In 2002, the Technical University of Munich was the first institution to launch a German university abroad:  
the German Institute of Science and Technology.**



And the winner is: Technical University of Munich (TUM)!

**Only last year the TUM won first prize for international university marketing.**

As early as the 1990s, TUM's President Wolfgang Herrmann declared marketing to be his top priority; he launched global campaigns to advertise the TUM brand and created a network of international partnerships. In 2002, the TUM was the first institution to launch a German university abroad, the German Institute of Science and Technology (GIST) in Singapore.

Since then, the GIST has been offering an 18-month master's degree course in industrial chemistry in close cooperation with its partner universities, the National University of Singapore (NUS) and **Nanyang Technological University (NTU)**. Together with the NTU, **integrated circuit design** was added to the curriculum two years ago. Starting in the summer of 2007, the GIST will be extending its portfolio further with three **new master's courses: microelectronics, intelligent transportation systems, and environmental engineering**. Food technology is now well-established as a bachelor's degree course.

GIST Director Markus Wächter is very satisfied with the way his German export has been developing: "Singapore is a highly interesting location from an academic and economic standpoint. With the help of the GIST, we want to expand academic cooperation with the universities in the region."

Fifty students are currently registered for the courses in industrial chemistry and integrated circuit design. The aim for 2007 is to increase the number of students to about 25 per course. A total of 35 to 40 are planned for the bachelor's course. Studying at the GIST is attractive for students, because the master's courses are industry-oriented fast-track programs. **This means that good and very good graduates with a bachelor's degree or university of applied sciences qualification can attain a master's degree in 18 months in a top-level course.**

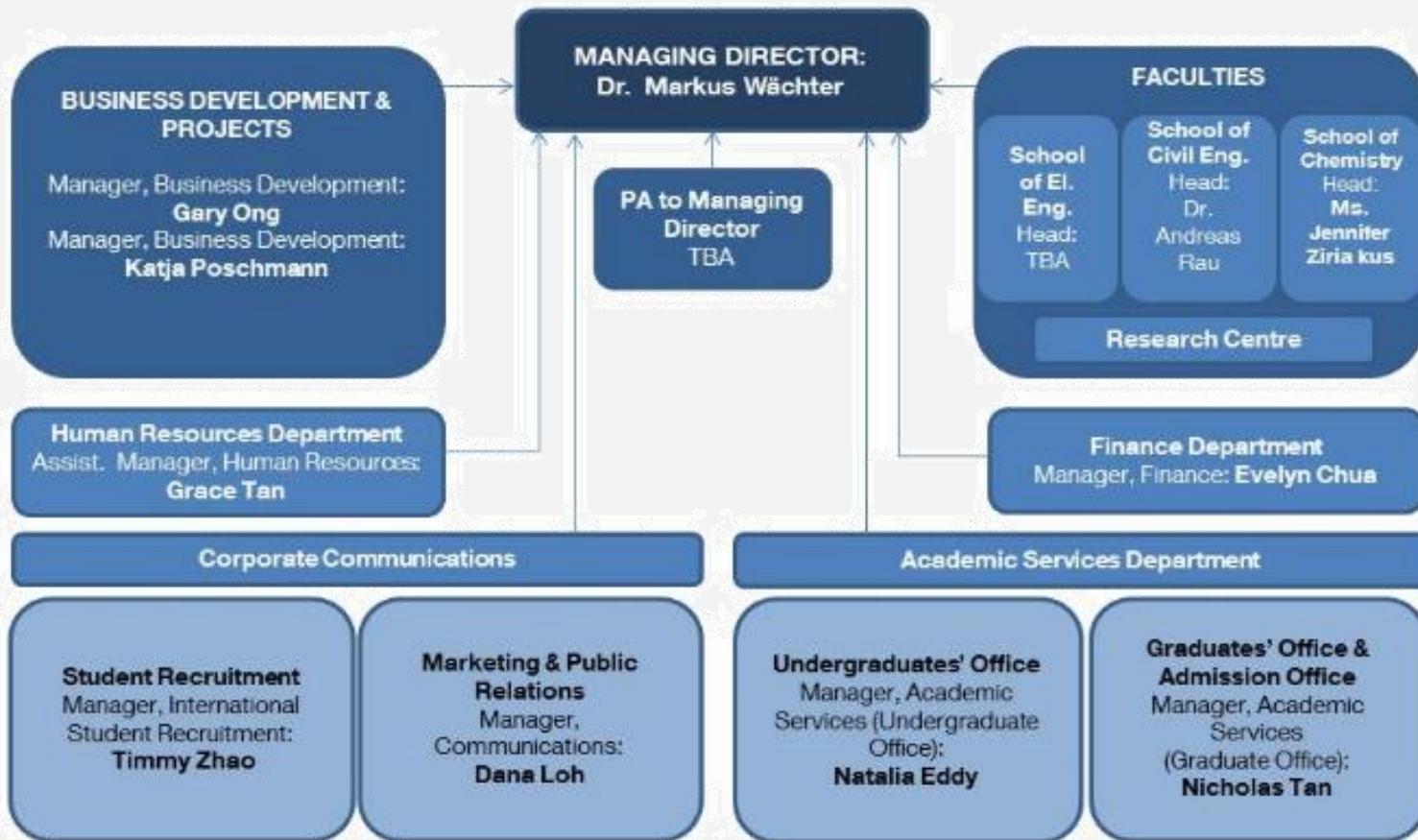
Another advantage is that all the master's degrees are double degrees awarded jointly by the TUM and the NTU, or by the TUM and the NUS. Furthermore, every master's student does a period of practical training in industry after the 10-month theoretical module in Singapore.

Some will also have the opportunity to write their master's thesis at a renowned German company such as BASF or Degussa.

However, all this comes at a price: the one-and-a-half-year course in industrial chemistry costs 45,000 Singapore dollars; the other courses cost 30,000 Singapore dollars. Approximately 30% of the students are supported by scholarships from German companies.

The project is not yet self-financing, however. The GIST is subsidized by the government of Singapore and the German Academic Exchange Service (DAAD). Katja Winckler 22.01.2007 [www.magazine-deutschland.de](http://www.magazine-deutschland.de)

# Organization Structure

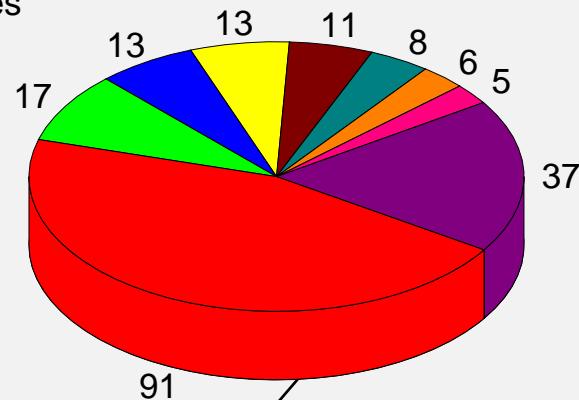


<http://tum-asia.edu.sg/about-tum-asia/organization-chart/>

# Global Ranking of Universities

## Distribution of the Top 202 Universities (in 2018)

<span style="color: red;">■</span>	United States
<span style="color: green;">■</span>	UK
<span style="color: blue;">■</span>	Germany
<span style="color: yellow;">■</span>	Canada
<span style="color: darkred;">■</span>	China
<span style="color: teal;">■</span>	Australia
<span style="color: orange;">■</span>	Netherlands
<span style="color: magenta;">■</span>	Switzerland
<span style="color: purple;">■</span>	Others



source: [www.webometrics.info](http://www.webometrics.info)

Germany: #3 in the world,  
the only non-native English speaking country  
among the top 4

2007-2019:

Technical University Munich: # 57 in world  
(2019) # 1-3 in Germany

source: Shanghai Academic Ranking: [www.shanghairanking.com](http://www.shanghairanking.com)

TUM takes the number six spot in the “Global University Employability Ranking”  
**TUM offers a world-class education**

The Technical University of Munich (TUM) is seen by international companies as one of the world's best universities in terms of the quality of its graduates. In the latest "Global University Employability Ranking", TUM is ranked sixth in the world – for the second consecutive year. It stands alongside the University of Cambridge as one of just two European institutions among the top ten.

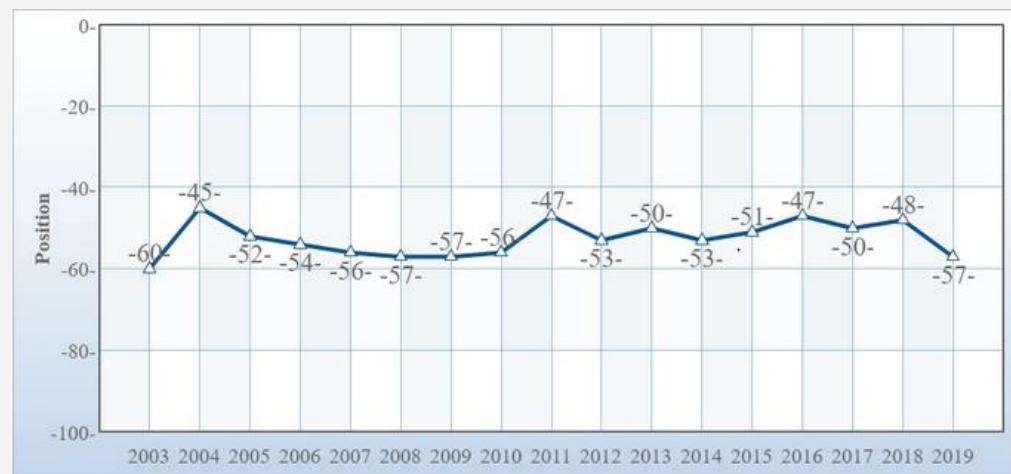
To prepare the rankings, which are compiled annually on behalf of the British magazine Times Higher Education (THE), the market research company Trendence surveys companies in all major industries worldwide, asking them for their views on the universities with the best graduates. For the latest rankings, Trendence collected responses from around 8,000 managers in 23 countries, many of whom are responsible for recruitment.

TUM has consistently been rated for years as the German university whose graduates are best prepared for entry into the working world.

### Only one other European university among the top 10

Along with TUM, the top ten spots in this year's rankings include six universities in the USA as well as the University of Cambridge (4th), the University of Tokyo (7th) and the Hong Kong University of Science and Technology (10th). The next-highest German university is Ludwig Maximilians University Munich, which placed 25th.

TUM also regularly achieves excellent results in other major university rankings. For example, it placed seventh among "Europe's Most Innovative Universities" and is listed as the best German university in the "QS World University Ranking".



## Industrial Partners of TUM



and many more ...

## 0. Overview

### 0.3 Remarks on Singapore

# What about Singapore ?

#### Most Globalized countries, 2018

1. Belgium (90.47)
2. Netherlands (90.24)
3. Switzerland (89.70)
4. Sweden (88.05)
5. Austria (87.91)
6. Denmark (87.85)
7. France (87.34)
8. UK (87.23)
9. Germany (86.89)
- ...
23. Singapore (80.01)

<https://www.kof.ethz.ch>



Singapore Economic Development Board, <http://www.edb.gov.sg/>



#### Quality of Education 2016

1. Singapore
2. Switzerland
3. Finland
4. Qatar
5. Belgium
6. Netherlands
7. Canada
8. New Zealand
- ...
20. Germany

<http://reports.weforum.org>

#### Innovation 2018

1. Switzerland
2. Netherlands
3. Sweden
4. United Kingdom
5. Singapore
6. United States
7. Finland
8. Denmark
9. Germany
10. Ireland

<http://https://www.wipo.int>

#### Technology Readiness 2016-2018

1. Singapore
2. Finland
3. Sweden
4. Norway
5. United States
6. Netherlands
7. Switzerland
8. United Kingdom
9. Luxembourg
10. Japan
- ...

15. Germany

<http://reports.weforum.org>

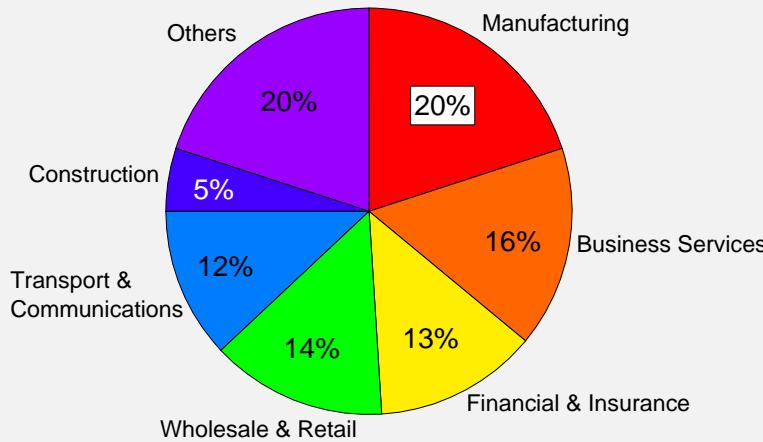
#### Livable cities 2018

1. Vienna (Austria)
2. Melbourne (Australia)
3. Osaka (Japan)
4. Calgary (Canada)
5. Sydney (Australia)
6. Vancouver (Canada)
- ...
25. Munich
- ...
37. Singapore

<https://www.businessinsider.de>

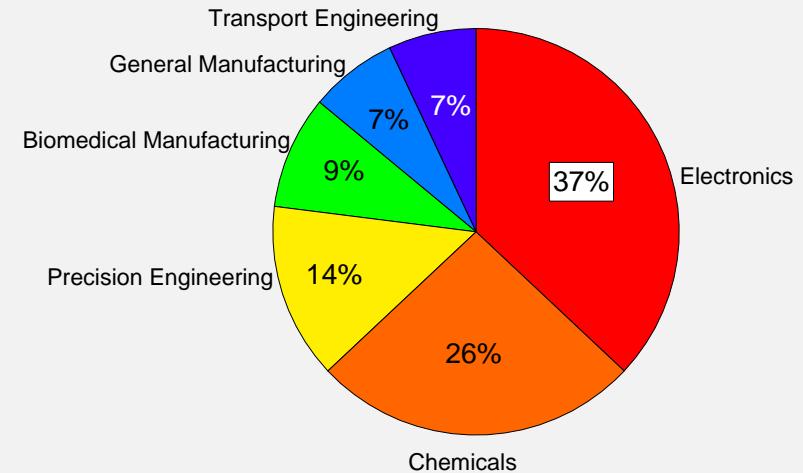
Manufacturing is the largest contributor to Singapore's GDP

Singapore's 2017 GDP: S\$447 bil



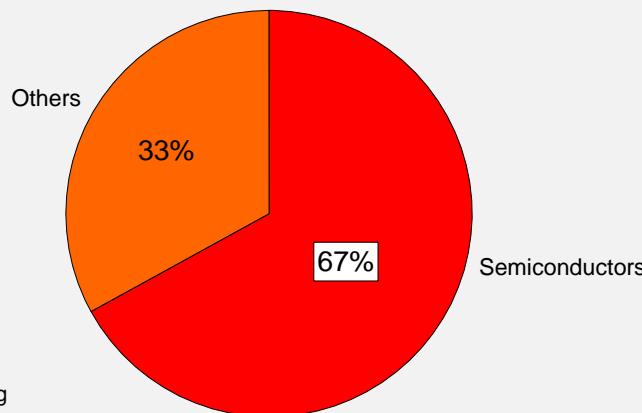
Electronics is the largest segment in manufacturing

2017 Manufacturing Output: S\$322 bil



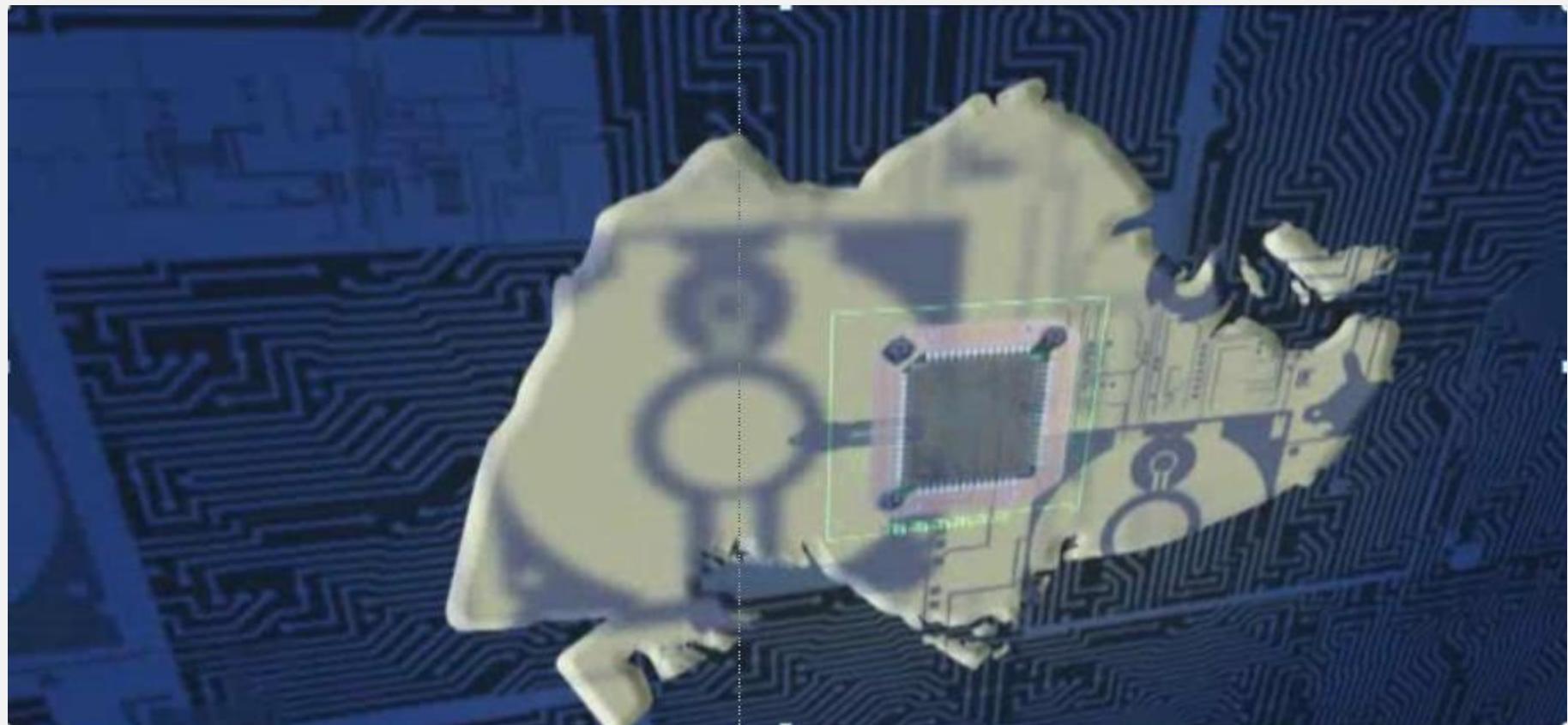
Semiconductors is the largest segment in electronics

2017 Electronics Manufacturing Output: S\$118 bil



A total of 68,000 people were employed in the electronics sector in 2017. That is about 17% of the total manufacturing workforce.

In 2017 Semiconductor industry had a growth rate of 48%.



# Singapore: a leading semiconductor hub

# Singapore is a leading semiconductor hub in the world

**Singapore ranked #2 city worldwide in terms of wafer capacity by Strategic Marketing Associates**

*Source: Solid State Technology (Dec 2006)*

10% global market share for semiconductor foundry wafer output

Home to the world's top 3 wafer foundry companies

Home to the world's top 3 sub-contract assembly-and-test companies

Home to 4 of the world's top 10 fabless IC design companies

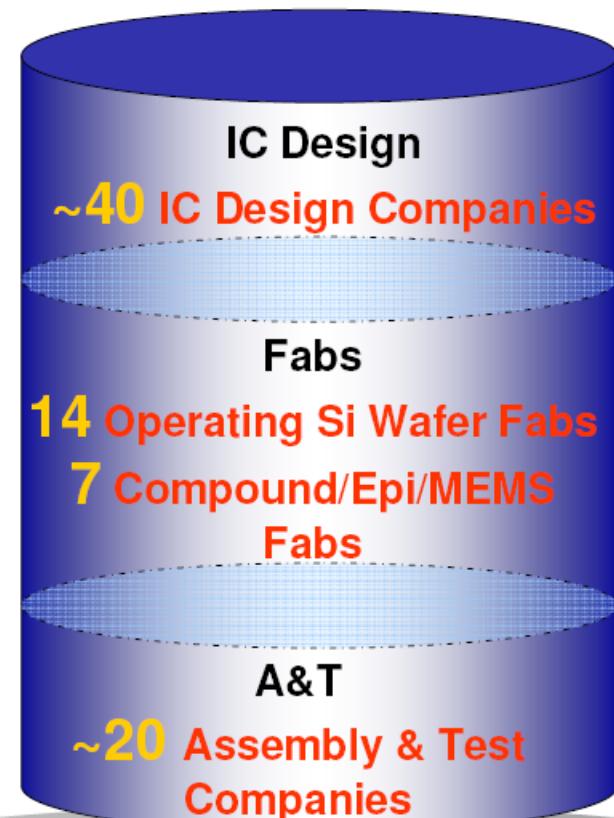
[www.sedb.com](http://www.sedb.com)



# A Vibrant Semiconductor Ecosystem

**Supporting Industry**  
(>300 companies)

- EDA tools
- Wafer substrates
- Equipment
- Photomask
- Gases & chemicals
- Facilities



**Research Institutes**

- IME
- IMRE
- I2R

**Universities**

- NTU
- NTU-TUM
- NUS
- 
- MIDAS

OEMs, EMS, End-System Companies  
IT Equipment, Communications, Consumer Electronics  
Medical, Automotives, Industrial

**EDB**  
SINGAPORE

[www.sedb.com](http://www.sedb.com)

**Recent wafer fab investments**

**IM Flash Technologies**  
12" NAND Flash Fab (Nov 06)

Cutting-edge chips to be made in new \$4.7b plant

Source: The Straits Times, 8 November 2006

Philips to open power LED plant here

**Philips Lumileds**

New Power LED manufacturing plant (Sep 06)



**Soitec**

12" SOI wafer production facility (Jul 06)  
Source: The Business Times, Weekend Edition, July 8-9, 2006

Wafer maker to invest US\$446m in S'pore plant

**Recent assembly & test investments**

**Panasonic Semiconductor**  
New A&T plant (Feb 06)



Panasonic invests \$150m in new plant

Source: The Straits Times, 8 Feb 2006

**Amkor Technology**  
New wafer bumping plant and test expansion (Feb 06)

Source: The Business Times, 27 Feb 2006

UTAC will invest \$500m to expand Singapore operations  
**UTAC**  
New A&T plant (Apr 06)

Source: The Straits Times, 20 Apr 2006

NEC's upgrade of S'pore operations to add 200 jobs



**NEC Electronics**  
Assembly and test expansion (Aug 06)

Source: The Straits Times, 5 August 2006

**Recent IC design investments**

**Xilinx puts up R&D team in Singapore**

**Xilinx Asia Pacific** Source: Electronic Engineering Times, 15 Jan 2007  
New R&D team for IC design (Jan 07)



**Solomon Systech**  
Expansion of R&D team (Jun 06)

**HK chip firm grows S'pore R&D ops**

Source: The Business Times, 19 June 2006

Panasonic to hire 220 and invest \$10m more in S'pore

Source: The Business Times, 11 April 2006

**Panasonic Semiconductor**  
Tripling of IC design team (Apr 06)

**Recent supporting industry investments**

**Samsung and Siltronic**  
12" silicon wafer plant (Jul 06)

\$1.6b silicon wafer plant to be built here

Source: The Straits Times, 15 July 2006

US chipmaking equipment firm opens factory here  
**KLA-Tencor**  
Company's 1<sup>st</sup> Asian wafer fab equipment assembly plant (Aug 06)

National Oxygen expands with \$70m plant

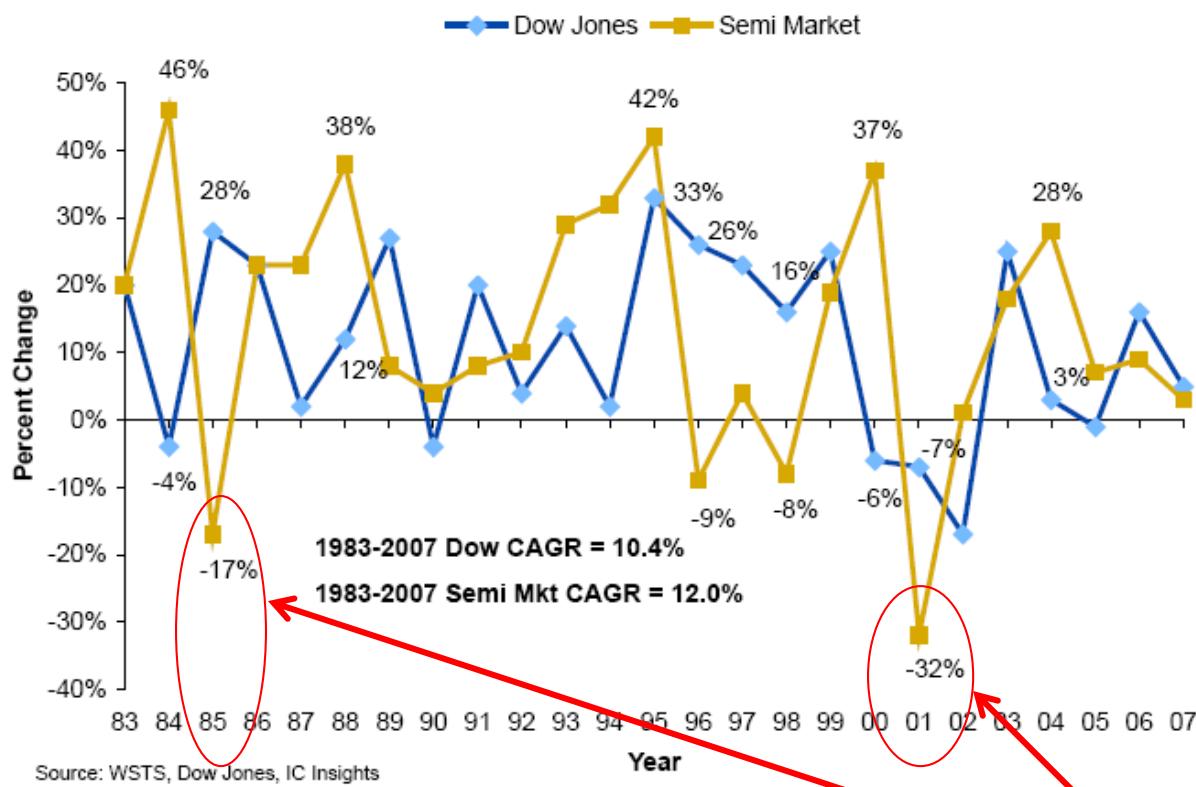
**National Oxygen Pte Ltd**  
3<sup>rd</sup> air separation plant for industrial/specialty gases (May 06)

Source: The Business Times, 26 May 2006

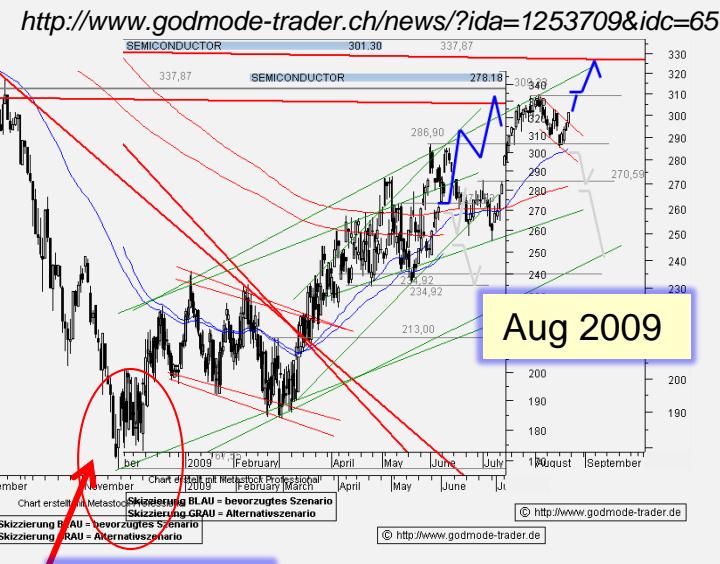
Starting around year 2000 Singapore was investing a lot of money to attract industry to Singapore

Billion dollars companies invested in Singapore

## Semiconductor Market Growth vs. Dow Jones Growth



## Semiconductor Index SOX



Dec 2008

## Global financial crisis in 2008



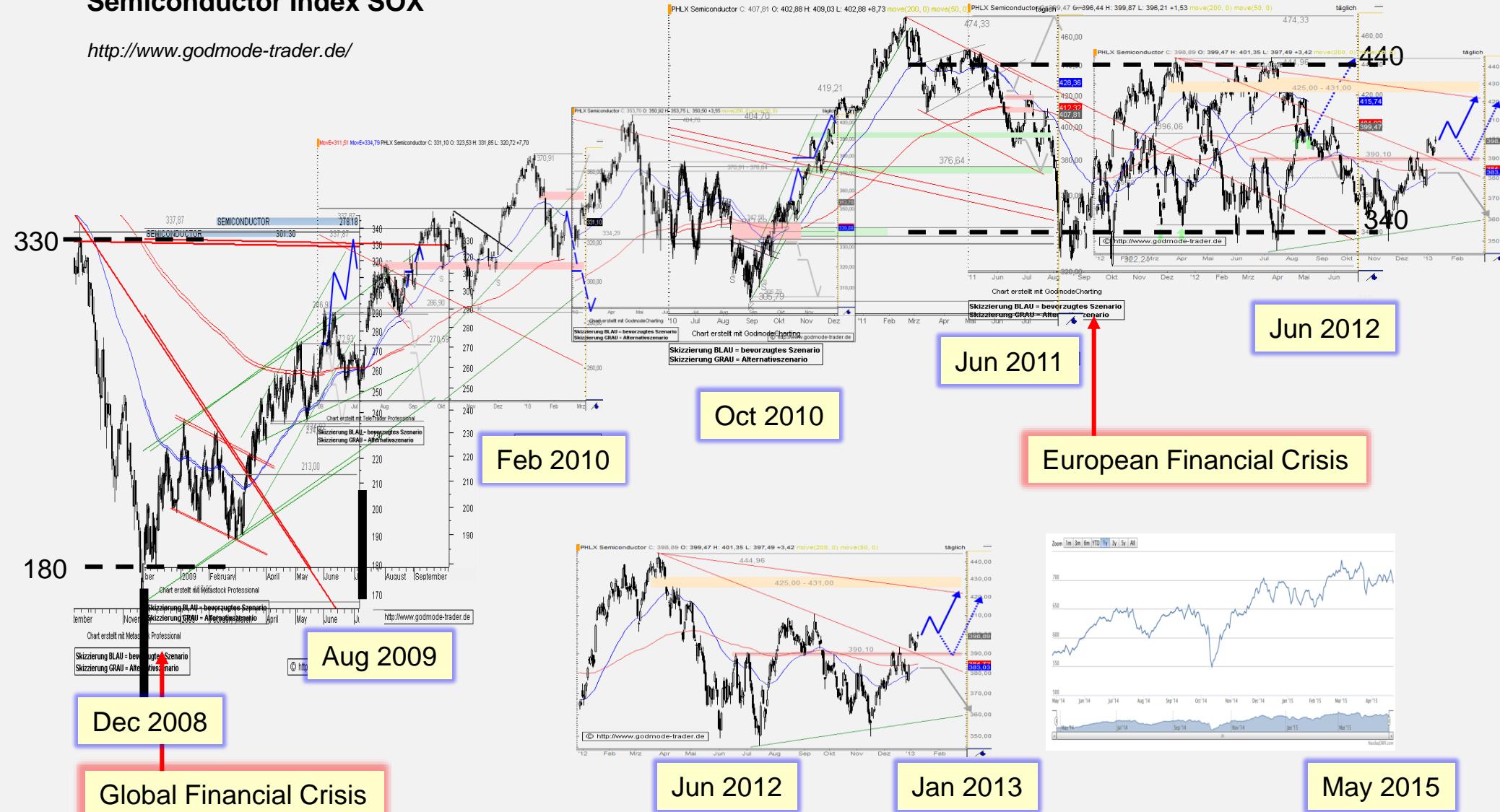
Depending on global economical prosperity always "ups" and "downs" exist

# What about Global Semiconductors ?

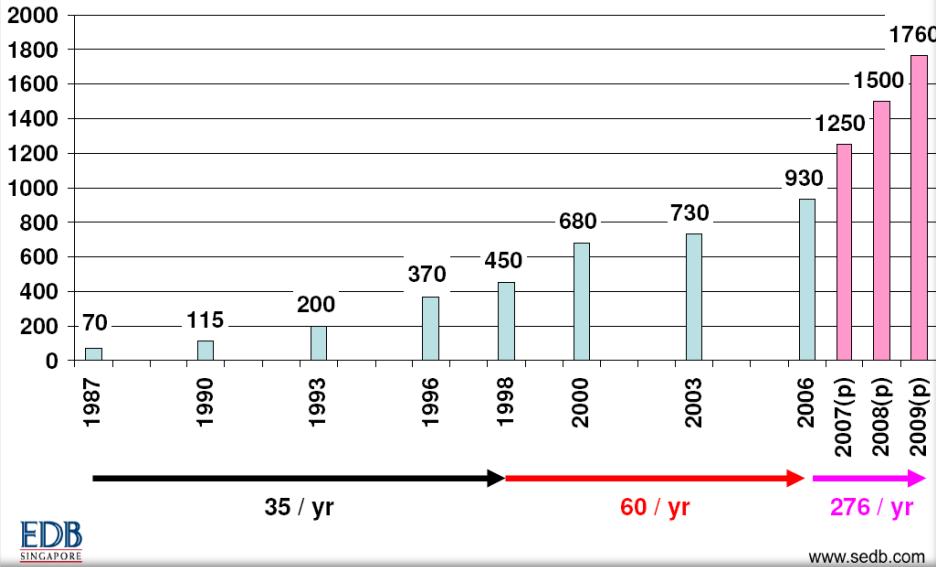
## Global Rise since 2008

### Semiconductor Index SOX

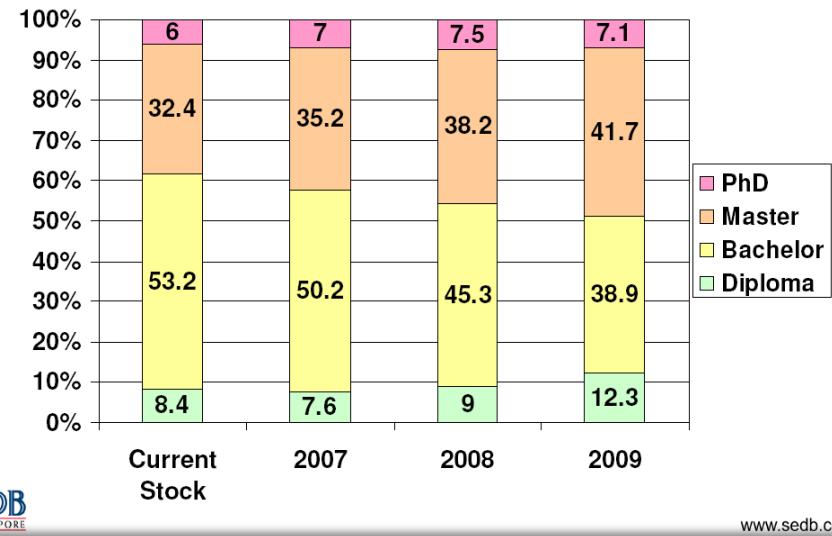
<http://www.godmode-trader.de/>



## Number of Design Engineers in Singapore



## Design Engineer Demand Projection by Qualification



### EDB Pumps S\$16 million to train 150 integrated circuit designers over 5 years

The Singapore Economic Development Board (EDB) is investing S\$16 million into a new initiative to encourage postgraduate students to specialize in integrated circuit (IC) design. The Integrated Circuit Design Postgraduate Scholarship (ICPS) aims to train...

June 29, 2009



## GLOBALFOUNDRIES Finalizes Integration, Emerges as World's First Truly Global Foundry

*GLOBALFOUNDRIES and Chartered combine under one brand to compete for market leadership as a full-service foundry company*

**Sunnyvale, Calif. - January 13, 2010** - GLOBALFOUNDRIES today announced it has officially integrated operations with Chartered Semiconductor Manufacturing started functioning as one company under the GLOBALFOUNDRIES brand. The announcement marks the emergence of the new GLOBALFOUNDRIES-the world's first full-service semiconductor foundry with a truly global manufacturing and technology footprint across Asia, Europe and the United States.

"As the world's leading chip design companies face increasing pressure to push the boundaries of innovation, they need a full-service foundry partner with the ability to invest and sustain an aggressive leading-edge technology roadmap while offering a full breadth of services," said Doug Grose, chief executive officer of GLOBALFOUNDRIES. "Thanks to the vision of our investors and months of dedicated work by teams across the globe, we have now created a new global company that leads the foundry market in advanced technology with unparalleled proximity to our customers and access to the world's best talent."

**The combined company employs approximately 10,000 people around the world**, anchored by headquarters in Silicon Valley and **advanced manufacturing operations in Singapore; Dresden, Germany**; and a new leading-edge fab under construction in Saratoga County, New York. **These sites are supported by a global network of R&D, design enablement, and customer support in Singapore, China, Taiwan, Japan, the United States, Germany, and the United Kingdom.**

The new GLOBALFOUNDRIES immediately takes its position as one of the top semiconductor foundries in the world, with 2009 revenues to date for GLOBALFOUNDRIES and Chartered in excess of \$2 billion. GLOBALFOUNDRIES launches with more than 150 customers across the semiconductor ecosystem, with plans to deepen existing relationships and to aggressively pursue new customers. Current customers include many of the world's top fabless and fab-lite companies, such as AMD, Qualcomm, STMicro and IBM.

....  
**GLOBALFOUNDRIES currently has five 200 mm fabs and one 300 mm fab in Singapore**, as well as one leading-edge 300 mm fab complex in Dresden, Germany. To meet the demands of a growing customer base, the company has an aggressive capacity build-out plan, including expansion of Fab 1 in Dresden and Fab 7 in Singapore, as well as construction of a new leading-edge 300mm facility in Saratoga County, New York. The New York facility, which will be renamed as Fab 8, is on track to begin ramping initial production in 2012.

With these plans in place, global leading-edge capacity is expected to expand to 1.6 million 300mm wafers annually by 2014. This will be supplemented by 2.2 million 200mm wafers annually, offering customers the full spectrum of foundry technology from mainstream to the leading edge, for a total of 5.8 million 200mm equivalents.

.....  
The new GLOBALFOUNDRIES brings a broad array of leading edge technology capabilities and services to market. The company is the foundry industry leader in time-to-volume on 40/45nm technology and expects to repeat this accomplishment with 32nm and "Gate First" High-K Metal Gate technology. The company embraces a collaborative R&D approach that also extends to packaging, IP solutions, and design enablement, built on what the company calls its "Virtual IDM" approach.

For more information on GLOBALFOUNDRIES, visit [www.globalfoundries.com](http://www.globalfoundries.com)

Singapore expects strong growth in wafer fabrication capacity this year

Last Updated(Beijing Time):2011-01-27 13:23

**Singapore's capacity for 300 mm wafer fabrication**, the cutting-edge star of the semiconductor industry, is **expected to grow 26 percent this year**, according to a latest industry report. This is in comparison with the forecast of 14 percent growth in the global capacity made by SEMI, the global semiconductor industry body.

**Singapore contributed 11.2 percent of global semiconductor output in 2009**, according to the SEMI. Local daily the Business Times said Thursday Singapore currently has 14 silicon wafer fabrication plants, 20 assembly and test operations and about 40 integrated circuit design centers. Out of this, Singapore is home to four 300 mm wafer plants.

**The world's top three wafer foundry companies have operations in Singapore**, as do **three of the world's top five assembly and test subcontractor companies** and **nine of the world's top ten fabless IC design companies**.

Source:Xinhuanet

The screenshot shows the official website of the Prime Minister's Office of Singapore. At the top, there is the Singapore Government logo with the tagline "Integrity • Service • Excellence". Below it, a search bar and navigation links for "Contact Info", "Feedback", and "Sitemap" are visible. The main menu includes "Home", "About PMO", "About Government", "Media Centre" (which is highlighted in red), and "PM @ Work". The breadcrumb navigation indicates the user is on the "Speeches and Interviews > Prime Minister" page.

**SPEECH BY PRIME MINISTER LEE HSIEH LOONG AT OPENING OF IM FLASH SINGAPORE'S NAND FLASH WAFER FAB, 21 APRIL 2011 AT IM FLASH SINGAPORE**

Mr Steve Appleton, Chairman and CEO of Micron Technology  
Mr David Baglee, Vice President of Technology and Manufacturing Group, Intel Corporation  
Distinguished guests  
Ladies and Gentlemen

**1.** Congratulate Intel and Micron on the grand opening of this NAND flash wafer fab

- Marks a new milestone for the semiconductor industry in Singapore
- At US\$3 billion, this is one of the largest investments in Singapore, and will bring significant spinoffs to supporting industries

**2.** New wafer fab is state of the art

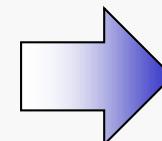
- Singapore's first 300 millimetre NAND facility
- Manufactures NAND flash memory chips using the 25 nanometre process technology
  - Most advanced volume production process for semiconductor and memory chips today
- Such leading edge capabilities will strengthen our semiconductor industry
- This is important for two reasons - good growth and good jobs

**Recent News**

22 AUGUST 2011  
PM: Singapore too small for political paralysis

22 AUGUST 2011  
Spore too small to afford gridlock: PM

17 AUGUST 2011  
Govt will work with whoever's elected: PM



## **Micron buying Intel's stake in two IM Flash fabs Dylan McGrath**

**2/28/2012 11:46 AM EST**

SAN FRANCISCO—Micron Technology Inc. will acquire Intel Corp.'s stake in two IM Flash Technologies LLC fabs operated by the two companies for about \$600 million, the companies said Tuesday (Feb. 28). Micron takes over Intel's stake in the 300-mm IM Flash Singapore fab in Singapore



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Search

Newsroom > DPM Tharman Shanmugaratnam at the opening of the Micron Fab 10 Expansion

## DPM Tharman Shanmugaratnam at the opening of the Micron Fab 10 Expansion



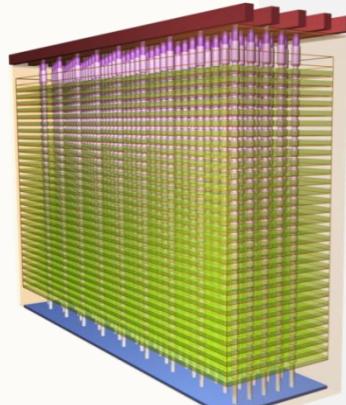
[PRINT](#) [TEXT SIZE](#)

SPEECH BY DPM THARMAN SHANMUGARATNAM AT THE OPENING OF THE MICRON FAB 10 EXPANSION ON MONDAY, 26 SEPTEMBER 2016 AT 1 NORTH COAST DRIVE, NORTH COAST INDUSTRIAL PARK, SINGAPORE 757432

Mr. Mark Durcan, CEO, Micron Technology Inc.,  
Mr Wayne Allan, VP Global Manufacturing, Micron Technology, Inc.,  
Mr Lee Kok Choy, Country Manager, Micron Technology, Inc.,  
Distinguished Guests,  
Ladies and Gentlemen,

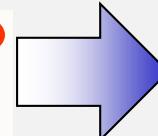
### Opening

It is a real pleasure for me to be here with all of you as we celebrate the opening of the Micron Fab 10 Expansion.



<https://www.micron.com/products/solid-state-storage/3d-nand-client-ssds>

Micron's Fab 10 expansion will produce the company's latest 3D NAND flash memory chips. This also makes Singapore Micron's largest and most advanced NAND wafer fab location in the world.



Working principle of a 3D-NAND will be explained in chapter 6.9

Building for the Future with the Power of 3D NAND

*Micron Opens Fab 10 Expanded Singapore NAND Flash Memory Fabrication Facility*

Corporate Communication

September 29, 2016

Memory Blog



Aerial Shot of Micron Fab 10 Expanded Facility

# Micron's new plant to provide 1,000 jobs

<http://www.straitstimes.com/business/companies-markets/microns-new-plant-to-provide-1000-jobs>

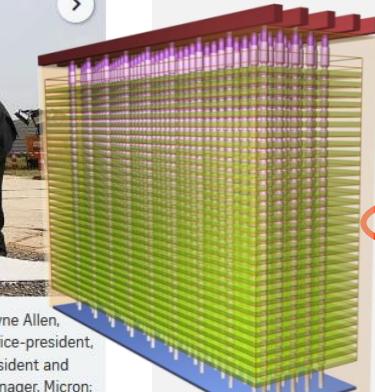


1 of 3

Doing the honours at Micron's ground-breaking ceremony in North Coast yesterday were (from left) Mr Wayne Allen, senior vice-president, global manufacturing, Micron; Mr Ng Lang, CEO of JTC; Mr Manish Bhatia, executive vice-president, global operations, Micron; Mr S. Iswaran, Minister for Trade and Industry (Industry); Mr Sanjay Mehrotra, president and CEO, Micron; Dr Beh Swan Gin, EDB chairman; Mr Chen Kok Siang, vice-president and Singapore country manager, Micron; and Mr Gursharan Singh, senior vice-president, backend operations, Micron. ST PHOTO: TIMOTHY DAVID

PUBLISHED APR 5, 2018, 5:00 AM SGT

The new semiconductor production facility represents the third phase of Micron's Fab 10 expansion and will be located adjacent to the existing complexes. The new plant will be built on a 165,000 m<sup>2</sup> land plot at North Coast Drive. The new Fab is expected to be completed sometimes in the middle of 2019. Micron plans to get the first wafers from the new fab sometimes in Q4 2019. The ramp up of the facility is going to take several quarters, so expect significant volumes of 3D NAND memory to come out of the new fab towards the end of calendar 2020.



<https://www.micron.com/products/solid-state-storage/3d-nand-client-ssds>

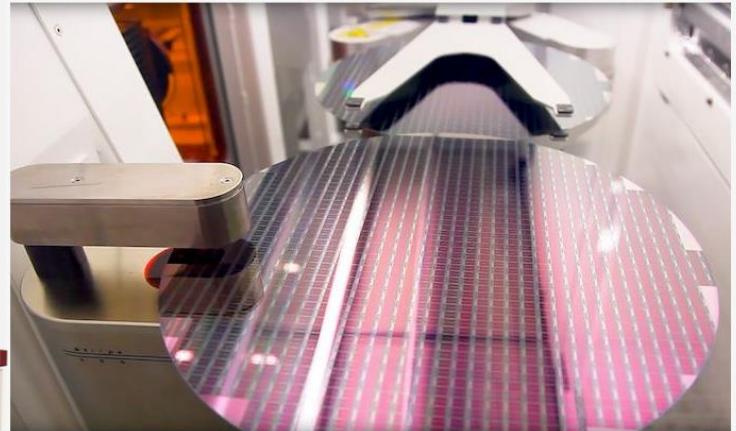
Micron's Fab 10 Expansion Completed: 96-Layer 3D NAND Production Starts in 2019

by Anton Shilov on August 16, 2019 4:30 PM EST

Posted in SSDs | Memory | Micron | NAND | 3D NAND

21  
Comments

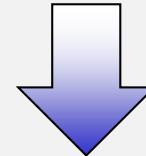
+ Add A Comment



Micron this week hosted a grand opening ceremony of its Fab 10 Expansion in Singapore. The new cleanroom is not expected to increase the company's production capacity in terms of wafer starts per month, but will enable Micron to continue adopting more advanced 3D NAND process technologies with a higher number of layers and bit density.

The new [Singapore Fab 10 Expansion](#) is an integral part of Micron's Fab 10 complex that was previously comprised of Fab 10N and Fab 10X. Officially, it's known that the new 3D NAND production facility is built on a 165,000 m<sup>2</sup> land plot, however Micron is not disclosing much else about the usable cleanroom space or other features of the expansion.

<https://www.anandtech.com/show/14743/microns-fab-10-expansion-completed-96-layer-nand-in-2019>



Working principle of a 3D-NAND will be explained in chapter 6.9

# SEMICON SEA 2020 Prospectus



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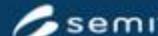
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**\$207.1 billion** – Estimated value of the Asia-Pacific chip market in 2016, down 22.7% year-over-year (YoY). – *Gartner*

## INDIA

**\$9.66 billion** – Value of India's semiconductor market in 2015. Overall consumption of semiconductors is expected to grow from \$6.1 billion in 2011 to \$9.66 billion in 2015.

**\$43.1 billion** – Revenue of India's semiconductor design segment in 2015

**7.6%** – India's forecasted gross domestic product (GDP) growth rate in 2015-2016.

## CHINA

**71.4 billion** – Number of semiconductors produced in China in 2016, accounting for 32.0% of the country's chip consumption.

**10.5%** – YoY percentage growth of IC demand in China in 2015

**6.7%** – China's forecasted gross domestic product (GDP) growth rate in 2015-2016.

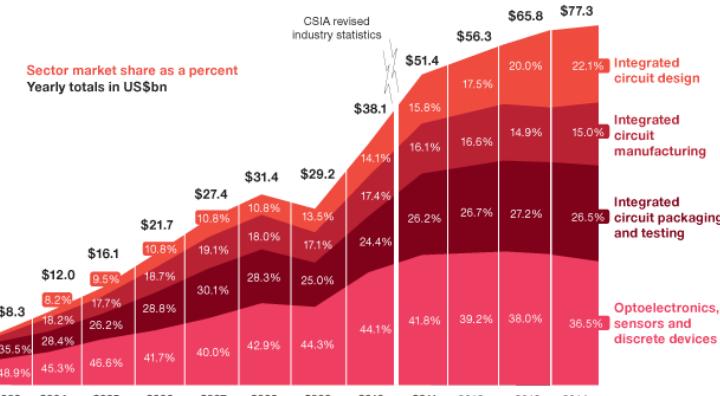


Please use keywords like "semiconductor", "market", ... to find economic data and news

## China semiconductor revenue forecast by major application market (\$US millions)

**China's semiconductor industry by sector**

2003-2014



For more information, please visit:  
[www.pwc.com/chinasemicon](http://www.pwc.com/chinasemicon)

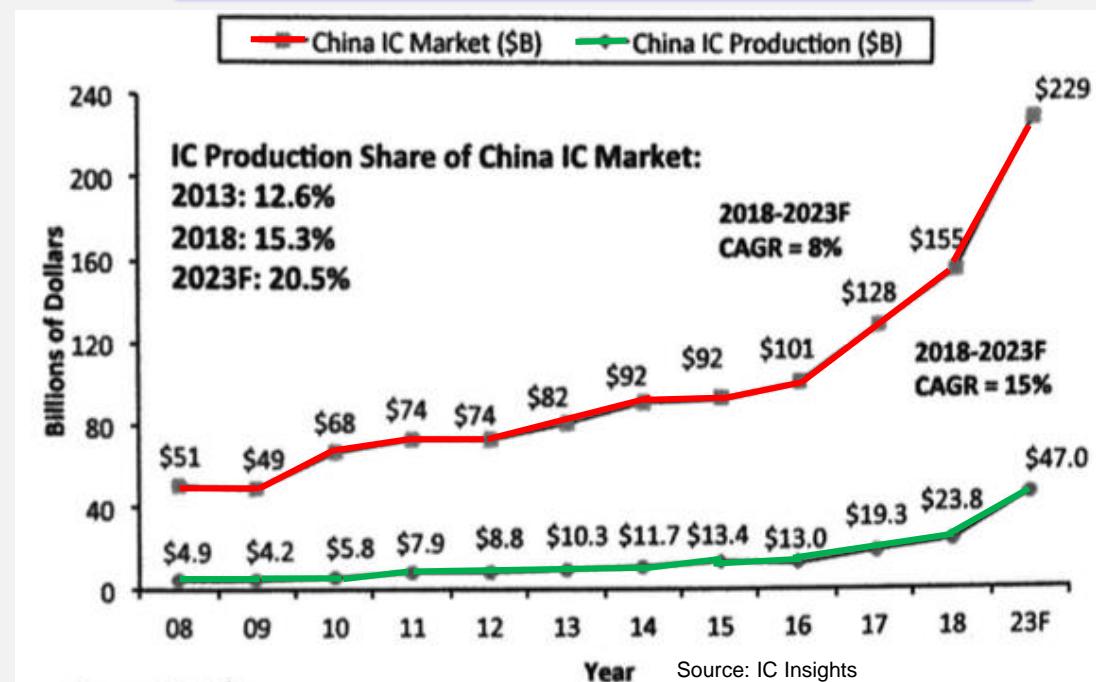
Revenue means value of semiconductor chips, which are sold in China



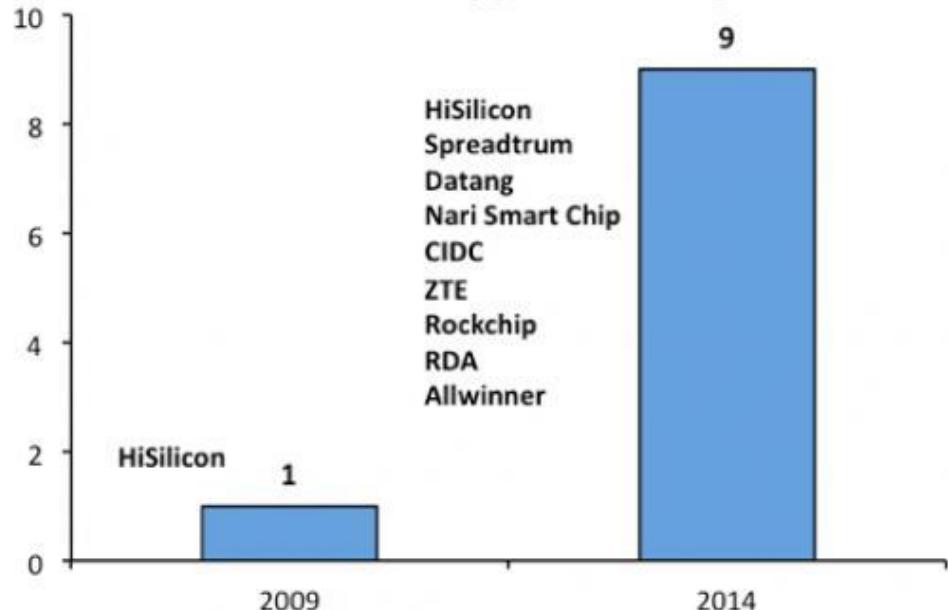
But China is fabricating only 30% of its consumption



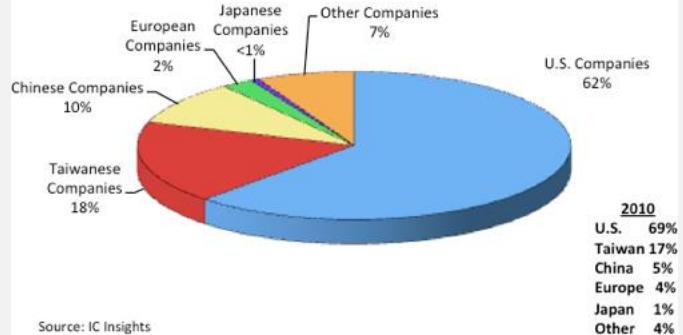
This makes China dependent on foreign markets



## Chinese Companies in the Top 50 Fabless IC Supplier Ranking



**2015 Fabless Company IC Sales by Company Headquarters Location (\$84.2B)**



New IC course for China and its Fabless! »

Monday 12th January 2015

China's ambitious late-1990s plan to create numerous high-volume indigenous IC manufacturers in the pure-play foundry segment did not come to fruition, but the Chinese government is still very serious about keeping China and Chinese IC suppliers relevant in the future IC industry.

In 2014, the Chinese government described new semiconductor industry programs that will utilize investment by both the Chinese national government (\$19.5 billion) and local government and private equity investors (\$97.4 billion). IC Insights believes that these outlays have the potential to significantly change the future IC supplier landscape.

As Chinese IC design houses continue to advance, IC Insights expects an increasing number of China-headquartered companies to move up in the ranking of top fabless IC suppliers. As shown in figure there were nine Chinese companies among the top-50 fabless companies in 2014 as compared to only one company in 2009.

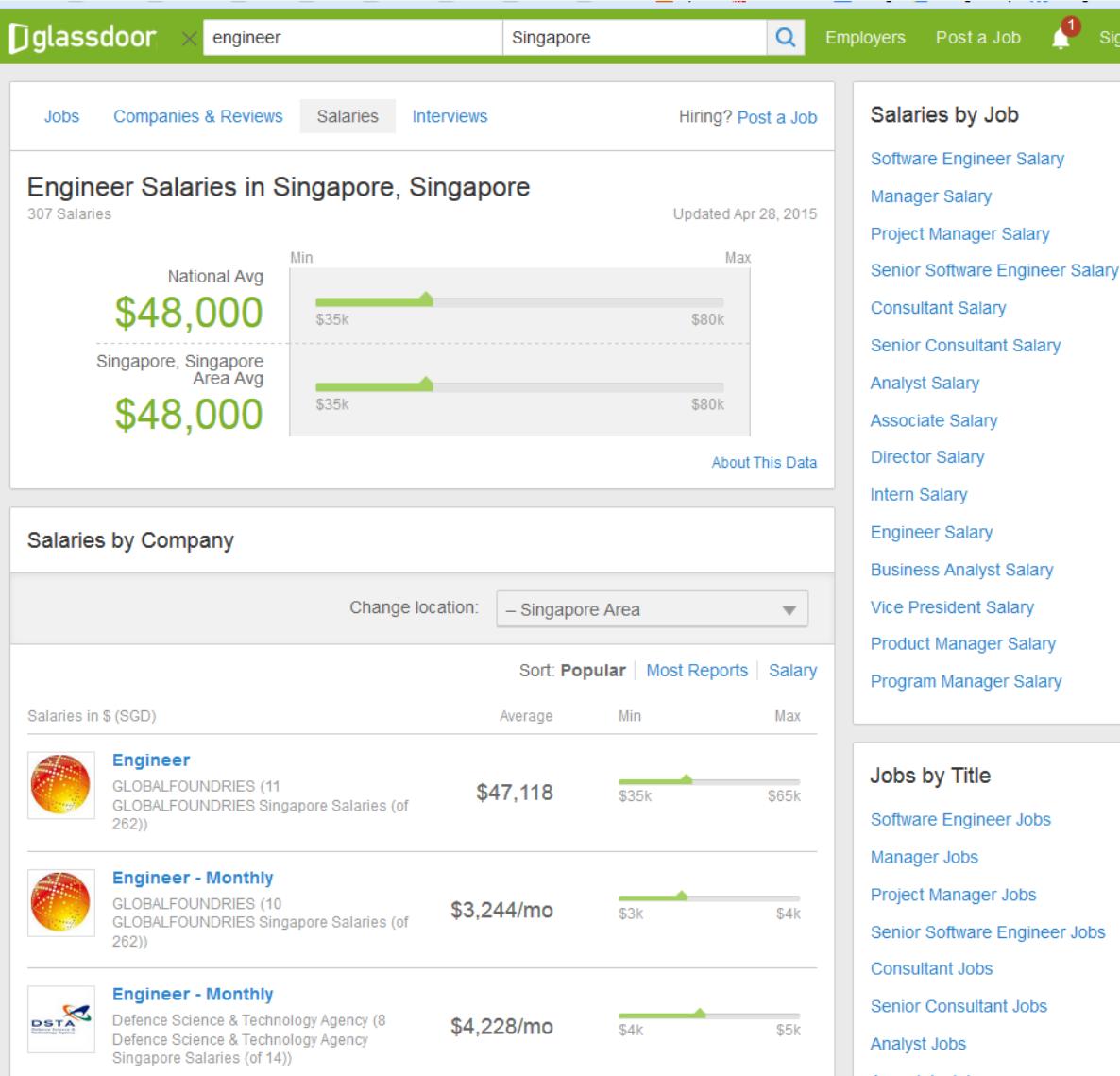
In total, the Chinese fabless IC suppliers held 8% of the top 50 fabless IC market (\$80.5 billion) in 2014 and currently hold twice as much top 50 fabless IC marketshare as the European and Japanese companies combined! Nineteen U.S. companies were represented among the top 50 fabless suppliers in 2014, and they accounted for 64% of the total top 50 fabless company IC sales. In 2014, Japan held less than 1% and the "other" countries (e.g., South Korea, Singapore, etc.) represented only 6% of the market held by the top 50 fabless IC suppliers.

Although its original plan of establishing numerous large indigenous IC manufacturers in China was not successful, it is obvious that the Chinese government still intends to create a dynamic environment in the China-based IC industry, including placing additional emphasis on establishing new fabless IC suppliers. IC Insights believes that the Chinese government's commitment to creating a more powerful Chinese presence in the future IC industry is alive and well and should be taken seriously.

## 0. Overview

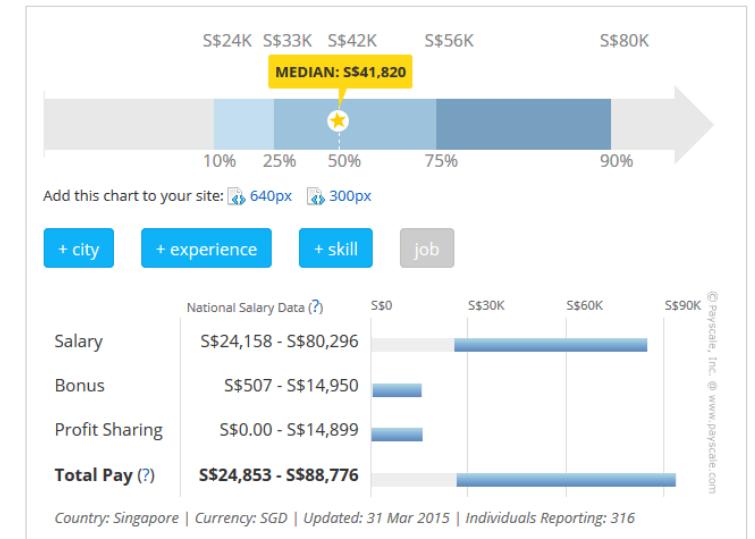
### 0.3 Remarks on Singapore

# What Income you can expect in Singapore ?



### Electrical Engineer Salary (Singapore)

The average pay for an Electrical Engineer is S\$41,821 per year. People in this job generally don't have more than 20 years' experience. Experience has a moderate effect on income for this job.



### Jobs by Title

- Software Engineer Jobs
- Manager Jobs
- Project Manager Jobs
- Senior Software Engineer Jobs
- Consultant Jobs
- Senior Consultant Jobs
- Analyst Jobs
- Associate Jobs

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## Advanced MOSFETs and Novel Devices

A Look at the future Development of Industrial Semiconductor Devices

Dr.-Ing. Josef Biba



German Institute of Science and Technology  
Cooperation of  
Nanyang Technological University and Technical University Munich



[https://tum-asia.edu.sg/wp-content/uploads/TUMAsia\\_MSc\\_GreenElectronics\\_22012020.pdf](https://tum-asia.edu.sg/wp-content/uploads/TUMAsia_MSc_GreenElectronics_22012020.pdf)

July	Year 1	Year 2	Graduation
Arrival in Singapore	<ul style="list-style-type: none"><li>Laboratory Modules</li><li>Core Technical Elective Modules</li><li>Specialisation Technical Elective Modules</li><li>Non-Technical Elective Modules</li></ul>	<ul style="list-style-type: none"><li>Non-Technical Elective Modules</li><li>Internship</li><li>Master Thesis at a company, university or research institute (Supervised by an NTU or TUM professor)</li></ul>	End of programme

**Specialisation Technical Elective Modules:**  
(Choose 7 modules)

**Advanced MOSFET & Novel Devices**  
Historical development of mainstream MOSFETs until today; economical, technological and physical fundamentals; properties of long channel and short channel MOSFETs; hot carrier effects; short channel effects; scaling rules; basics of charge carrier transport (quantum mechanical, hydrodynamics, ballistic); proposed new MOSFET structures (strain engineering, metal-gate, high-k, vertical MOSFETs; double gate MOSFETs); hot electron transistors; tunneling transistors; low dimensional devices; single electron transistors, single electron memories, quantum electronics.

**Green Nanotechnology**  
Energy flow in environment; Optical properties of nanomaterials; Spectral selective windows; Solar thermal collectors; Solar cells; Cooling and energy harvesting; Electrochemical energy storage.

**Nanophotovoltaics**  
Third generation photovoltaics; Quantum dot tandem cells; Hot carrier cells; Multiple electron hole pair generation; Impurity and intermediate band devices.

**Polymer Electronics**  
Fundamentals of electronic and optoelectronic devices and technologies based on polymer semiconductors; An overview of Polymer Electronics; Electronic structure and band theory; Beyond polyacetylene; Optoelectronic properties; Charge transport; Synthesis and macromolecular design; The physics of polymers; Surfaces and interfaces; Polymer transistors; Optoelectronic devices; Photovoltaic devices (organic and dye sensitized solar cells) and Polymeric memories.

**Semiconductor Power Devices**  
Fundamentals of semiconductor device physics: electronic band structure, intrinsic and extrinsic conductivity, mobility, carrier transport by drift and diffusion, carrier generation and recombination, impact ionization, pn-junction, MOS field effect; Power device structures: PIN diode, Schottky diode, bipolar junction transistor, thyristor, power MOSFET, insulated gate bipolar transistor (IGBT); Robustness and destruction mechanisms of power devices: thermal breakdown, electrical breakdown, dynamic avalanche, latch-up in IGBTs and cosmic ray induced failure.

**Lower Power Displays and Solid-State Lighting**  
Low power flexible displays; OLED displays on flexible substrates; Printing processes for information displays; Evolution of Visible-Spectrum Light Emitting Diodes; LED Design Principles; Visible-Spectrum LED; White LED; Current Topics in Solid State Lighting.

**Modern Semiconductor Devices**  
Bipolar transistor operation principles. Bipolar device modelling. State-of-the-art bipolar structures. CMOS device scaling effects. Semiconductor memories. Future trends and challenges.

**MASTER OF SCIENCE**

# Integrated Circuit Design

**At a Glance**

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- Nurturing innovators to take on the dynamic semiconductor industry
- Joint degree conferred by TUM and NTU
- Vast career prospects regionally and worldwide
- Apply online at [www.tum-asia.edu.sg](http://www.tum-asia.edu.sg)

**NANYANG TECHNOLOGICAL UNIVERSITY**

Technical University of Munich

## Specialisation Technical Elective Modules\*

(Choose 4 out of 7 modules)

### Advanced MOSFET & Novel Devices

Historical development of mainstream MOSFETs until today; economical, technological and physical fundamentals; properties

of long channel and short channel MOSFETs; hot carrier effects; short channel effects, scaling rules; basics of charge carrier transport (quantum mechanical, hydro dynamics, ballistics); proposed new MOSFET structures (strain engineering, metal-gate, high-k, vertical MOSFETs, double gate MOSFETs); hot electron transistors; tunneling transistors; low dimensional devices; single electron transistors, single electron memories, quantum electronics.

### Nano-Electronics

Low dimensional structures: quantum wells, quantum wires and quantum dots. Electronic, optical, transport properties of nanostructures. Quantum semiconductor devices. Fabrication and characterisation techniques of nanotechnology. Applications of nanostructures, nanodevices and nanosystems. The bottom-up approach to nanotechnology: introduction to molecular electronics and optoelectronics. Organic materials for

electronics: self-assembled monolayers, conducting polymers, carbon nanotubes. Circuit implementations and architectures for nanostructures: quantum cellular automata and cellular non-linear networks. Introduction to quantum computing.

### Design for Testability of VLSI

Fault Models and Testability concepts. Test Generation and Fault Simulation Algorithms. Shift-register polynomial division. Pseudo-random sequence generators. Special purpose shift-register circuits. Random pattern BIST. Build-in boundary scan structure. Limitations and other concerns of random pattern test. Test techniques for automatic test equipment.

### Embedded Systems

The lectures cover the topics: Basics of embedded processor architectures; Bus and memory architectures; Performance/Timing analysis of embedded systems; Models for real-time systems; Principles of embedded software development; Basic real-time programming language concepts (e.g. Esterel); real-time operating systems; Power management; Design space exploration.

### IC Marketing / Business Management

Trends in the IC industry: technology and manufacturing trends, demand applications and product trends. Market characteristics: the customers, business cycles, demand lead and supply lag (the bull-whip effect), IC industry, supply and value chain, stakeholders, geographical distribution of excellence centres, technology centres, design centres, fabrication centres, the disintegration of the value chain and outsourcing trends. Managing the marketing function: the sources of product ideas, the role of standards, formats,

and intellectual property. Strategic partnership, distributorship, demand forecast, matching supply with demand.

### RF IC Design

System design considerations, CMOS RF components and devices, Low-noise amplifier (LNA), Mixers, Voltagecontrolled oscillators (VCOs), RF power amplifiers, Phase-Locked Loops and Frequency Synthesizers.

### Simulation and Optimisation of Analog Circuits

Principles of circuit simulation: DC/AC/TR analysis. Basic analog optimization tasks: worst-case analysis, yield analysis, nominal design and design centring. Basic principles of optimisation: optimality conditions, line search, Nelder-Mead method, Newton approach, Conjugate Gradient approach, Quadratic Programming and Sequential Quadratic Programming. Structural analysis of analog circuits.

## Time Table for Lecture

Module:  
Advanced MOSFET & Novel Devices (TUM)- Elective

Course Code:  
NM6012

Lecturer:  
Dr Josef Biba

Total Hours:  
TUM 46

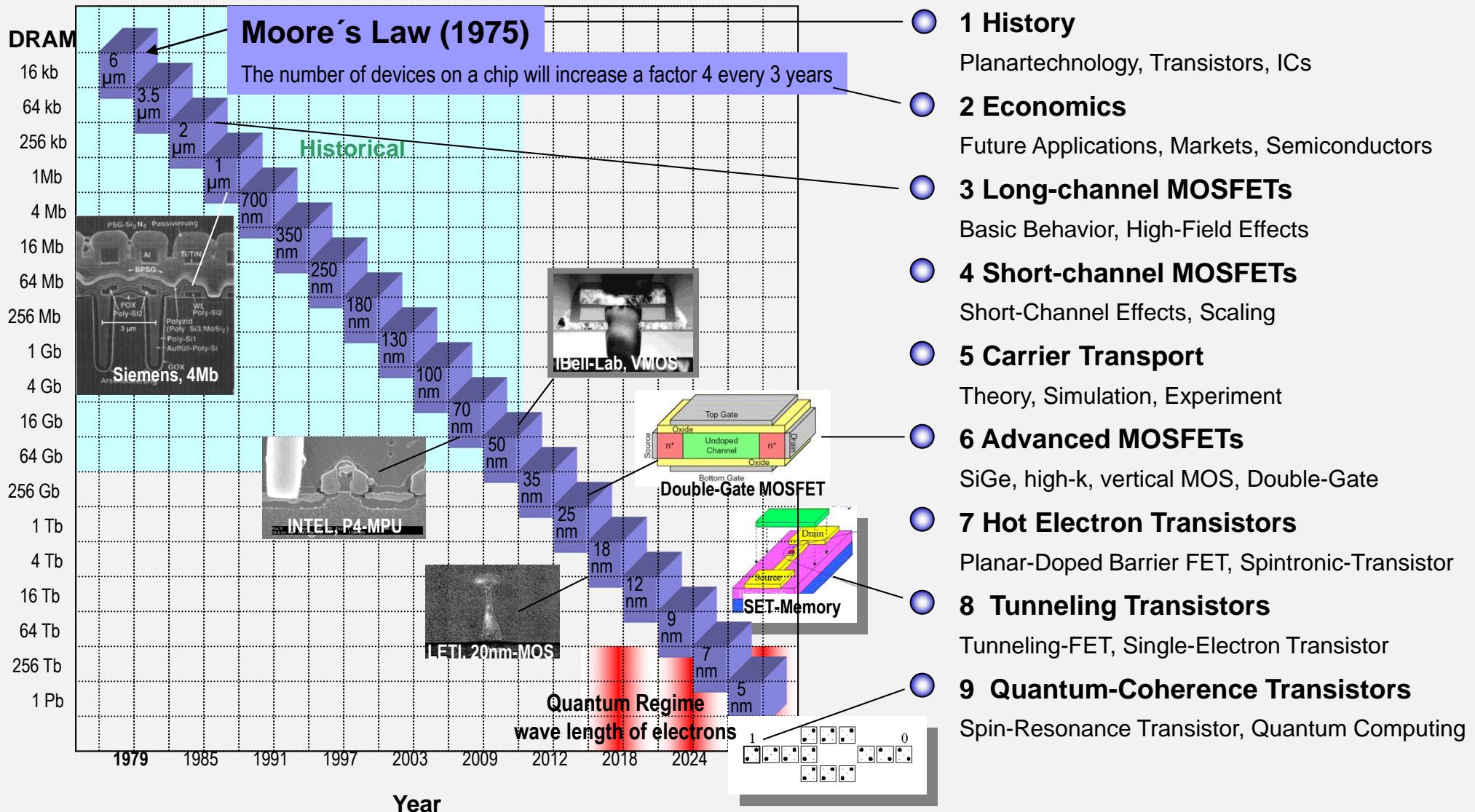
Venue:  
TUM Asia Classroom -TBA

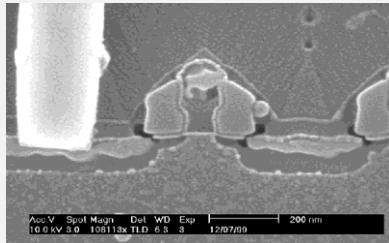
Combined with MSc. GE

Time:	13 Apr - 17 Apr 2020	Mon, 13 Apr 20	hours	Tue, 14 Apr 20	hours	Wed, 15 Apr 20	hours	Thu, 16 Apr 20	hours	Fri, 17 Apr 20	hours	Sat, 18 Apr 20	hours	
0930 - 1030														
1030-1130	0900 - 1200	3		0900 - 1200	3	0900 - 1200	3	0900 - 1200	3	0900 - 1200	3			
1130-1230	NM 6012			NM 6012		NM 6012		NM 6012		NM 6012				
1230-1330	Dr Josef Biba			Dr Josef Biba										
1330-1430														
1430-1530	1300 - 1430	1.5		1300 - 1430	1.5	1300 - 1430	1.5	1300 - 1430	1.5	1300 - 1430	1.5			
1530-1630	NM 6012			NM 6012		NM 6012		NM 6012		NM 6012				
1630-1730	Dr Josef Biba			Dr Josef Biba										
1730-1830														
1830-1930														
1930-2030														
2030-2130														
2230-2330														

Time:	20 Apr - 24 Apr 2020	Mon, 20 Apr 20	hours	Tue, 21 Apr 20	hours	Wed, 22 Apr 20	hours	Thu, 23 Apr 20	hours	Fri, 24 Apr 20	hours	Sat, 25 Apr 20	hours
0930 - 1030	0900 - 1200	3		0900 - 1200	3	0900 - 1200	3	0900 - 1200	3	0900 - 1200	3		
1030-1130	NM 6012			NM 6012		NM 6012		NM 6012		NM 6012			
1130-1230	Dr Josef Biba			Dr Josef Biba									
1230-1330													
1330-1430	1300 - 1430	1.5		1300 - 1430	1.5	1300 - 1430	1.5	1300 - 1430	1.5	1300 - 1430	1.5		
1430-1530	NM 6012			NM 6012		NM 6012		NM 6012		NM 6012			
1530-1630	Dr Josef Biba			Dr Josef Biba									
1630-1730													
1730-1830													
1830-1930													
1930-2030													
2030-2130													
2230-2330													

Time Schedule: 9.00 - 10.30 + 10.40 - 12.00 + 13.00 - 14.30



CMOS mainstream historical

active length: 130nm - 50nm

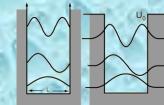
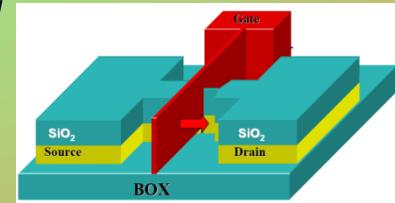
1 Historical review

2 Economics determines devices

3 Long-channel MOSFETs

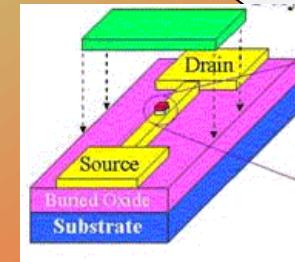
4 Short-channel MOSFETs

## 5 Transport

Advanced CMOS

50nm – 10nm

## 6 Advanced CMOS

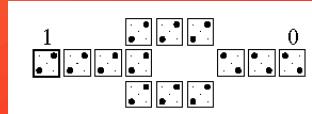
Quantum MOS

10nm – 1nm

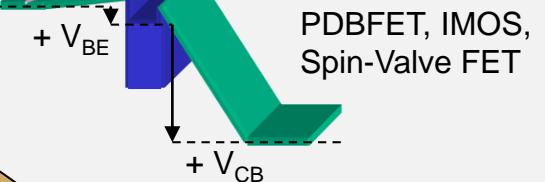
## 8 Quantum Transport Devices

## 9 Quantum Coherence Transistors

Q-bits

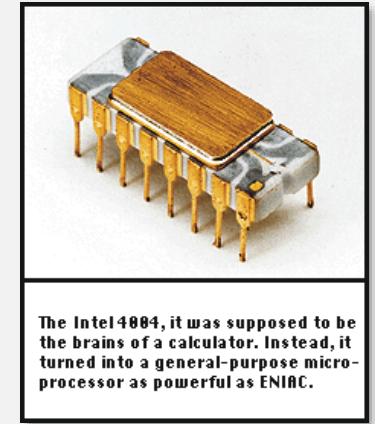
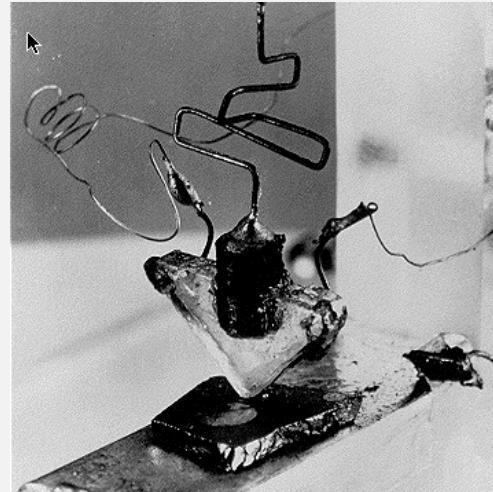


## 7 Hot Electron Transistors

PDBFET, IMOS,  
Spin-Valve FETTunneling Transistor  
Single Electron Transistor

## Chapter 1: Introduction

In this first chapter a historical, technological, physical and economical overview is given which explains the background why CMOS has developed in the past to the mainstream device technology.



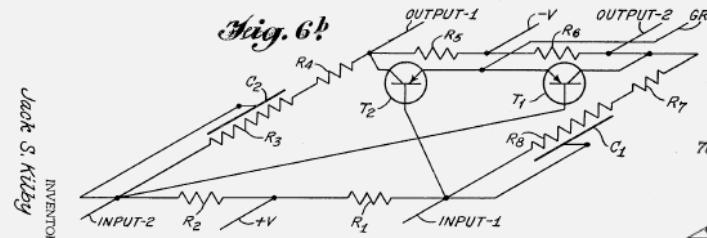
The Intel 4004, it was supposed to be the brains of a calculator. Instead, it turned into a general-purpose microprocessor as powerful as ENIAC.

# First Integrated Circuits

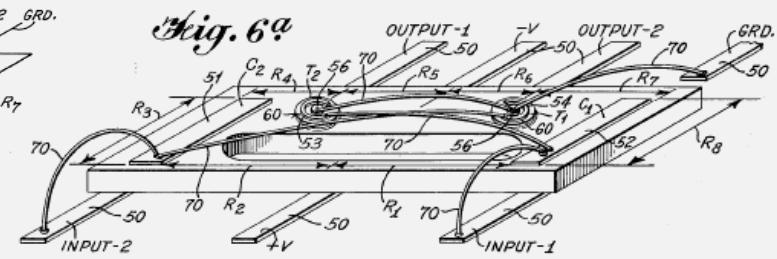


J. Kilby (TI): first IC 1958,  
patent submission Feb.1959,  
granted in 1964

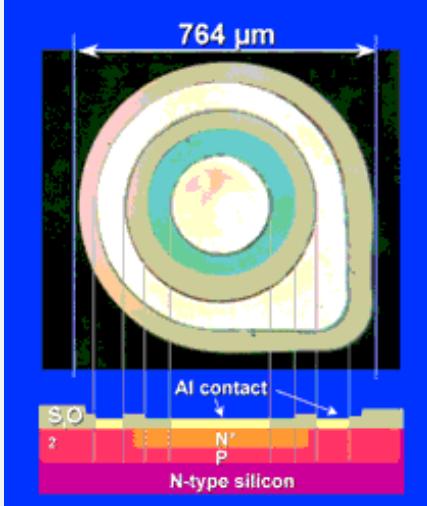
Nobel price 2000



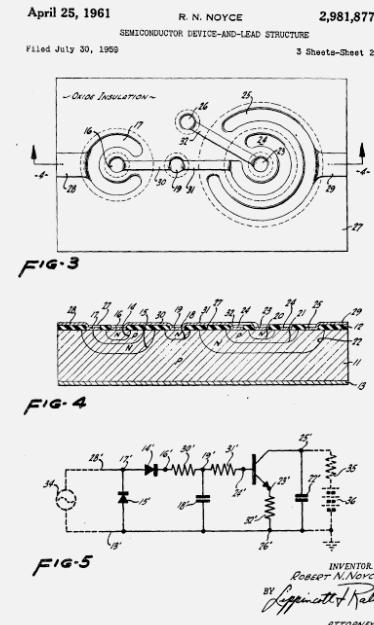
Realization of a multivibrator:  
2 transistors + 8 resistors + 2 capacitors



IC with Ge-Mesa transistors,  
but **interconnections with external wiring**



Silicon planar transistor  
**Hoerni (Fairchild) 1959**



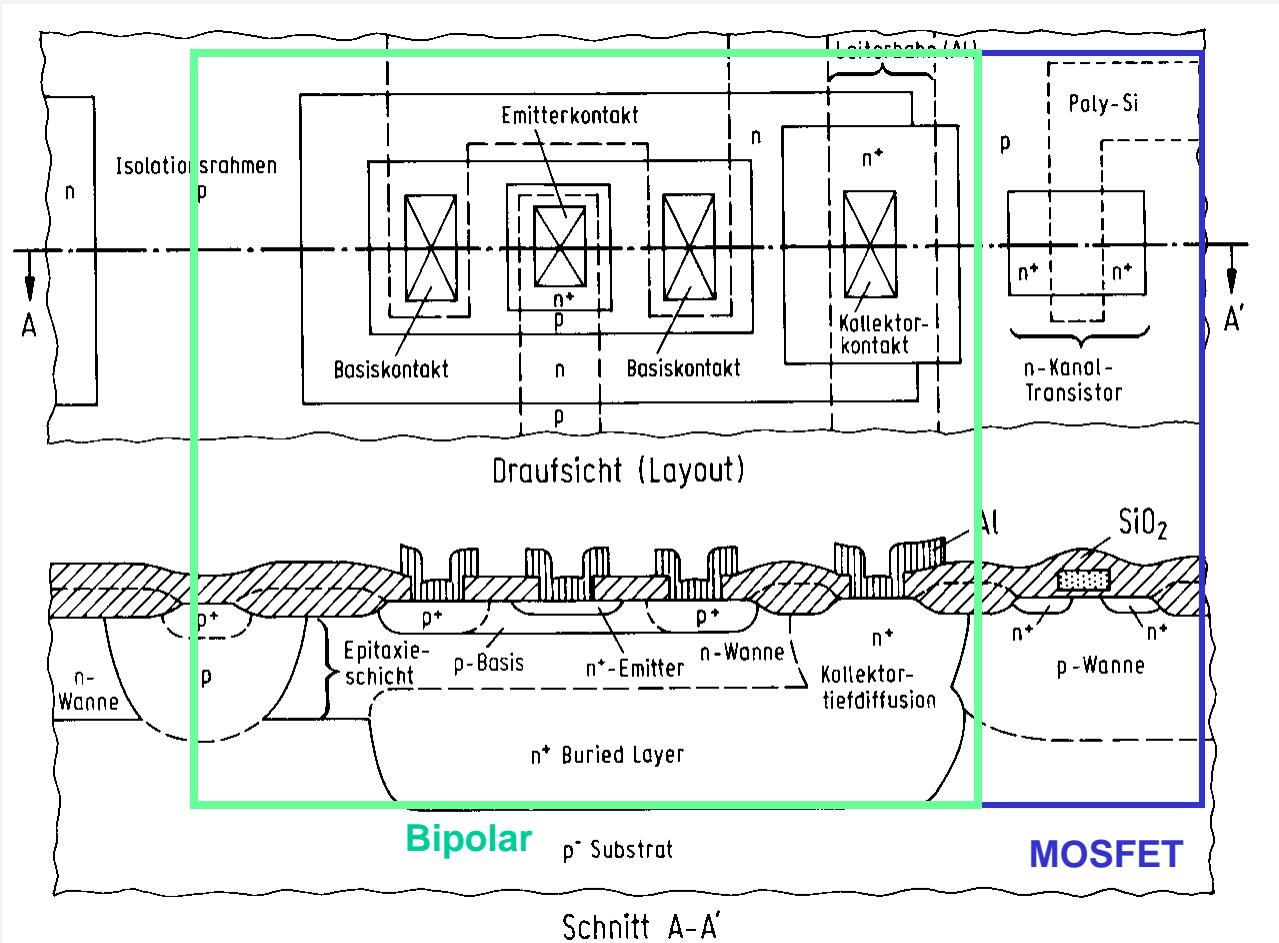
**Noyce (Fairchild):** patent submission July 1959,  
granted in 1961  
# IC with **Si planar transistors including wiring**

1961: start of IC mass production (~4'000/week)  
(logic: flip-flops, counters, NAND, XOR, ..)  
up to 1968: US space program buys 95% of IC production  
-> price decrease from 1'000 \$US / IC -> 30 \$US

1970: First DRAM (1kb, INTEL)  
1971: First microprocessor 4004 (2kb, INTEL)

...

2006-2011: daily production ~  $10^8$  ICs

**Integration means:**

many devices side by side must be switched on/off separately

-> Isolation

-> all contacts on top

**Basic device design:****Bipolar:** 6 masks

-> large area

-> expensive

-> low yield

**MOS:** 4 masks

-> smaller area

-> cheaper

-> higher yield

about 4-10 MOSFETs can be placed on the same area of one BiP using the same technology

-> scalable -> safety for shrinking

-> easy design

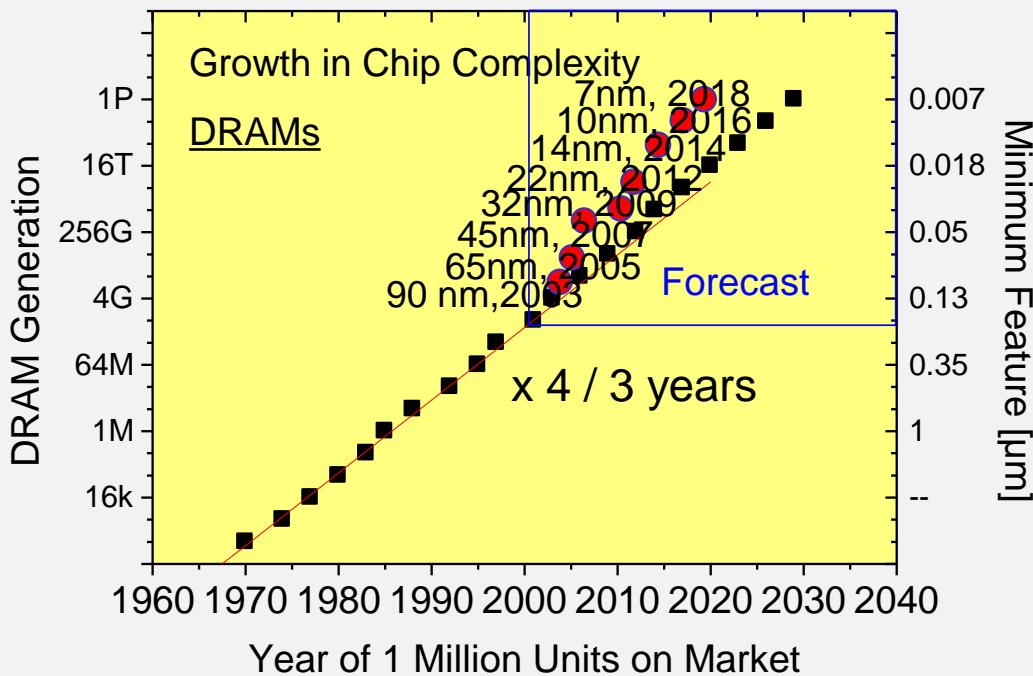


MOS is much more suitable for integration than bipolar

## Chapter 2: Economical considerations

\* 85% of all semiconductor money is earned in CMOS-technology  
 -> we will find out: why ?

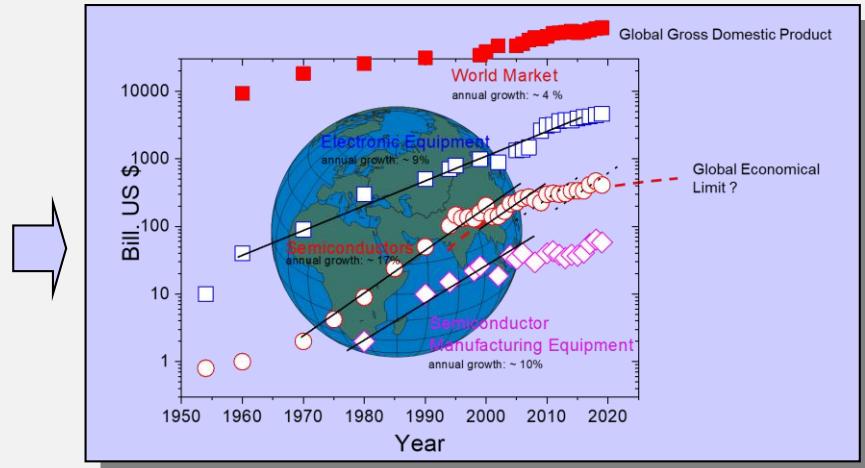
\* Fab-costs are about 20 Billion \$US, daily manufacturing costs are about 2 Mill. \$US, but DRAM selling prices are falling to 2 \$US per chip, manufacturing costs per transistor function are only  $10^{-8}$  \$ US falling 30% every year  
 -> how can semiconductor industry survive ?



1

Electronic Equipment is the world's largest market

A lot of  
**money**

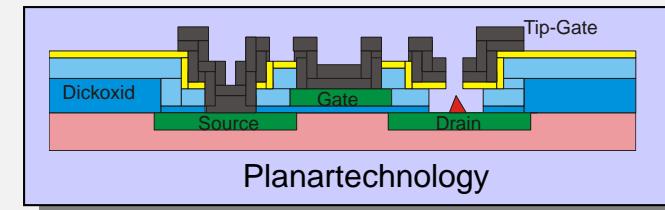


2

**Planar technology**

is the technological engine to keep the money running

As smaller the devices are, as cheaper they are

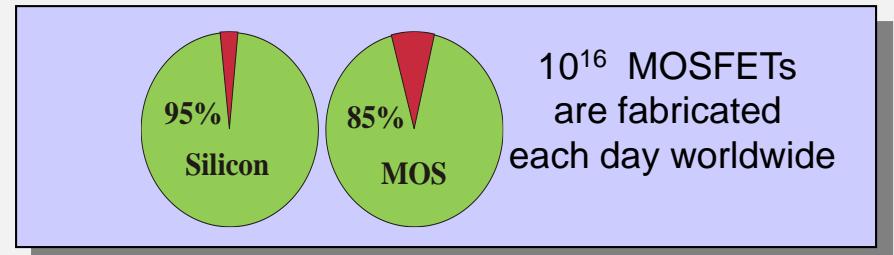


3

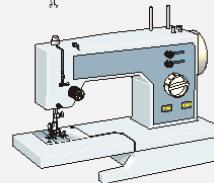
**Silicon MOSFET devices**

are:

- most easy to shrink
- are faster with shrink
- consume less power with shrink



CMOS is the far dominant device technology where the mainstream money is in



1973  
1000 ICs of 1kb  
~75'000 €

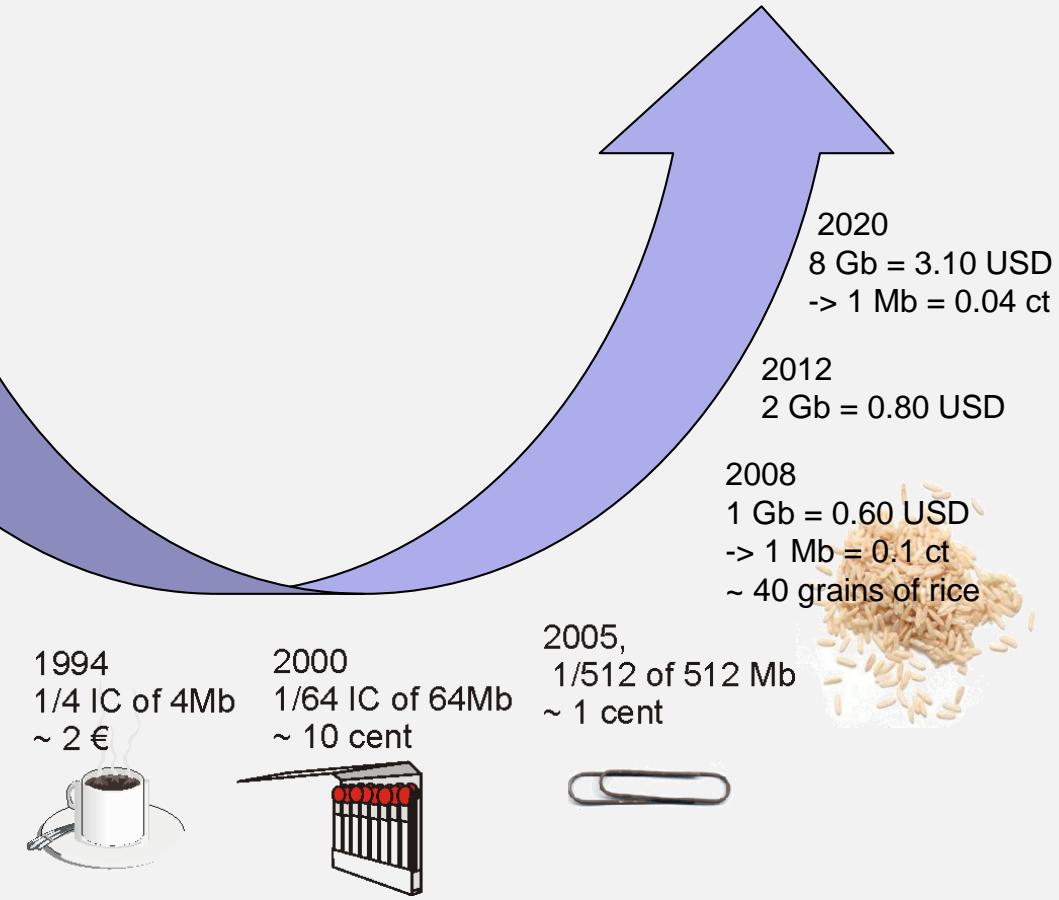
1977  
64 Ics of 16kb  
~ 5'000 €

1981  
16 ICs of 64kb  
~ 400 €

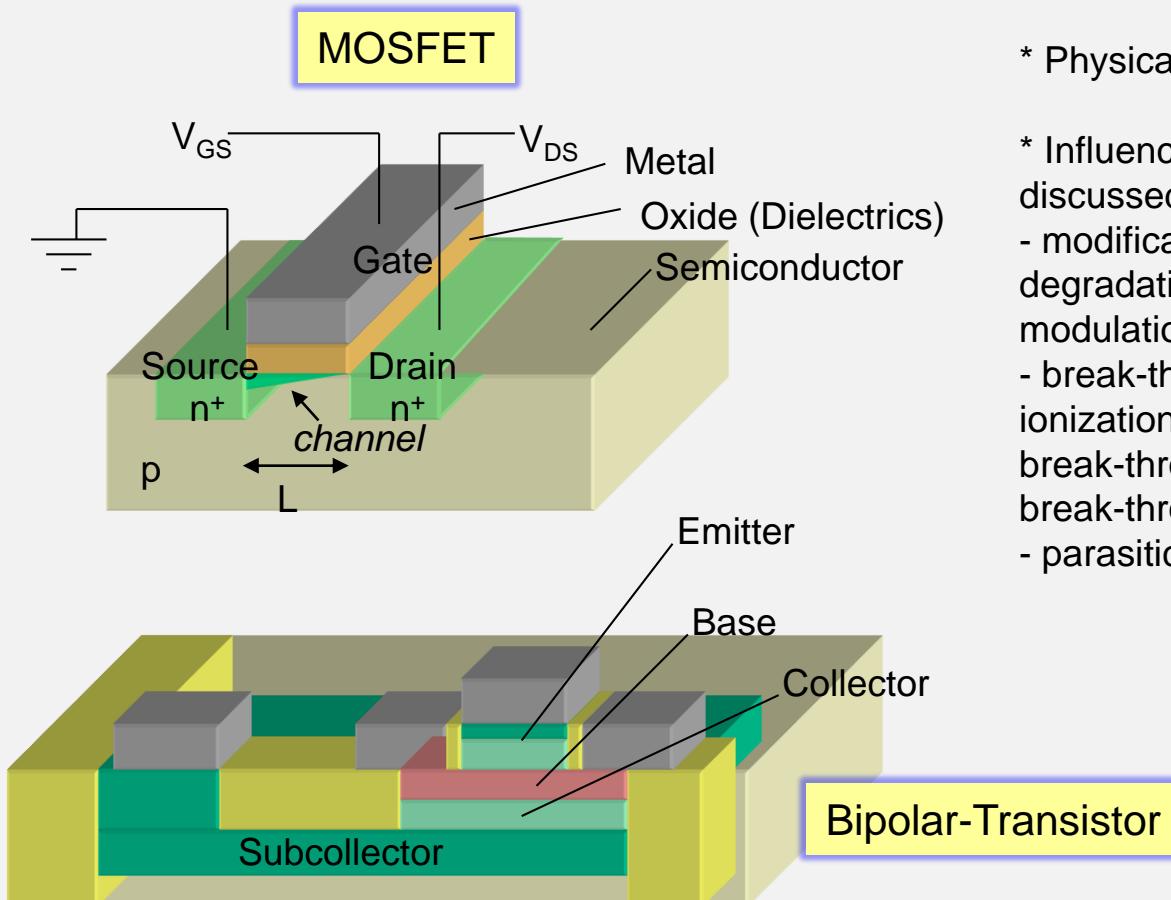
1984  
4 ICs oft 256kb  
~120 €

1990  
1 IC of 1Mb  
~ 5 €

The equivalent of 1Mb:



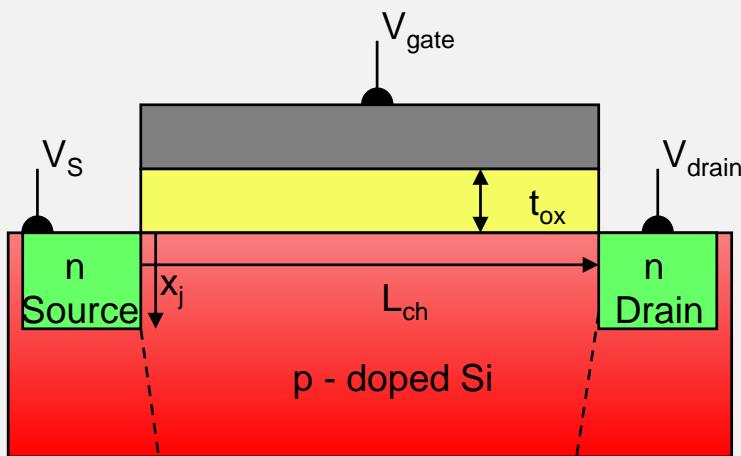
## Chapter 3: The classical long-channel MOSFET



\* Physical models of device behavior are discussed

\* Influence of internal high electric fields are discussed:

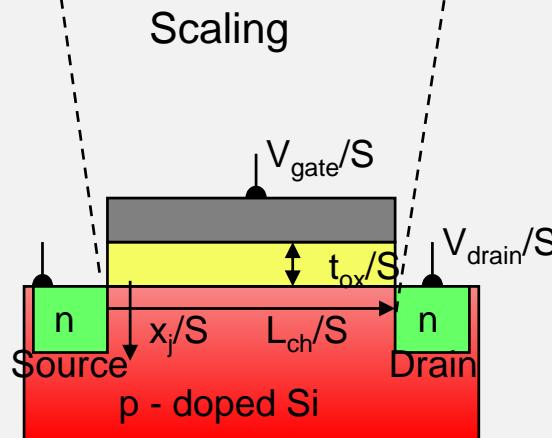
- modification in carrier transport (mobility degradation, velocity saturation, channel length modulation)
- break-through effects (hot electrons, impact ionization, avalanche multiplication, drain break-through, parasitic bipolar action, gate break-through, punch-through)
- parasitics (source-drain resistors, capacitors)



## Scaling of MOSFETs

MOSFETs are field-effect devices

if all dimensions and voltages are shrunk with a factor S  
(e.g. 1.13 per year),  
the IV-characteristics remain the same



faster switching

$$\tau = \frac{L}{v} \rightarrow \tau' = \frac{L/S}{v} \rightarrow \tau' = \frac{\tau}{S}$$

reduced area consumption

$$A = w \cdot L \rightarrow A' = \frac{w}{S} \cdot \frac{L}{S} \rightarrow A' = \frac{A}{S^2}$$

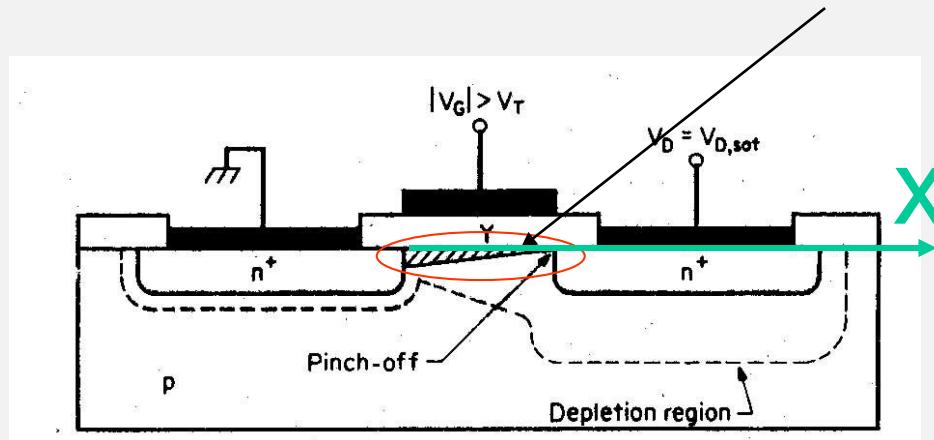
strong reduced energy consumption (power-delay product)

$$P = V \cdot I \cdot \tau \rightarrow P' = \frac{V}{S} \cdot \frac{I}{S} \cdot \frac{\tau}{S} \rightarrow P' = \frac{P}{S^3}$$

Basic MOSFET IV-characteristics are derived under the following ideal conditions:

1. Ideal MOS-Structure
2. doping in the channel and bulk is uniform
3. only drift current is considered
4. mobility is constant
5. the normal gate field  $E_y$  is much larger than the longitudinal field  $E_x$  ( this is called the **gradual channel approximation GCA**)

In the GCA the charge  $Q(x)$  under the gate is completely determined by the local voltage difference  $V_G - V_{DS}$



Compared to the constant-charge model in the GCA the charge and therefore the channel resistance are not constant, but dependent from the channel position x.

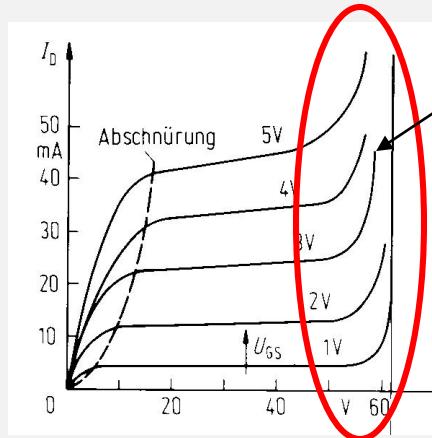
The drain current  $I_D$  is calculated by integrating charge and resistance (or conductance) over the channel length L

IV-characteristics:

$$I_D = \mu \cdot C_{ox} \cdot \frac{W}{L} \cdot \left[ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Basic threshold voltage:

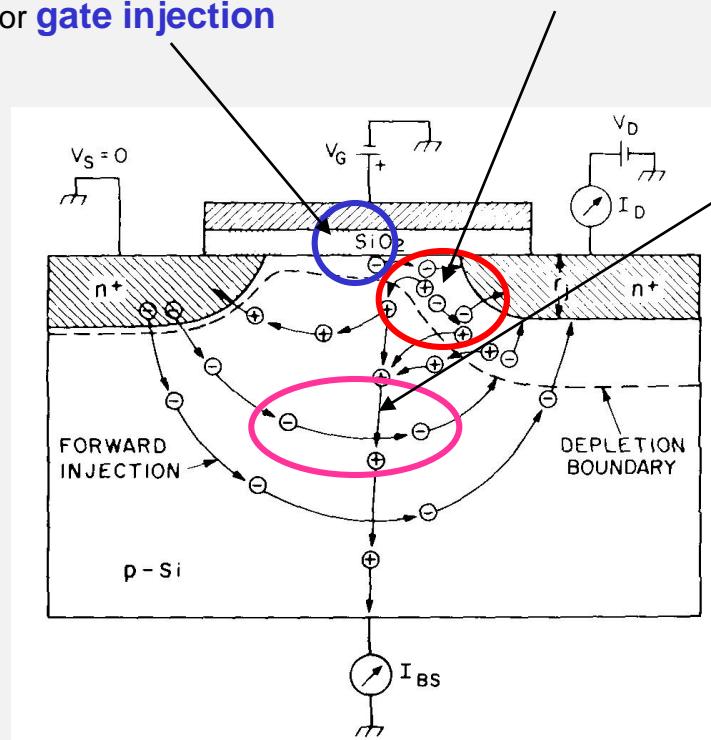
$$V_T = \frac{Q_s}{C_{ox}} + 2\Psi_{bulk} = \frac{\sqrt{2\epsilon_0\epsilon_{Si} \cdot qN_{dop} \cdot 2\Psi_{bulk}}}{C_{ox}} + 2\Psi_{bulk}$$



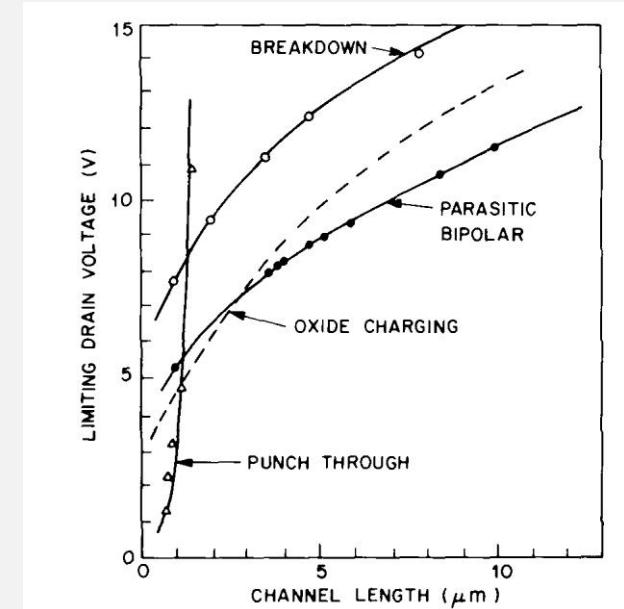
With increasing drain voltage  $V_{SD}$  high electric fields are induced, which cause several so-called **break-through effects**.

Physically these effects are caused by so-called **hot electrons**, which have much more kinetic energy as the room temperature equivalent of  $kT = 0.026\text{eV}$ .

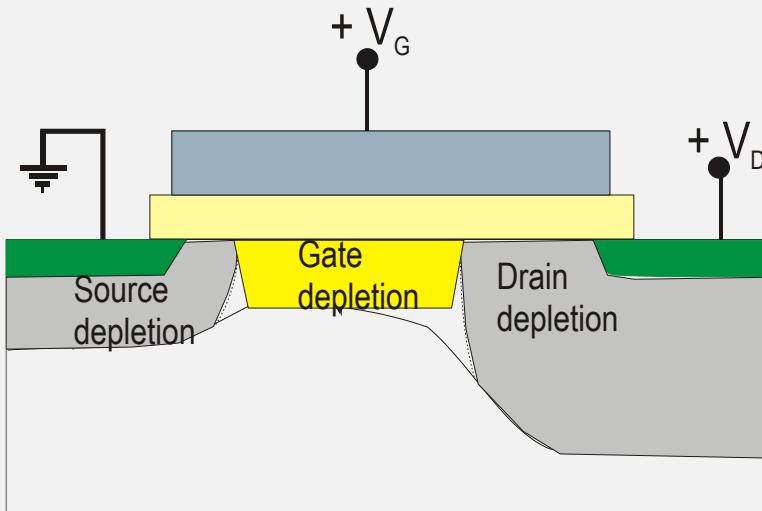
These hot electrons can do **impact ionization**, trigger **parasitic bipolar action** or **gate injection**



Onset of break-through effects



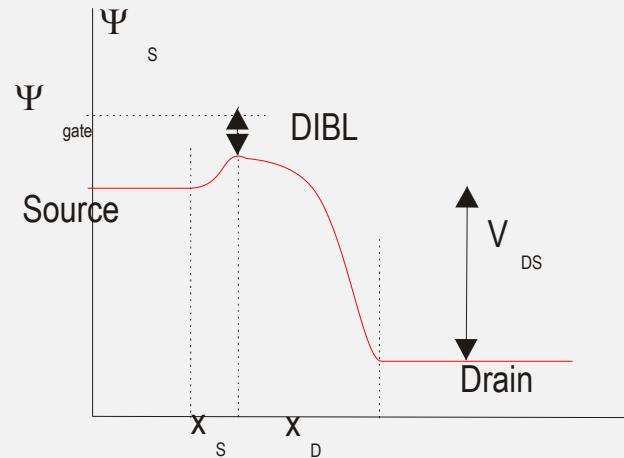
## Chapter 4: The short-channel MOSFET

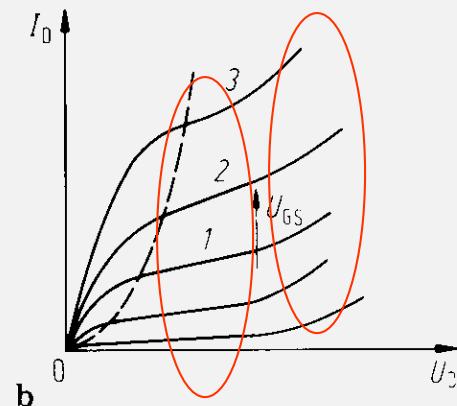
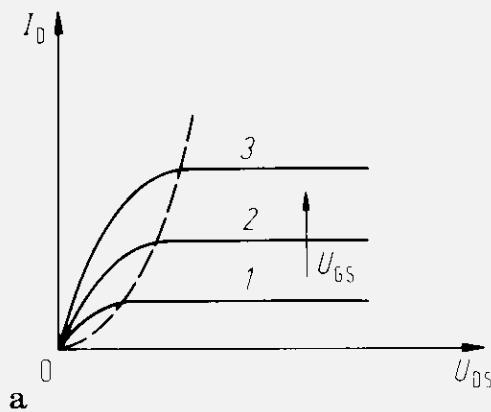


Shrinking of MOSFETs increases performance (faster, reduces power consumption) and reduces fabrication costs.

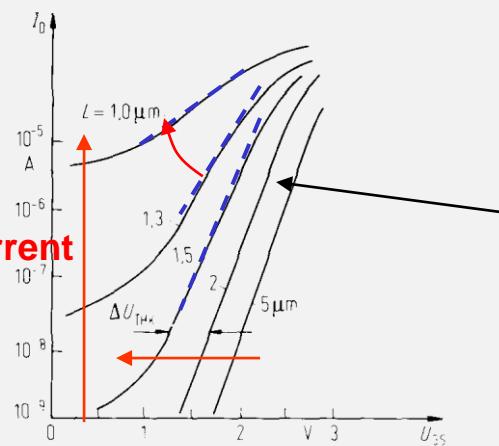
But with shrinking derivations from ideal long-channel I-V characteristics appear.

- \* Physical models of short-channel MOSFETs are discussed (charge-sharing model, DIBL-model)
- \* Short-channel effects are discussed (drain-induced barrier lowering DIBL, narrow-channel effects)



**Output characteristics:**

- \* **no saturation** -> bad for analog application
- \* early, weak **break-through**

**Sub-threshold behavior:**

- \* increase in **subthreshold slope S** (from ideal value 60mV/dec -> higher values)  
-> higher voltage swing needed to turn device on/off

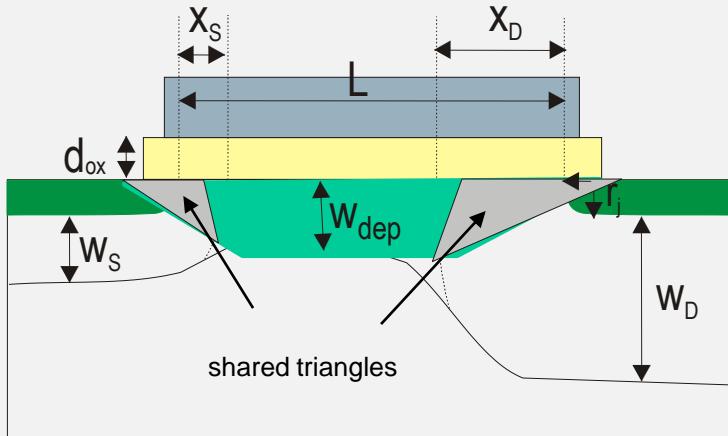
**Drain Induced Barrier Lowering (DIBL)**

\* increase of **leakage current**

\* **dynamic lowering of threshold voltage**

**Shrinking dimensions induces:**

worse **static** behavior (higher leakage, lower reliability)



2

**Short channel, but the contribution of S/D depletion is high:**  
(very short channel and/or  $V_{DS}$  high)

1) with high  $V_{DS}$  the shared triangles increase to unsymmetrical triangles:

$$x_S = \sqrt{\frac{2\epsilon_0\epsilon_{Si} \cdot (V_{bi} - \Psi_S)}{qN_A}} \approx \sqrt{\frac{2\epsilon_0\epsilon_{Si} \cdot (V_{bi} - 2\Psi_{bulk})}{qN_A}}$$

at Source using:  
 $\Psi_S = 2 \Psi_{bulk}$

$$x_D = \sqrt{\frac{2\epsilon_0\epsilon_{Si} \cdot (V_{bi} - \Psi_S + V_{DS})}{qN_A}} \approx \sqrt{\frac{2\epsilon_0\epsilon_{Si} \cdot (V_{bi} - 2\Psi_{bulk} + V_{DS})}{qN_A}}$$

at Drain  
(reverse biased)

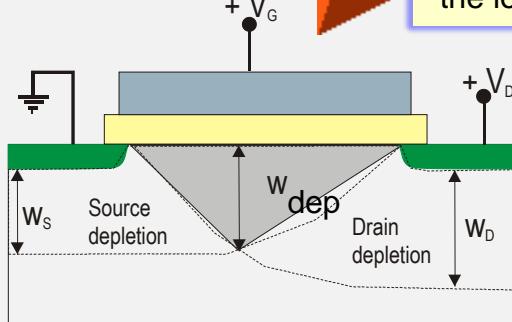
keeping  $\Psi_S = 2 \Psi_{bulk}$  approximately constant  $\rightarrow w_{dep} \sim \text{const}$

2) the threshold voltage shift is then:

$$\Delta V_{th} = V_{th}^{new} - V_{th}^{old} = V_{th}^{SC} - V_{th}^{LC} = \pm \frac{q | N_A w_{dep} \cdot r_j |}{2LC''_{gate}} \cdot \left[ \left( \sqrt{1 + \frac{2x_S}{r_j}} - 1 \right) + \left( \sqrt{1 + \frac{2x_D}{r_j}} - 1 \right) \right]$$



the long channel threshold voltage now decreases with shrinking channel length  $L$  and  $V_{DS}$  (via  $\Psi_S$  or  $x_D$ )



3

**Short channel, the contribution of S/D depletion dominates:**  
(very short channel and/or  $V_{DS}$  high)

1) the gate controlled charge is assumed to reduce to a triangle:

$$w_{dep} = \frac{L}{2r_j} \cdot \left( r_j + \frac{L}{4} \right) \longrightarrow \text{independent of } V_{DS}$$

To avoid short-channel effects (2/3-dim geometry, hot electrons (high-field) und transport degradations) **scaling laws** are investigated

The aim of scaling is to reduce the economically needed device size  
and

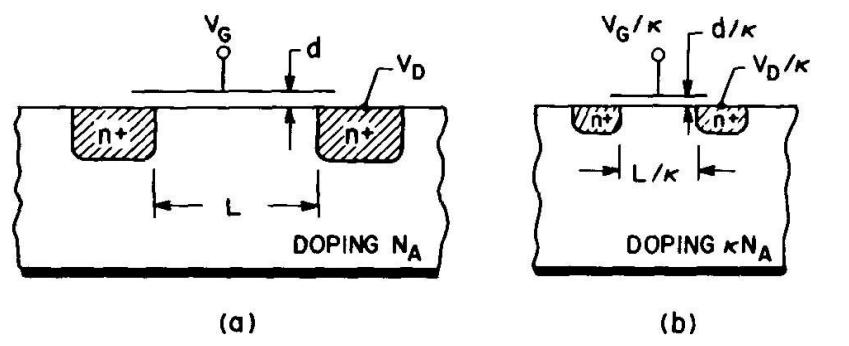
keep the desired electrical advantages (saturation, power reduction, speed increase)  
without the electrical disadvantages (degradation, hot carrier effects, reliability reduction)

Two basic scaling approaches exist

### Electrostatic scaling

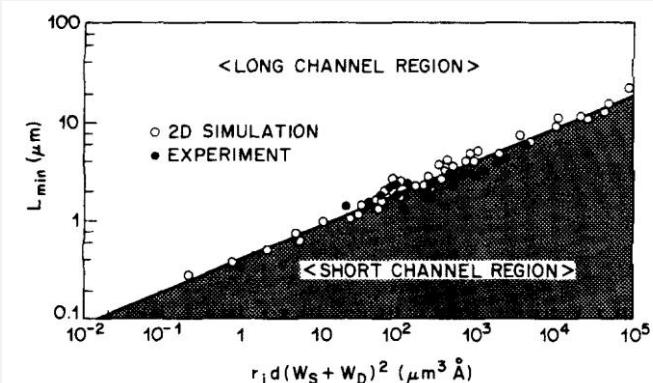
(based on physics, advantage for analog application, but practical limits)

- ideal (constant field)
- constant voltage
- quasi-constant voltage
- free scaling

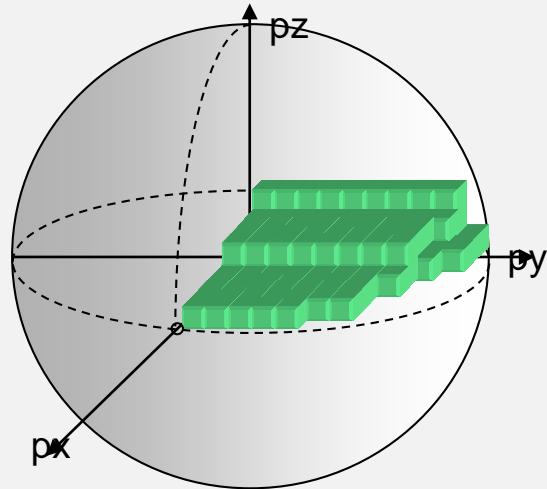


### Subthreshold scaling

(empirical, focus for digital ULSI-circuits (leakage, switching))



## Chapter 5: Carrier Transport



The motion of charge carriers depends on the interaction of the carrier with external and internal, time varying electrical, magnetical and thermal fields. In the classical regime (time and geometrical variations are large compared to carrier scattering effects) the **Boltzmann equation** is a good approximation for carrier transport.

In long-channel MOSFETs the classical solution of the Boltzmann equation results in the **drift-diffusion approximation**. Including energy exchange of the carriers with the silicon lattice, transport effects in short-channel MOSFETs like velocity overshoot or ballistic transport can be described by so-called **hydrodynamic equations** which are derived from Boltzmann equation.

In novel devices like tunneling transistors, where geometries are in the same dimensions as electron wavelength or external fields vary as fast as scattering time scales, retarded transport or fully **quantum mechanical transport** with solving of the Schrödinger equation describes the transport of the carriers.

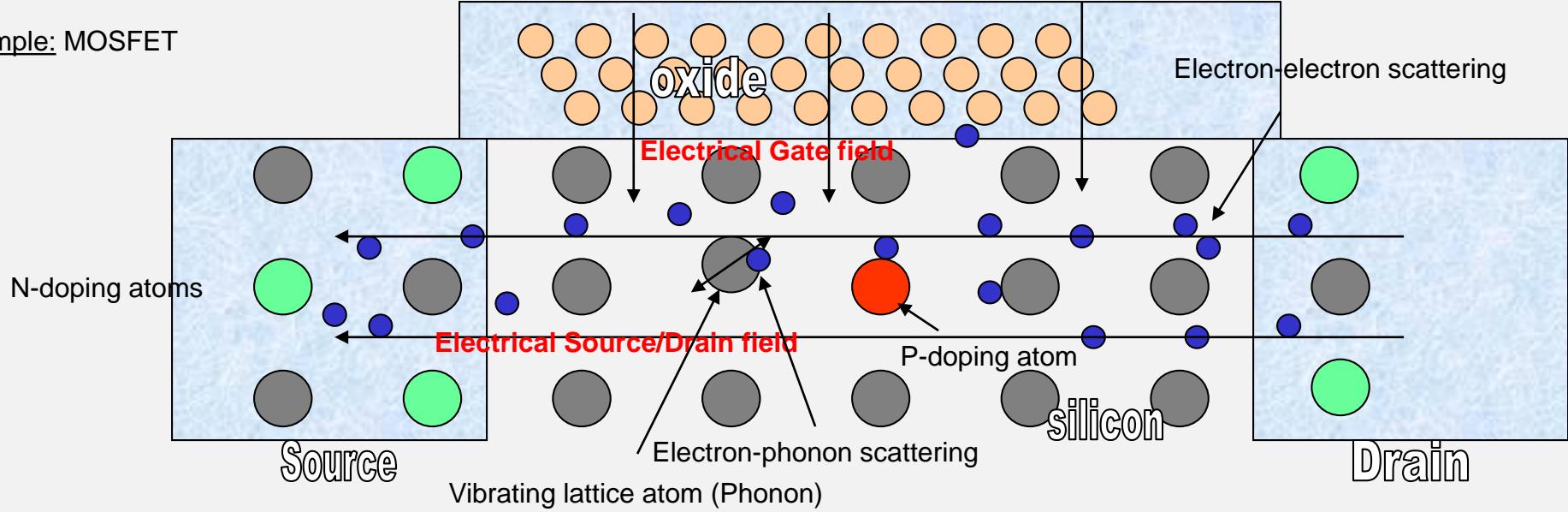
Understanding of the physical basics in transport is essential for the understanding of future devices.

**Carrier transport in a spatially inhomogenous device, subjected to time-varying driving forces**

will be

**a nonlinear, nonstationary, nonequilibrium statistical, quantum mechanical problem**

Example: MOSFET



1) all particles (electrons and atoms) are quantum mechanical particles (Fermi-statistics, Pauli-principle)

Nature of particles and statistics

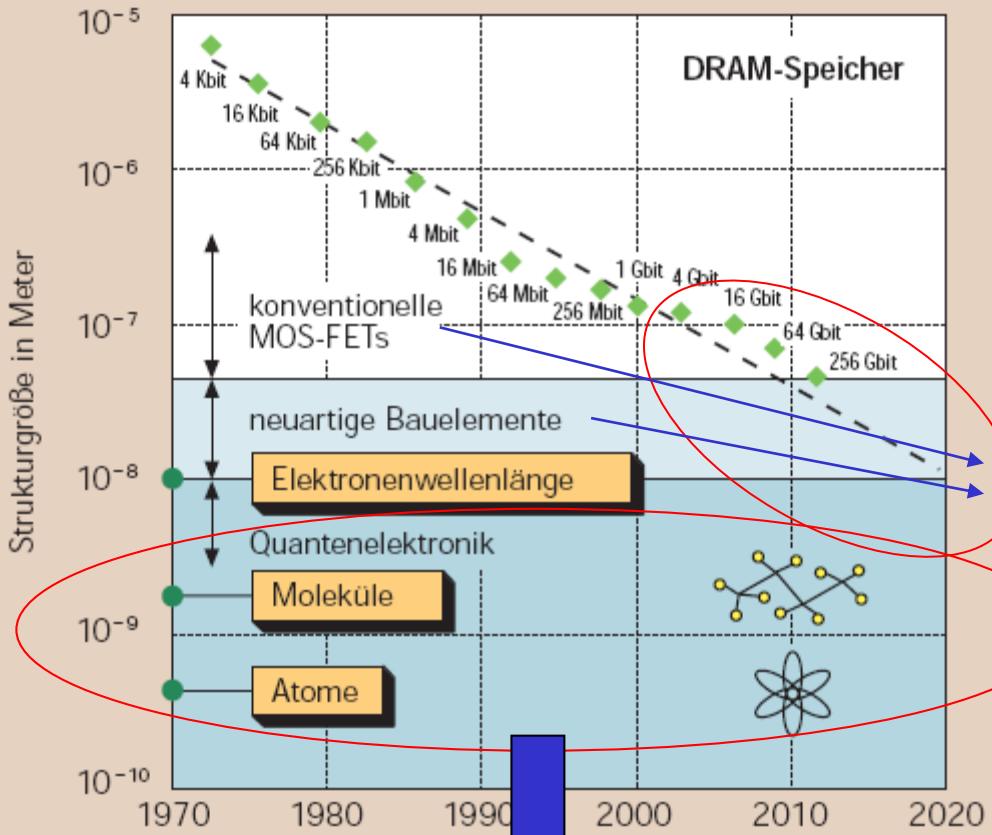
2) different atoms (oxide, silicon, doping atoms) provide different intrinsic potentials and properties (electron density, scattering cross section,...)

3) Local distortions in space (defects,...) and time (phonon vibration) exist

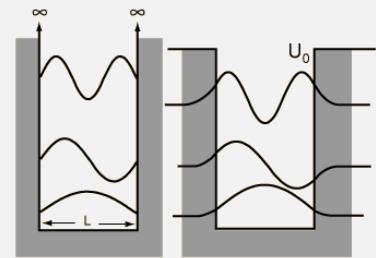
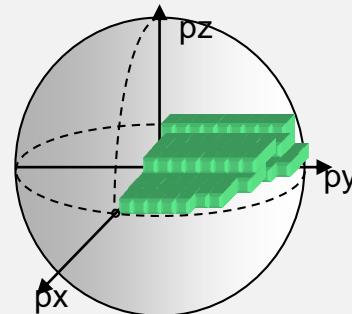
environment

4) time and space varying external fields influence the motion of the charge carriers

Forces and motion -> transport

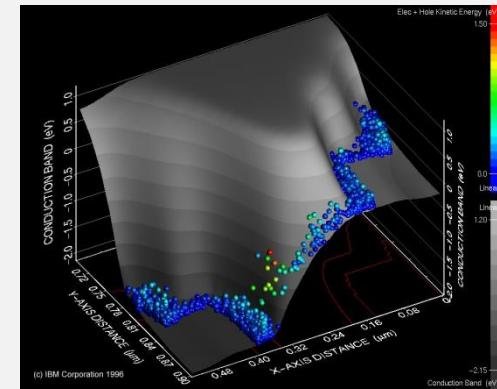
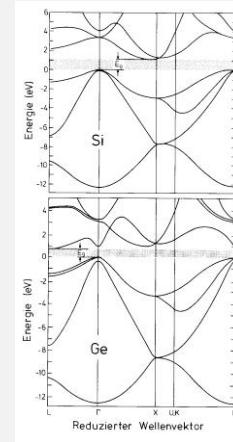
**Das Mooresche Gesetz**

Lecture "Nanoelectronics"  
of Prof. Lugli

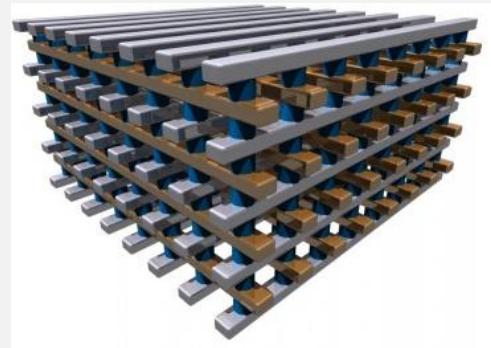
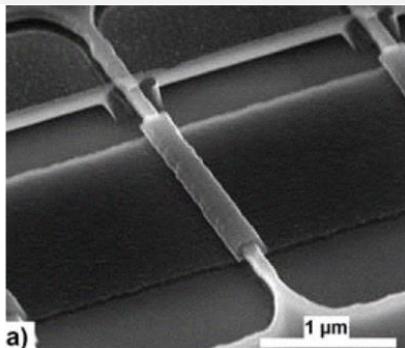
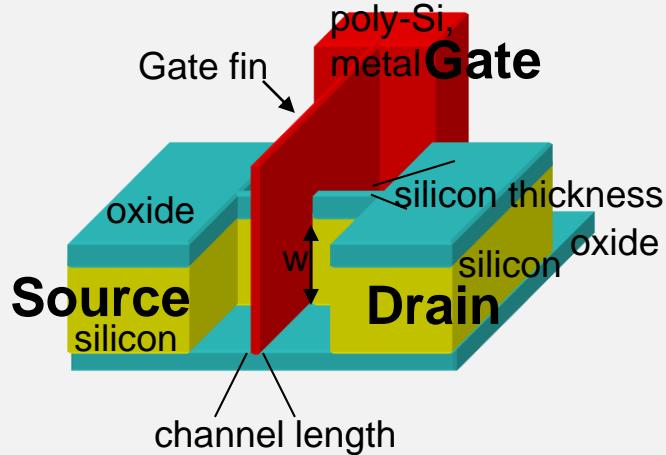


$$\frac{\partial f}{\partial t} = - \left[ \frac{1}{\hbar} \nabla_k \epsilon(k) \cdot \nabla_r f + \frac{q\vec{E}}{\hbar} \cdot \nabla_k f \right] + \frac{\partial f}{\partial t} \Big|_{coll}$$

Lecture "Advanced MOSFETs and Novel Devices"



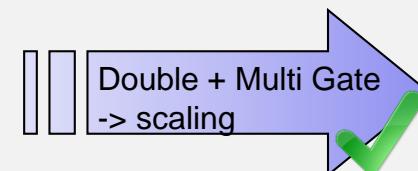
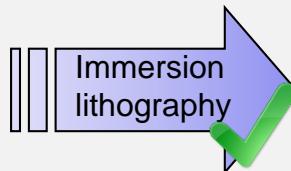
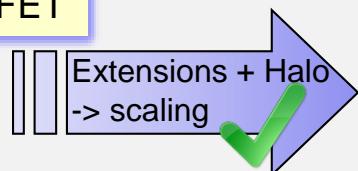
## Chapter 6: Advanced MOSFETs



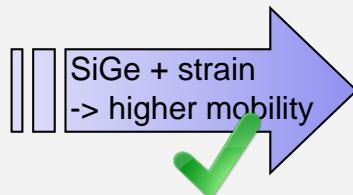
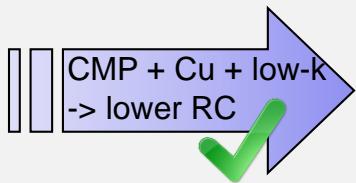
Industrial roadmaps scale down MOSFETs with channel length of 25 nm in the year 2012. Due to technological problems several ways of realization are discussed:

- \* including **SiGe** in the channel region for higher carrier mobilities
- \* **vertical MOSFETs** for easy realization on nanometer channel length
- \* **SOI-MOSFETs** on insulating substrates to reduce leakage currents
- \* **Halo-doping** to avoid punch-through and source-drain leakage
- \* **high-k gate dielectrics** to avoid quantum mechanical gate tunneling
- \* **metal gate** to avoid gate depletion and random dopant effects
- \* **double-gate MOSFETs** to avoid threshold voltage roll-off
- \* **advanced memory devices** to achieve a higher density

## Planar MOSFET



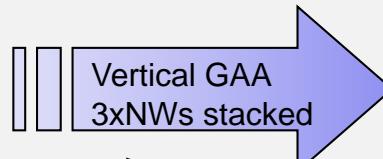
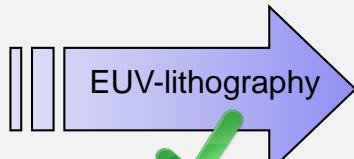
180 nm node 140nm – 100nm 1999 - 2001	130 nm node 90nm – 70nm 2002 - 2004	100/90 nm node 65nm – 50nm 2004 - 2006	70/65 nm node 45nm – 35nm 2006 - 2008	50/45 nm node 30nm – 25nm 2008 - 2010	35/32 nm node 20nm – 17nm 2010 - 2012	22 nm node 14nm – 10nm 2012 - 2014
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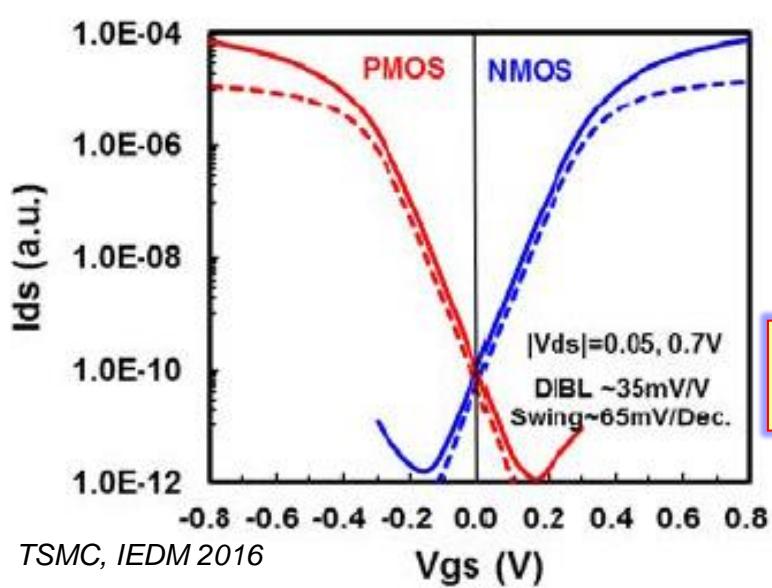
## FinFET



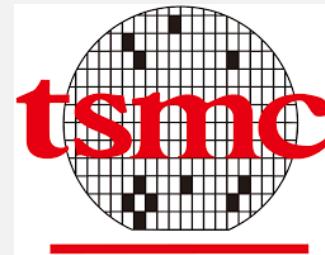
16/14 nm node 24nm 2014 - 2016	10 nm node 20nm 2017 - 2018	7 nm node 20nm 2018 - 2020	5 nm node 18nm 2020 - 2022	3 nm node 16nm 2022 - 2025	2.1 nm node 14nm 2025 - 2028	1.5 nm node 12nm 2028 - 2031	1.0 nm node 12nm 2031 - 2034
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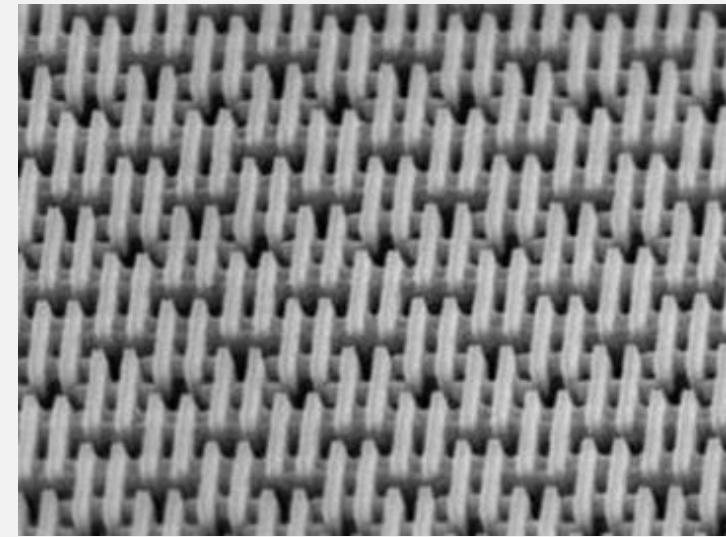
2018 Node (FinFET): 7 nm



TSMC, IEDM 2016



$S: \sim 65mV/dec$   
 $DIBL: \sim 35mV/V$



<https://www.tsmc.com/english/dedicatedFoundry/technology/7nm.htm>

- SRAM cell of  $0.027 \mu\text{m}^2$
- High-k/Metal-Gate
- Replacement-Gate Process
- Channel strain through Source/Drain epitaxy
- 12-level Cu/low-k
- Channel length 15 nm

DESIGNLINES | WIRELESS AND NETWORKING DESIGNLINE

## Apple Describes 7nm iPhone SoC

New handsets expand to 512 GB and \$1,099

By Rick Merritt, 09.12.18 □ 6

[https://www.eetimes.com/document.asp?doc\\_id=1333705](https://www.eetimes.com/document.asp?doc_id=1333705)

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SAN JOSE, Calif. — Apple announced a family of three iPhones powered by a 7nm SoC enabling up to 512 GBytes of memory. The handsets range in starting prices from \$749 to \$1,099, increase battery life by 30 to 90 minutes, and ship within two to six weeks.

The smartphones, and two new models of the Apple Watch, generally packed larger screens and upgraded chips, in some cases in slightly smaller devices. None of the devices support 5G cellular networks, expected to start switching on later this year, but the handsets support Gbit/s data rates, an LTE capability that Qualcomm was early to support.

Apple's 7nm A12 Bionic chip packs 6.9 billion transistors and is "the most powerful chip in a smartphone," said chief executive Tim Cook.

## Cannon Lake stumbles into the market: The IdeaPad 330-15ICN is the first laptop with a 10-nm-CPU

*Intel Cannon Lake once was a very highly anticipated CPU-release. After massive delays, the first Intel CPU generation that is manufactured in the advanced 10 nanometer process has finally arrived – and it enters the market silently, in a low-budget device.*

by Benjamin Herzig, 2018/05/13

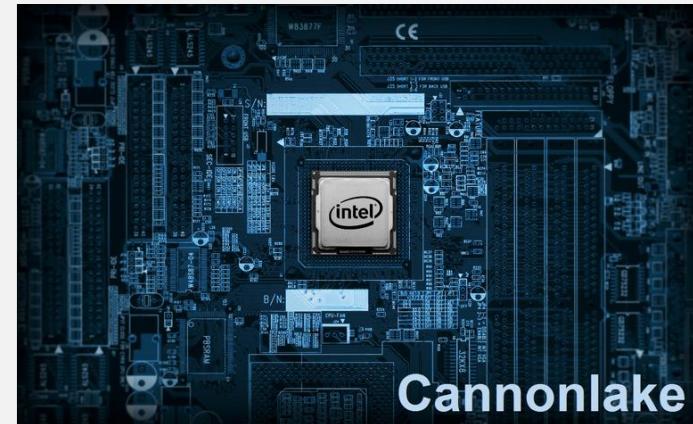
Cannon Lake Ultrabook Laptop Coffee Lake AMD

The first 10 nm laptop has been announced: When Lenovo introduced a couple of new IdeaPad laptops [a few days ago](#), this release also included the IdeaPad 330-15ICN – "ICN" stands for "Intel Cannon Lake". For those not in the know, Cannon Lake was once upon a time announced as the next big step in Intels release schedule, the first CPU generation to be manufactured in the 10 nm process. Originally, its release was expected in late 2016, almost two years ago.

<https://www.notebookcheck.net/Cannon-Lake-stumbles-into-the-market-The-IdeaPad-330-15ICN-is-the-first-laptop-with-a-10-nm-CPU.303330.0.html>



*Cannon Lake stumbles into the market: The IdeaPad 330-15ICN is the first laptop with a 10-nm-CPU*



<https://www.tweaktown.com/news/59209/intel-delays-10nm-cpu-tech-third-time-late-2018/index.html>

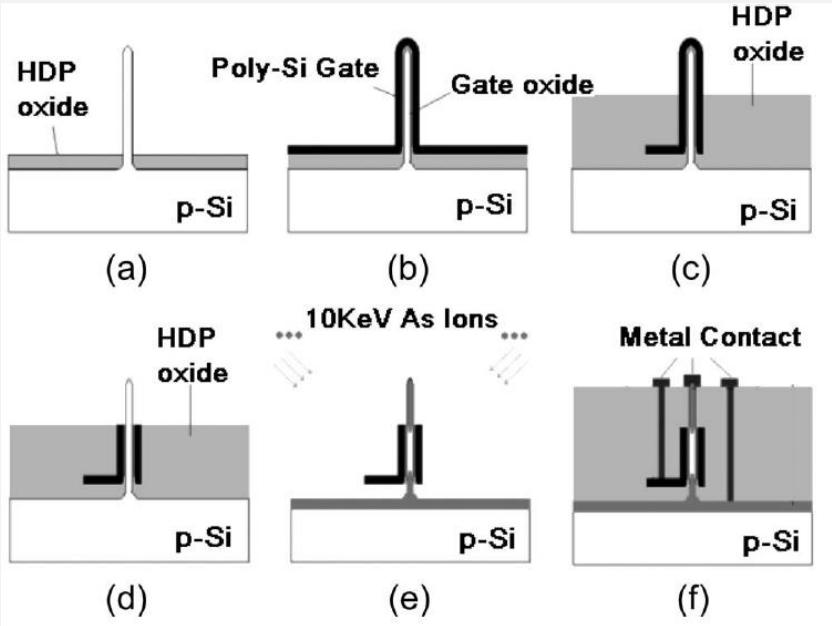
Because of yield problems, mass production of the new Cannon Lake processors will start 2019

It is expected that Cannon Lake is a test drive for 10 nm production, will be replaced by Ice Lake in 2020

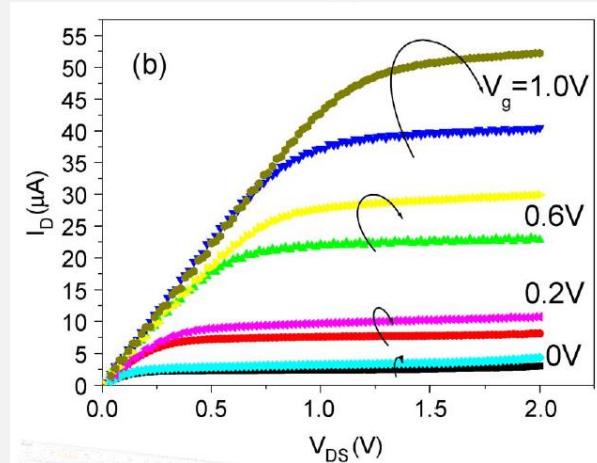
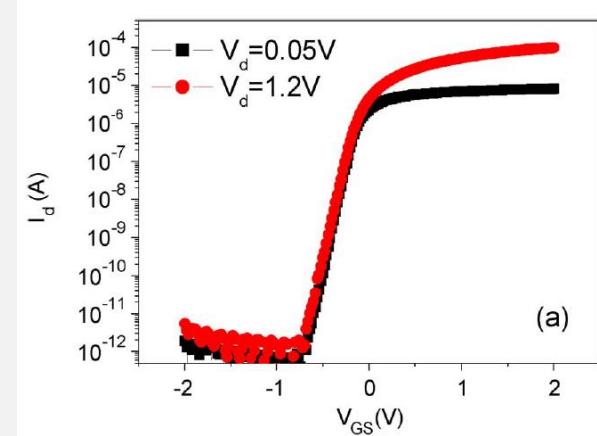
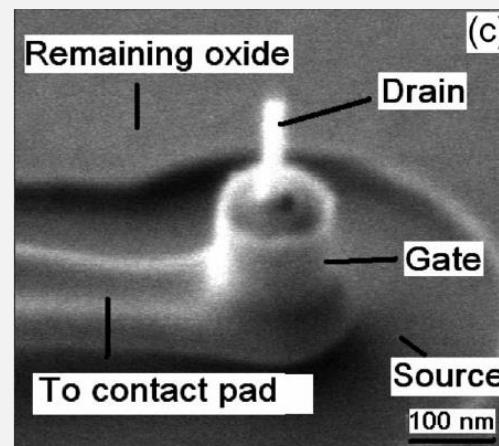
# Vertical Silicon-Nanowire Formation and Gate-All-Around MOSFET

IEEE 2008

B. Yang, K. D. Buddharaju, S. H. G. Teo, N. Singh, G. Q. Lo, and D. L. Kwong



$L_G = 150 \text{ nm}$   
 $D = 25 \text{ nm}$

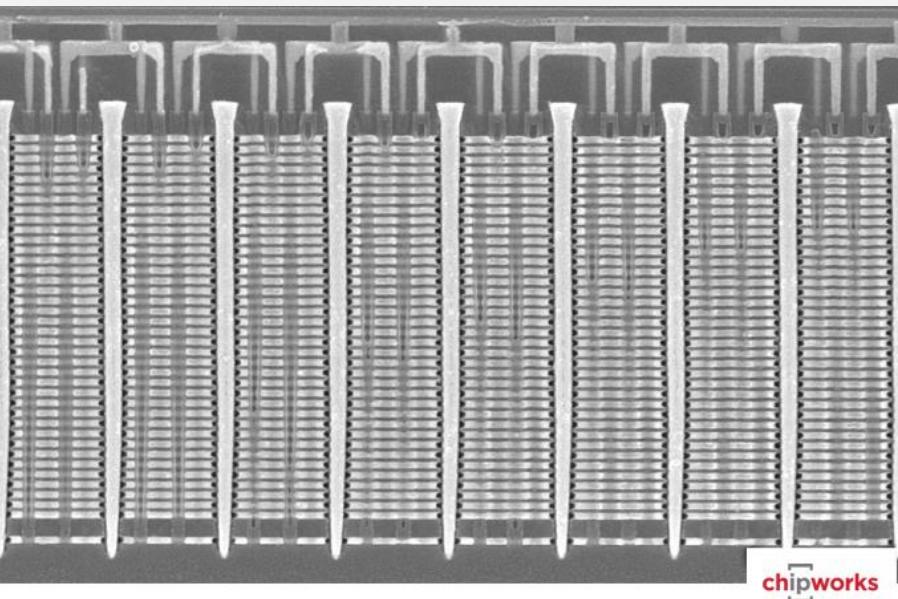
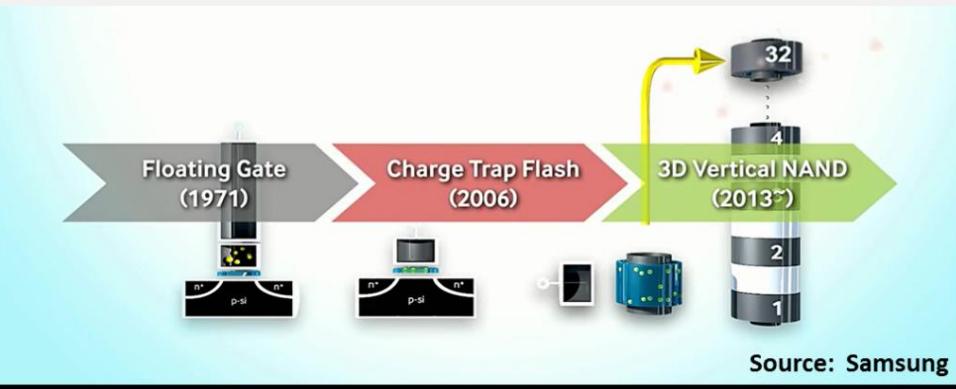


Nanowires with diameters from 20 to 450 nm

Subthreshold Slope 75 mV/dec, DIBL 10~50 mV/V

CMOS fabrication technology was used

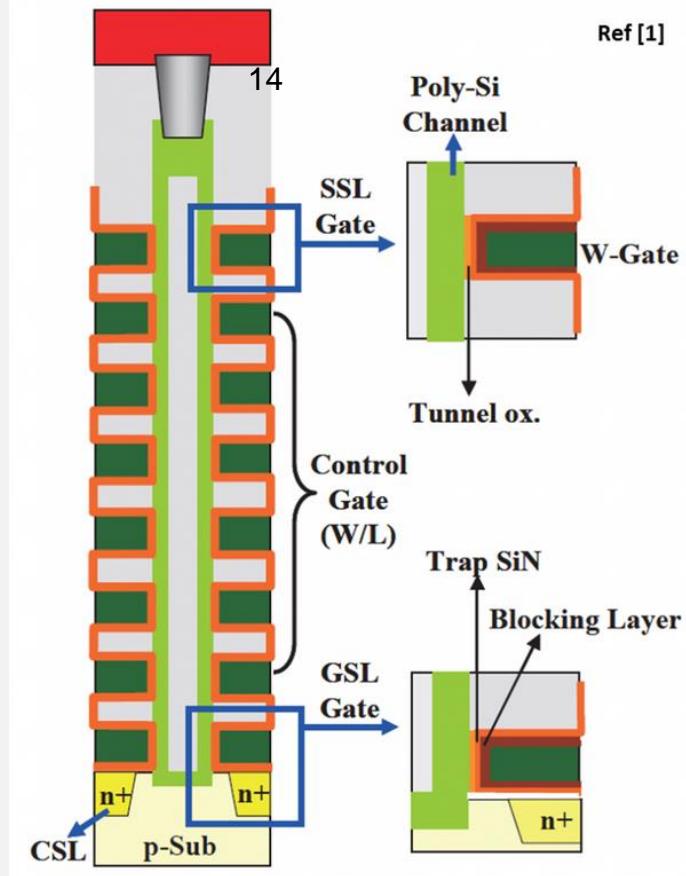
August 5, 2014

**The Second Shoe Drops - Samsung V-NAND Flash**

Close-up image of V-NAND flash array

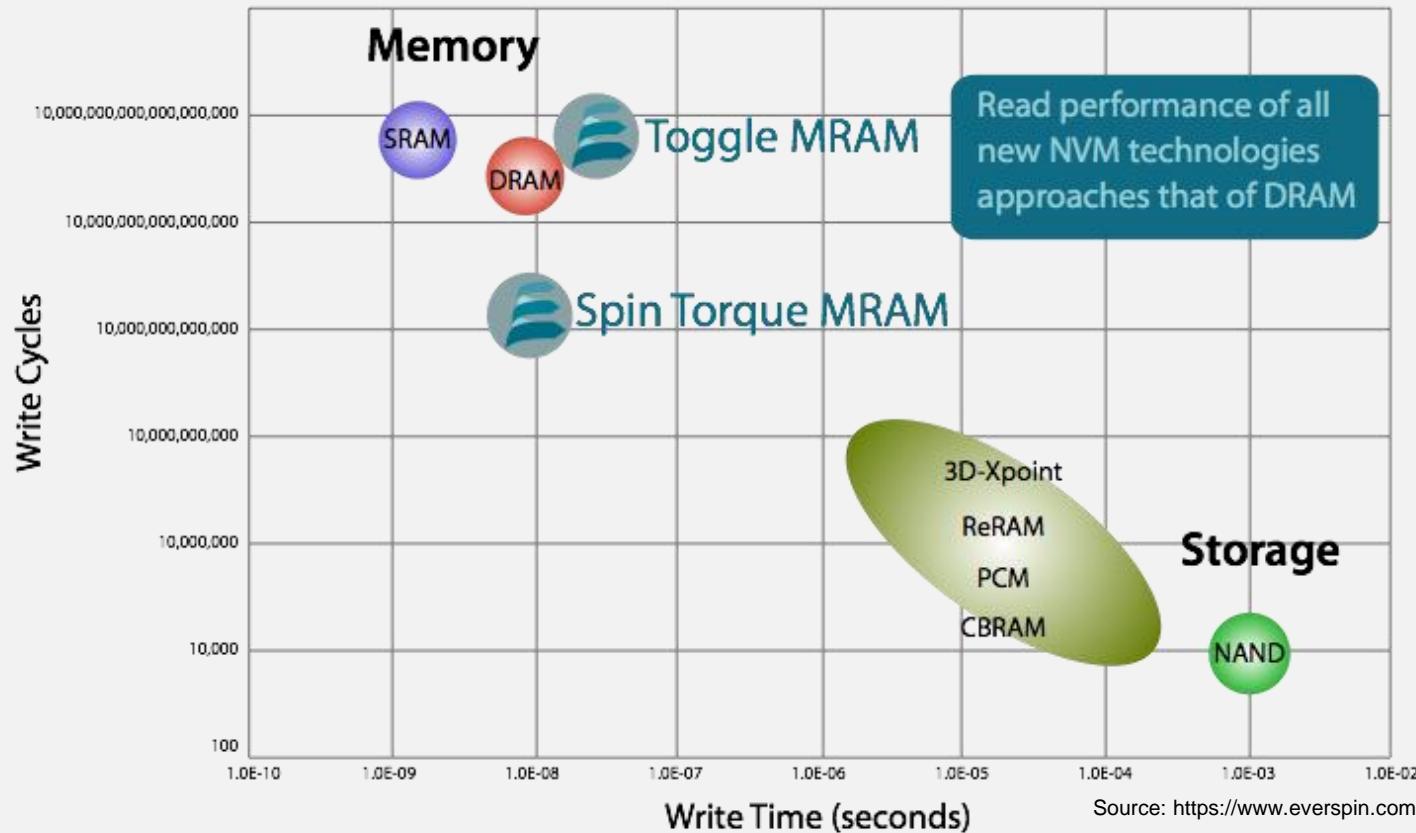
der Bundeswehr

Ref [1]



Planar technology is overruled by 3D-Technology

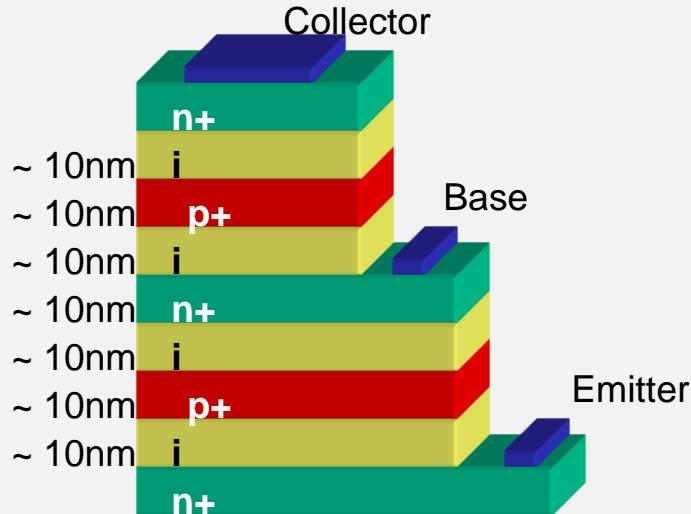
To understand the 3D-NAND, we look first at the 2D-NAND



► ST-MRAM seems to be a good candidate to replace DRAM/SRAM, because it is non-volatile and scalable

► RRAM/PCM seems a good candidate for Storage

## Chapter 7: Hot Carrier Devices

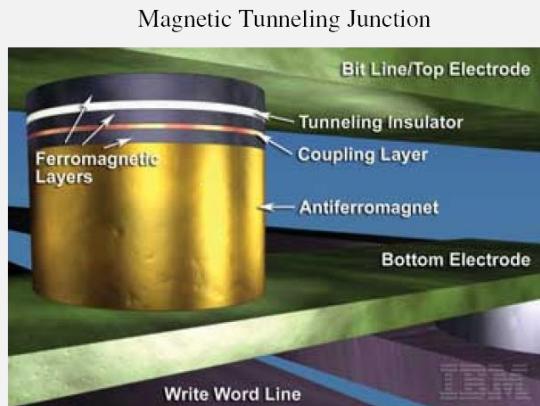


In hot carrier devices the geometrical layout is optimized to achieve very fast electron motion and such very fast devices, still operating under classical transport conditions.

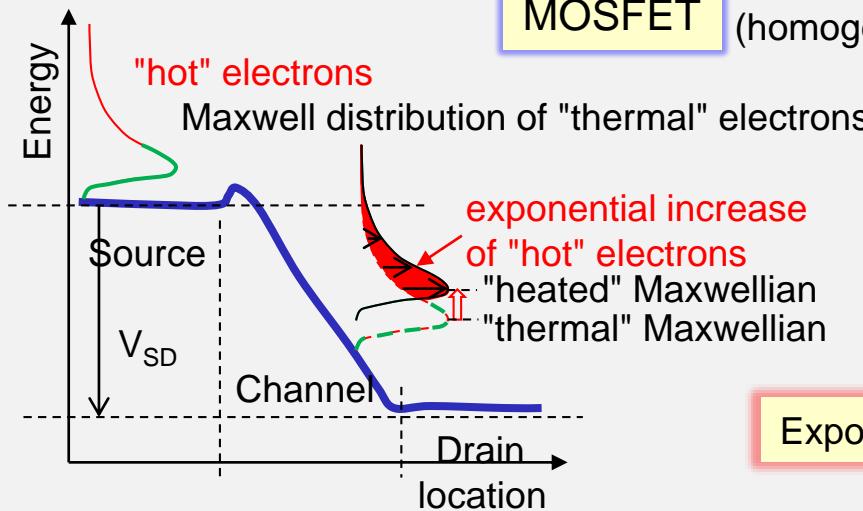
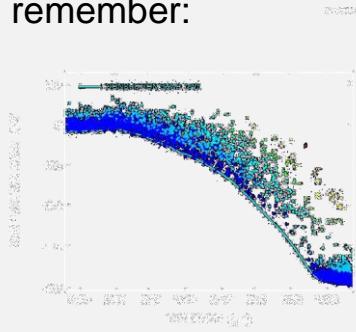
Device concepts far away from CMOS-technology are discussed to study the physical background, but also possible CMOS-candidates are presented:

- \* Hetero-junction transistors
- \* Metal base transistors
- \* Planar-doped barrier transistors
- \* Impact Ionization MOSFET

Furthermore we will take a look at Spin Valve transistors and at Magnetic Random Access Memory devices, which are sold today.



remember:



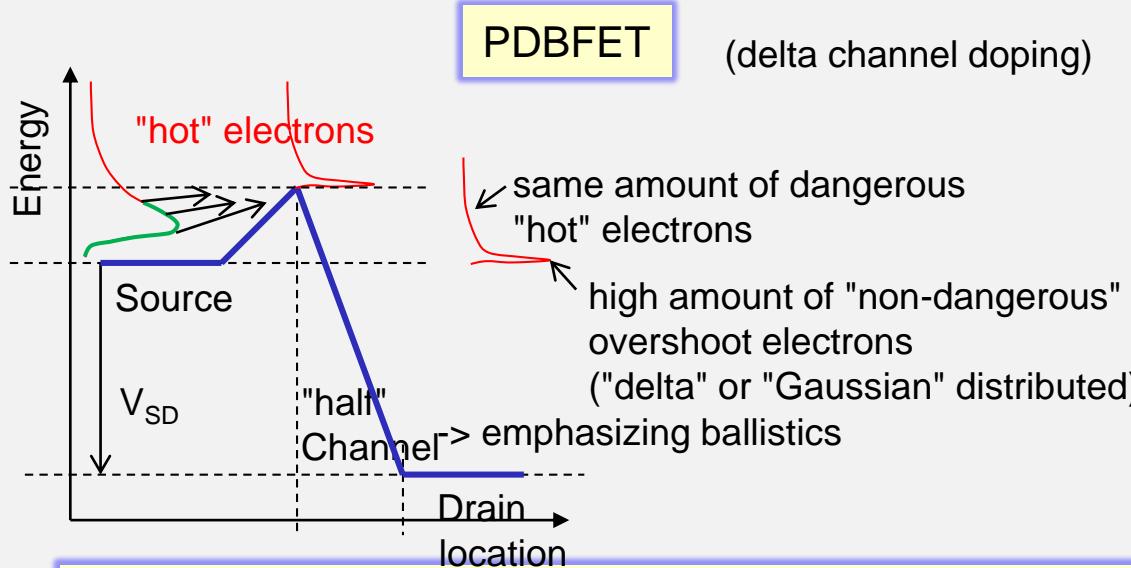
- > short channel tries to heat electrons
- > remaining scattering limits heating

Result:

- > displaced Maxwellian
- > exponential increase of "hot" electrons



Exponential increase of Avalanche electrons



- > top of barrier "collects" electrons in rest
- > barrier acts as electron energy filter

Result:

- > basically "tailed" Gaussian distribution
- > no increase of impact "hot" electrons

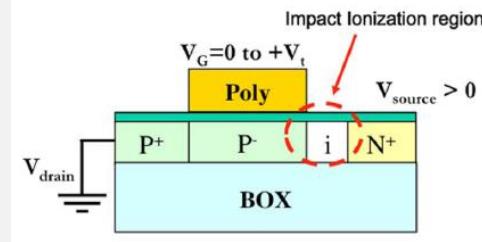
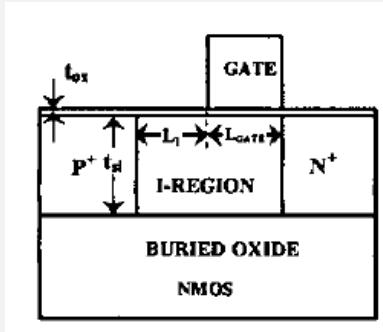
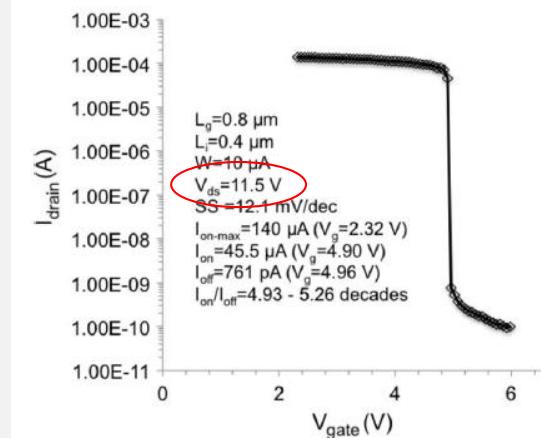
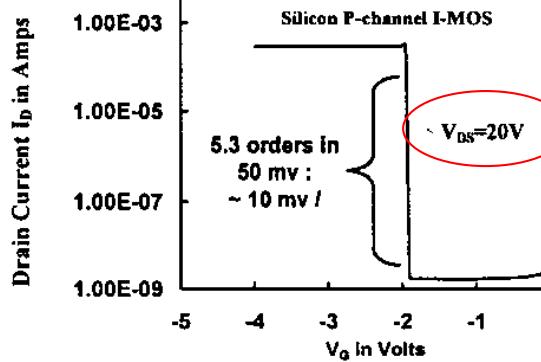


No increase of Avalanche electrons

Generation of "overshoot" electrons

In a MOSFET with low channel barrier always harmful hot electrons  $E > 3\text{eV}$  are present

In a PDBFET no harmful hot electrons are present, although all electrons have higher energy than in a MOSFET

 $I_D$  vs.  $V_g$  for the I-MOS

2002 Plummer: Experimental  $V_{DS} \sim 20 \text{ V}$

2009 EDL, Plummer et al.:

"A Novel Depletion-IMOS (DIMOS) Device with Improved Reliability and Reduced Operating Voltage"

\* normally-on device

\* Experimental  $V_{DS} \sim 12 \text{ V}$

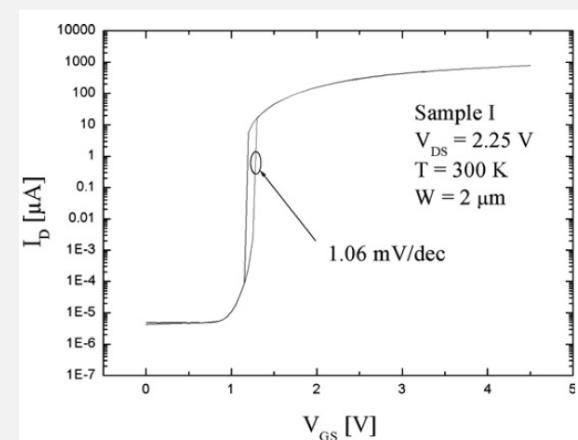
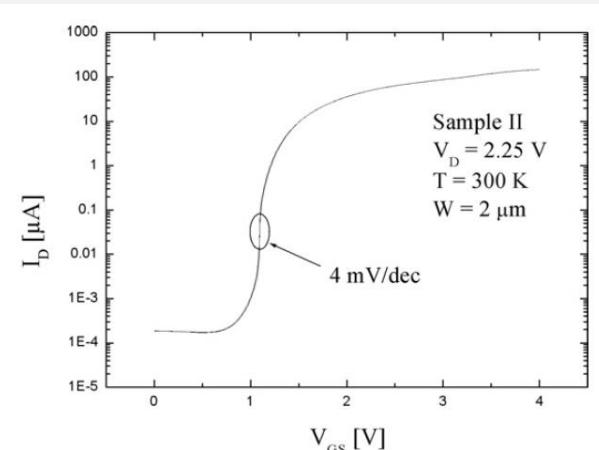
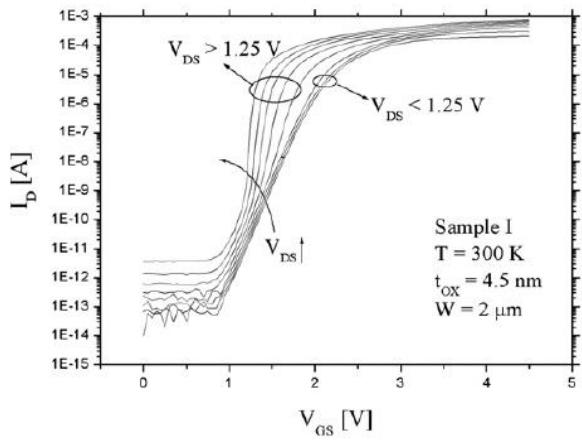
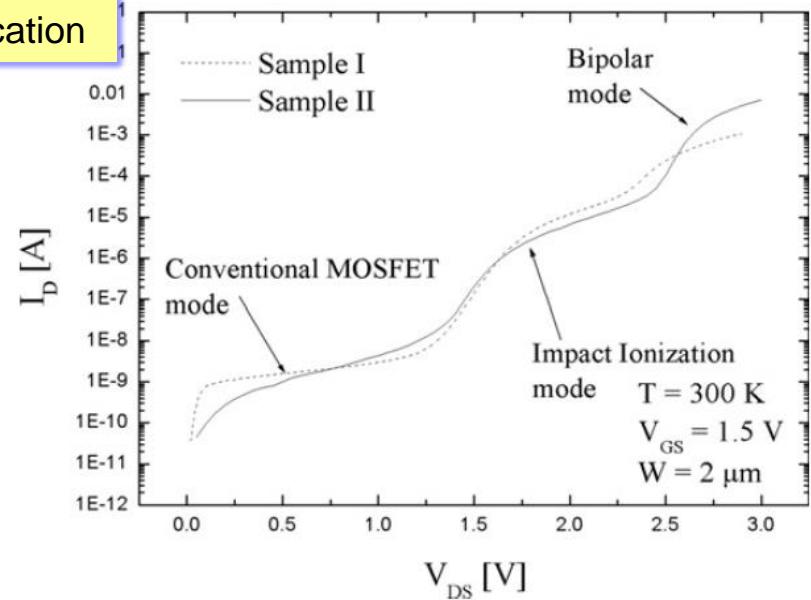
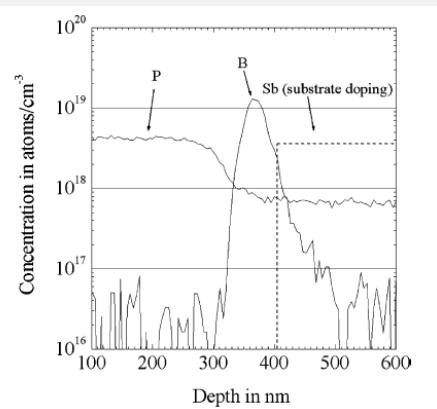
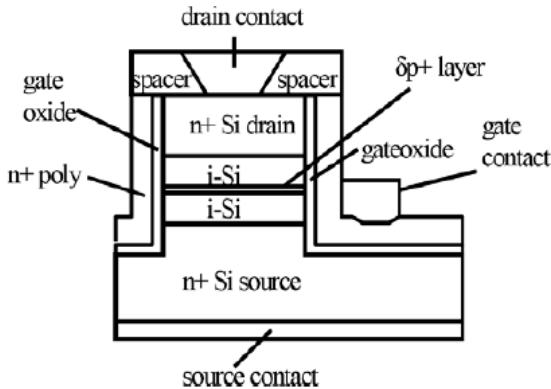


The operating voltage  $V_{DS}$  still high ( $\sim 12 \text{ V}$ )



Where is the limit ?

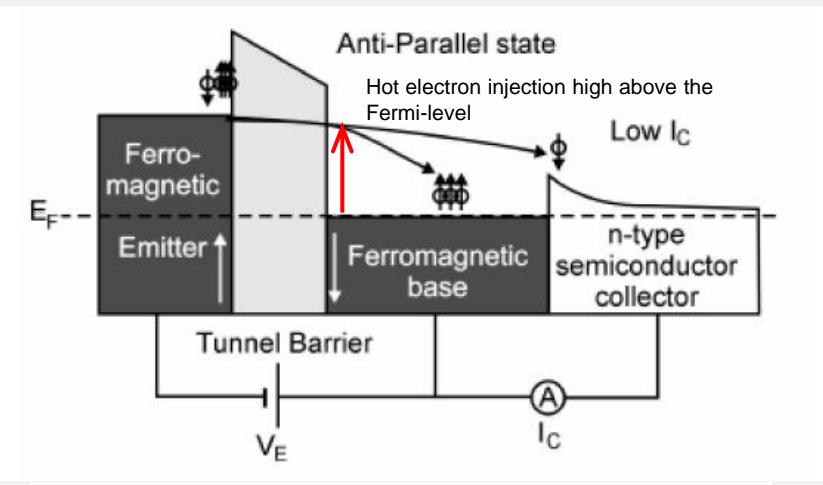
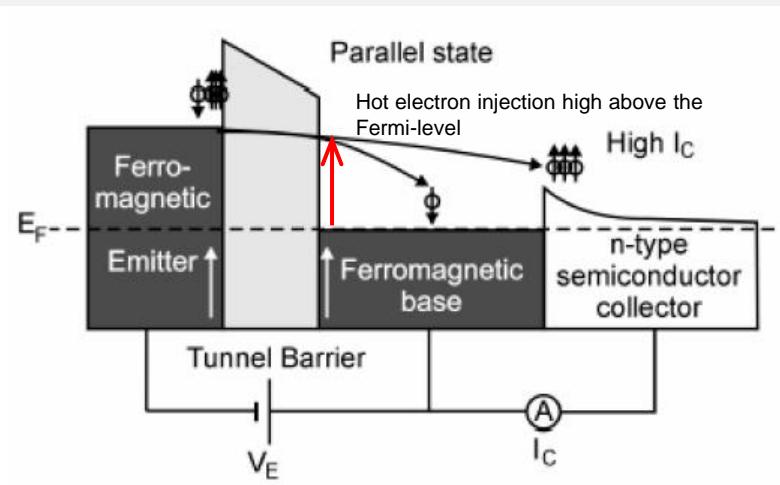
Optimization of  $\delta$ -doping profile enables additional bipolar amplification



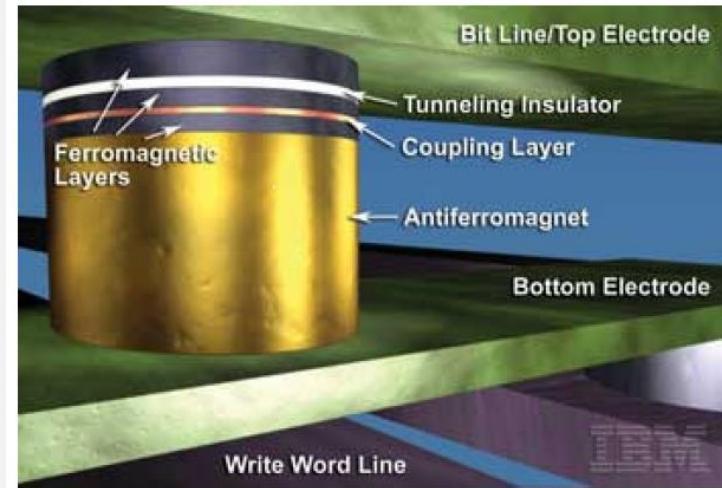
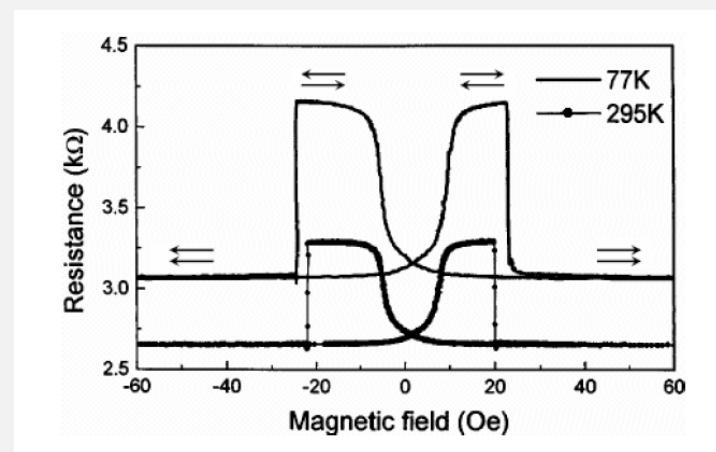
with bipolar action steep slopes and hysteresis is enabled

Introducing tunneling barriers in the working principle of hot electron transistors.  
Remember: Hot electrons mean energy above the Fermi-level.

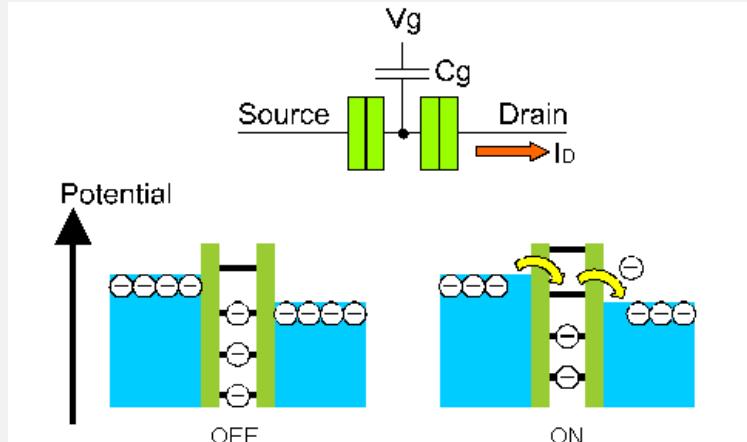
tunnel emitter with already polarized injection:



Magnetic Tunneling Junction

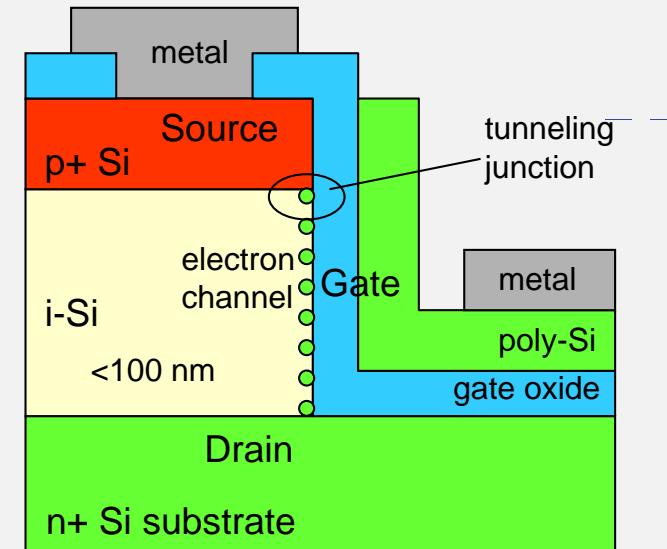


## Chapter 8: Tunneling Devices



Devices where quantum mechanical transport takes place are discussed.

- \* Tunneling Transistor
- \* Single Electron Transistors



### First fabricated vertical Esaki-Tunneling-FET



Thin Solid Films 369 (2000) 387–389



A vertical MOS-gated Esaki tunneling transistor in silicon

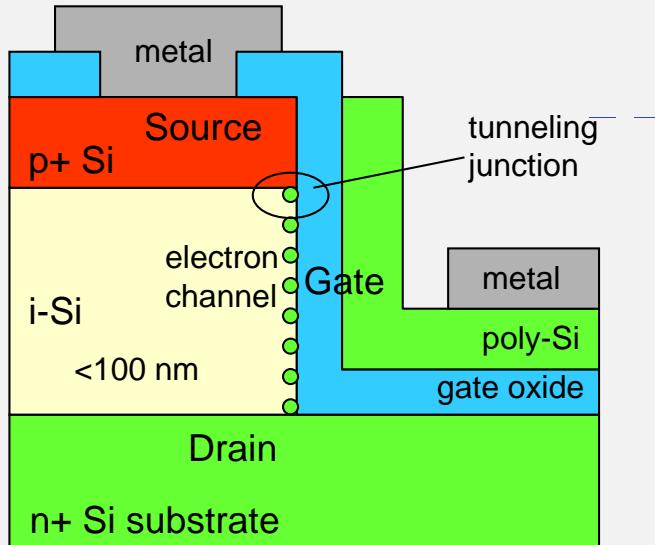
W. Hansch\*, C. Fink, J. Schulze, I. Eisele

Universität der Bundeswehr München, Institut für Physik, D-85577 Neubiberg, Germany

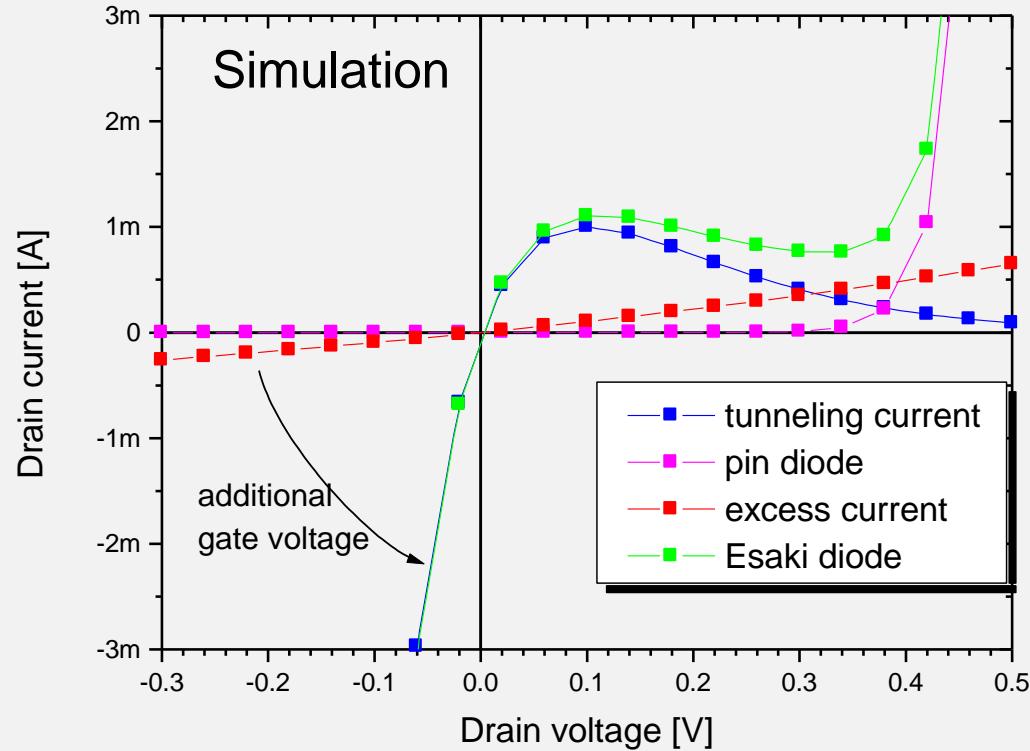
**Abstract**

For the first time a vertical, MOS gated tunneling transistor in silicon is fabricated. The necessary sharp doping profile structure is created by means of MBE. Pronounced transistor action due to Esaki tunneling is demonstrated at room temperature. At a low supply voltage of  $-0.2$  V a current gain of three magnitudes with saturation behaviour is achieved. MOS-gate, low supply voltage and exponential current increase make this device attractive for ULSI applications. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: Molecular beam epitaxy; Vertical tunneling device; Esaki diode

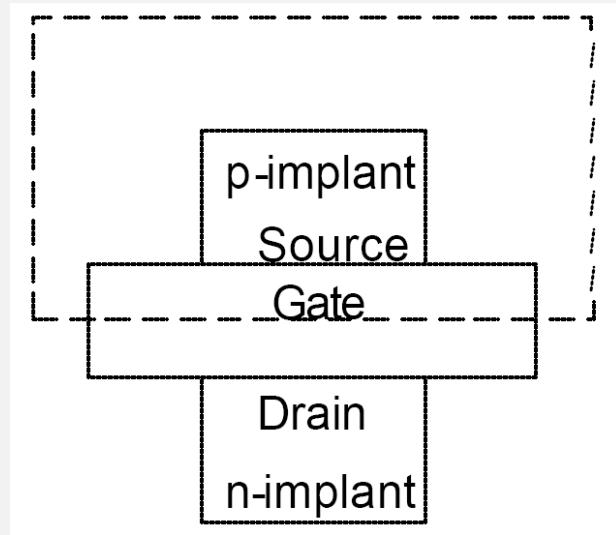


The Esaki-Tunneling MOSFET looks like a vertical MOSFET, but the drain is oppositely doped as the source.

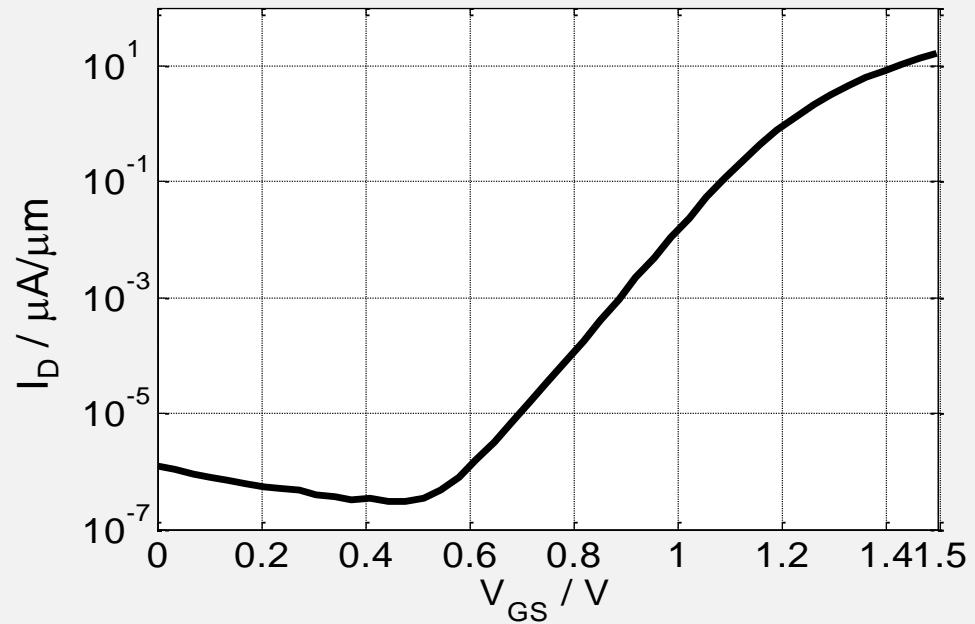


In the reverse-biased pin-diode the current can be switched on and off by creating a MOS-channel

- Infineon's standard CMOS process flow without any modifications was used for the fabrication of a tunneling device
- By shifting the p+ implant for the contact of the p-well over one half of a NMOSFET a diode is formed



transfer characteristic of the tunneling device fabricated in the 130nm technology

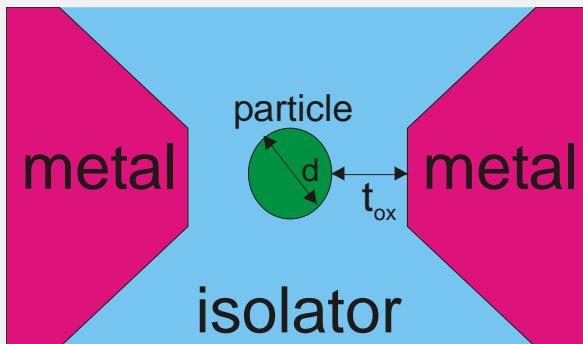


$W/L=1\mu\text{m}/300\text{nm}$ ,  $V_{DS}=V_{DD}=1.5\text{V}$



Never stop thinking

Principle:



A small particle is embedded in a isolator between two metal plates

Looking at the particle:

1

the particle forms a self-capacitance:

$$C = 2\pi\epsilon_0\epsilon \cdot d$$

for a spheric particle

2

if the capacitor is charged with  $Q$ , it creates a potential difference  $\Delta\varphi$  with the surroundings:

$$C = \frac{Q}{\Delta\varphi} = \frac{Q}{V}$$

3

the **electrostatic Coulomb-energy** of a charged capacitor is:

$$E_{coul} = \frac{1}{2}CV^2$$

Using eqs. 2,3 the Coulomb-energy of a capacitor can be expressed:

$$E_{coul} = \frac{Q^2}{2C}$$



**the Coulomb-energy of a capacitor, charged with a single-electron is:**

$$E_{coul} = \frac{e^2}{2C}$$

If the charging of a capacitor should be controlled by a voltage of  $\sim 1V$  with single-electron precision, eq. 2 delivers:

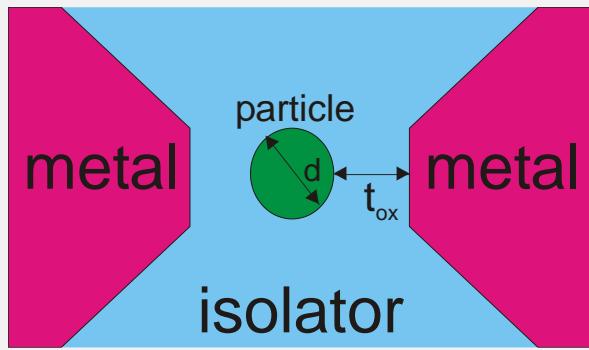
$$C = \frac{e}{V} = \frac{1.6 \cdot 10^{-19} As}{1V} \approx 10^{-19} F \approx 0.1 aF$$

With this capacitance the particle exhibits a diameter of (eq.1):

$$d = \frac{C}{2\pi\epsilon_0\epsilon} \approx \frac{10^{-19} F}{2\pi \cdot 8.85 \cdot 10^{-14} F/cm} \approx 10^{-7} cm \approx 1 nm$$



Single-electron handling requires nanometer particles with attoFarad (at  $\sim 1 V$  !)



The energy of the particle (called **Coulomb-island**):

1

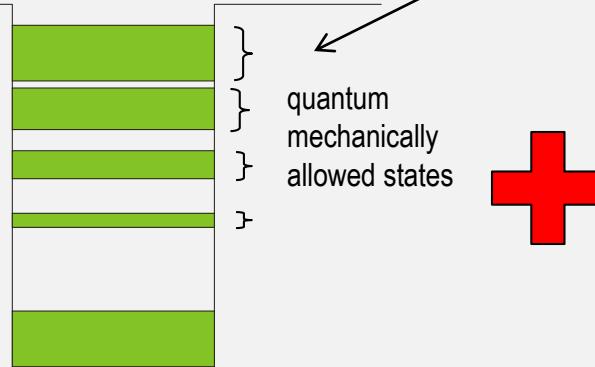
If the particle (with capacitance C) is charged with individual electrons, only discrete values of energy are allowed ( $n=1$  electron, 2 electrons, 3,...)

$$E_{coul} = n \cdot \frac{e^2}{2C}$$

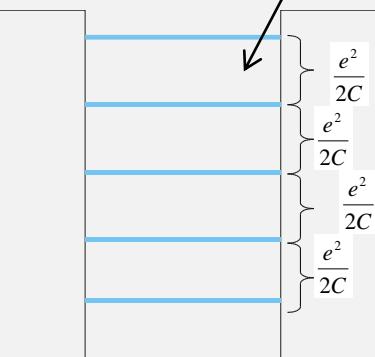
These energy levels are **equidistant**

2

Because Coulomb-particles are very small (nm) an additional quantum-mechanical size quantization exists:



Quantum-mechanically  
size quantization  
**non-equidistant levels**



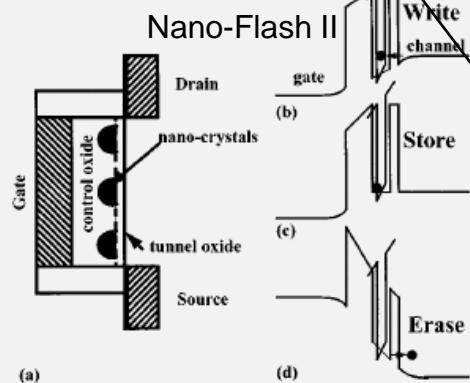
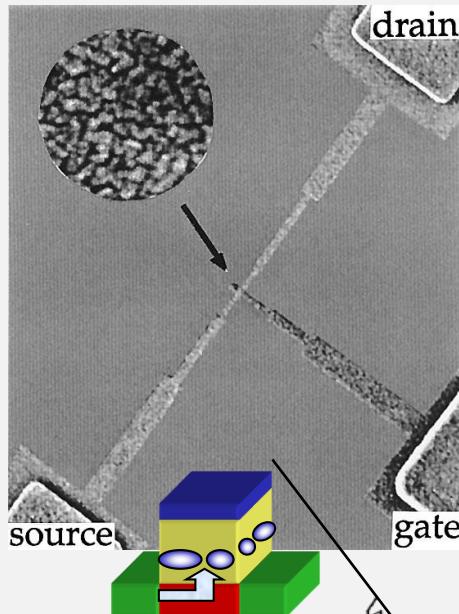
"Classical" energy separation due  
to electron charge quantization  
**equidistant levels**



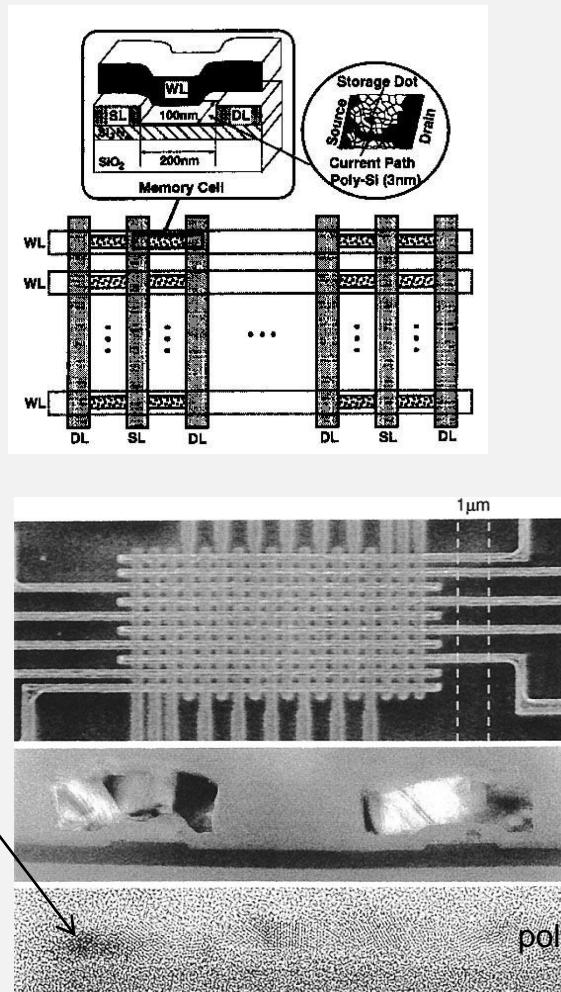
result may be non-equidistant  
energy levels

In small particles a classical, equidistant Coulomb-ladder exists, which is usually overlaid by quantum-mechanically energy levels

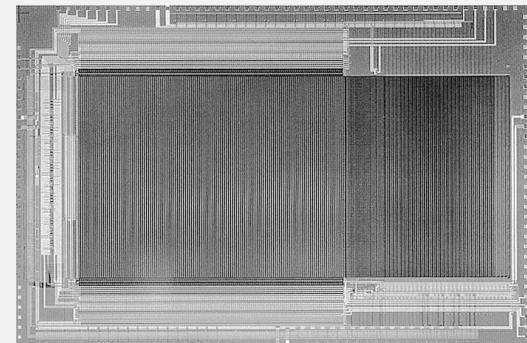
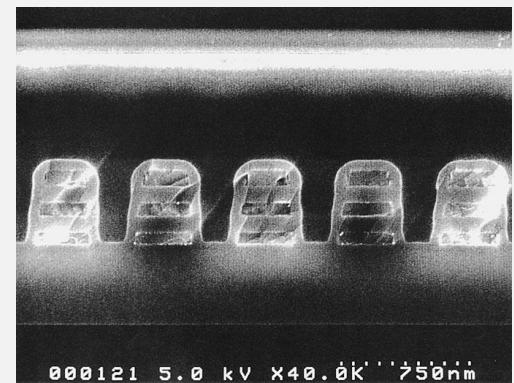
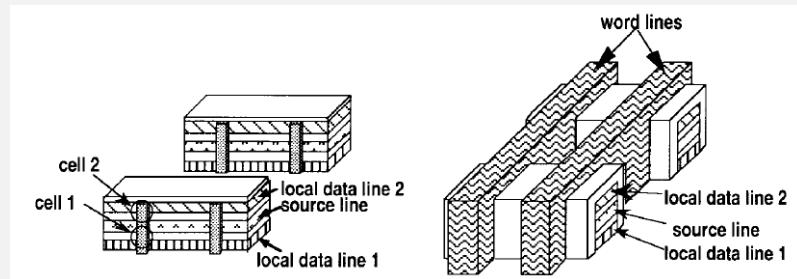
**SET**  
Room-temperature operation in 1993  
Yano, (Hitachi)

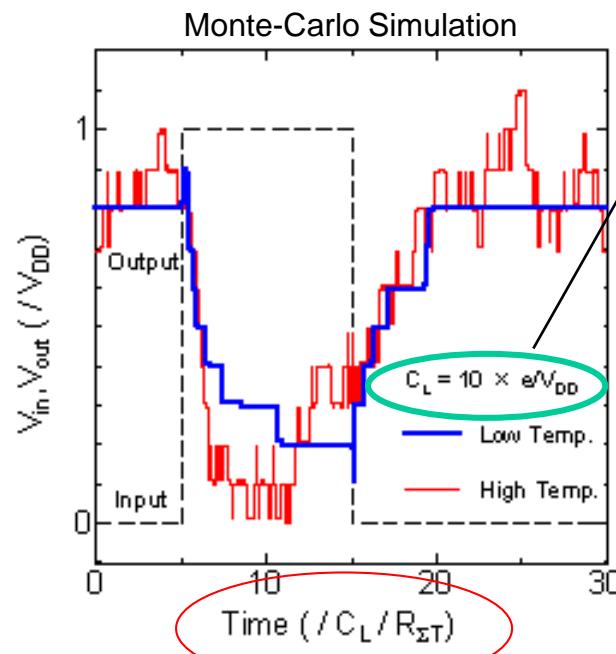
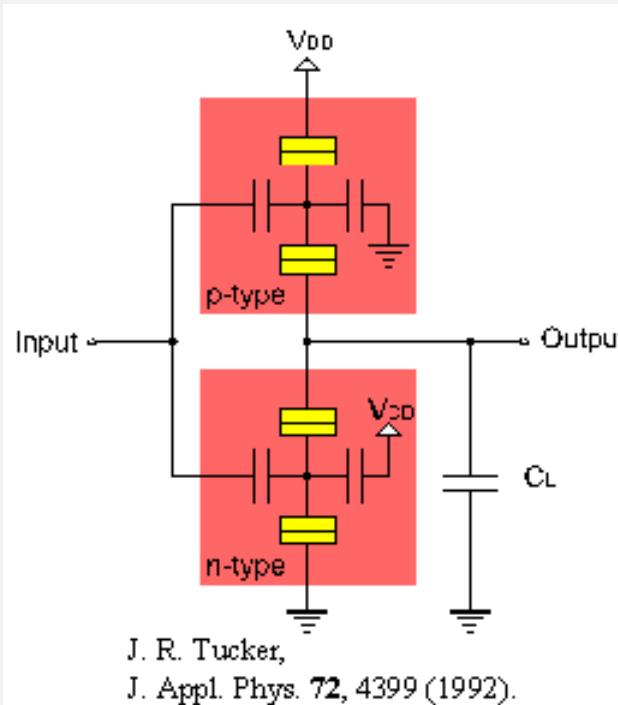


**64-bit array in 1996**



**128 Mb in 1998**



**Single-Electron Inverter:**

simulation for load capacitance = 10 electrons

simulations for all C's = equal value

-output voltage is proportional the charge stored in the load capacitor

- output voltage < V<sub>DD</sub>



no voltage gain -> no stage drive

Simply expressed:  
a few electrons will always be lost to charge parasitic capacitances



**BUT ...**

Tucker (1992) also showed,  
that a SET- logic gatter will not  
have any FANOUT >1

because of 2 tunnel junctions with R~25 kΩ

$$\text{SET: } RC \sim 10^{-18} F * 50 \text{ k}\Omega = 0.05 \text{ psec}$$

$$\text{CMOS: } RC \sim 10^{-15} F * k\Omega = 1 \text{ psec}$$

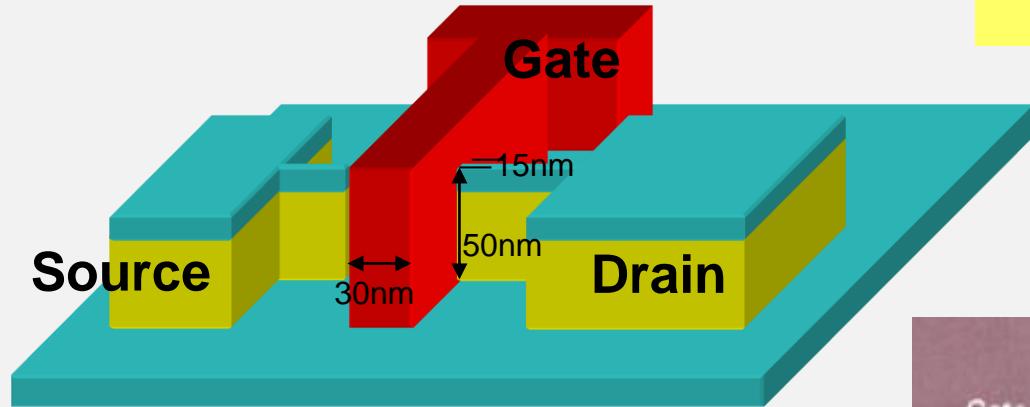


intrinsically high output impedance ( $R_{\text{Tun}} > 50 \text{ k}\Omega$ ) makes SET not much faster than CMOS

and the main problem is not the device but the interconnects with  $RC > RC_{\text{device}}$  !

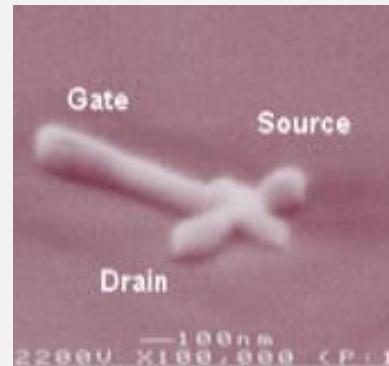
\* have a view on midterm horizons (next 10 - 15 years) of industrial fabricated devices

- \* based on fabrication capability (continuous shrinking)
- \* based on high reproducibility ( $10^{18}$  devices per day)
- \* based on high yield (better 90 %)
- \* based on high reliability (10 years)
- \* based on exponential decreasing fabrication costs

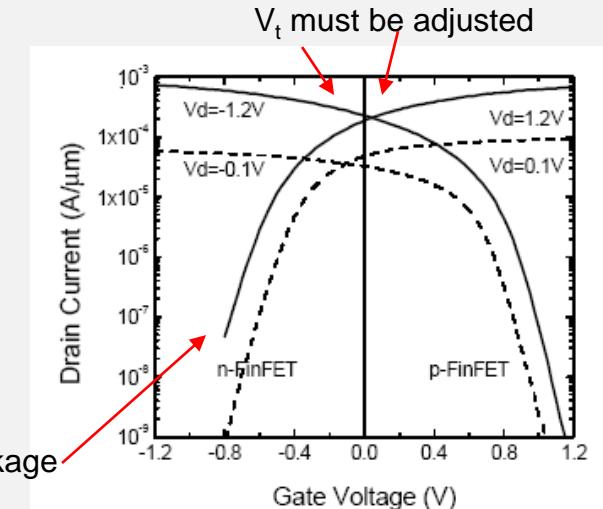


$L = 10 \text{ nm}$  shortest channel length demonstrated

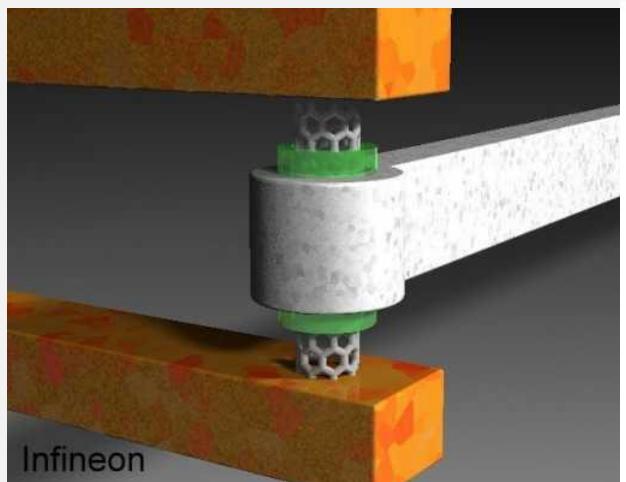
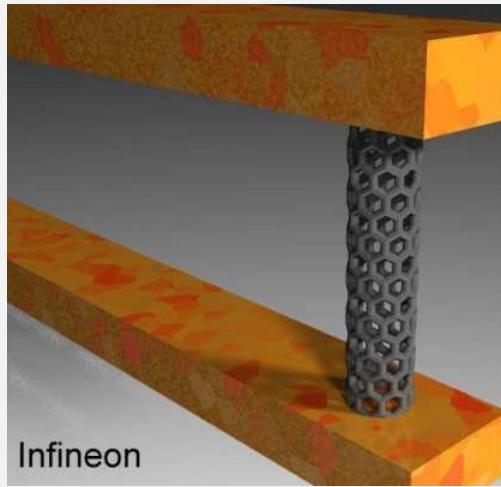
$T_{Si} = 12 \text{ nm}$



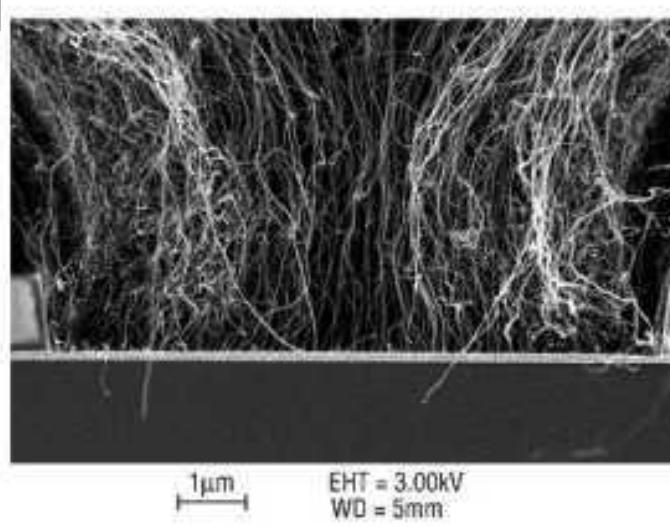
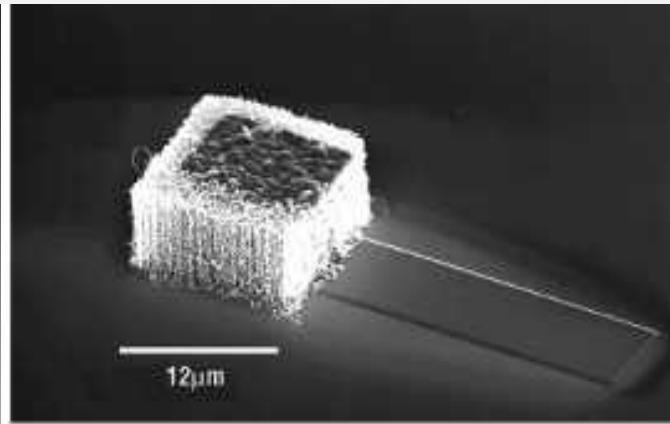
and with leaving some money to the company !



\* many dreams and hopes on long term scale (next 20 -40 years) and many efforts to compete with CMOS !

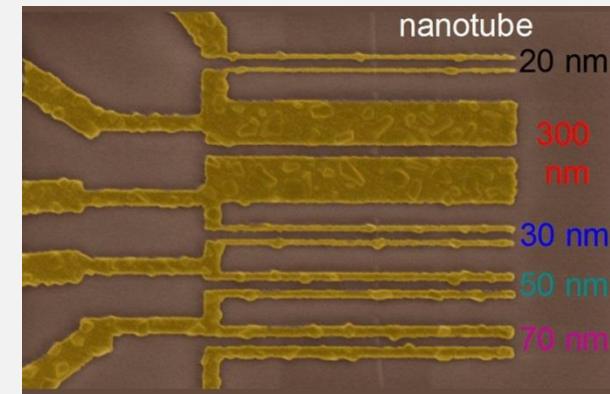


This is the dream

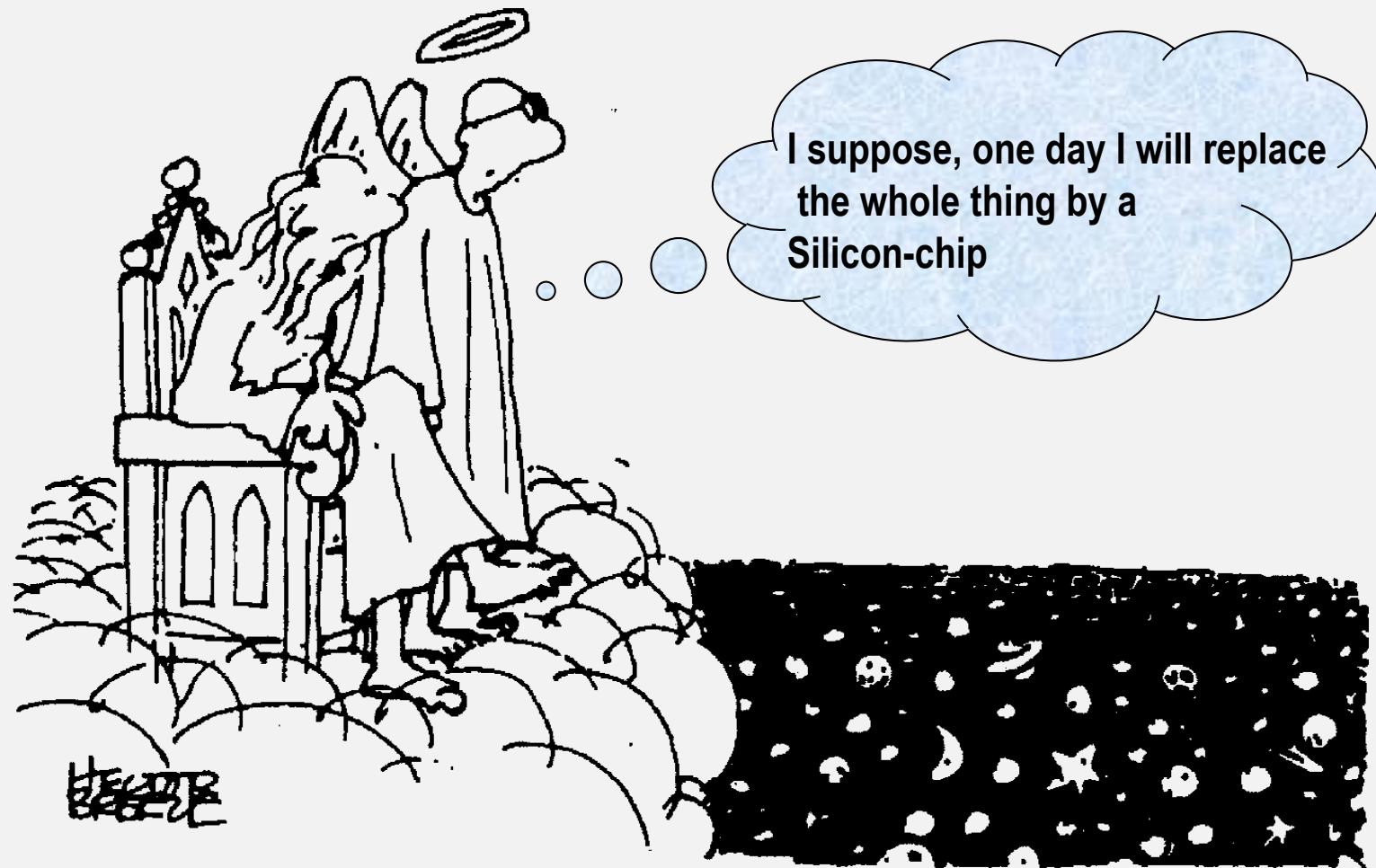


This is still reality

**IBM's carbon nanotube breakthrough takes processors beyond silicon 2015**



Density is still to low  
Missing information:  
- IV-characteristics  
- Reliability



## After all: there will be an examination

The content on the transparencies is very detailed, to understand all the interrelations for your own work.

In the examination you should demonstrate a good understanding of the content.

Just take part in the examination without visiting the lecture is not recommended.

Nearly all examination questions may be answered in a few words. This sounds easy, but then every word must be correct.

Don't be shy to show your large knowledge by little paintings or equations.

### **The examination will be in written form, 1h, no aids .**

Every participant will receive 9 examination sheets, 2-3 questions per sheet.

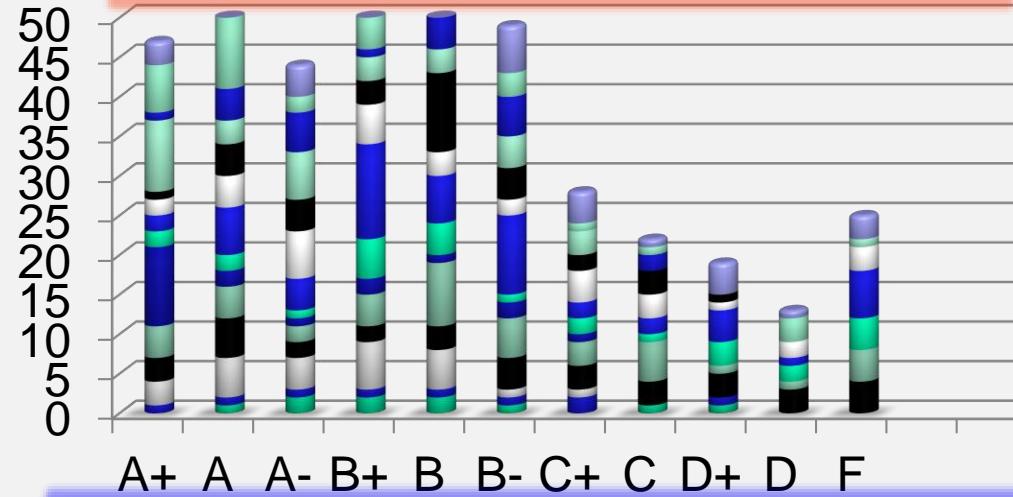
Each complete answer will result in 2 points, if several answers are needed, the points will be splitted (see example next page). sometimes the answer may be only one word.

! For bosh following the motto, something correct will be in the answer, you will get 0 points, although there may be something correct !

The working time per sheet will be some minutes.

Per sheet around 6 points may be achieved, this are 40 points maximum!

To pass the exam at least 40% of points must be achieved !



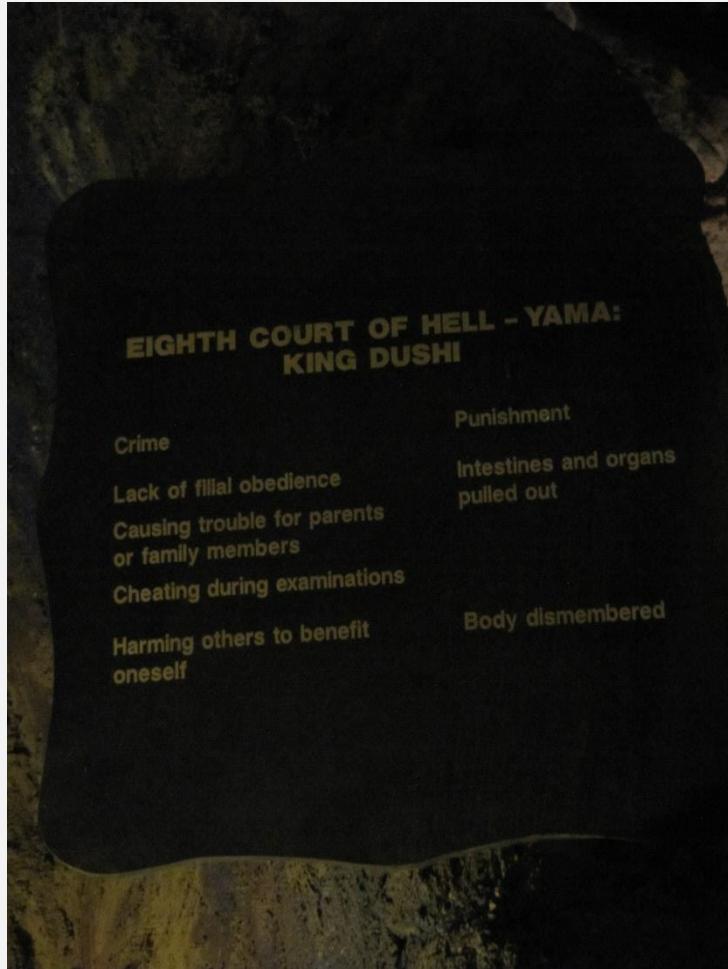
- AdMOS GIST 2019
- AdMOS GIST 2018
- AdMOS GIST 2017
- AdMOS GIST 2016
- AdMOS GIST 2015
- AdMOS GIST 2014
- AdMOS GIST 2013
- AdMOS GIST 2012
- AdMOS GIST 2011
- AdMOS GIST 2010
- AdMOS GIST 2009
- AdMOS GIST 2008
- AdMOS GIST 2007
- AdMOS GIST 2006

You decide on your own about your mark with your working effort



Please compare this distribution of marks with other lectures to find out your needed working effort

## Cheating during examinations



You will end in the Eighth Court of Hell



Intestines and organs will be pulled out

# Example of Examination Questions

a) What is the market share for MOS-Technology compared to other technologies?

85 %

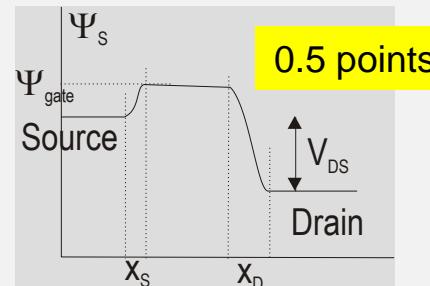
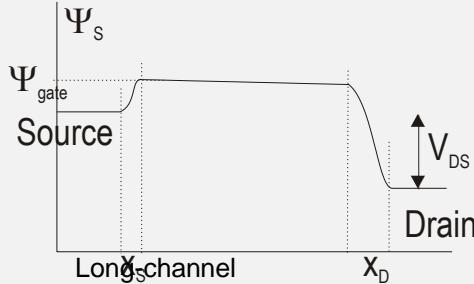
2 points

b) Which tunneling effects may be observed in classical MOSFETs?

Gate tunneling, direct S/D tunneling, GIDL

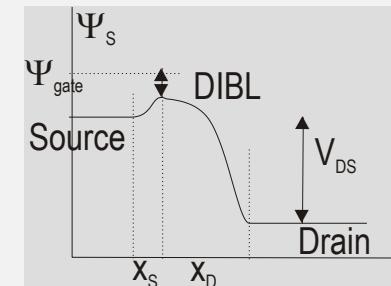
2 points

c) Which two models are used to describe the short-channel MOSFET ? Give the names and a short description.



**Charge-sharing model (Yau)**  
 \* depletion zones of S/D already deplete large part of channel  
 \* channel barrier still ok -> lower  $V_t$

0.5 points

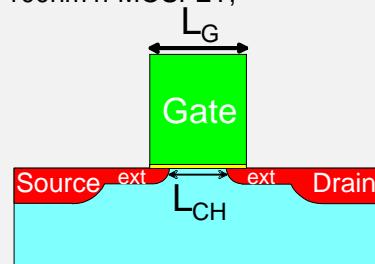


**DIBL model**  
 \* depletion zones of S/D already deplete channel  
 \* barrier is lowered -> lower  $V_t$

0.5 points

d) Calculate the intrinsic switching time of a 100nm n-MOSFET, use the highest possible carrier velocity.

remember:  $1\text{nm} = 10^{-7}\text{cm}$



$$\tau_{\text{transit}} = \frac{L_{ch}}{v} = \frac{L}{\mu \cdot E} \approx \frac{L^2}{\mu \cdot V_{DS}}$$

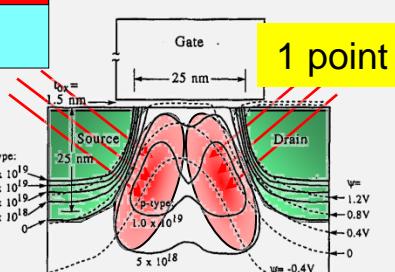
1 point

$$\tau_{\text{transit}} = \frac{L_{ch}}{v} = \frac{100\text{nm}}{10^7 \text{cm/sec}} = \frac{10^{-5} \text{cm}}{10^7 \text{cm/sec}} = 10^{-12} \text{sec} = 1\text{ps}$$

1 point

e) Give a schematic picture of a so-called Halo-MOSFET, add values for scales.

Which problems may be solved with Halo, which problems arise?



Halo will reduce short-channel effects  
 -> threshold voltage will be independent of  $V_{DD}$

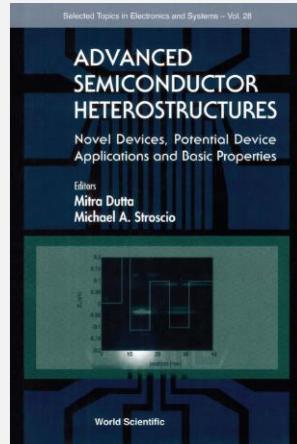
problems: nm-implantation and avoiding diffusion during recrystallization

1 point



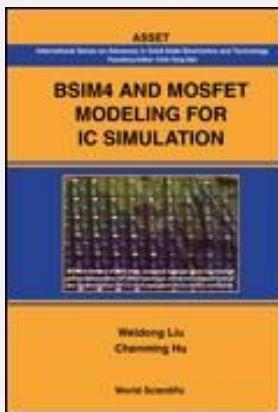
This book explains the physics and properties of multi-gate field-effect transistors (MuGFETs), **how they are made and how circuit designers can use them** to improve the performances of integrated circuits. It covers the emergence of quantum effects due to the reduced size of the devices and describes the evolution of the MOS transistor from classical structures to SOI (silicon-on-insulator) and then to MuGFETs.

2010, 356 pages  
~ 135 USD



This book also illustrates **how new carrier-transport phenomena are made possible** through the use of advanced semiconductor heterostructures. Semiconductor heterostructures are playing a fundamental role in the continuing down scaling of electronic and optoelectronic device features into the nanodimensional regime. The diversity of heterojunctions as well as dramatic advances in semiconductor growth and processing technologies are opening the way to new hetero junction-device technologies and leading to many new avenues for realizing novel families of quantum-based electronic and optoelectronic devices and systems.

2003, 240 pages, ~ 122 USD



This book presents the art of **advanced MOSFET modeling for integrated circuit simulation and design**. It provides the essential mathematical and physical analyses of all the electrical, mechanical and thermal effects in MOS transistors relevant to the operation of integrated circuits. Particular emphasis is placed on how the BSIM model evolved into the first ever industry standard SPICE MOSFET model for circuit simulation and CMOS technology development.

Special attention is paid to **MOSFET characterization and model parameter extraction methodologies**, making the book particularly useful for those interested or already engaged in work in the areas of semiconductor devices, compact modeling for SPICE simulation, and integrated circuit design.

2011, 436 pages, ~ 104 USD

## Integrated Circuit Design and Green Electronics

# The End of Overview

This lecture on

## Advanced MOSFETs and Novel Devices

A Look at the Future Development of Industrial Semiconductor Devices