

## 7.1 Motivation for Hot Carrier Devices

## 7.2 Overview of Hot Carrier Devices

Fabrication Technology: Epitaxy  
Examples of Hot Carrier Devices

## 7.3 The Planar-Doped Barrier FET (PDBFET)

Fabrication  
Electric Field Tailoring  
Modification of Charge Carrier Transport  
Experimental IV-Characteristics  
Low-temperature Physical Transport Effects

## 7.4 The Impact Ionization MOSFET (IMOS)

Advantage as Steep-Slope Device  
Working Principle  
Experimental Devices  
Circuit application  
Outlook

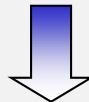
## 7.5 Spintronics

Spin Valve Transistor  
Magnetic RAM

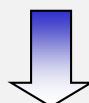
For future applications the devices:

- ▶ should be faster,
  - ▶ consume less power
  - ▶ and be cheaper  
(smaller footprint)
- than today's devices

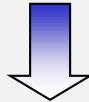
Why faster ?



most realtime applications  
need huge amounts of  
computational power

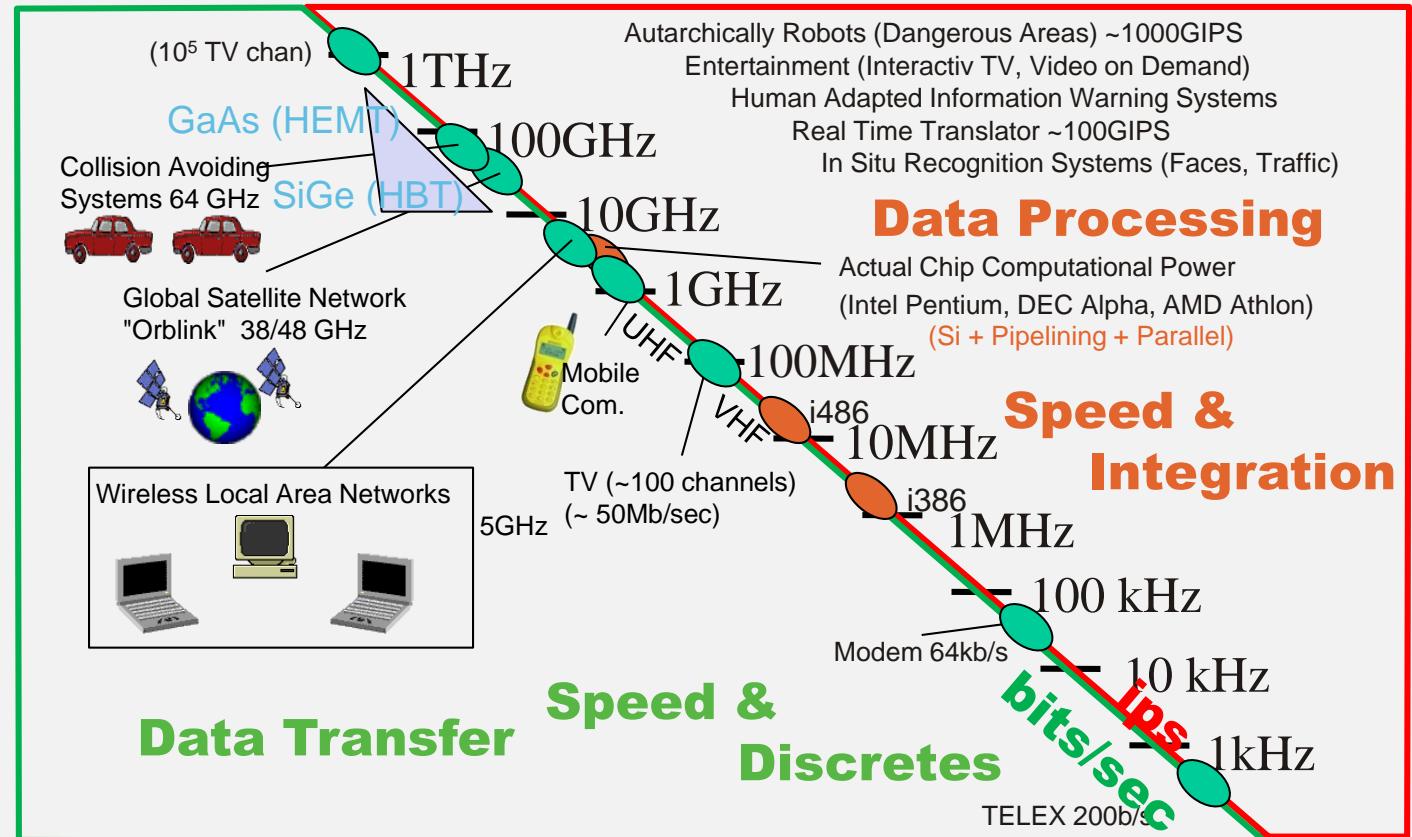


fast devices and ULSI



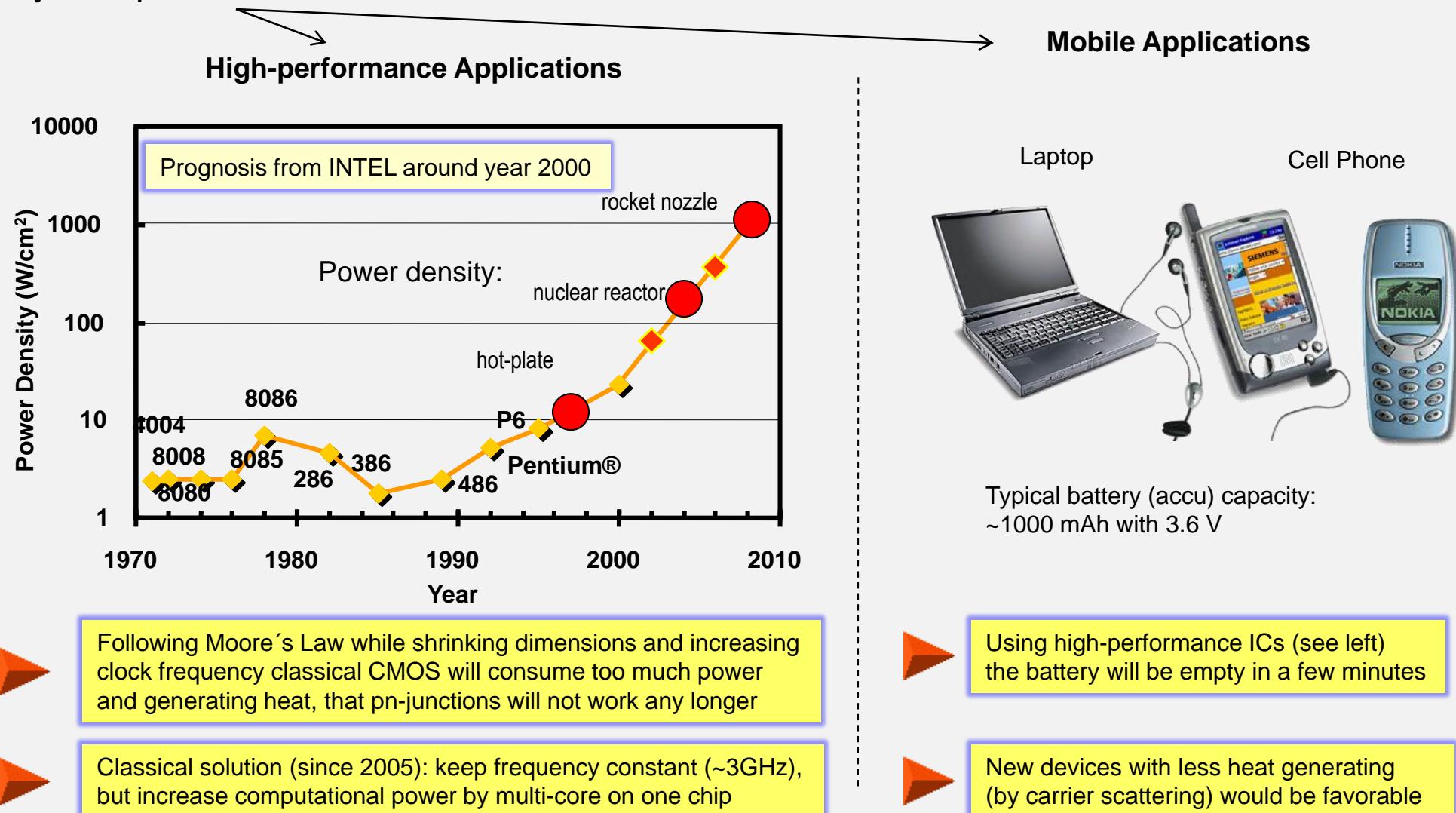
Power-Delay-Product  
(= energy per switching)

$$E = P \cdot \tau = V \cdot I \cdot f$$

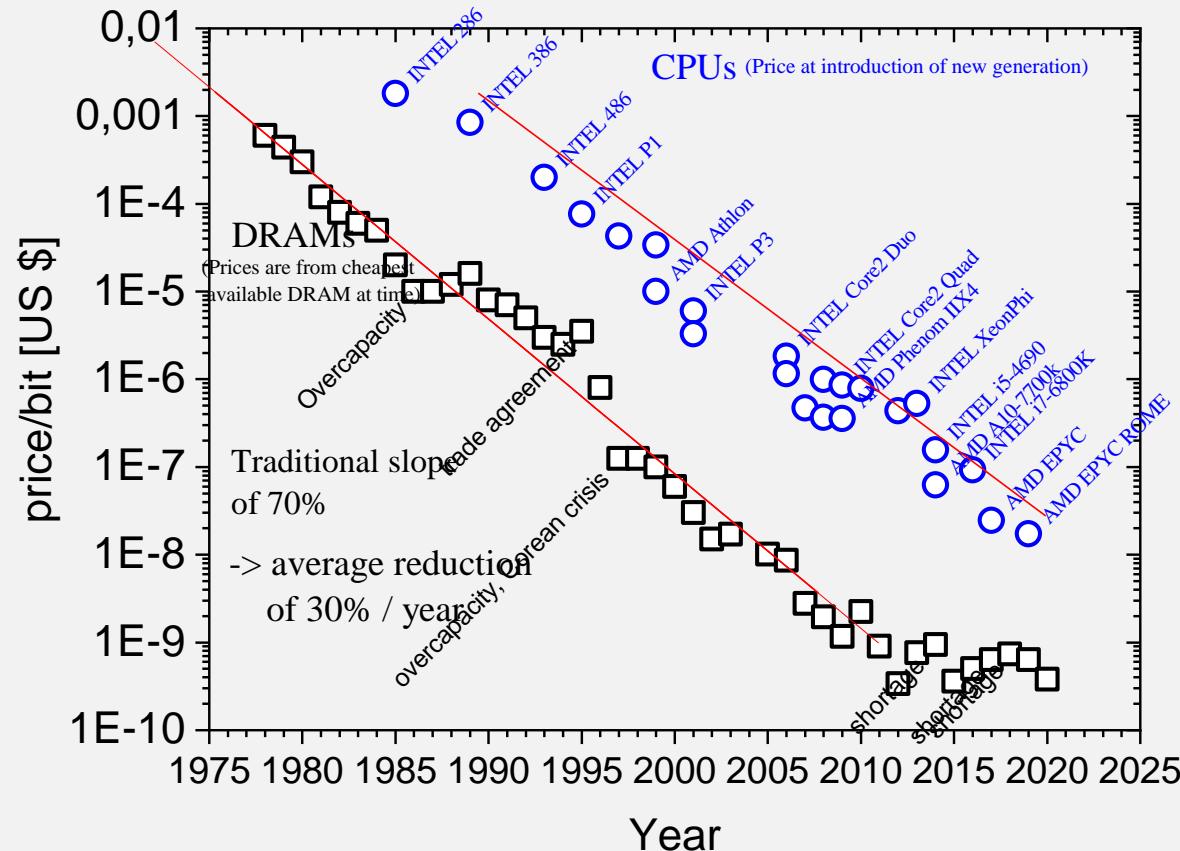


But: due to Power-Delay-Product "faster" results in higher power consumption and heat generation

Why less power ?



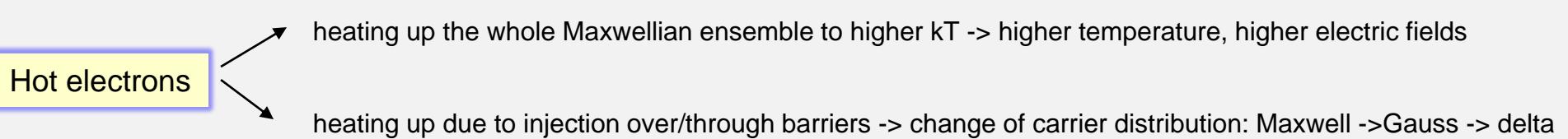
why cheaper ?



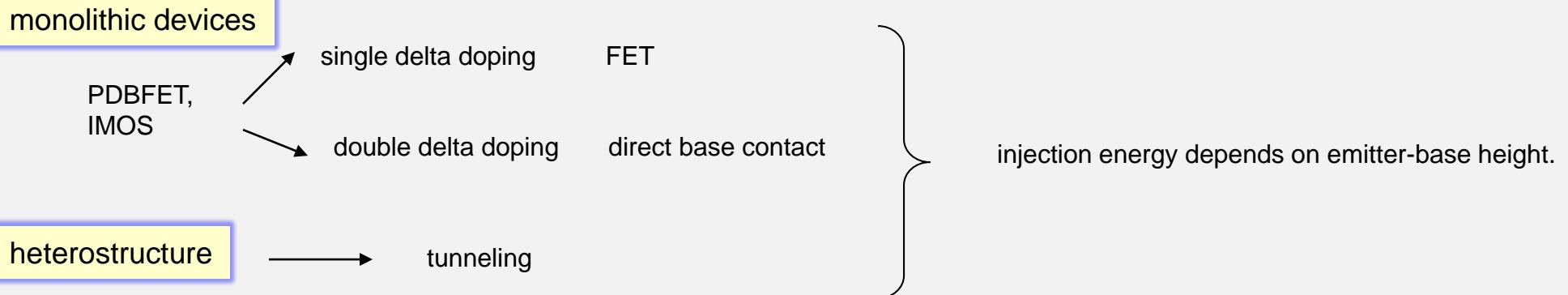
In 2019 a MOSFET function cost around  $10^{-10}$  \$US in memory and about  $10^{-8}$  \$US in MPUs

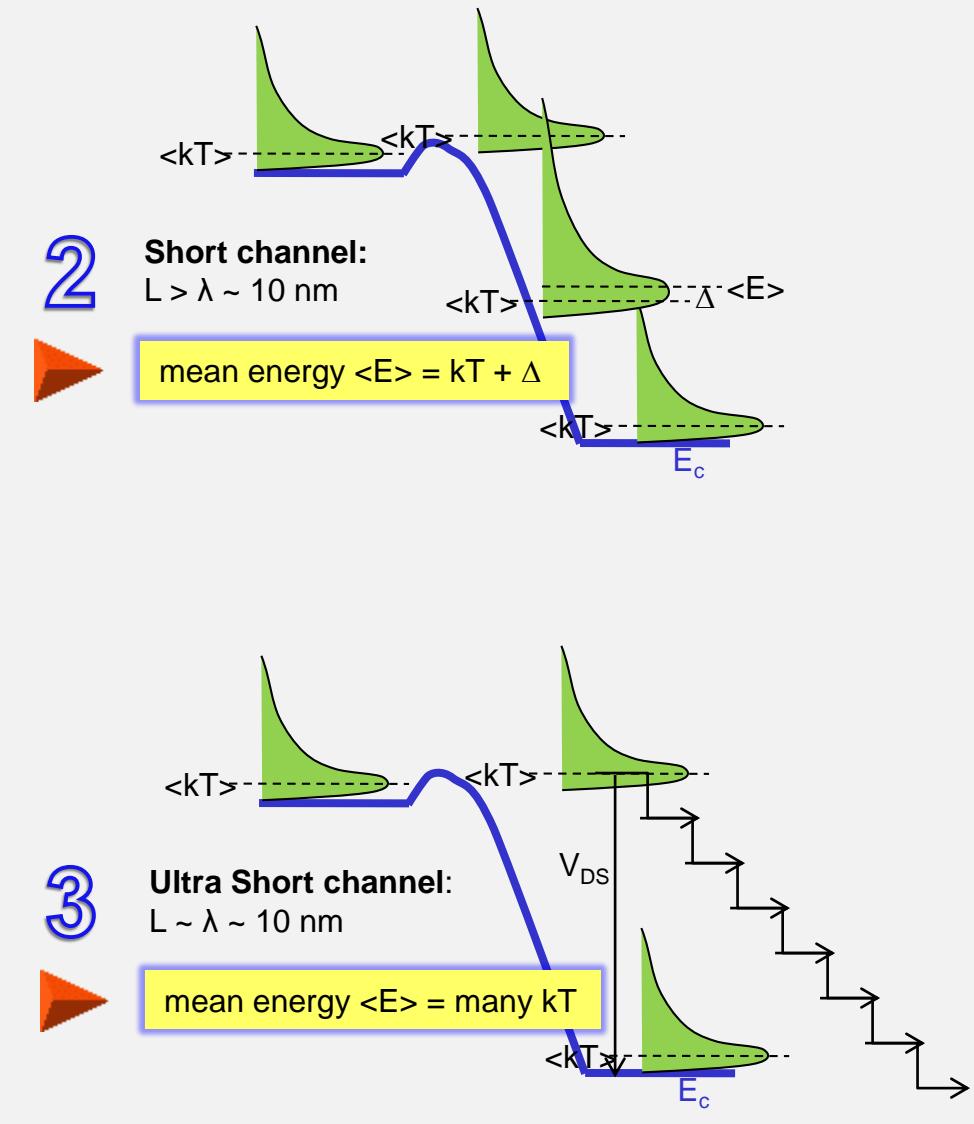
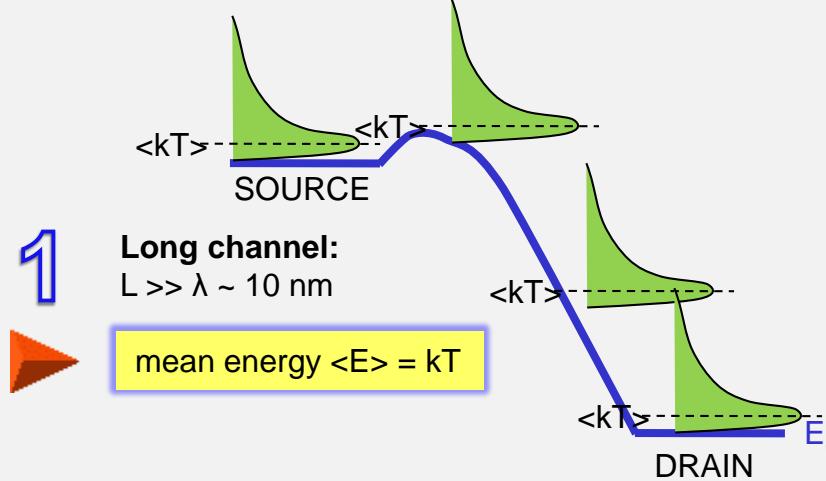
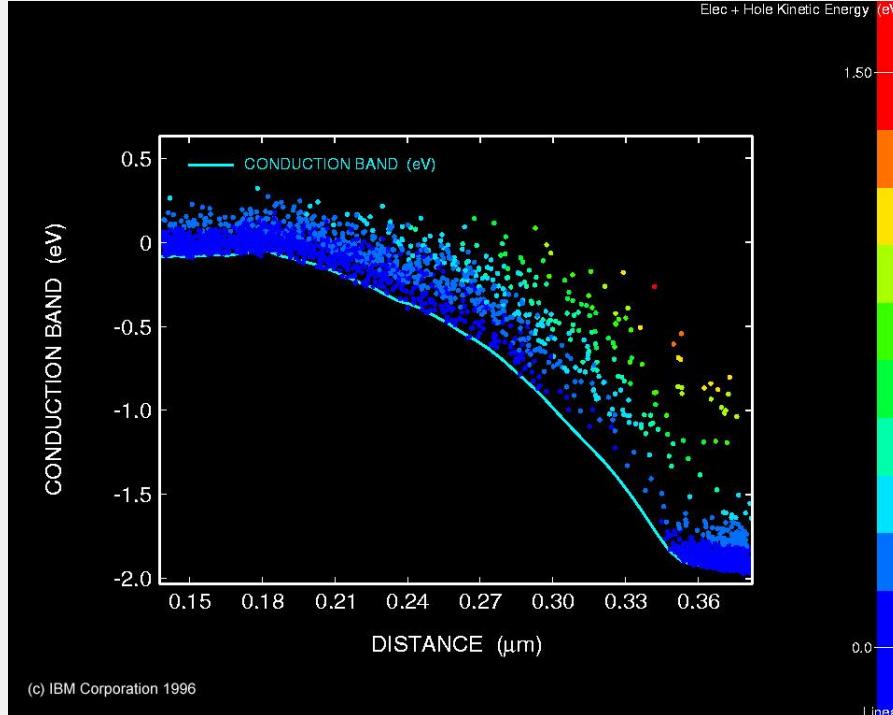
We have seen, that small geometries are necessary, but in achieving minimum geometries some physical limitations may exist.

Another approach of achieving high-speed devices is to speed up carrier velocity by somewhat relaxed geometries



Basically we can do this in:





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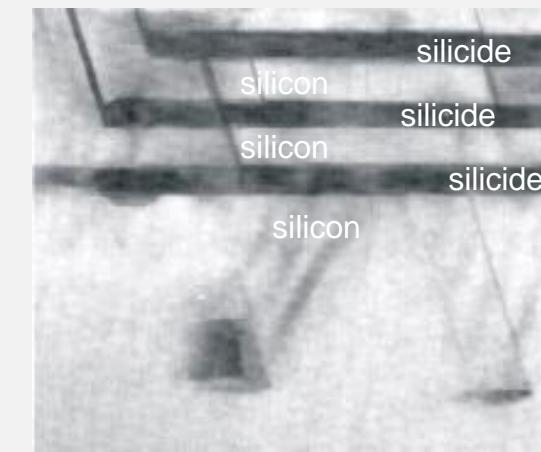
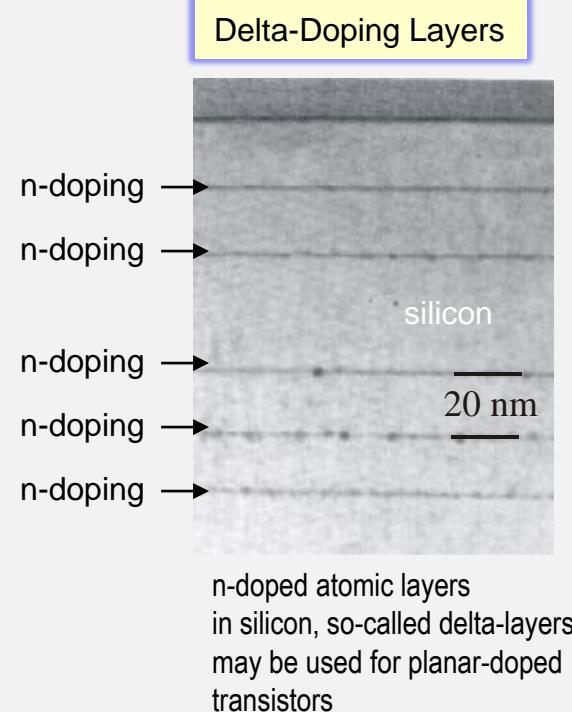
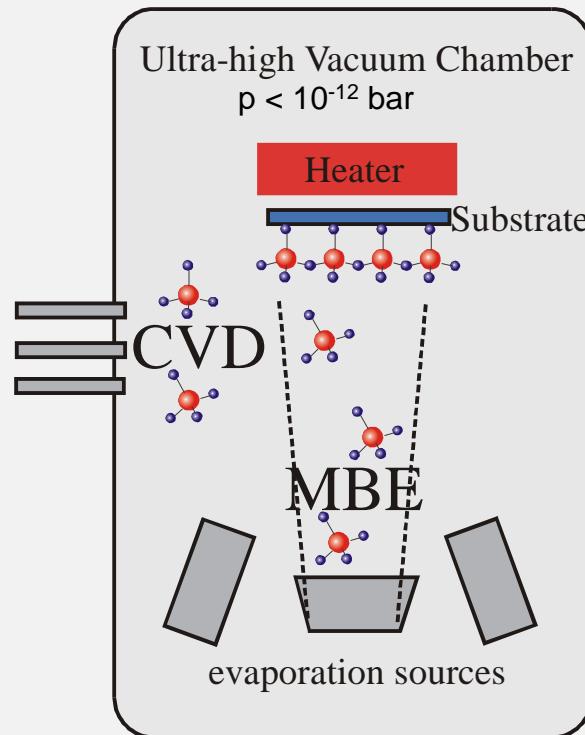
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The technique of Molecular Beam Epitaxy (MBE) was developed around 1975 for Silicon and III-V semiconductors. This was possible due to the development of commercial ultra-high vacuum (UHV) pumping systems.



In MBE the materials are heated to the melting points. The evaporated atoms can reach in UHV the substrate without collisions or reactions with rest vacuum molecules. On clean crystalline substrates the incoming atoms can find regular lattice positions and proceed crystal growth.

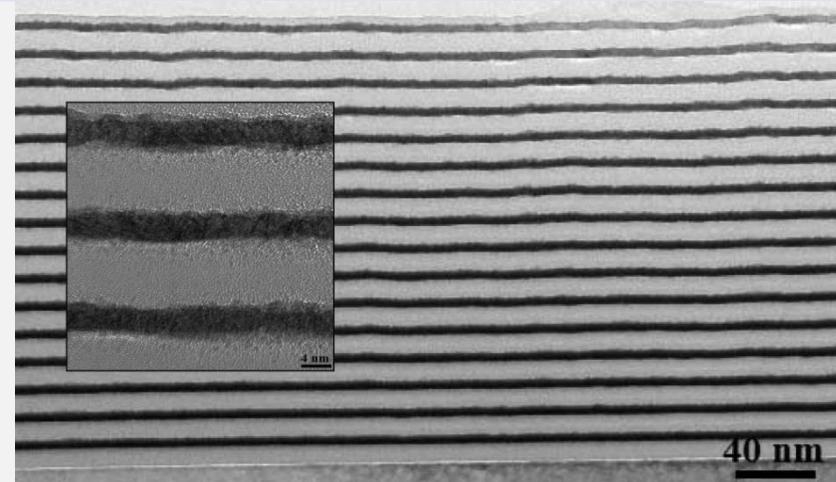
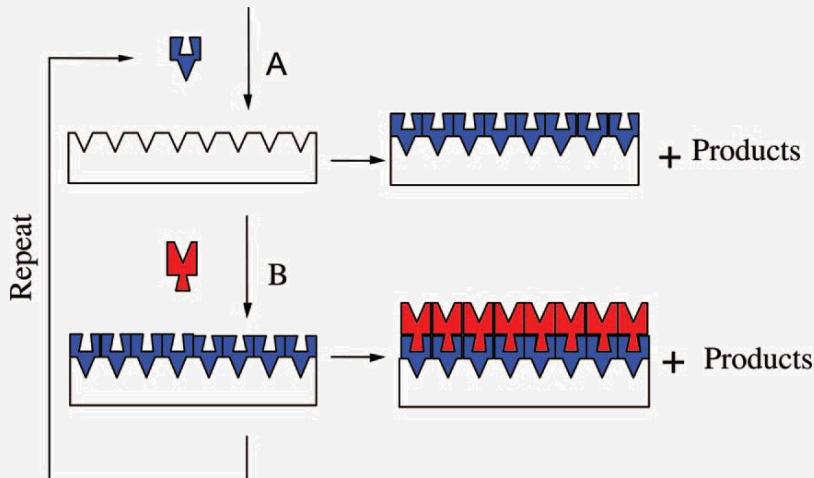
MBE offers the possibility of controlled deposition of atomic layers



Vertical devices with nm-layers can be fabricated without sophisticated lithography

ALD is a self-limiting (the amount of film material deposited in each reaction cycle is constant), sequential surface chemistry that deposits conformal thin-films of materials onto substrates of varying compositions. Due to the characteristics of self-limiting and surface reactions, ALD film growth makes atomic scale deposition control possible. ALD is similar in chemistry to chemical vapor deposition (CVD), except that the ALD reaction breaks the CVD reaction into two half-reactions, keeping the precursor materials separate during the reaction. By keeping the precursors separate throughout the coating process, atomic layer control of film growth can be obtained as fine as  $\sim 0.1 \text{ \AA}$  ( $10 \text{ pm}$ ) per cycle. Separation of the precursors is accomplished by pulsing a purge gas (typically nitrogen or argon) after each precursor pulse to remove excess precursor from the process chamber and prevent 'parasitic' CVD deposition on the substrate.

ALD can be used to deposit several types of thin films, including various oxides (e.g.  $\text{Al}_2\text{O}_3$ ,  $\text{TiO}_2$ ,  $\text{SnO}_2$ ,  $\text{ZnO}$ ,  $\text{HfO}_2$ ), metal nitrides (e.g.  $\text{TiN}$ ,  $\text{TaN}$ ,  $\text{WN}$ ,  $\text{NbN}$ ), metals (e.g.  $\text{Ru}$ ,  $\text{Ir}$ ,  $\text{Pt}$ ), and metal sulfides (e.g.  $\text{ZnS}$ ).



TEM image of a 16-bilayer  $\text{Al}_2\text{O}_3/\text{W}$  superlattice  
Fabreguette, F. H.; Wind, R. A.; George, S. M. *Appl. Phys. Lett.* **2006**, 88, 013116.

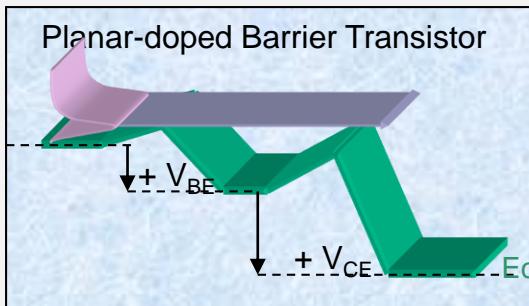
Si and Ge ALD were both demonstrated on silicon and germanium surfaces. However, a difficulty with Si and Ge ALD is their nucleation on other types of surfaces. Si and Ge are both very reactive and easily react with oxygen from oxide substrates to form  $\text{SiO}_2$  or metals from metallic substrates to form silicides. Consequently, the nucleation of Si and Ge ALD is very difficult.

**The nucleation problems have limited the surface chemistry for Si and Ge ALD to only silicon and germanium surfaces.**

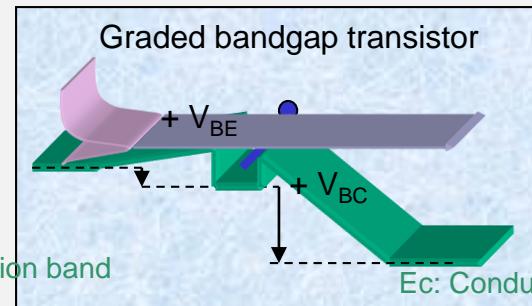
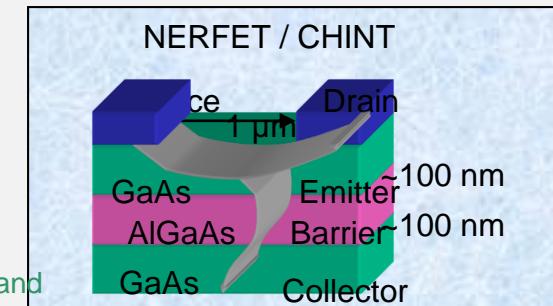
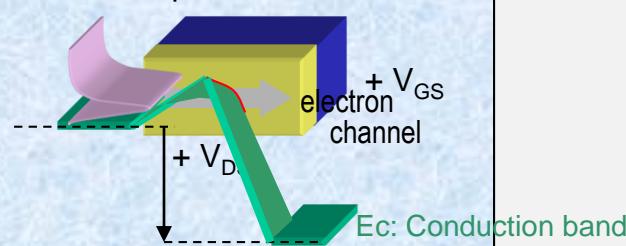
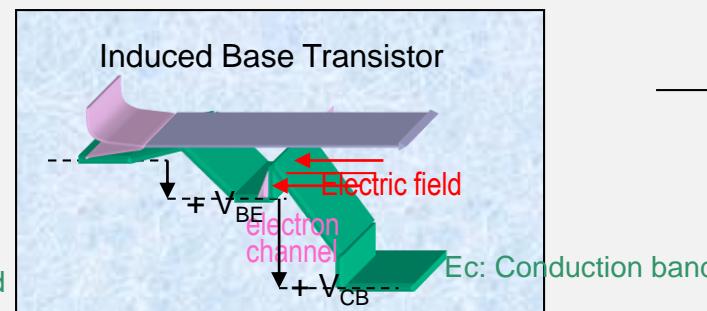
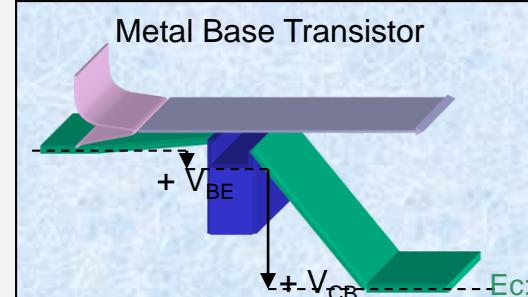
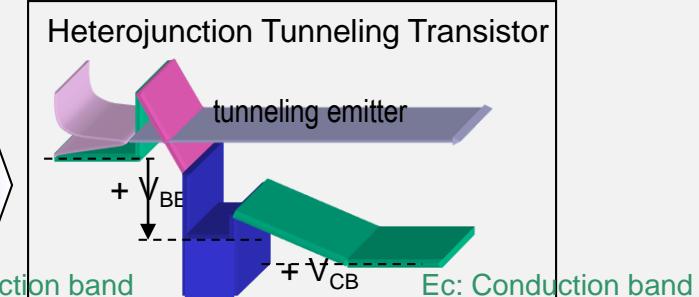
## Examples of "Hot Electron Transistors"

**"Jet"- devices**

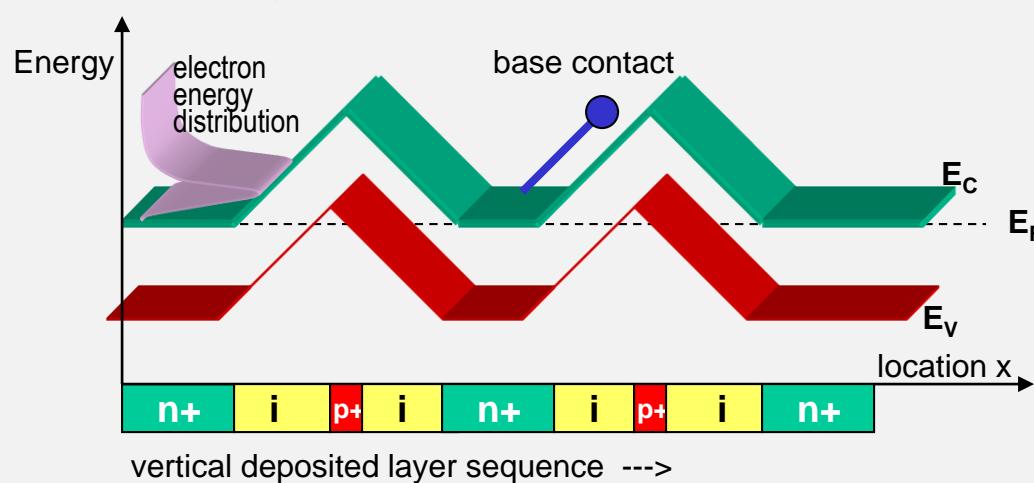
monolithic



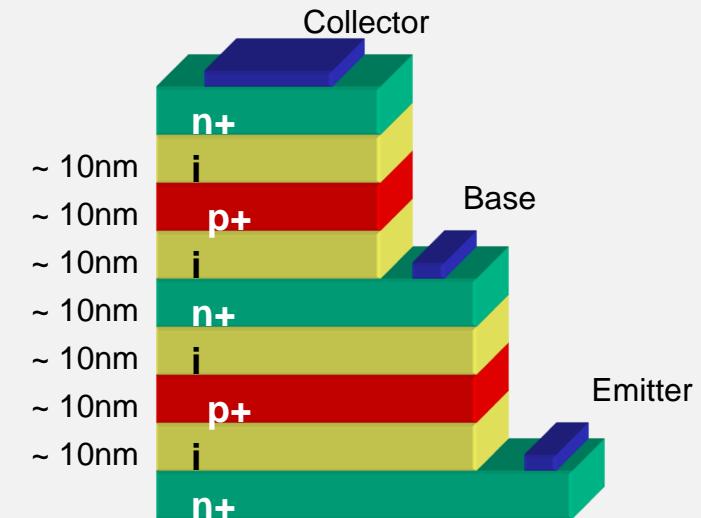
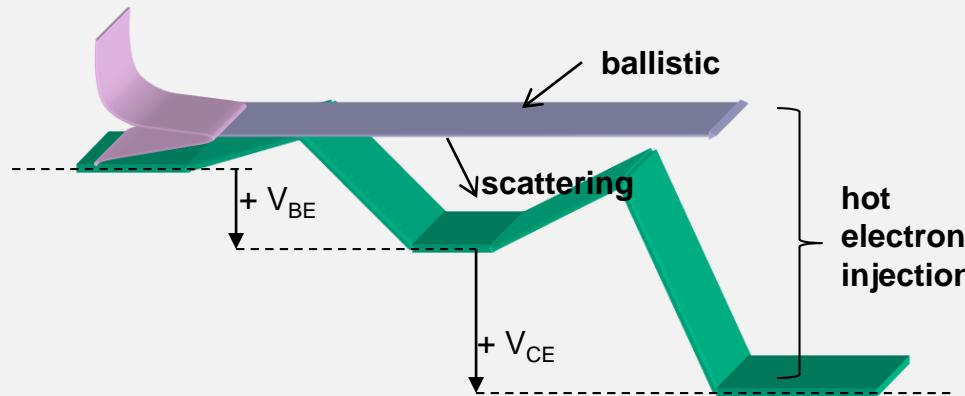
heterostructures

**real space-charge transfer devices****Planar-doped Barrier FET****Induced Base Transistor****Variation with Schottky-Emitter****Heterojunction Tunneling Transistor**

Band diagram in equilibrium



Band diagram under forward bias

Fabrication:

Deposition of thin, doped semiconductor layers by epitaxy

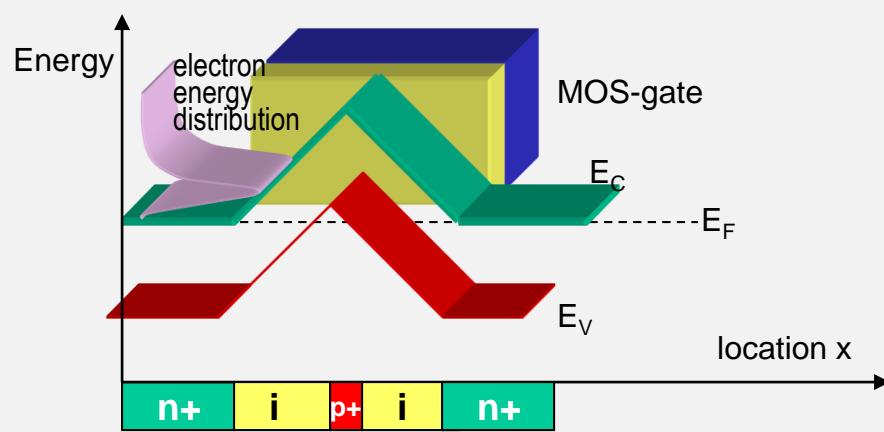
Advantage:

- \* homogeneous semiconductor structure (single-crystalline)
  - > no problems with fabrication
- \* high volume current through whole cross section

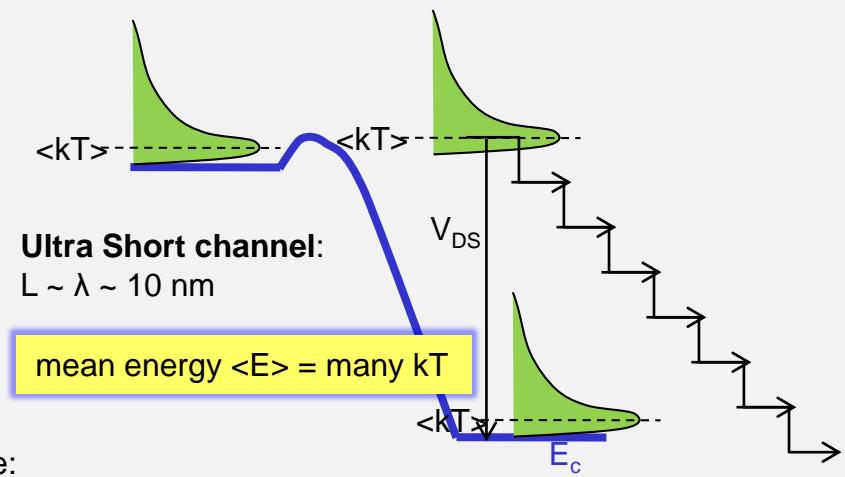
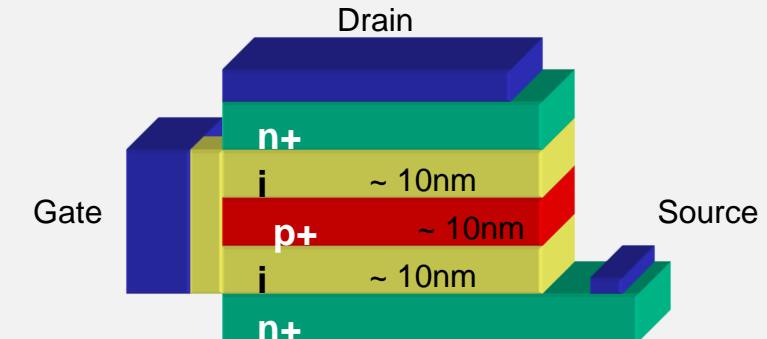
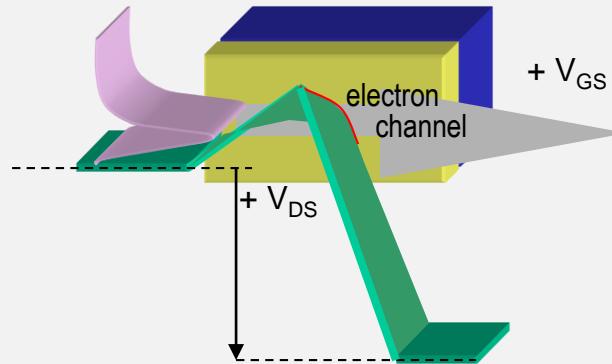
Disadvantage:

- \* thin, doped base -> high resistivity
- \* many epi-layers -> high thermal budget -> no sharp layers
- \* both downhill intrinsic regions are necessary to prevent tunneling between p+ und n+ base
  - > long base -> high probability of scattering -> loss of ballistics

Band diagram in equilibrium



Band diagram under forward bias



3

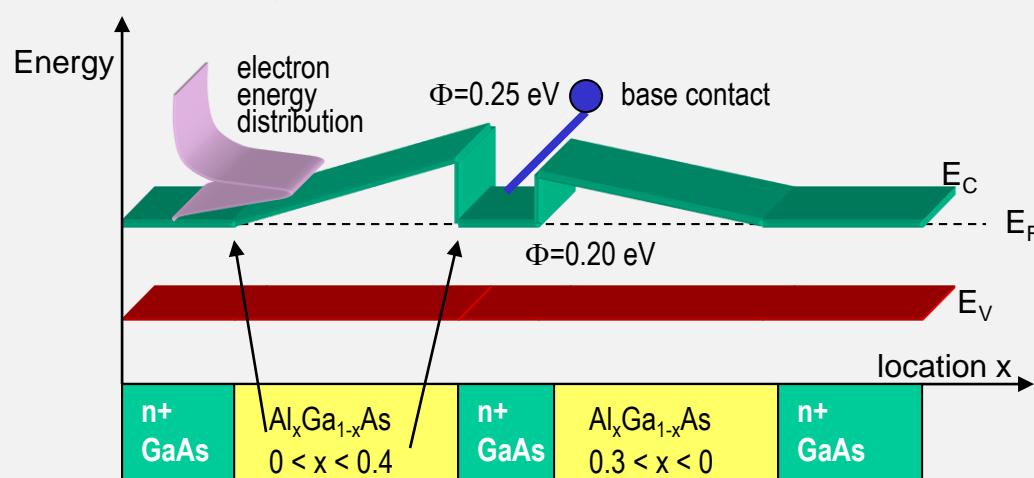
Ultra Short channel:  
 $L \sim \lambda \sim 10 \text{ nm}$ mean energy  $\langle E \rangle = \text{many } kT$ Advantage:

- \* homogeneous semiconductor structure  
-> no problems with fabrication
- \* MOS device -> good for mainstream
- \* shorter dimensions as PDBT -> less scattering -> higher current

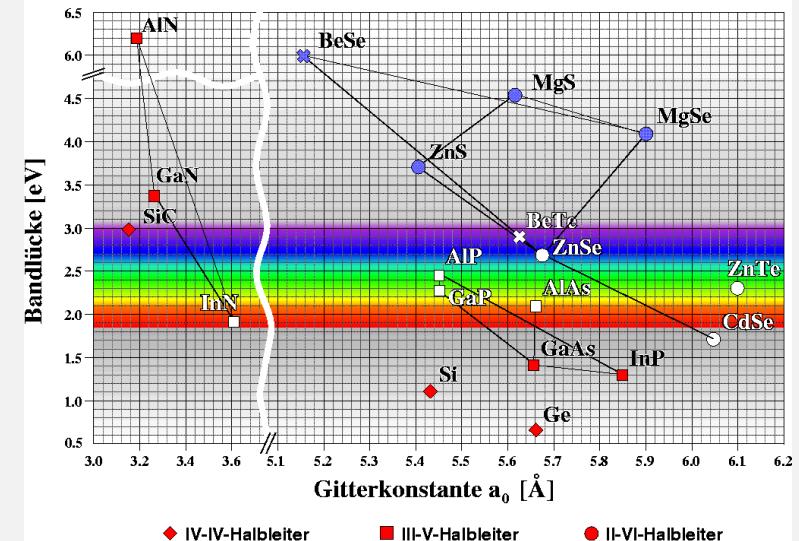
Disadvantage:

- \* higher leakage, because only 1 barrier
- \* reduced current drive because current is 2-dim MOS-channel

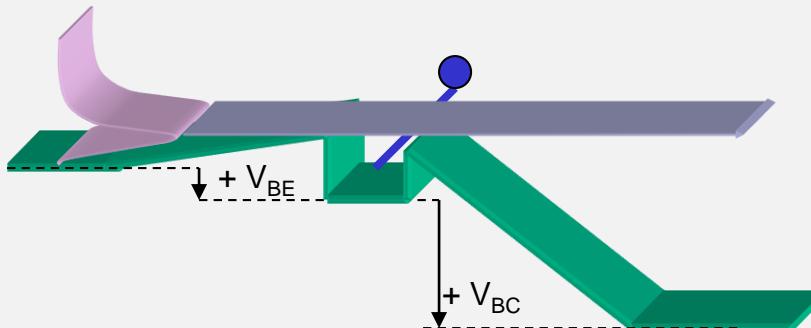
Band diagram in equilibrium



Bandlücke als Funktion der Gitterkonstante



Band diagram under forward bias

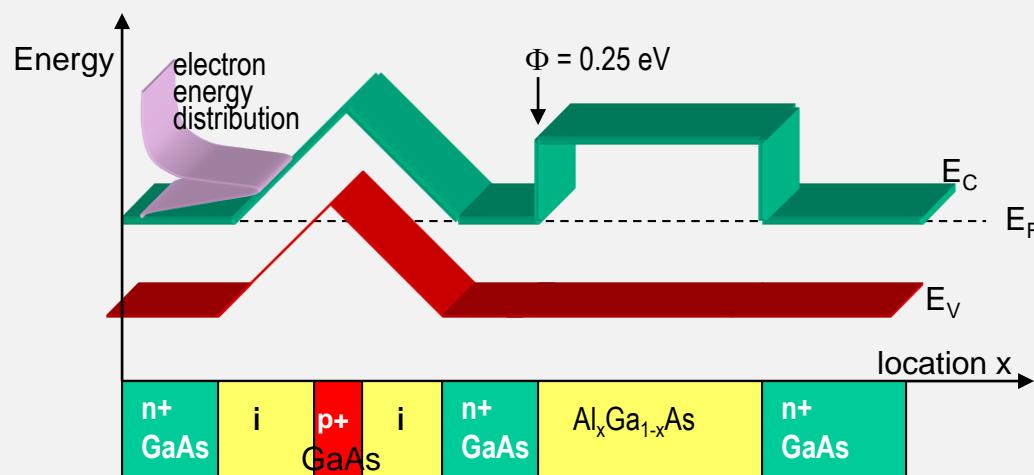
Advantage:

- \* well-established compound semiconductor technology  
(-> nearly monolithic)
- \* only 1 kind of doping (n)

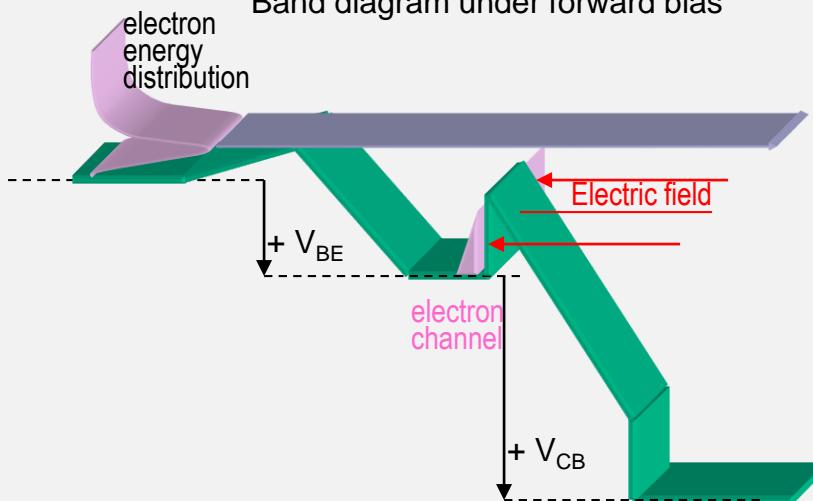
Disadvantage:

- \* very low barrier -> high leakage current

Band diagram in equilibrium



Band diagram under forward bias

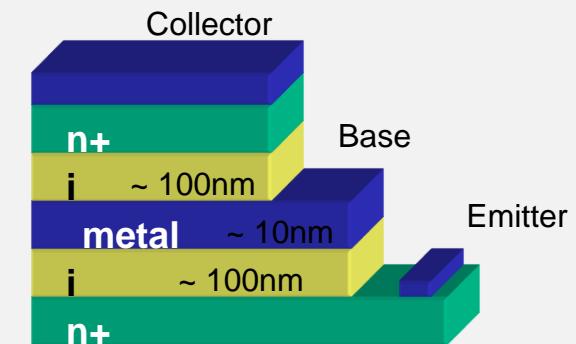
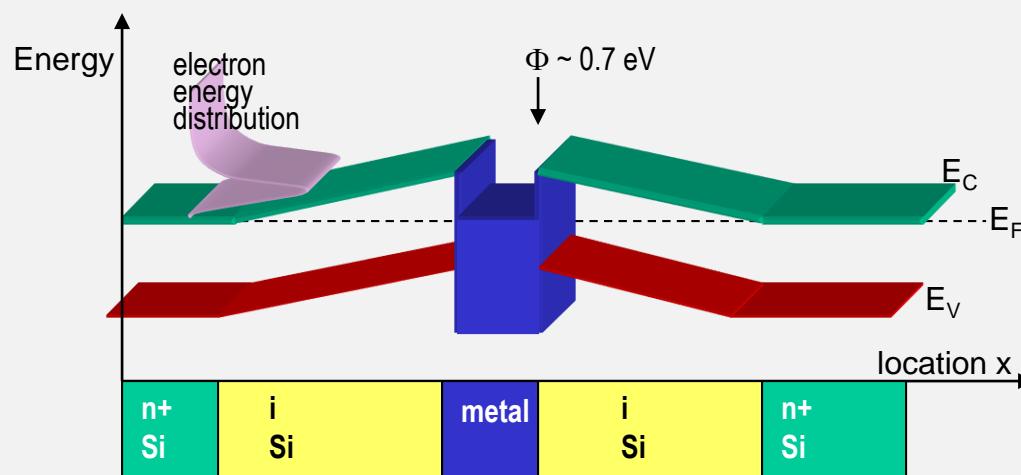
Advantage:

- \* well-established compound semiconductor technology  
(-> nearly monolithic)
- \* using electron channel -> maybe 2 devices in one ?

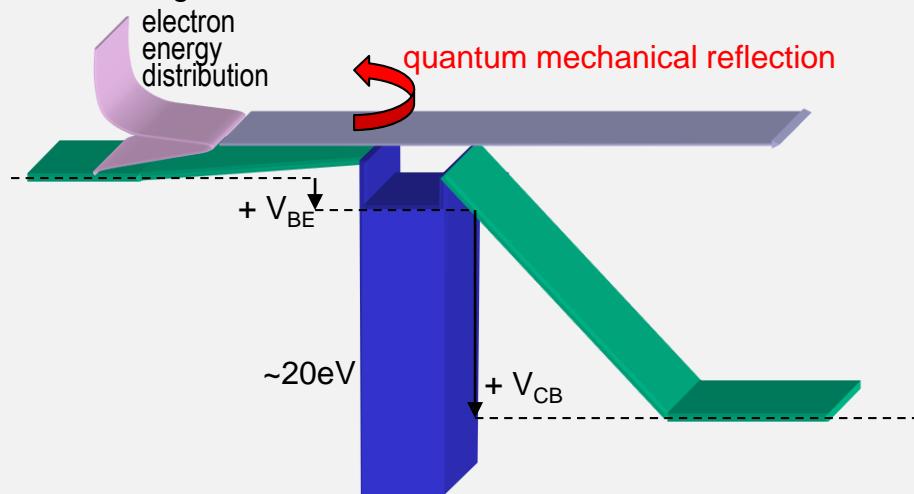
Disadvantage:

- \* longer active region -> higher scattering -> lower current

Band diagram in equilibrium



Band diagram under forward bias

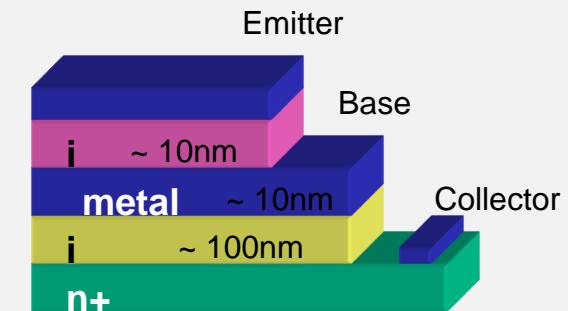
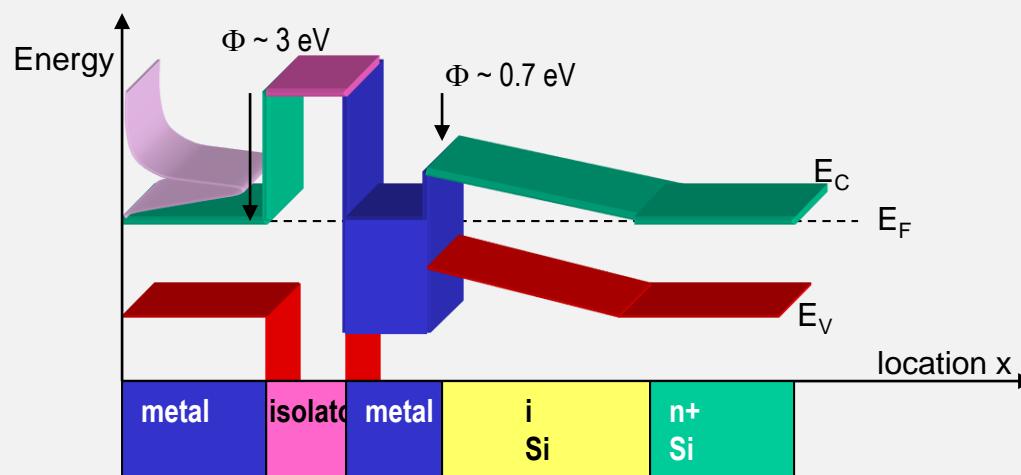
Advantage:

- \* very fast, due to metal base switching

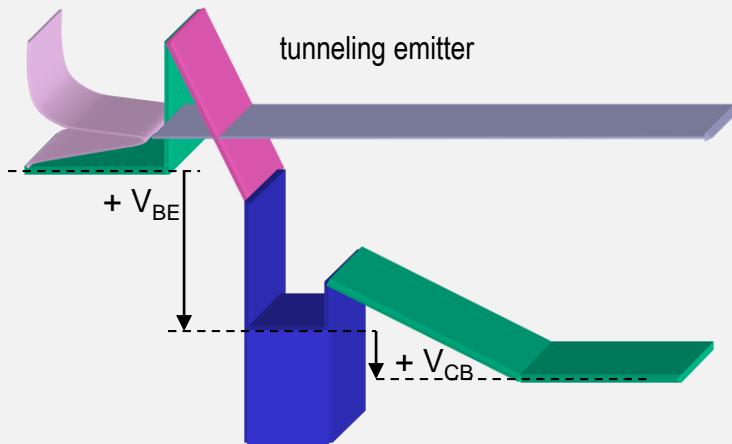
Disadvantage:

- \* various materials -> no good epitaxy -> many defects -> yield
- \* deep metal conduction band -> qm reflection at base -> no current

Band diagram in equilibrium



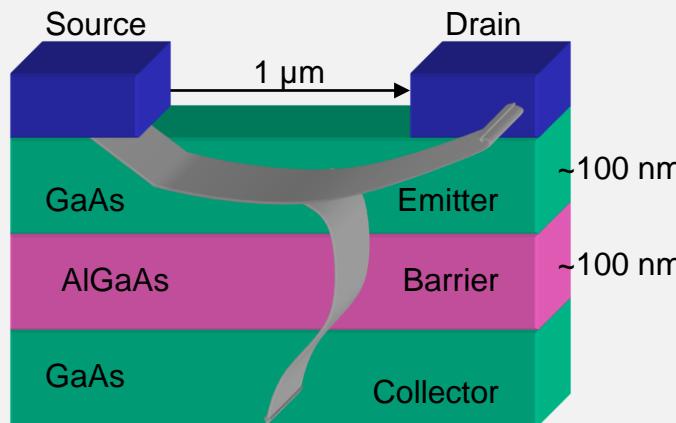
Band diagram under forward bias



## Problem in fabrication:

- \* Thin film high quality layers must be deposited at high temperatures  
-> usually interreactions between materials -> destruction of device
- \* if fabricated in GaAs/AlGaAs the emitter barrier is low ( $<0.3\text{eV}$ )  
-> tunneling current overruled by thermionic emitter current

Basic structure:



For the CHINT/NERFET various geometries and materials are proposed:

Kastalsky/Luryi, EDL-4(9), (1983)334

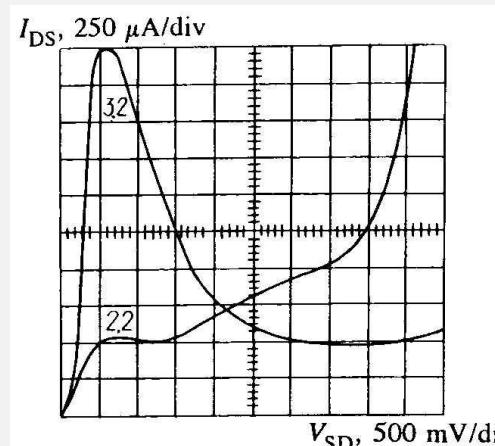
Kastalsky et al., Appl.Phys.Lett.48 (1986)71  
-> GaAs/AlGaAs, fT=29GHz, gm= 1S/mm, delay ~ 30psec

Operation:

Increasing  $V_{DS}$  the electrons are accelerated from Source to Drain. If the energy of the electrons is high enough to overrun the barrier two effects take place:

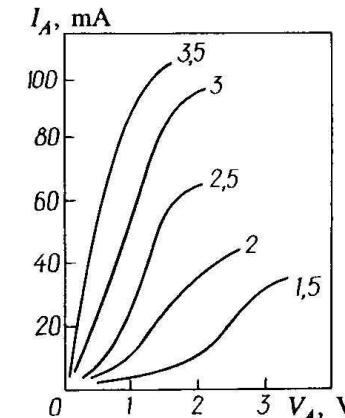
NERFET (Negative Resistance Field-Effect Transistor)  
looking at the Source-Drain current:

the Drain-Source current decreases with higher  $V_{DS}$   
because of missing electrons, which are now collected by  
the collector.



CHINT (Charge Injection Transistor):  
looking at the emitter-collector current

dependent on the  $V_{DS}$  the collector may attract all electrons  
out of the emitter channel

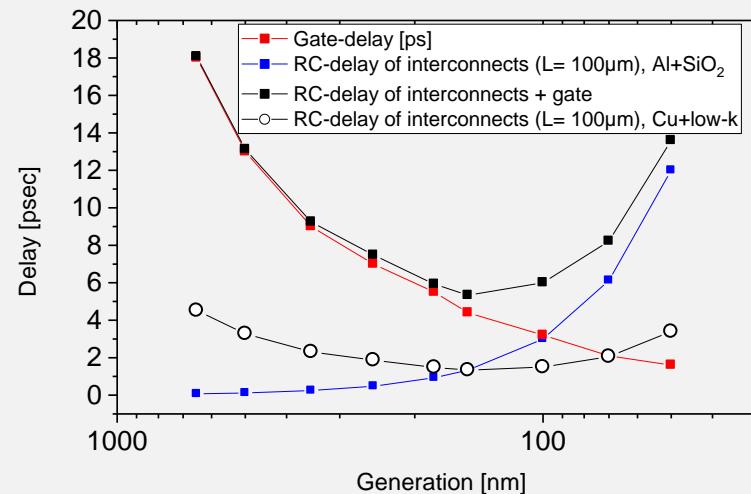


The fabrication argument:

- \* ULSI circuits (needed for high computational power) cannot be fabricated in compound semiconductors, because of high intrinsic defect densities ( $\sim 10^4 \text{ cm}^{-2}$ , Si: 1 defect on ten 300mm wafer) -> no yield
- > **ULSI circuits will be fabricated in Si-technology**

The speed argument:

- \* MOSFETs today (year 2015, channel length  $\sim 14 \text{ nm}$ ) are in the range of a few psec for gate delay.
- > in ULSI circuits the speed limiting factor is RC-delay of interconnects (same order of delay)
- > **no need for faster ULSI devices when limited by interconnect RC**



values from ITRS roadmap 1999

- \* Extrapolating CMOS to 10 nm channel length (which seems the limit today, year 2015), the active regions of MOSFETs are in the same dimension as needed for Hot-electron devices
- > the switching speed will be the same
- > **no advantage for Hot-Electron devices in high-speed circuits when CMOS does the same**
- > other advantages: lower leakage, lower  $V_T$ , higher  $I_{on}$  ????

The economical argument:

**Compared to silicon CMOS, the fabrication costs of ULSI compound semiconductor circuits is too high for consumer application**

Hot-Electron Devices seemed to be attractive within the past 20 years

(1980: ability to fabricate such devices by inventing MBE to 2000: forecast to end CMOS at 0.1 $\mu\text{m}$  channel length)

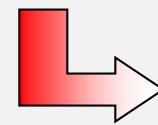
But today (year 2015), when 10 nm MOSFETs are looking achievable, there is no speed advantage for Hot-Electron Transistors

Are there additional advantages, which may overrule CMOS ?

Taking into account the fabrication argument and the economical argument a promising candidate should be fabricated in silicon technology

hot electron structures in silicon reduce to two candidates:



 Metal Base Transistor were not successfull,  
a useful one has never been realized  
and certainly not for lack of effort !



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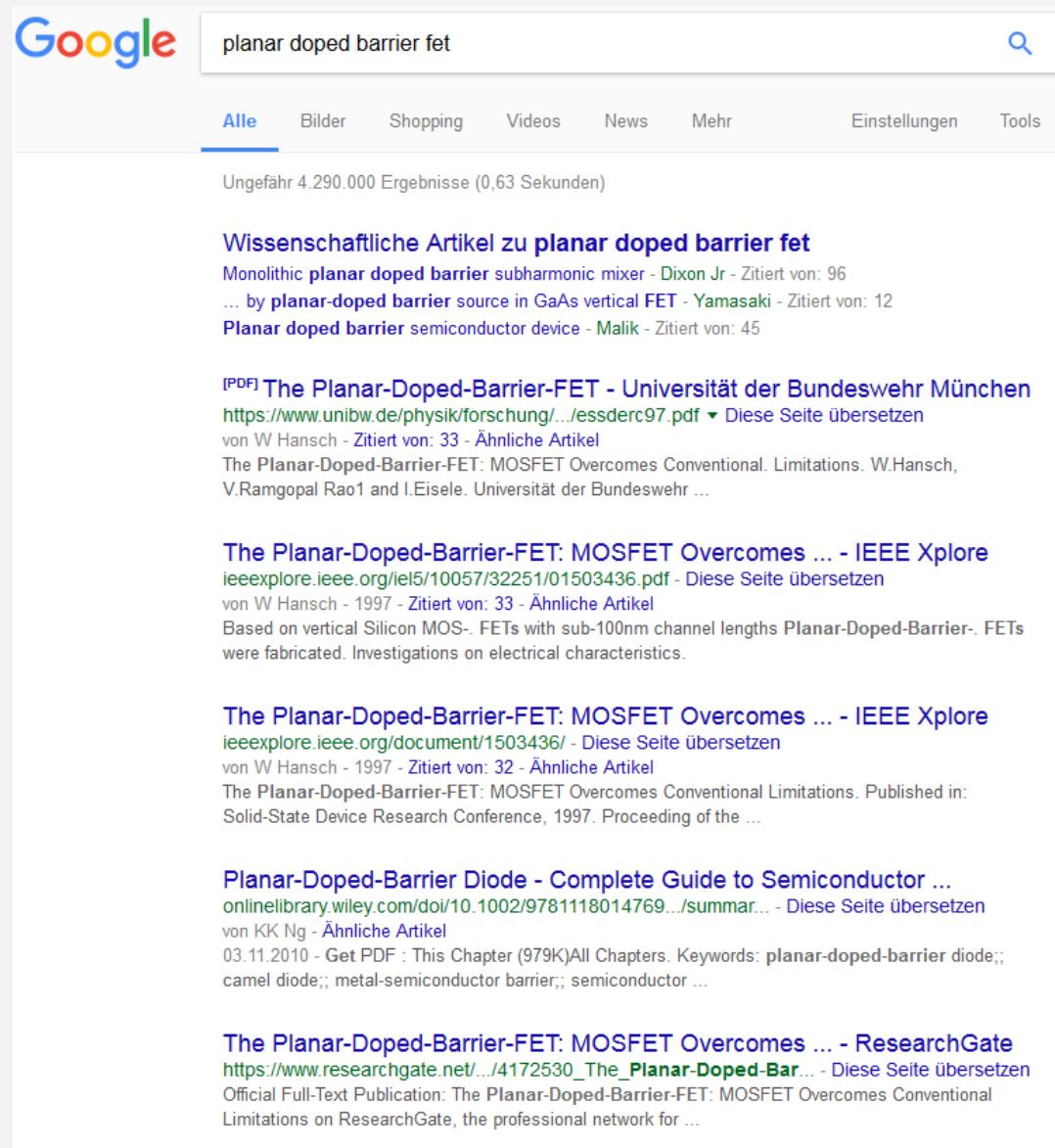
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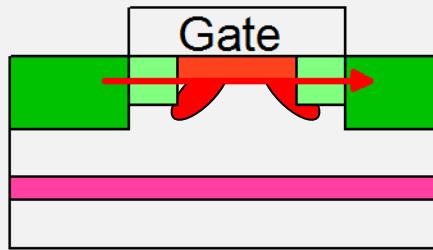
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Magnetic RAM



Google search results for "planar doped barrier fet". The search bar shows the query. Below it, a row of filters: Alle (selected), Bilder, Shopping, Videos, News, Mehr, Einstellungen, Tools. The results section starts with a summary: "Ungefähr 4.290.000 Ergebnisse (0,63 Sekunden)". The first result is a link to a scientific article: "Wissenschaftliche Artikel zu planar doped barrier fet". It includes a snippet: "Monolithic planar doped barrier subharmonic mixer - Dixon Jr - Zitiert von: 96 ... by planar-doped barrier source in GaAs vertical FET - Yamasaki - Zitiert von: 12 Planar doped barrier semiconductor device - Malik - Zitiert von: 45". The second result is a PDF link: "[PDF] The Planar-Doped-Barrier-FET - Universität der Bundeswehr München". It includes a snippet: "The Planar-Doped-Barrier-FET: MOSFET Overcomes Conventional Limitations. W.Hansch, V.Ramgopal Rao1 and I.Eisele. Universität der Bundeswehr ...". The third result is from IEEE Xplore: "The Planar-Doped-Barrier-FET: MOSFET Overcomes ... - IEEE Xplore". It includes a snippet: "The Planar-Doped-Barrier-FET: MOSFET Overcomes Conventional Limitations. Published in: Solid-State Device Research Conference, 1997. Proceeding of the ...". The fourth result is from Wiley: "Planar-Doped-Barrier Diode - Complete Guide to Semiconductor ...". It includes a snippet: "The Planar-Doped-Barrier-FET: MOSFET Overcomes Conventional Limitations. Published in: Solid-State Device Research Conference, 1997. Proceeding of the ...". The fifth result is from ResearchGate: "The Planar-Doped-Barrier-FET: MOSFET Overcomes ... - ResearchGate". It includes a snippet: "Official Full-Text Publication: The Planar-Doped-Barrier-FET: MOSFET Overcomes Conventional Limitations on ResearchGate, the professional network for ...".

### Planar MOSFET



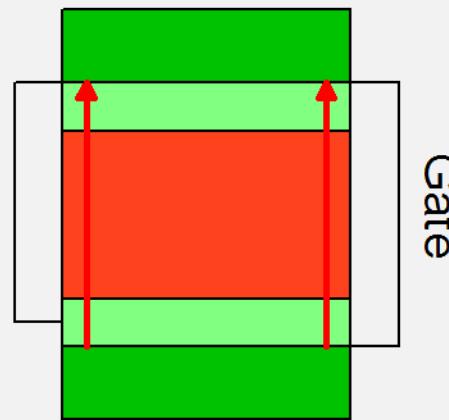
Trouble with  
Electric Fields

Compromise =  
Passive Electric Field  
by Doping Structures

Trouble with  
well-defined structures  
on a nanometer scale

Performance  
Reproducibility

### Vertical MOSFET

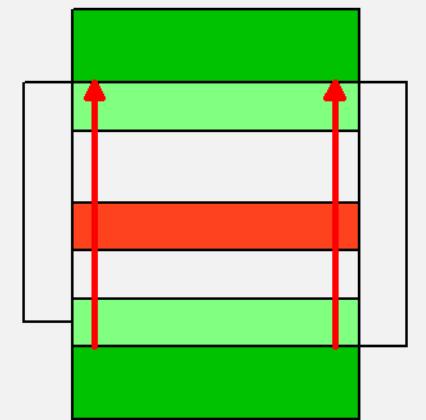


Vertical Concept

MBE

+  
sharp doping profiles  
Performance  
Reproducibility  
Integration

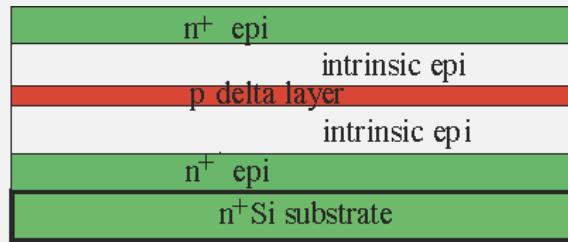
### Vertical PDBFET



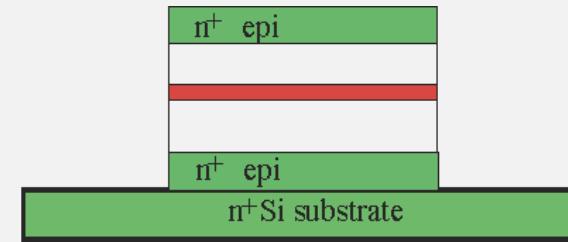
Electric Field Tailoring

Active Electric Field  
by Planar Doping

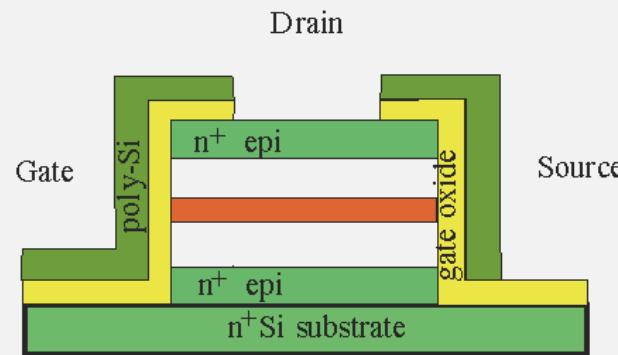
Superior performance  
+  
CMOS mainstream



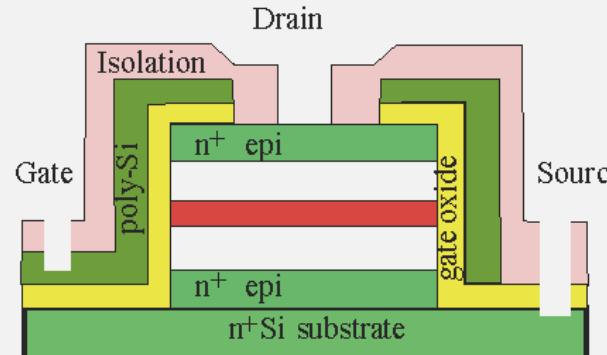
Deposition of layers by epitaxy



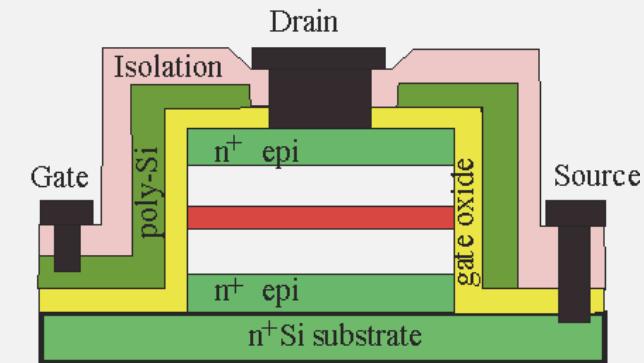
Device patterning by anisotropic dry etching



Gate oxidation,  
poly-Si deposition,  
gate patterning



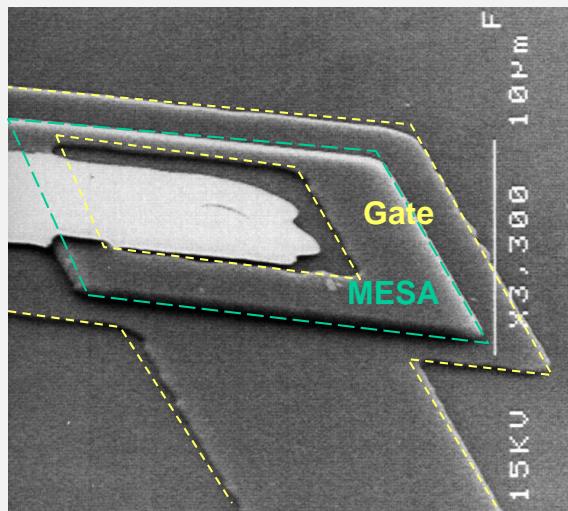
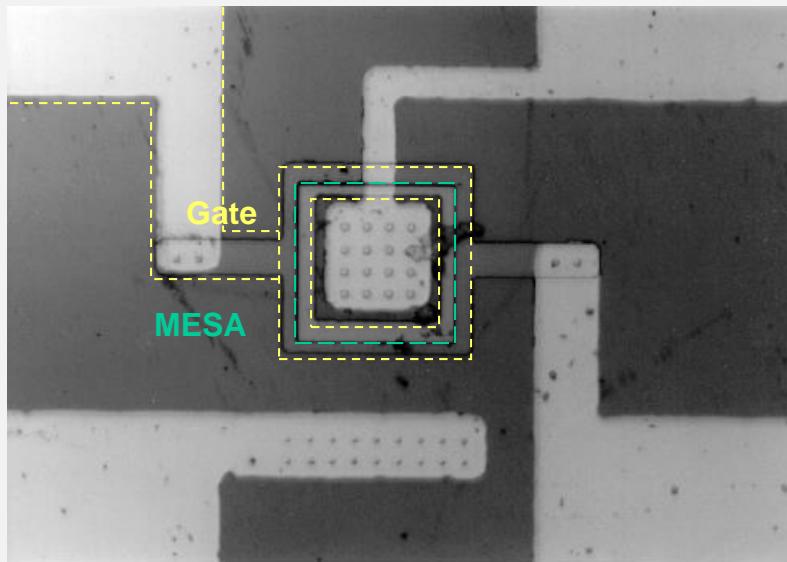
Isolation by LPCVD nitride,  
opening contact windows



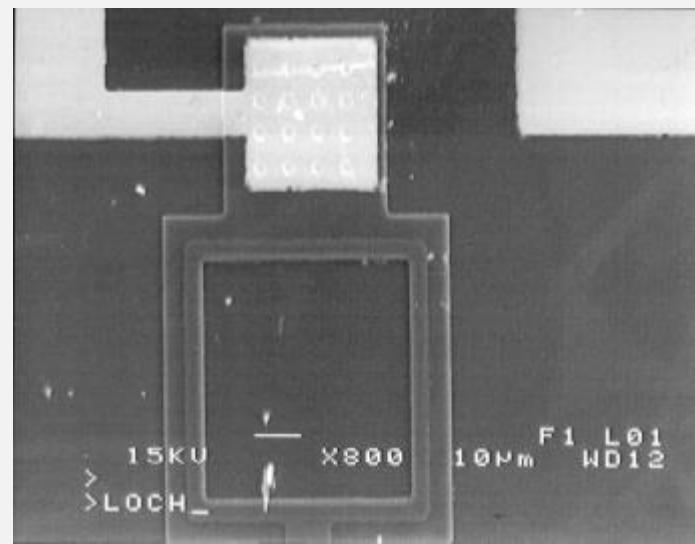
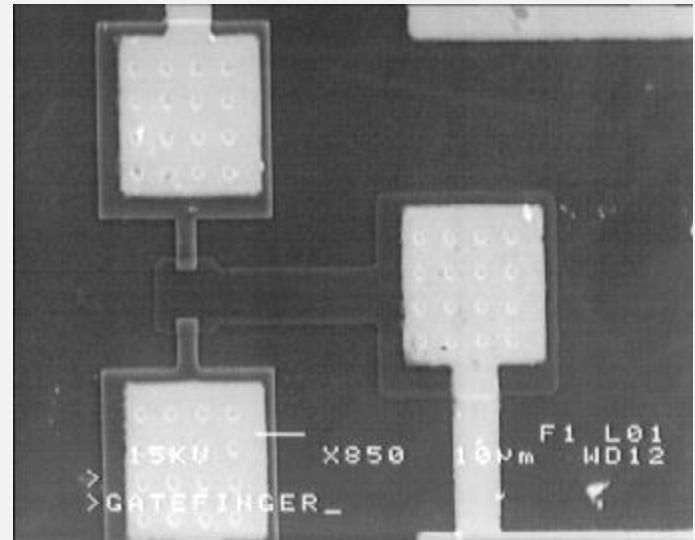
Metallization,  
patterning of metal



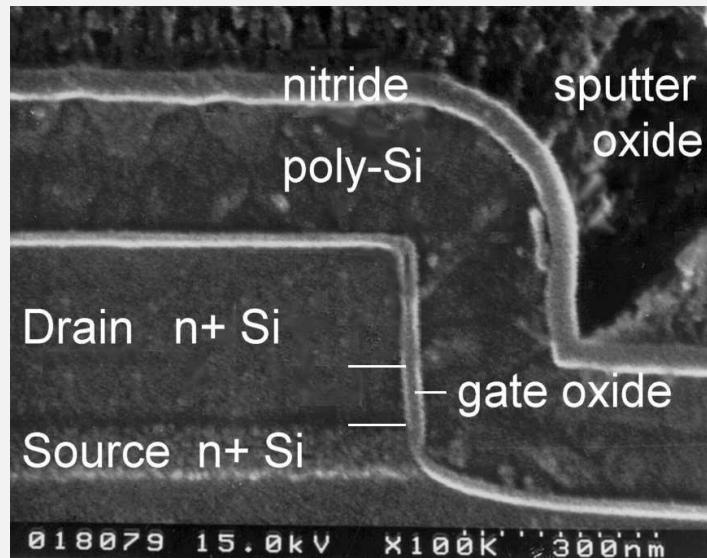
Vertical PDBFET is fabricated in a 4 mask process sequence by using CMOS-compatible equipment



Pictures from  
electron microscope

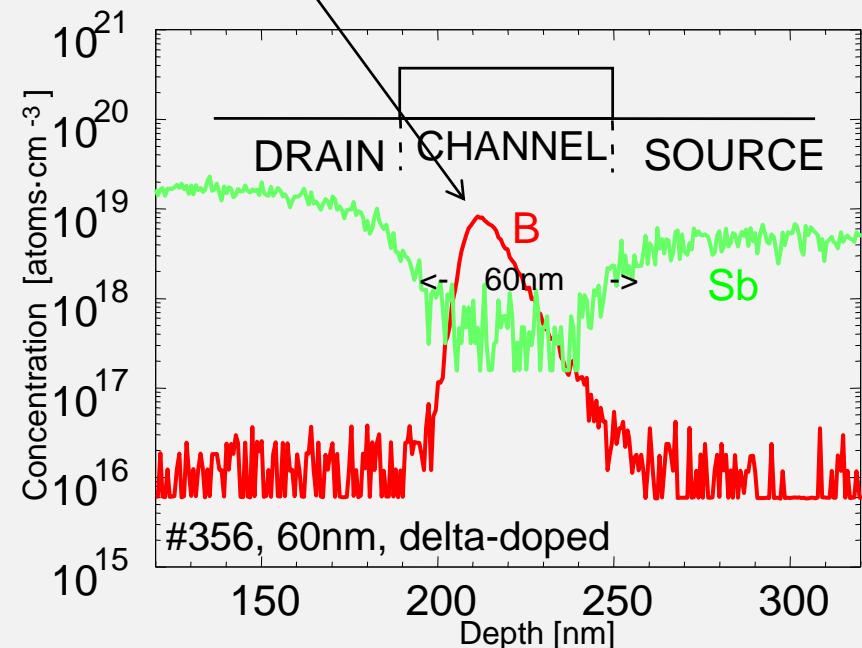


Vertical mesa etch and conformously gate oxide



picture from electron microscope

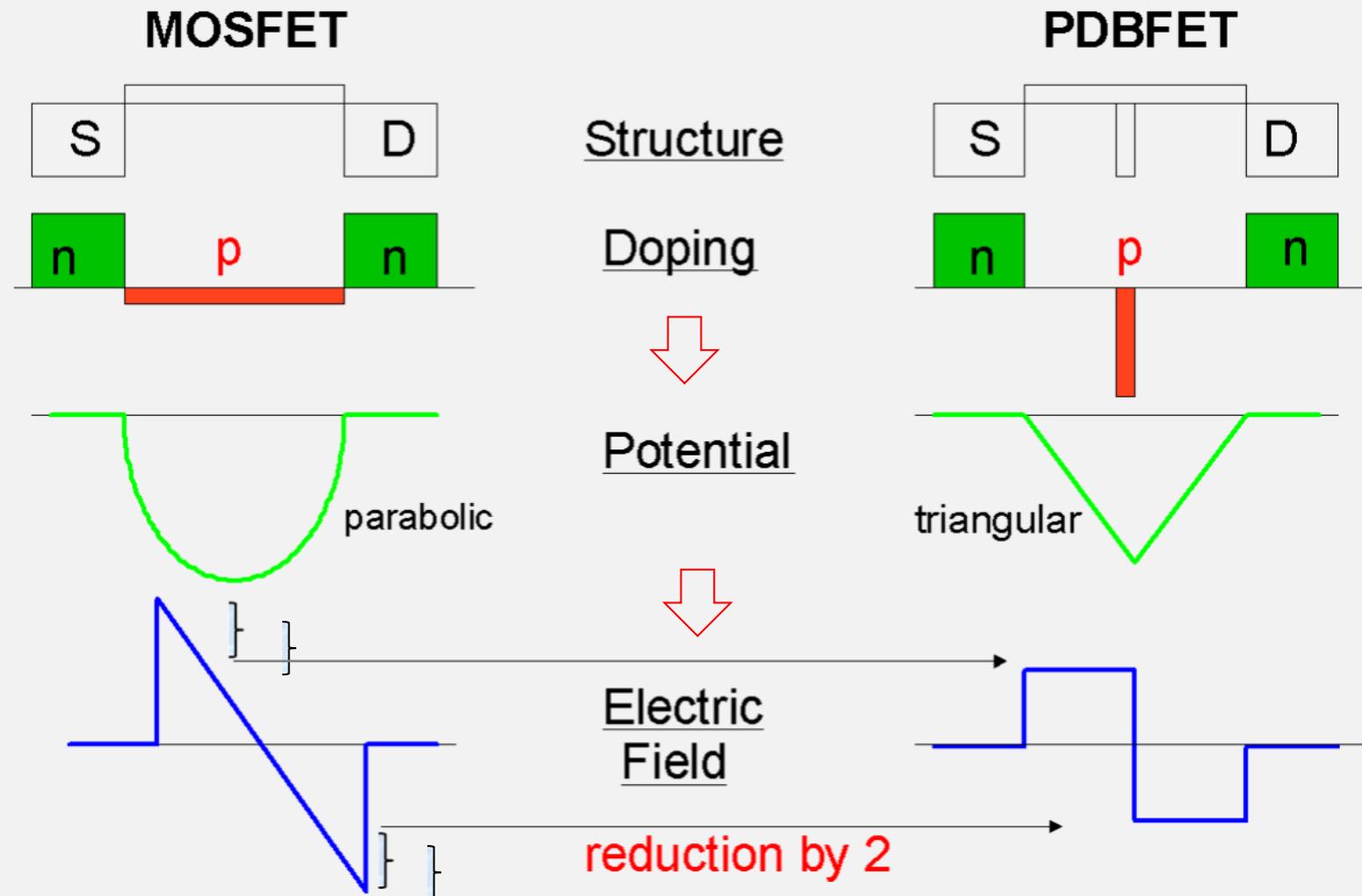
Delta-doping confined within 60nm channel



Secondary Ion Mass Spectrometry (SIMS)



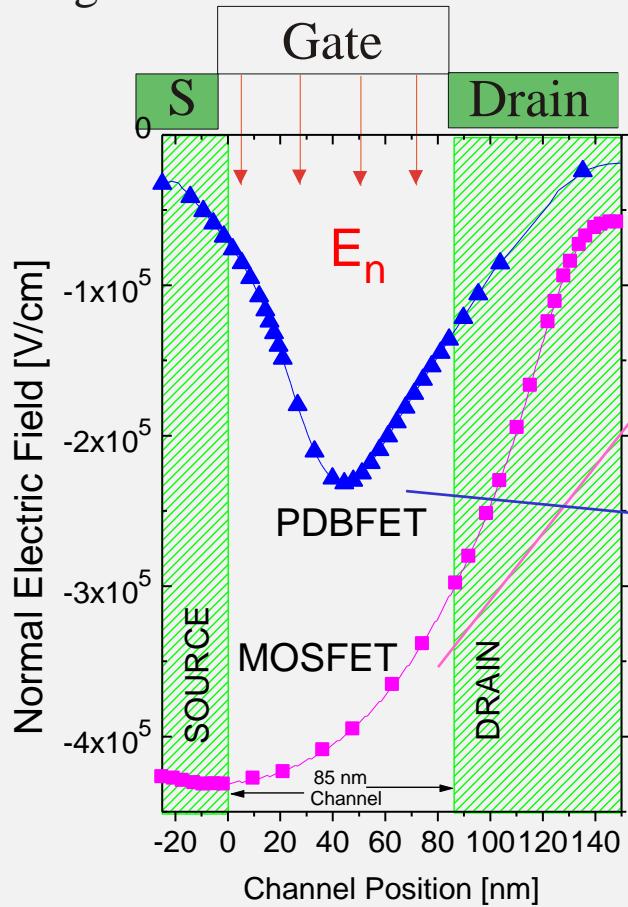
Geometrical structure and planar-doping structure are well-achieved after complete process sequence



By planar-doping the electric field is reduced by a factor of two by using same potential height (= same leakage current, same threshold voltage)

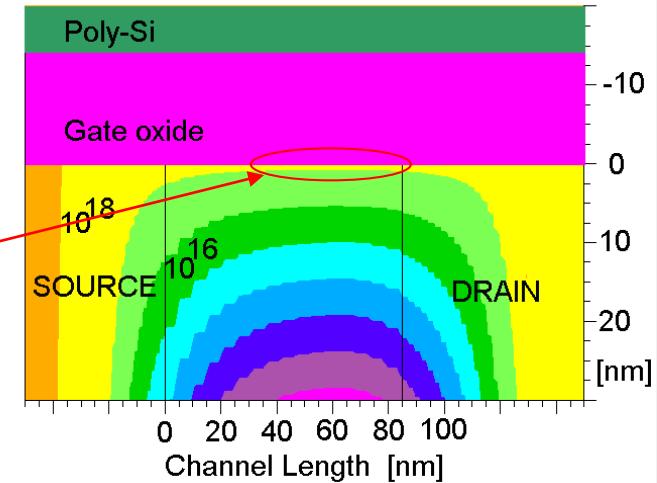
## Gate Field => Channel Confinement

$V_g = 2V$



### MOSFET

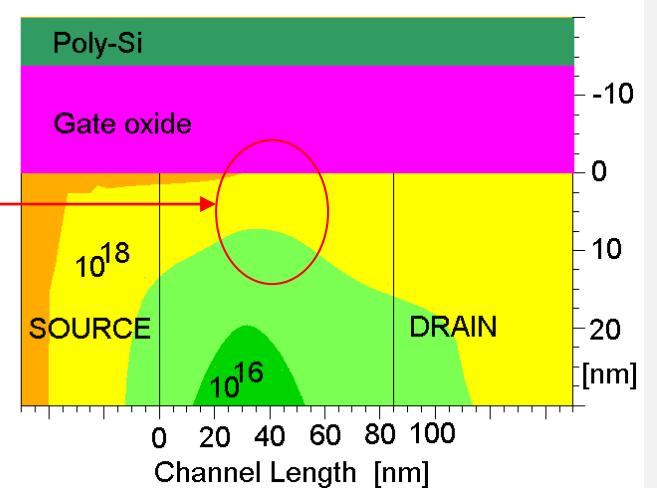
- \* **High gate field**
  - > narrow channel
  - > high scattering
  - > low mobility



Electron densities, Simulations done by MEDICI

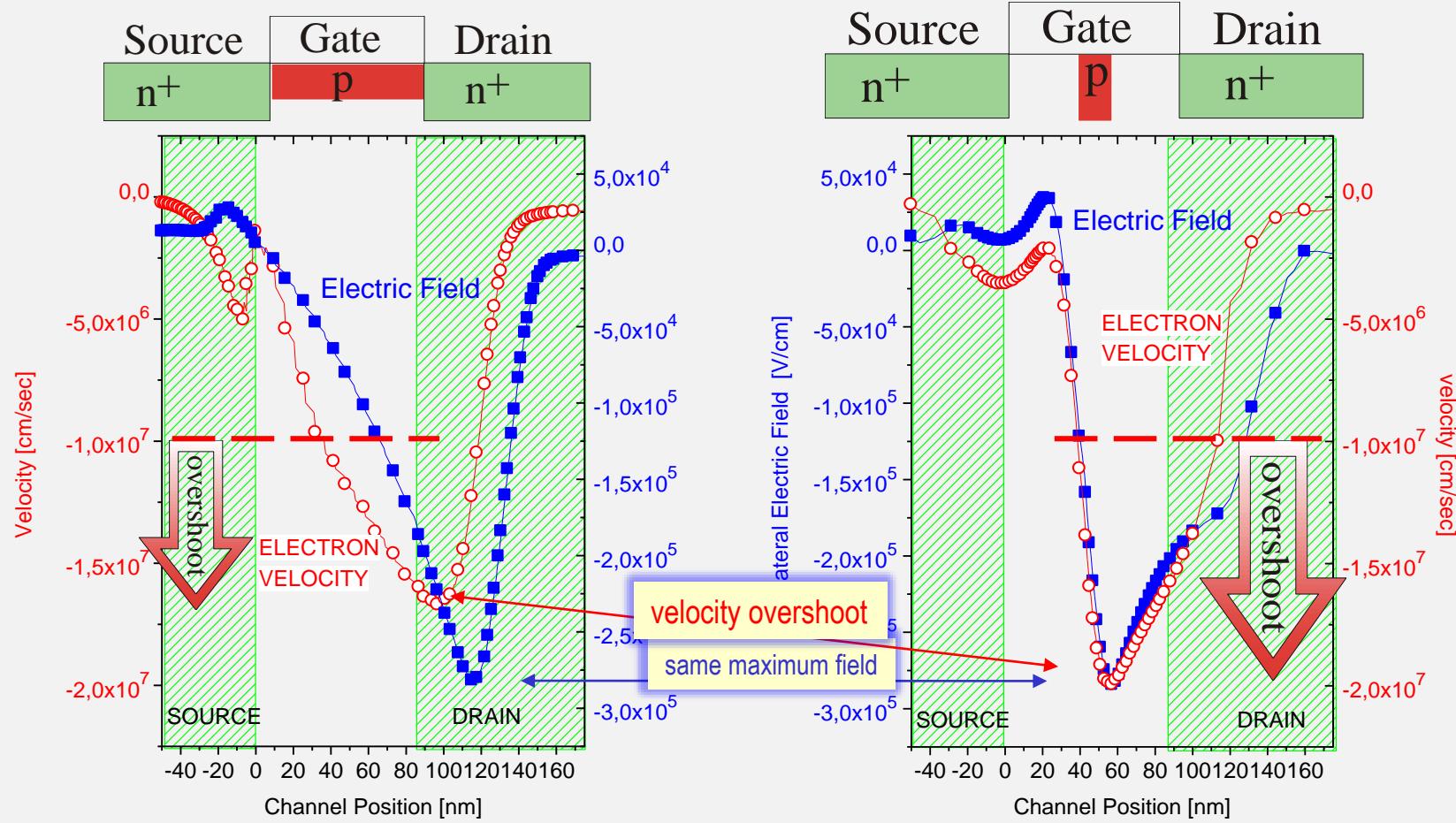
### PDBFET

- \* **Low gate field**
  - > wide channel
  - > low scattering
  - > high mobility



The highest gate field is only half of a uniformly doped MOSFET

Lateral Field => Carrier Speed

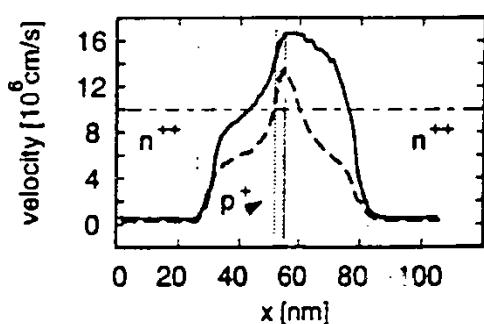


MOSFET: highest field and electron velocity at Drain end

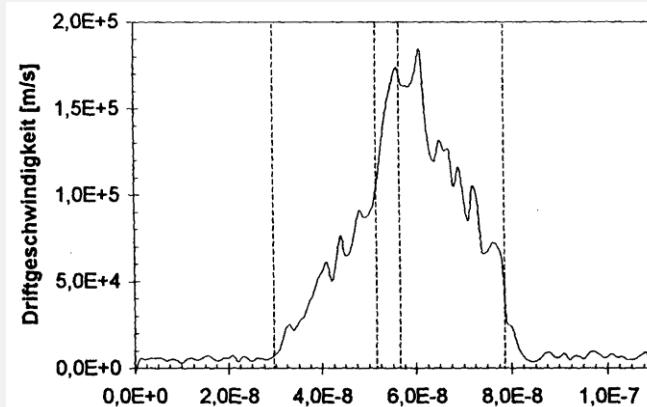
PDBFET: highest field and electron velocity at planar-doping



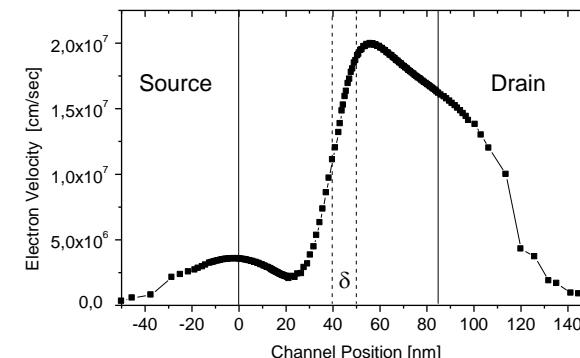
same maximum field, but higher overshoot in PDBFET



PDBFET, 50 nm  
 $V_g=1V$ ,  $V_{sd}=1V$   
[Cellular Automata Methods](#)  
WSI München,  
Rein et al., IEDM '95



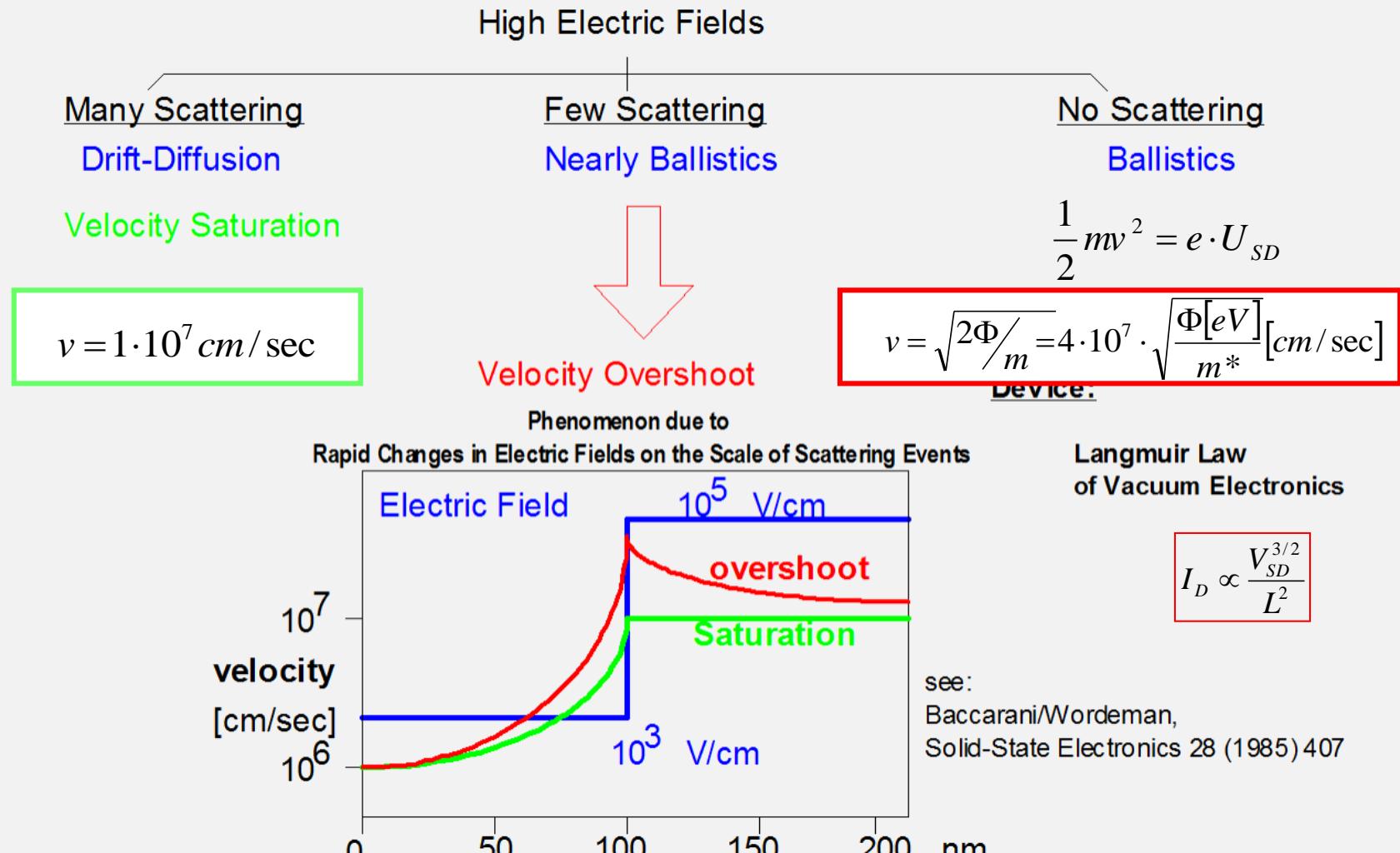
PDBFET, 50 nm  
 $V_g=0.7V$ ,  $V_{sd}=1V$   
[Monte-Carlo-Simulations](#)  
Uni Hannover,  
Fischer 1996



PDBFET, 85 nm  
 $V_g=2V$ ,  $V_{sd}=2V$   
[Hydrodynamic Equations](#)  
UniBw München,  
Rao, Hansch et al., IEDM '97

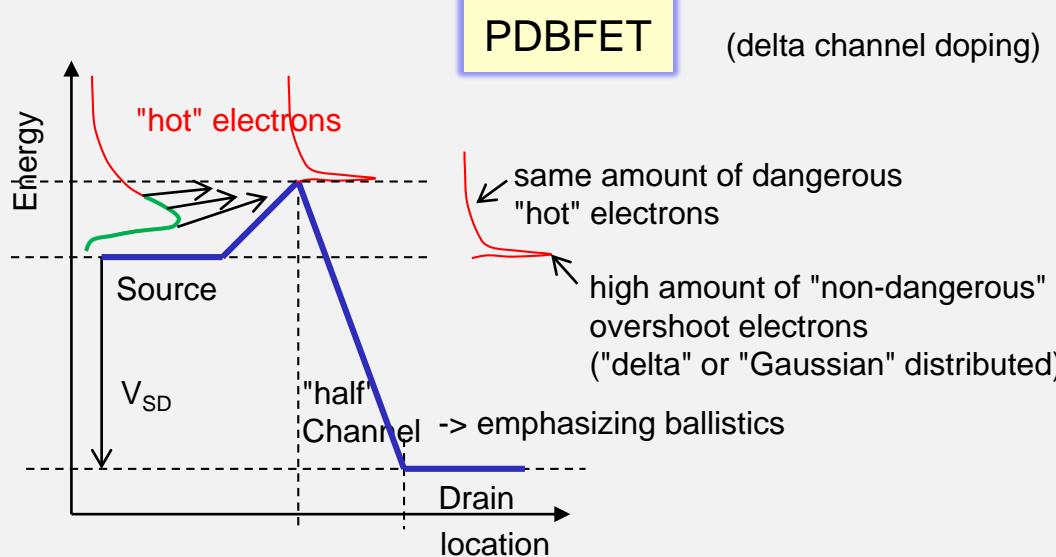
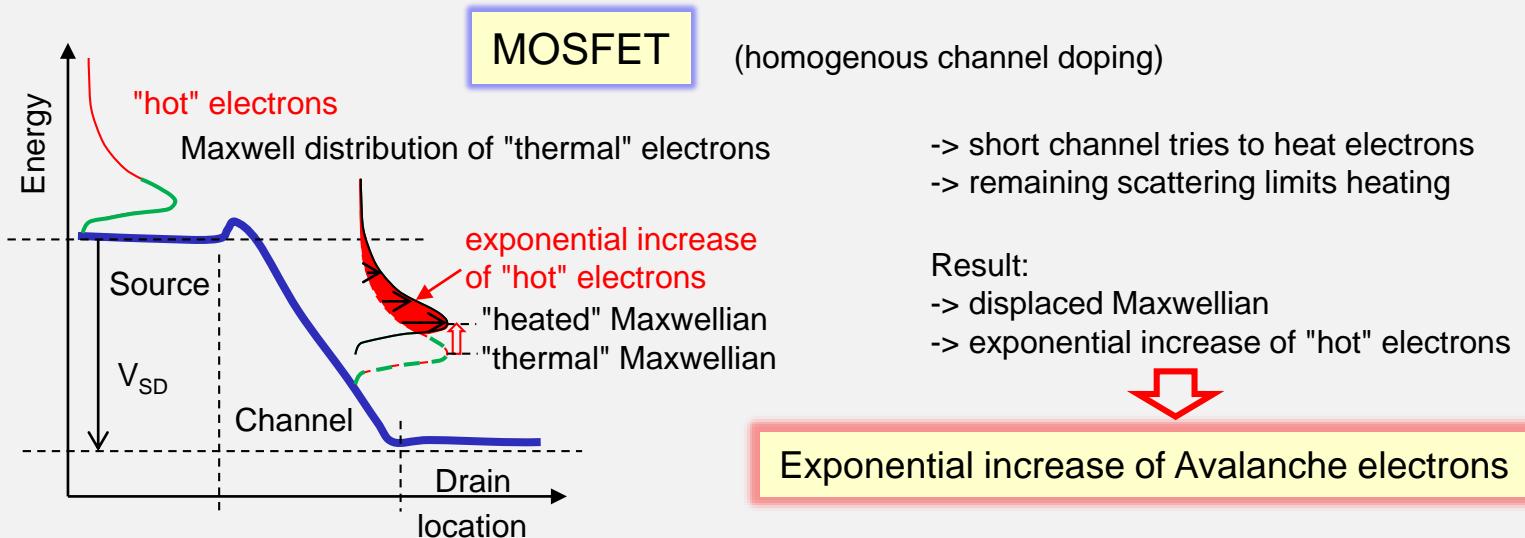
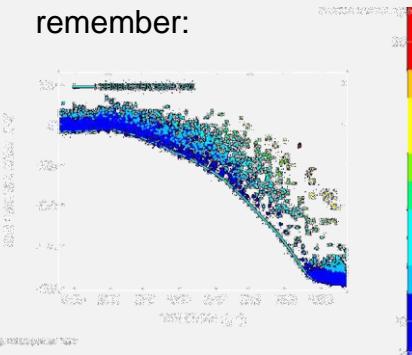


Various simulations propose overshoot



In abrupt electric fields a velocity overshoot is reasonable for channel lengths up to 100nm

remember:

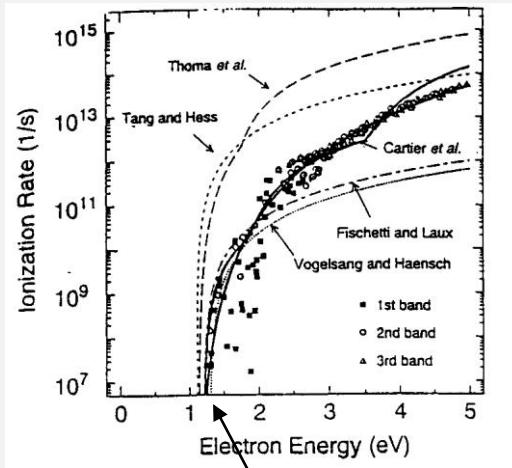


-> top of barrier "collects" electrons in rest  
-> barrier acts as electron energy filter

Result:  
-> basically "tailed" Gaussian distribution  
-> no increase of impact "hot" electrons

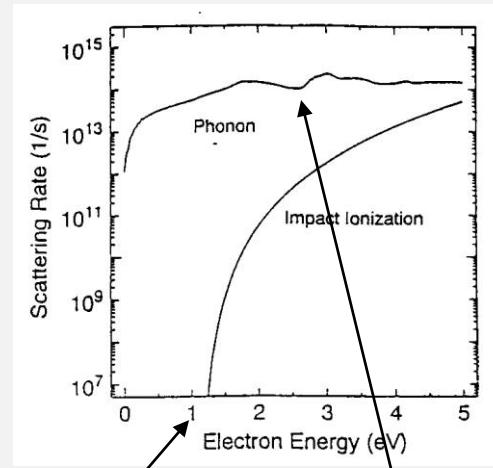
In a MOSFET with low channel barrier always harmful hot electrons  $E > 3\text{eV}$  are present

In a PDBFET no harmful hot electrons are present, although all electrons have higher energy than in a MOSFET



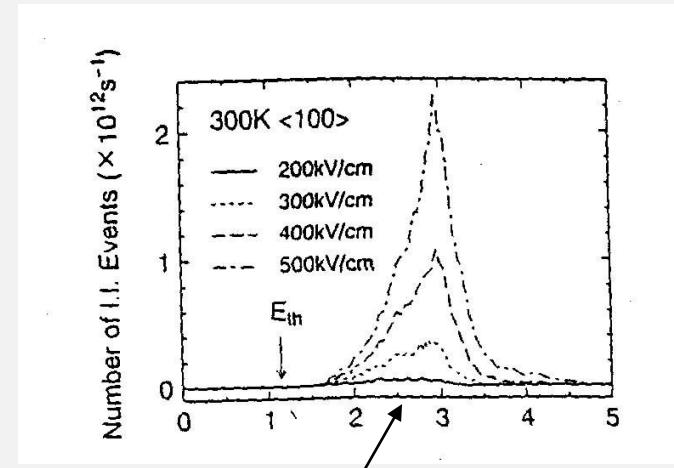
Calculated impact ionization using various models

ionization threshold at electron energies  $> E_{\text{gap}}$



Phonon and impact scattering

Phonon scattering is dominant over ionization scattering



Impact ionization rates vs. electric field

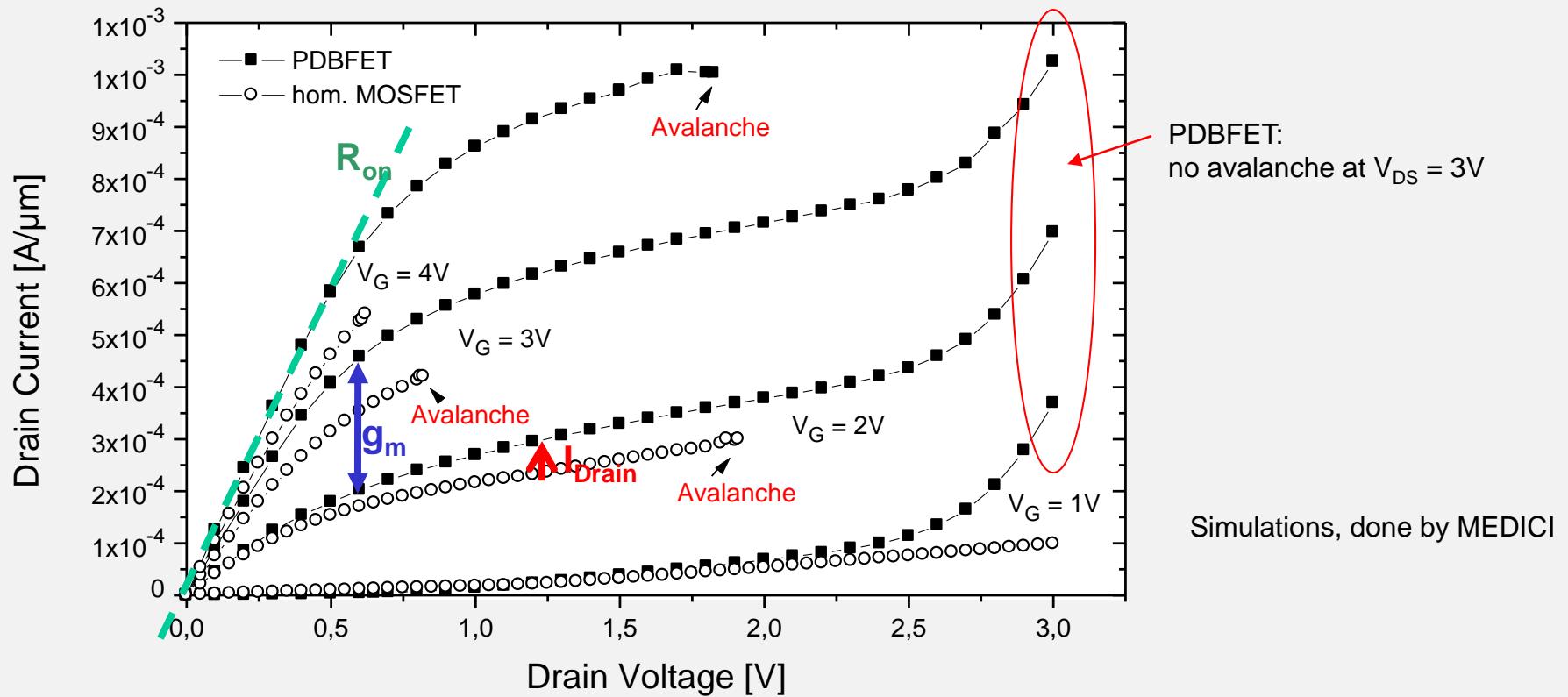
Independent of electric field the optimum energy for impact ionization is around 3eV



In a MOSFET with low channel barrier always harmful hot electrons  $E > 3\text{eV}$  are present

In a PDBFET no harmful hot electrons are present, although all electrons have higher energy than in a MOSFET

## Avalanche Suppression



Homogeneous doped MOSFET limited by early Avalanche, PDBFET not !

PDBFET exhibits:

higher currents  
higher transconductance  
lower  $R_{on}$

-> driver capability  
-> speed  
-> Power FETs

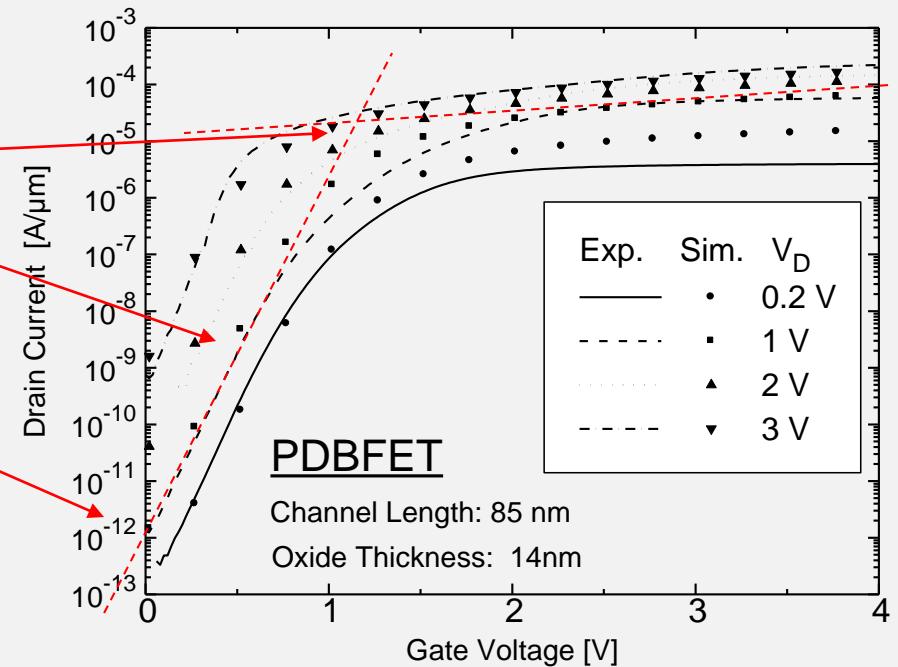
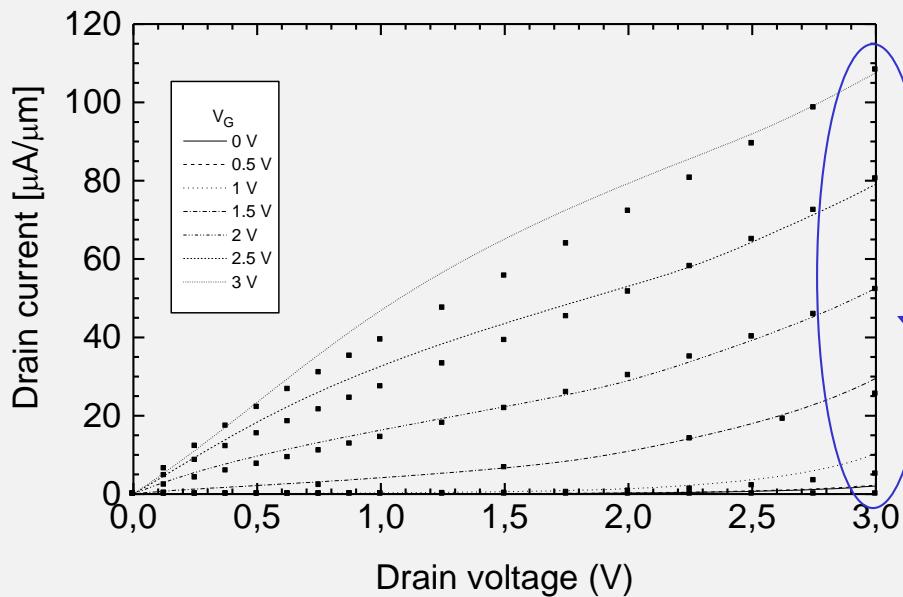
Hansch et al.  
Thin Solid Films, 321(1998)206  
Conference paper ESSDERC 1997, Tech.Dig., p.624

der Bundeswehr

## Transfer Characteristics

Threshold Voltage: ~ 1V  
 Subthreshold Slope: ~ 150mV/dec  
 (14nm oxide)

Leakage Currents:  
 $10^{-12} \text{ A}/\mu\text{m}$  at 1V (battery)



## Output Characteristics

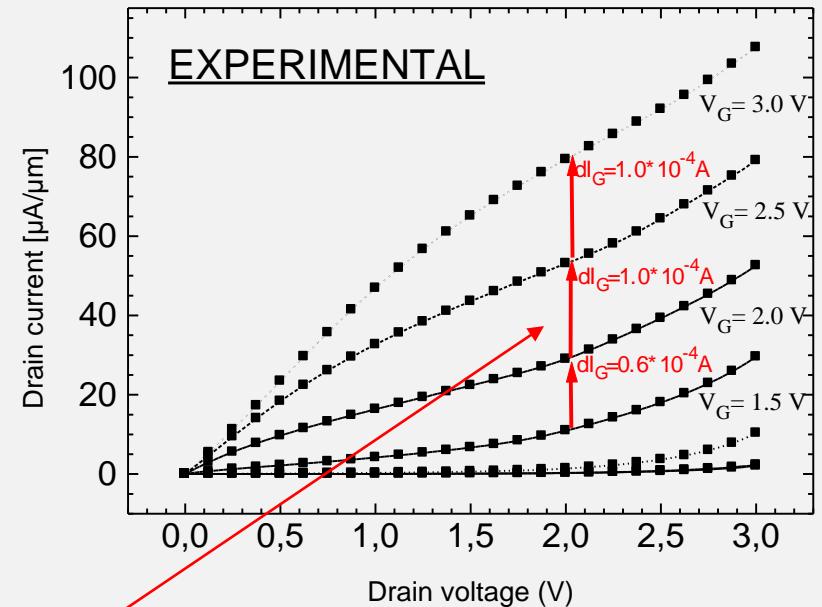
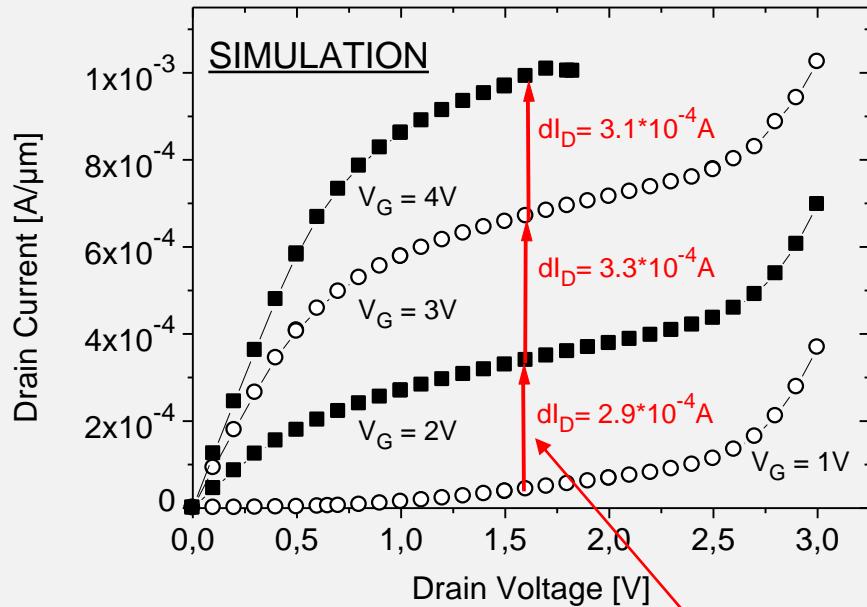
Typical Short Channel Behavior  
 but: Avalanche suppressed

This is the proof:

Maxwellian  $\rightarrow$  Gaussian

## 1. From Saturation Current

Theory: Drift-Diffusion Regime:  
Constant velocity:  $I_D \sim V_G^2$   
 $I_D \sim V_G$



Result:

Simulation:  $I_D \sim V_G$   
Experiment:  $I_D \sim V_G$



A fixed value of  $v$  can be assumed !  
Saturation or overshoot ?

## 2. From Transconductance

Theory:  $g_m(\max) = w \cdot C_{ox}'' \cdot v_{sat} = 246 \text{ mS/mm}$

see chap.3

Experiment:  $g_{mi} = 483 \text{ mS/mm} \rightarrow v = 1.9 \cdot 10^7 \text{ cm/sec}$   
Simulation:  $v \sim 1.9 \cdot 10^7 \text{ cm/sec}$



Overshoot exists of a factor 1.9  
as predicted by simulations

SIA Roadmap 1997:

Table 14 Memory and Logic Technology Requirements

Year of First Product Shipment Technology Generation	1997 250 nm	1999 180 nm	2001 150 nm	2003 130 nm	2006 100 nm	2009 70 nm	2012 50 nm
Min. Logic $V_{dd}$ (V) (desktop)	2.5-1.8	1.8-1.5	1.5-1.2	1.5-1.2	1.2-0.9	0.9-0.6	0.6-0.5
$V_{dd}$ Variation	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
$T_{ox}$ Equivalent (nm)	4-5	3-4	2-3	2-3	1.5-2	< 1.5	< 1.0
Equivalent Maximum E-field (MV/cm)	4-5	5	5	5	> 5	> 5	> 5
Max $I_{off}$ @ 25°C (nA/ $\mu$ m) (For minimum L device)	1	1	3	3	3	10	10
Nominal $I_{on}$ @ 25°C ( $\mu$ A/ $\mu$ m) (NMOS / PMOS)	600/280	600/280	600/280	600/280	600/280	600/280	600/280
Gate Delay Metric (CV/I) (ps)*	16-17	12-13	10-12	9-10	7	4-5	3-4
$V_T$ 3σ Variation ( $\pm$ mV) (For minimum L device)	60	50	45	40	40	40	40
$L_{gate}$ 3σ Variation (For nominal device)	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%	≤ 10%
<hr/>							
Drain structure	Drain Extension			+ Elev. S/D	Elev. Single Drain		
Contact Xj (nm)	100-200	70-140	60-120	50-100	40-80	15-30	10-20
Xj @ channel (nm)	50-100	36-72	30-60	26-52	20-40	15-30	10-20
Silicid thickness (nm)	70	55	45	40	45-70	New Structure	
Contact silicide sheet Rs ( $\Omega/\square$ )	2	2.7	3.3	3.8	2	2	2
Si/Silicide max resistivity ( $\Omega\text{-cm}$ )	< 1 × 10 <sup>-6</sup>	< 6 × 10 <sup>-7</sup>	< 4 × 10 <sup>-7</sup>	< 3 × 10 <sup>-7</sup>	< 2 × 10 <sup>-7</sup>	< 8 × 10 <sup>-8</sup>	< 3 × 10 <sup>-8</sup>
Drain extension conc. ( $\text{cm}^{-3}$ )	1 × 10 <sup>18</sup>	1 × 10 <sup>19</sup>	1 × 10 <sup>19</sup>	1 × 10 <sup>19</sup>	1 × 10 <sup>20</sup>	1 × 10 <sup>20</sup>	1 × 10 <sup>20</sup>
Channel conc. for $W_{depletion} < 1/4L_{eff}$ ( $\text{cm}^{-3}$ )	1 × 10 <sup>18</sup>	2 × 10 <sup>18</sup>	2.5 × 10 <sup>18</sup>	3 × 10 <sup>18</sup>	4 × 10 <sup>18</sup>	8 × 10 <sup>18</sup>	1.4 × 10 <sup>19</sup>
Unif. channel conc. ( $\text{cm}^{-3}$ ), for $V_t=0.4$	4-6 × 10 <sup>17</sup>	6-10 × 10 <sup>17</sup>	7-13 × 10 <sup>17</sup>	1-2 × 10 <sup>18</sup>	2-3 × 10 <sup>18</sup>	> 3.5 × 10 <sup>18</sup>	> 7 × 10 <sup>18</sup>
Retro channel peak depth (nm)	50-100	36-72	30-60	26-52	20-40	15-30	10-20
Retro channel peak conc. ( $\text{cm}^{-3}$ )	5-20 × 10 <sup>17</sup>	2-6 × 10 <sup>18</sup>	4-8 × 10 <sup>18</sup>	6-10 × 10 <sup>18</sup>	1-2 × 10 <sup>19</sup>	1.5-4 × 10 <sup>19</sup>	2-8 × 10 <sup>19</sup>
<hr/>							
Solutions Exist	■	Solutions Being Pursued		No Known Solution	■	■	■
DRAM 1 <sup>st</sup> Year Electrical $D_0$ @ 60% Yield / 3 <sup>rd</sup> Year @ 80% Yield ( $d/m^2$ )	2080 / 1390	1455 / 985	1310* / 875*	1040 / 695	735 / 490	520 / 350	370 / 250
MPU 1 <sup>st</sup> Year Electrical $D_0$ @ 60% Yield / 3 <sup>rd</sup> Year @ 80% Yield ( $d/m^2$ )	1940 / 1310	1710 / 1150	1510* / 1025*	1355 / 910	1120 / 760	940 / 640	775 / 525
ASIC 1 <sup>st</sup> Year Electrical $D_0$ @ 60% Yield / ( $d/m^2$ )	1210	725	685*	645	580	530	450

## 50nm MOSFET

Supply Voltage: (0.5-0.6) V

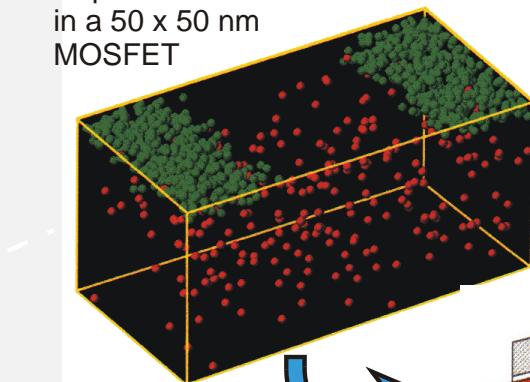
Max Ioff: 10nA/ $\mu$ mIon: 600 $\mu$ A/ $\mu$ m $\rightarrow \triangle I = 5 \text{ dec}$  $\rightarrow \triangle V = 315 \text{ mV}$ 

with S(ideal) = 63mV/dec

 $\rightarrow V_{th} \sim 0.3 \text{ V}$  $\Delta V_{th} (3\sigma): 40 \text{ mV } \sim 14\%$ Channel doping level:  $\sim 10^{19} \text{ cm}^{-3}$ 

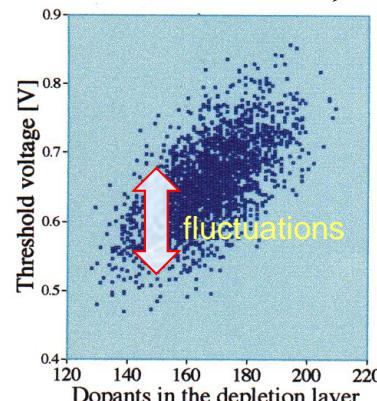
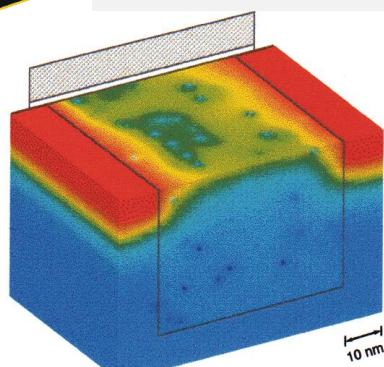
Starting Yield: 60%

Dopant Distribution  
in a 50 x 50 nm  
MOSFET



## Statistical 'Atomistic' Simulation

Potential Distribution

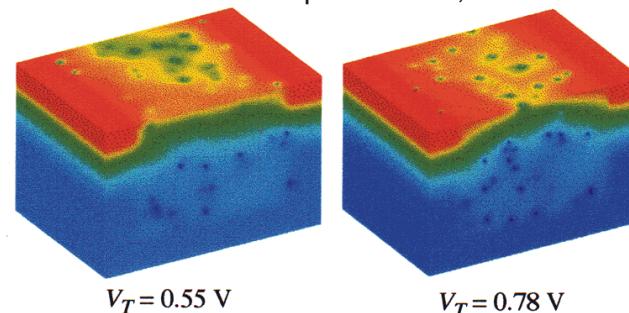


from: A.Asenov@elec.gla.ac.uk

1. "Homogeneously" doped  
50nm MOSFETs  
can not be fabricated !

2. Due to random arrangement  
of doping atoms  
a threshold voltage fluctuation  
of  $\sigma V_{th} \sim 50\text{-}100\text{mV}$  is proposed !

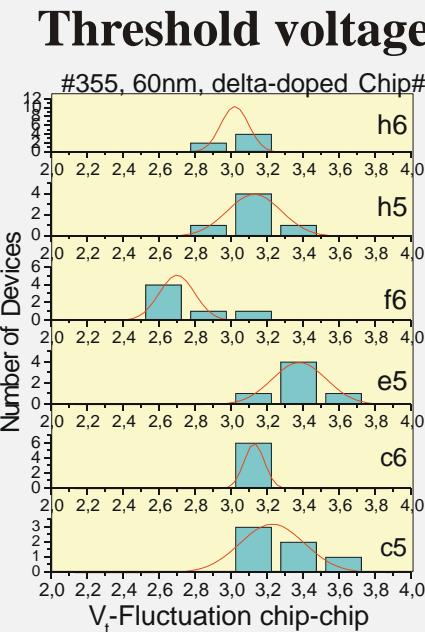
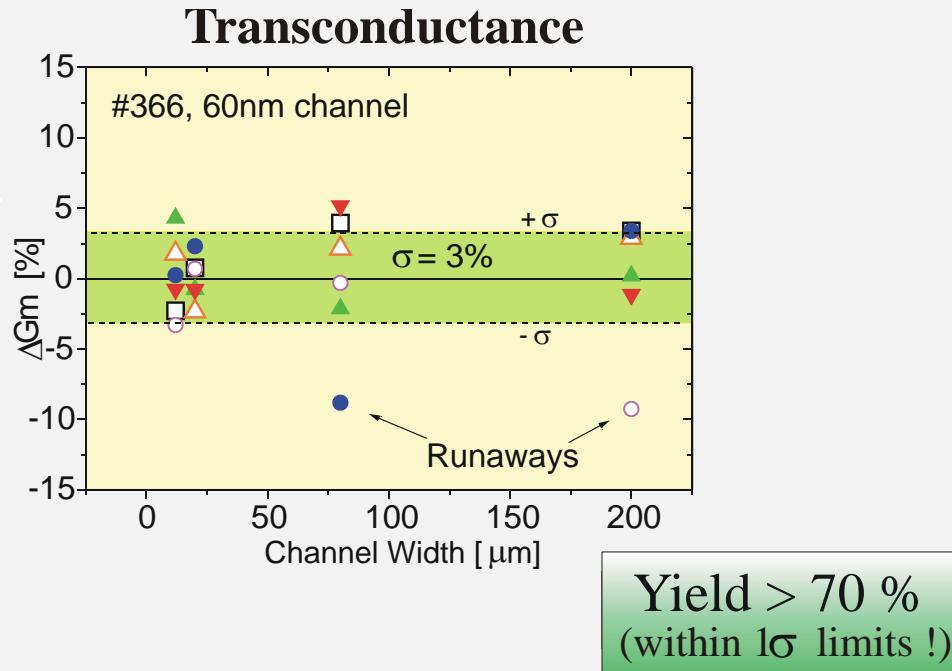
Same number of Dopant Atoms, but different  $V_{th}$



! From SIA-Roadmap a  $3\sigma=40\text{mV}$  is recommended !



## Vertical 60nm PDBFETs:



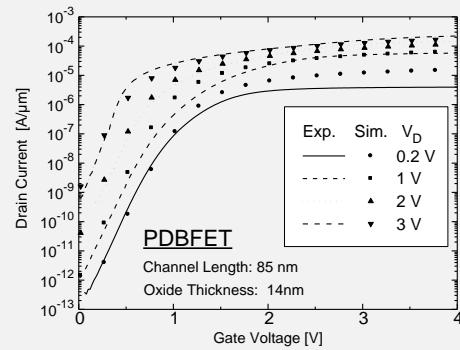
gm = f(tox, Rser, Lchan,..) is well-controllable

Fluctuations in transconductance:  $\sigma_{gm} \sim 3\%$

Variation of threshold voltage due to doping fluctuations

Fluctuations in threshold voltage  $\sigma_{Vt} \sim 3\%$  on chip

Demands of SIA-roadmap:  $3\sigma_{Vt} < 13\%$  in 50nm MOSFETs (year 2012)  
are achieved with vertical, delta-doped MOSFETs

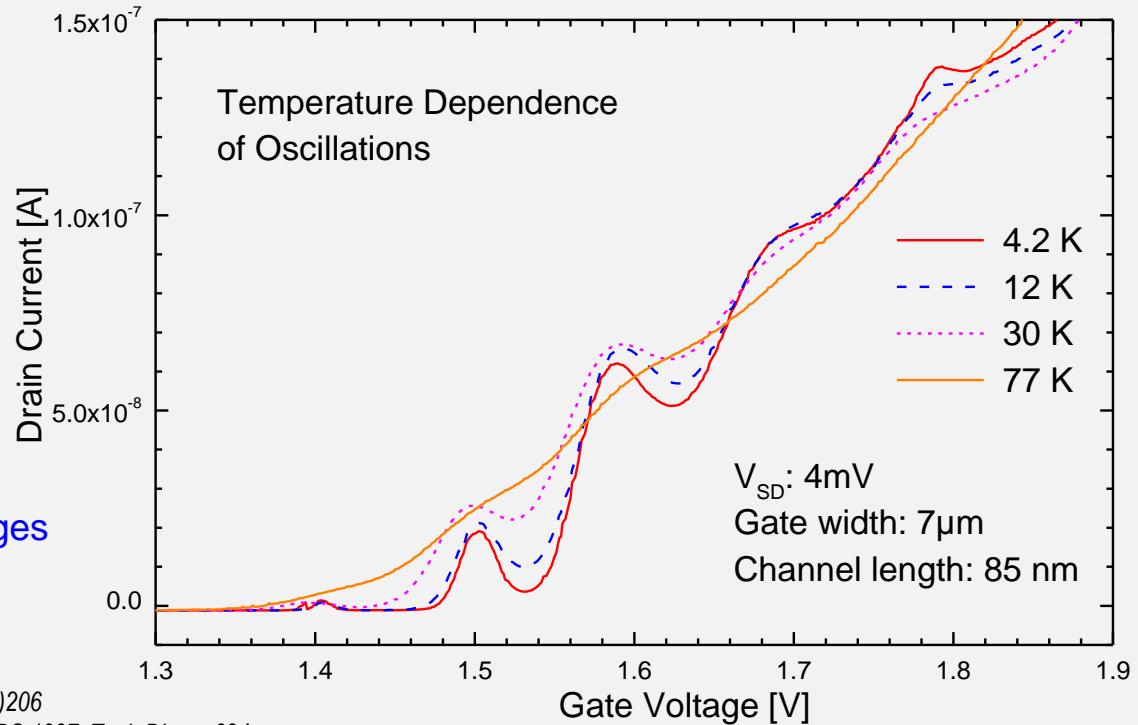


We have seen:

Overshoot and nearly ballistics at room temperature

Cooling down

Transfer Characteristics at Low Temperatures



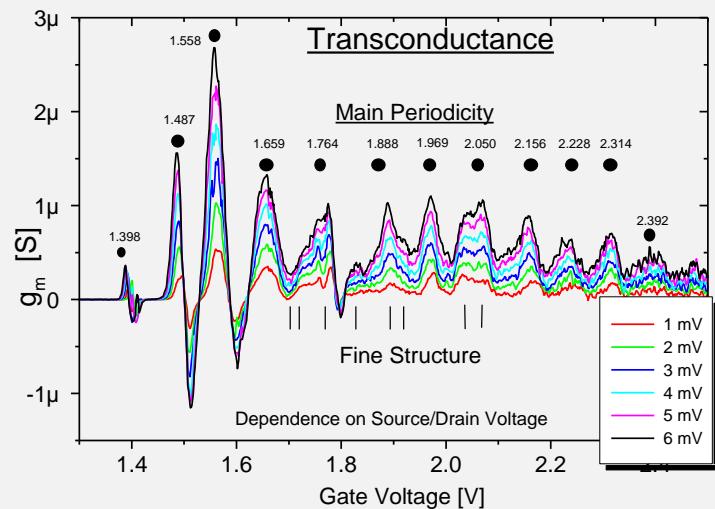
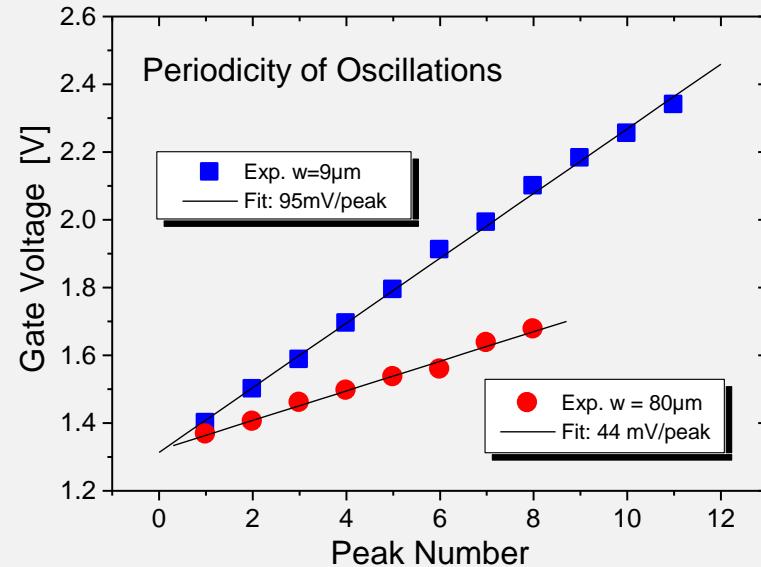
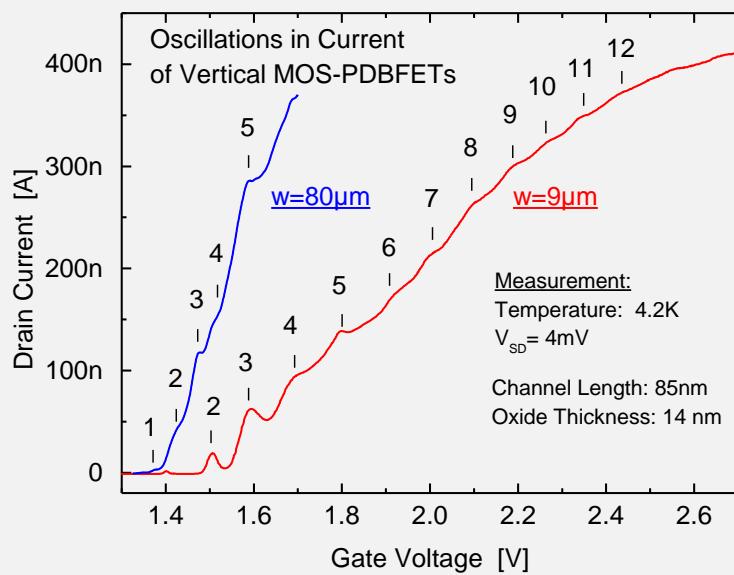
Hansch et al.  
*Thin Solid Films*, 321(1998)206  
Conference paper ESSDERC 1997, Tech.Dig., p.624

At low temperatures clear current oscillations dependent on gate voltage appear

Up to 77K

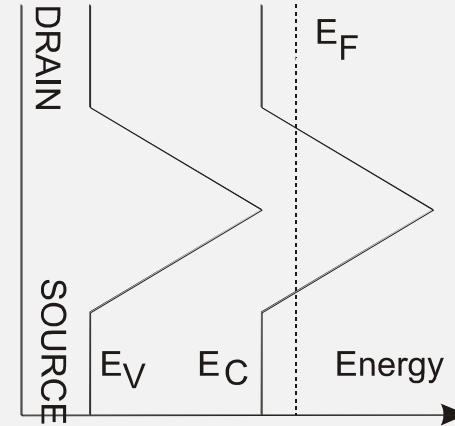
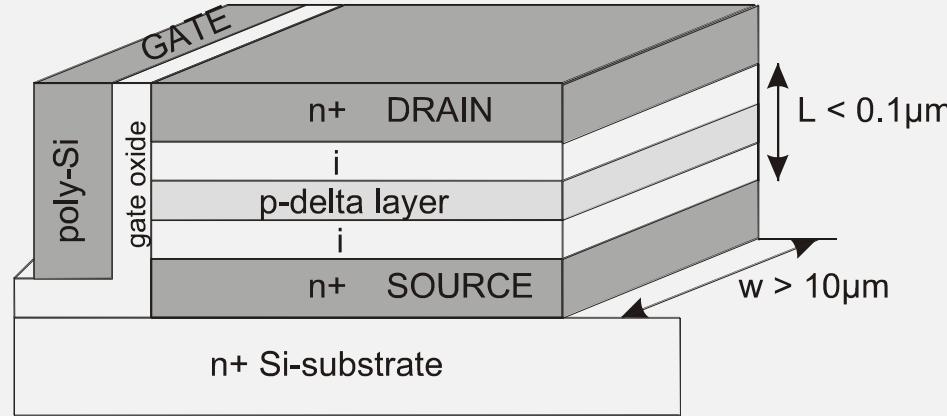
Up to high gate voltages

## Examples of Oscillations

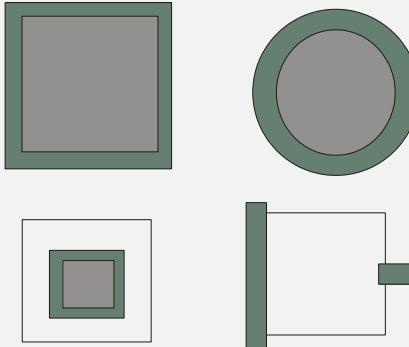


Oscillations are equidistant in gate voltage

Hansch et al., VLSI'98, Nanoelectronics Workshop, Tech.Dig 27



## Variations in Layout:



## Variations in Technology:

- MBE / CVD
- Gate oxide 5 - 17 nm
- Gate width 5 - 700 $\mu\text{m}$
- Channel Length 30nm - 120nm
- Metallization / Contact Area
- delta-doping: 1-20x10 cm



Current Oscillations are visible in all PDBFETs

## No Coulomb blockade oscillations:

1. Absolute value not reasonable:

for gate width  $\sim 100\mu\text{m}$  the gate capacity  $C$  is  $\sim 1000 \text{ aF}$   
the periodic distance in gate voltage is  $V_G \sim 100 \text{ mV}$

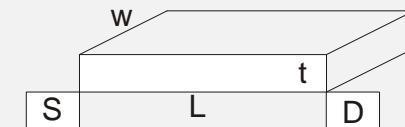
} Charging of around  
 $\Delta Q = C * \Delta V_g \sim 1000 \text{ electrons}$

2. As shown below, all devices with various geometries reproduce same universal value

## Proposed model of charge carrier density quantization:

### Assumption:

The basic formula for the inversion charge:  $\Delta Q = Cg * \Delta(V_G - V_T)$  (1)



can be evaluated in:

$$\Delta N = \frac{\epsilon_0 \epsilon_{ox}}{e} * \frac{w * L}{t_{ox}} * \Delta V_G = f(L, w, t) \quad (2a) \text{ if } \Delta N \text{ is a specified number of electrons}$$

$$\Delta N_s = \frac{\epsilon_0 \epsilon_{ox}}{e} * \frac{1}{t_{ox}} * \Delta V_G = f(t) \quad (2b) \text{ if } \Delta N_s \text{ is a area density of electrons}$$

If a equidistant  $\Delta V_G$  is observed, a equidistant  $\Delta N$  is the consequence

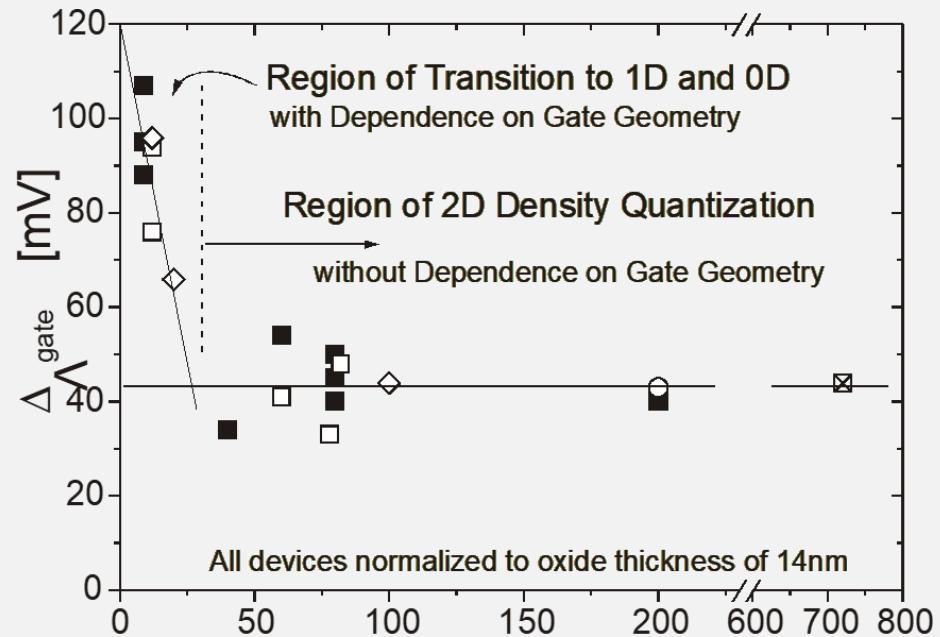


## Proof of equations (2):

1 All measured  $\Delta V_g$  are normalized to the same oxide thickness:

$$V_g(\text{norm}) = V(\text{meas}) * t(\text{norm}) / t(\text{meas})$$

2 Devices with various channel length, oxide thickness, doping and channel width are presented:



## Result:

All various devices independent of channel length and gate width result in an universal value of gate voltage:

A universal value of electron density quantization must be assumed.

The measured value of carrier density quantization amounts:  $(8 \pm 2) \cdot 10^{10} \text{ cm}^{-2}$

## Consequences:

①

In the presented PDBFETs all electrons overcoming the potential barrier exhibit:

same energy  
same direction of motion

Filter in energy and momentum

due to short channels, low doping and low temperature: no scattering takes place

Ballistic transport

An artificial 2-dim free electron gas is created

②

Periodic arrangement of electrons is proposed by:

Wigner 1934

(in free electron gas in metals)

Phys.Rev.46 (1934)1002

Crandall/Williams 1971

(for electrons on liquid helium surface)

Phys.Lett.A34 (1971)404

Chaplik 1972

(in inversion layers)

Sov.Phys. JETP 35 (1972)395

if Coulomb energy exceeds kinetic energy

$$\langle E_{\text{Coul}} \rangle = \frac{e^2}{4\pi\epsilon_0 r} \gg E_{\text{kin}} = \begin{cases} \rightarrow eV_{SD} : \text{electric field} \\ \rightarrow kT : \text{classical limit } T >> 0 \\ \rightarrow E_F : \text{quantum limit } T \rightarrow 0 \end{cases}$$

In MOSFET channels at low temperatures

$$\Gamma = \frac{\langle E_{\text{Coul}} \rangle}{E_F} = \frac{e^2 * (\pi * N_S)^{1/2} / 4 \pi \epsilon}{\hbar^2 * 2 \pi N_S / 2m} \geq 100$$

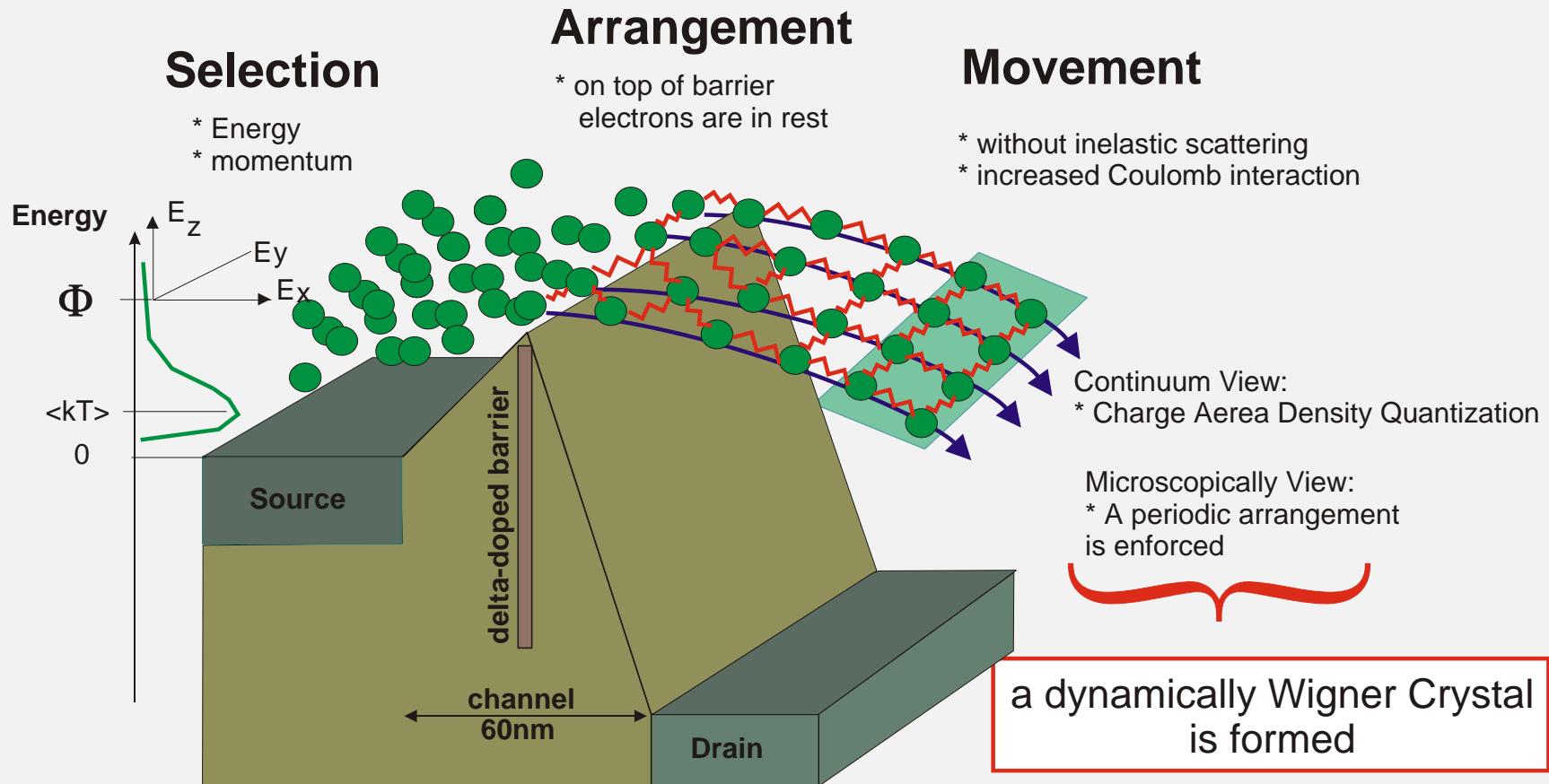
Coulomb interaction strongly dominates all other energies  
in scattering-free channels at common inversion charge densities

③

In all PDBFETs the same value of density quantization is measured. This represents a periodic arrangement of electrons in transport.



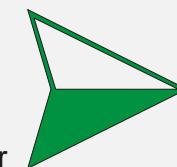
The observation of a dynamically Wigner crystal can be followed



Thermodynamics:  $\langle E_{kin} \rangle = E_{kin}(x) + E_{kin}(y) + E_{kin}(z)$

an electron with  $E_\Phi$  only has 1/3 of  $\langle E_{kin} \rangle$  in x-direction

only "lucky" electrons with  $E_{kin} > E_\Phi$  and  $E_{kin}(y) = E_{kin}(z) = 0$  can overcome the barrier



Filter  
in  
Energy  
and  
Momentum

## 7.1 Motivation for Hot Carrier Devices

## 7.2 Overview of Hot Carrier Devices

Fabrication Technology: Epitaxy  
Examples of Hot Carrier Devices

## 7.3 The Planar-Doped Barrier FET (PDBFET)

Fabrication  
Electric Field Tailoring  
Modification of Charge Carrier Transport  
Experimental IV-Characteristics  
Low-temperature Physical Transport Effects

## 7.4 The Impact Ionization MOSFET (IMOS)

Advantage as Steep-Slope Device  
Working Principle  
Experimental Devices  
Circuit application  
Outlook

## 7.5 Spintronics

Spin Valve Transistor  
Magnetic RAM

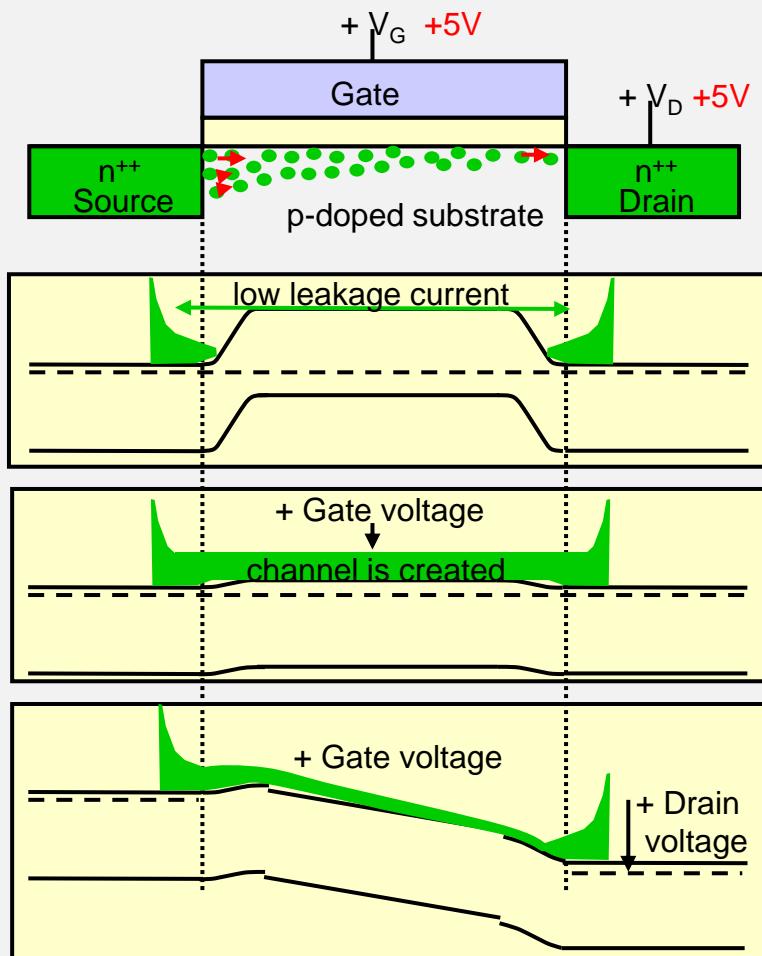
Table 47a High-performance Logic Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2009	Technology Requirements—Long-term					
Technology Node		hp90			hp65		2010	2012	2013	2015	2016	2018
DRAM $\frac{1}{2}$ Pitch (nm)	100	90	80	70	65		hp45		hp32		hp22	
MPU/ASIC Metal 1 (M1) $\frac{1}{2}$ Pitch (nm)	120	107	95	85	76		45	35	32	25	22	18
MPU/ASIC $\frac{1}{2}$ Pitch (nm)	107	90	80	70	65		54	42	38	30	27	21
MPU Printed Gate Length (nm)	65	53	45	40	35		45	35	32	25	22	18
MPU Physical Gate Length (nm)	45	37	32	28	25		25	20	18	14	13	10
Physical gate length high-performance (HP) (nm) [1]	45	37	32	28	25		18	14	13	10	9	7
EOT: equivalent oxide thickness (physical) for high-performance (nm) [2]	1.3	1.2	1.1	1.0	0.9		18	14	13	10	9	7
Electrical thickness adjustment for gate depletion and inversion layer effects (nm) [3]	0.8	0.8	0.7	0.7	0.4		1.1	1.1	1.0	1.0	0.9	0.9
Equivalent electrical oxide thickness in inversion (nm) [4]	2.1	2.0	1.8	1.7	1.3		1.1	1.1	1.0	1.0	0.9	0.9
Nominal gate leakage current density limit (at 25°C) ( $A/cm^2$ ) [5]	2.2E+02	4.5E+02	5.2E+02	6.0E+02	9.3E+02		1.9E+03	2.4E+03	7.7E+03	1.0E+04	1.9E+04	2.4E+04
Nominal power supply voltage ( $V_{dd}$ ) (V) [6]	1.2	1.2	1.1	1.1	1.1		1.0	0.9	0.9	0.8	0.8	0.7
Saturation threshold voltage (V) [7]	0.21	0.20	0.20	0.21	0.18		0.15	0.14	0.11	0.12	0.10	0.11
Nominal high-performance NMOS sub-threshold leakage current, $I_{sd,leak}$ (at 25°C) ( $\mu A/\mu m$ ) [8]	0.03	0.05	0.05	0.05	0.07		0.1	0.1	0.3	0.3	0.5	0.5
Nominal high-performance NMOS saturation drive current, $I_{dsat}$ (at $V_{dd}$ , at 25°C) ( $mA/mm$ ) [9]	980	1110	1090	1170	1510		1900	1790	2050	2110	2400	2190
Required "mobility/transconductance improvement" factor [10]	1.0	1.3	1.3	1.4	2.0		2.0	2.0	2.0	2.0	2.0	2.0
Sub-threshold slope adjustment factor (full depletion/multiple-gate effects) (0–1) [11]	1.0	1.0	1.0	1.0	1.0		0.6	0.5	0.5	0.5	0.5	0.5
Effective saturation carrier velocity enhancement factor (due to quasi-ballistic transport) [12]	1.0	1.0	1.0	1.0	1.0		1.1	1.1	1.1	1.3	1.3	1.3
Parasitic source/drain series resistance ( $R_{sd}$ ) ( $\Omega \cdot \mu m$ ) [13]	180	180	180	171	162		135	116	107	88	79	60
Ideal NMOS device gate capacitance ( $F/\mu m$ ) [14]	7.40E-16	6.39E-16	6.14E-16	5.69E-16	6.64E-16		5.65E-16	4.39E-16	4.49E-16	3.45E-16	3.45E-16	2.69E-16
Parasitic fringe/overlap capacitance ( $F/\mu m$ ) [15]	2.40E-16	2.40E-16	2.40E-16	2.30E-16	2.20E-16		1.80E-16	1.50E-16	1.40E-16	1.20E-16	1.00E-16	8.00E-17
High-performance NMOS intrinsic delay, $\tau = C_{gate} * V_{dd} / I_{dsat}$ (ps) [16]	1.20	0.95	0.86	0.75	0.64		0.39	0.30	0.26	0.18	0.15	0.11
Relative NMOS intrinsic switching speed, $1/\tau$ , normalized to 2003 [17]	1.00	1.26	1.39	1.60	1.86		3.06	4.05	4.64	6.80	8.08	10.77
Nominal logic gate delay (NAND Gate) (ps) [18]	30.24	23.94	21.72	18.92	16.23		9.88	7.47	6.52	4.45	3.74	2.81

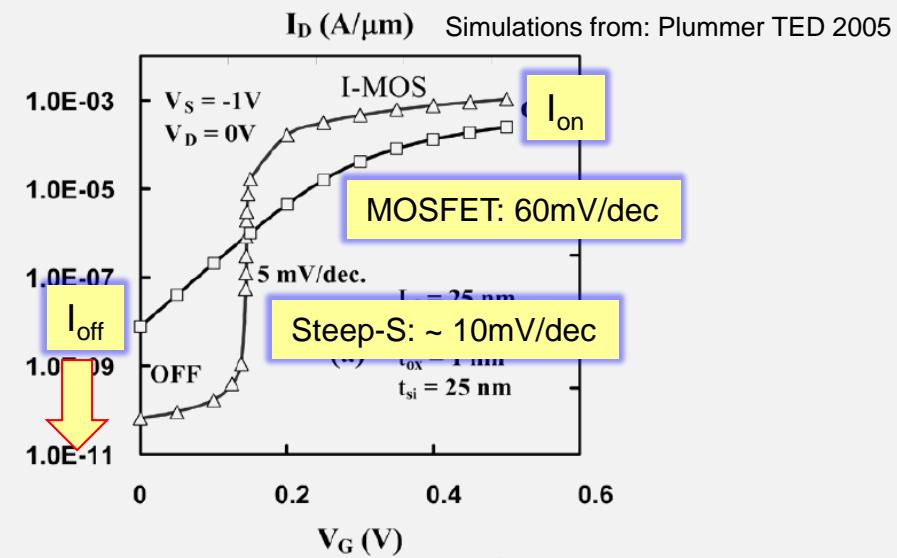
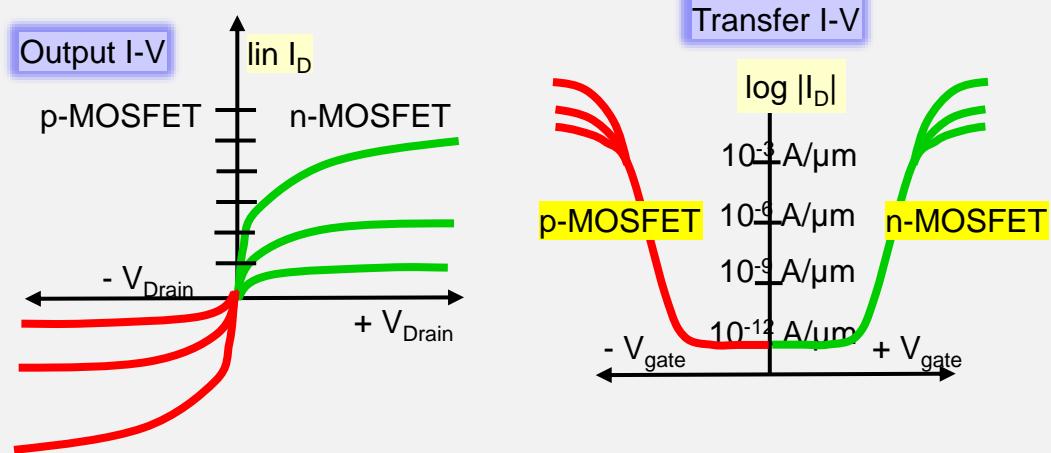
Many problems may arise with future MOSFETs

One problem is subthreshold leakage current

How can we handle this problem ?



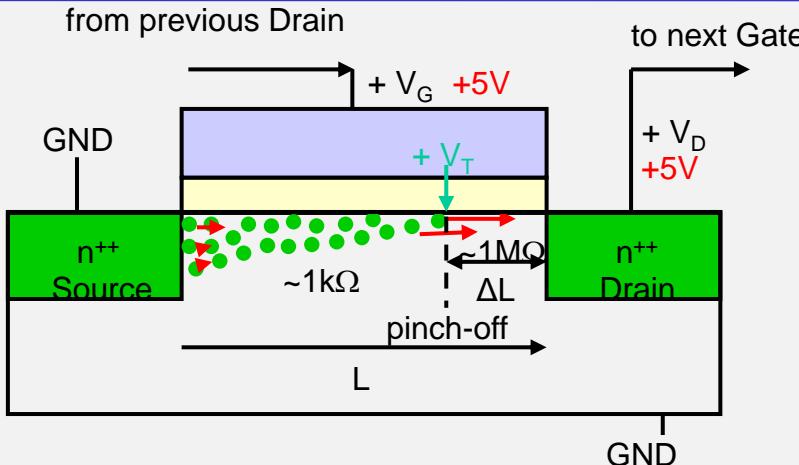
$$I_D = \mu C_{ox} \cdot \frac{w}{L} \cdot \left[ (V_{GS} - V_T) \cdot V_{DS} - \frac{V_{DS}^2}{2} \right]$$



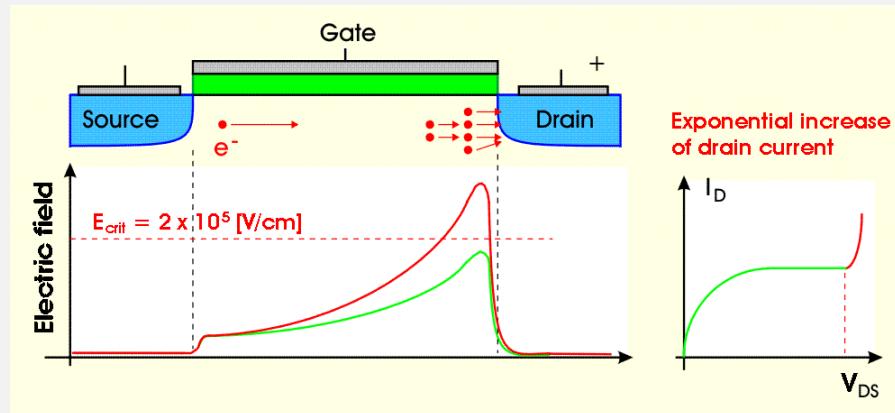
For reduction of power consumption :

- reducing  $V_{supply}$
- reducing  $V_{th}$
- reducing  $I_{off}$

Steep-S Devices



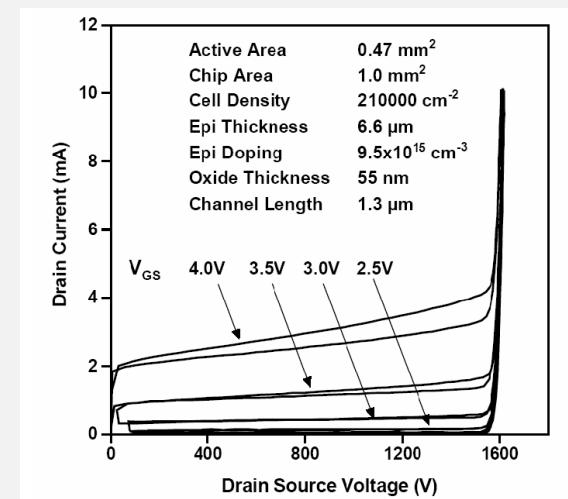
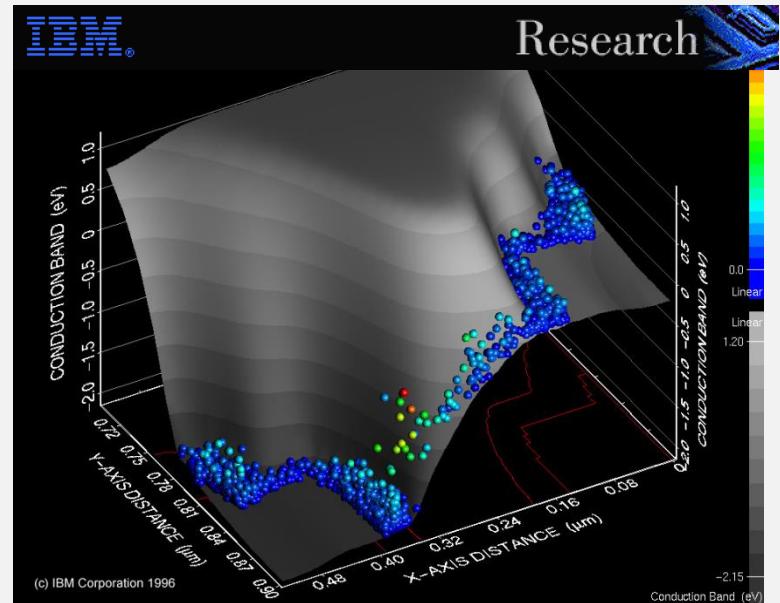
Current transport: continuity equation:  $\vec{j} = n \cdot e \cdot \vec{v} = \text{const}$

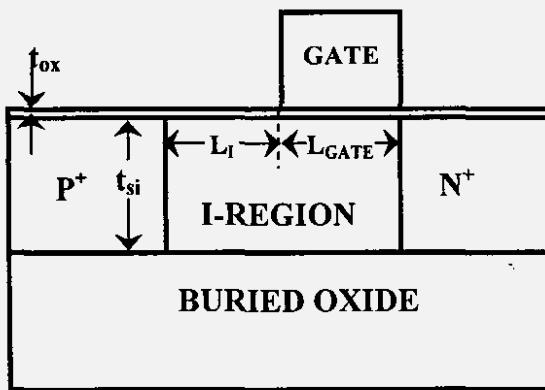


Any MOSFET is able to create impact ionization

basically we need a high electric field -> two types:

- npn type
- pin type

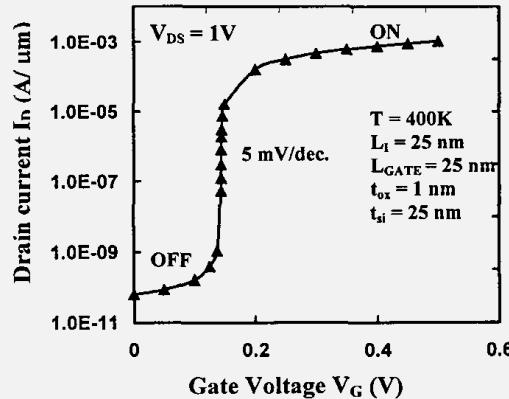




2002 Stanford, Plummer et al.

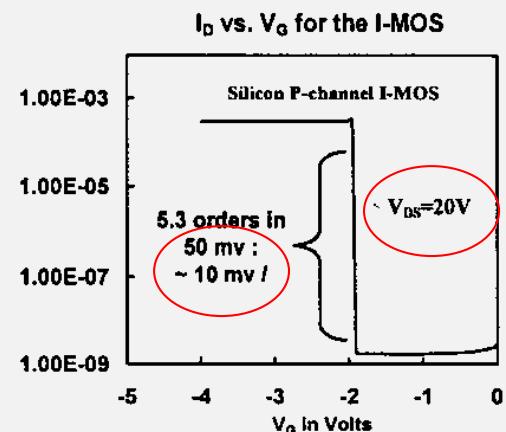
Operating principle: MOS-Gated pin-diode

- without Gate voltage: below break-down
- with Gate voltage:
  - reduction of channel length
  - > increase of electric field
  - > impact ionization
  - > fast current increase
  - > steep-S

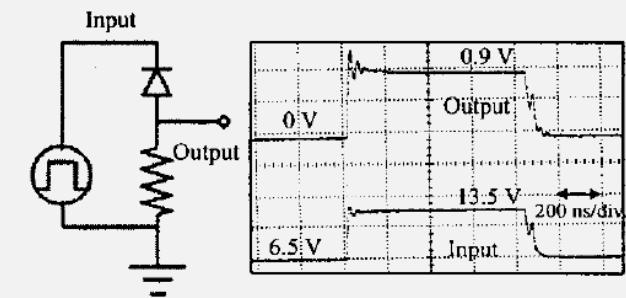


Simulation: Ge-IMOS  
Steep-S: ~5mV/dec

Drain Current  $I_D$  in Amps



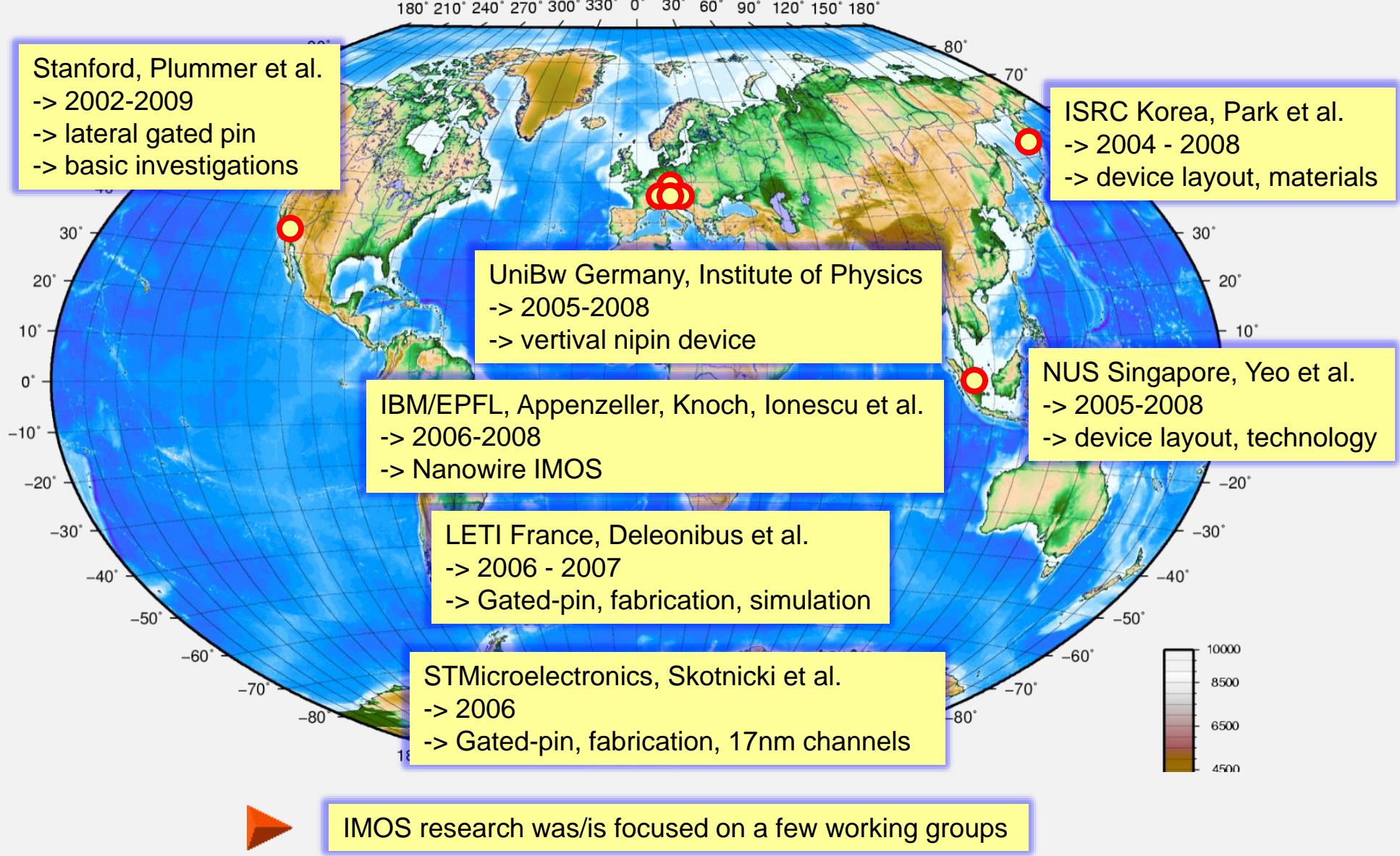
Experimental:  
-  $S \sim 10 \text{ mV/dec}$ ,  $-I_{on}/I_{off} \sim 5 \text{ dec}$   
-  $V_{DS} = 20 \text{ V}$ , - no reliability !



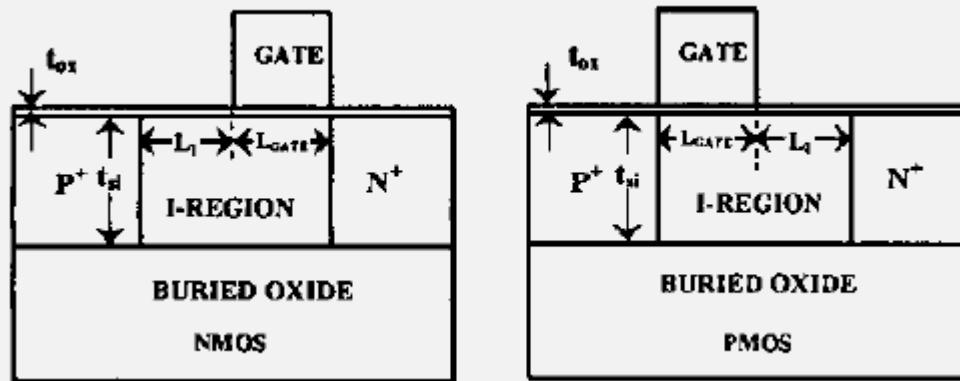
Simulation Switching:  
- not IMOS, but pin-diode  
- off-switching  $\sim 100 \text{ nsec}$

IMOS looks basically promising





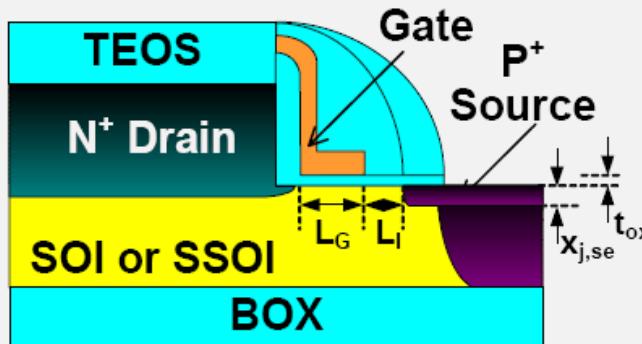
pin-IMOS



This type is investigated by:

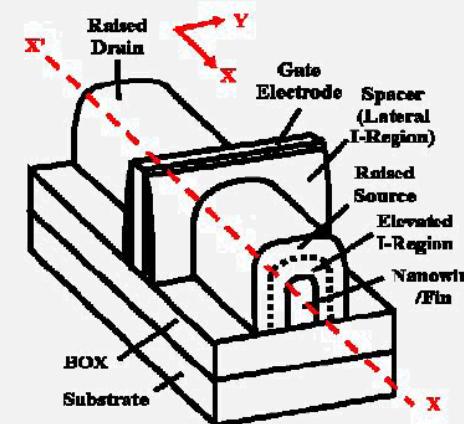
- \* Stanford, Plummer et al., 2002
- \* STMicroelectronics, Skotnicki et al., 2006
- \* LETI, Deleonibus et al., 2006

- \* lateral pin
- \* Gate creates channel, reducing i-zone, increasing field -> impact
- \* complementary types proposed
- \* high voltages, low reliability



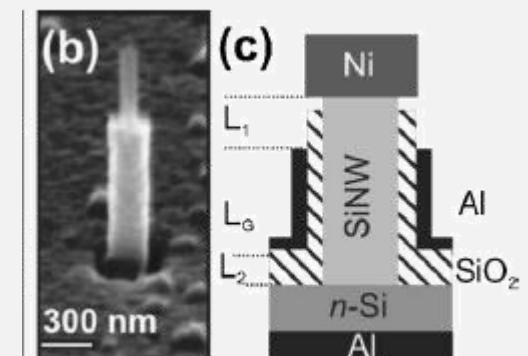
NMDC 2006, ISRC Korea, Park et al.

\* self-aligned spacer fabrication process



2007 IEDM, NUS Singapore, Yeo et al.

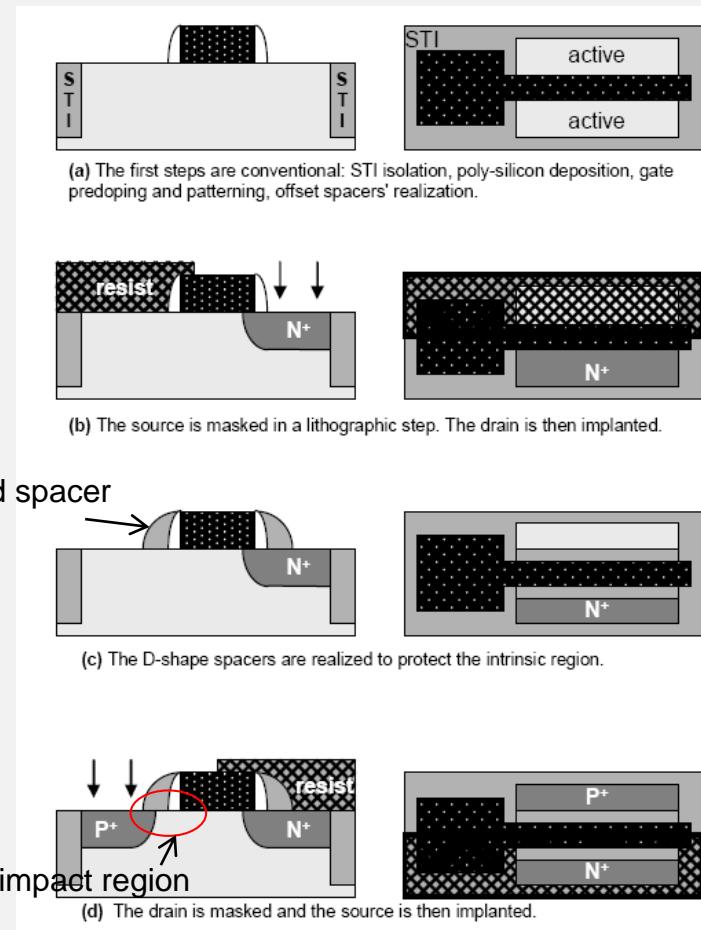
\* Nanowire (Si, SiGe) with wrapped Gate



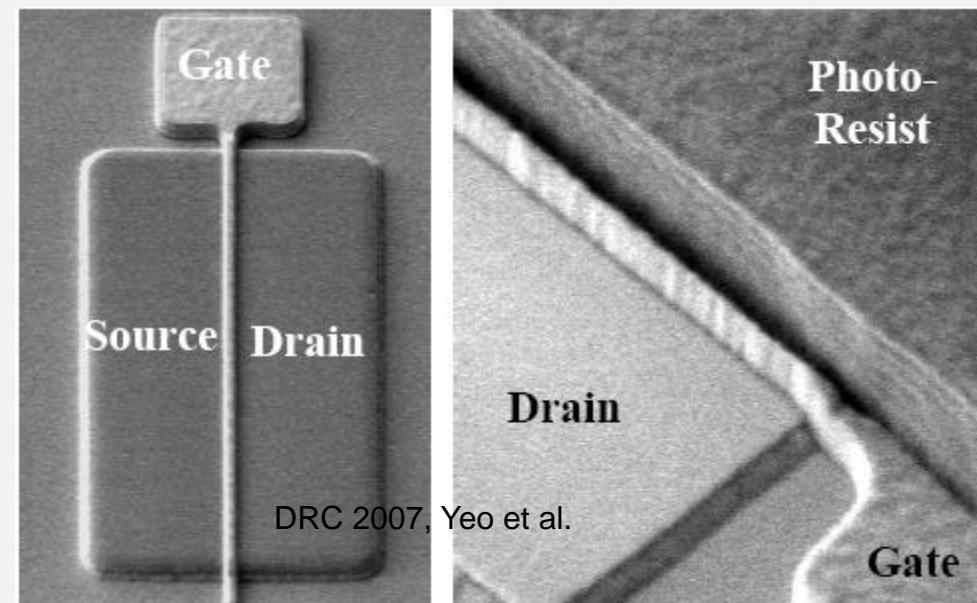
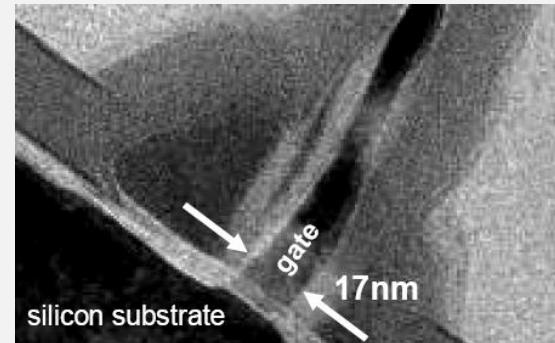
2007 APL, IBM Swiss, Björk et al

\* Vertical Si-Nanowire with wrapped Gate

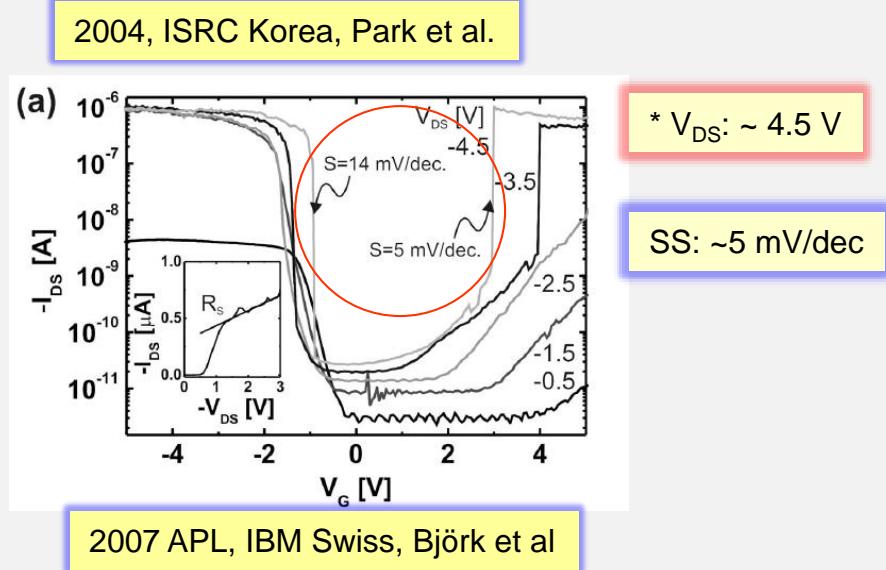
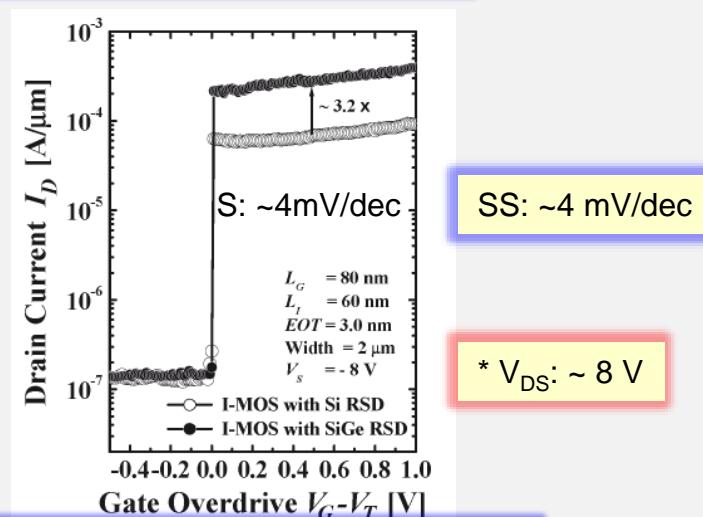
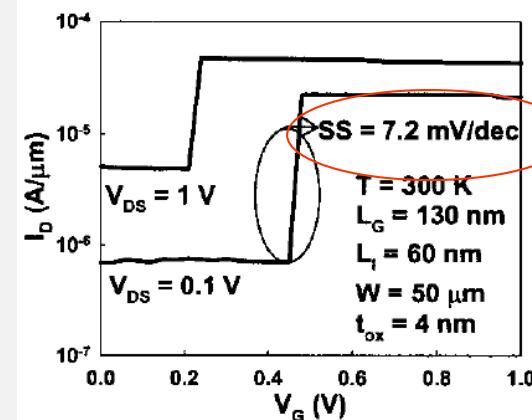
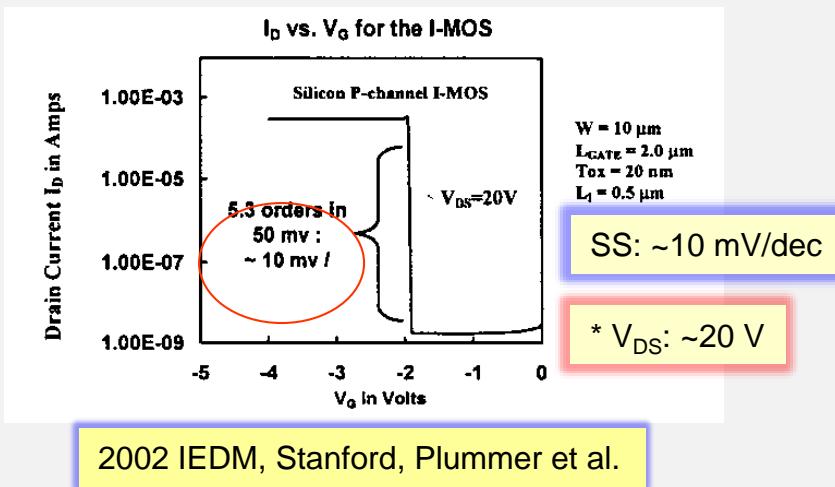
Typical CMOS-compatible Fabrication Process:



from STMicroelectronics Skotnicki

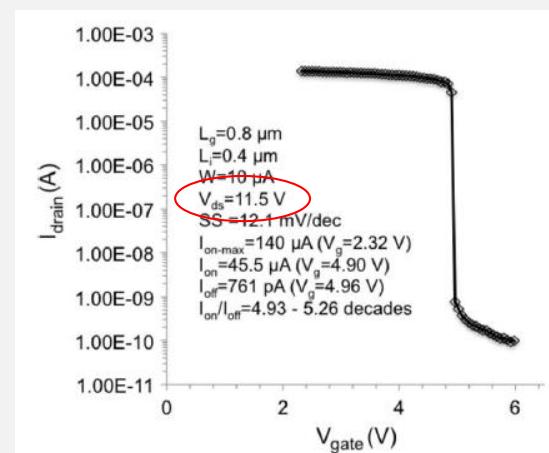
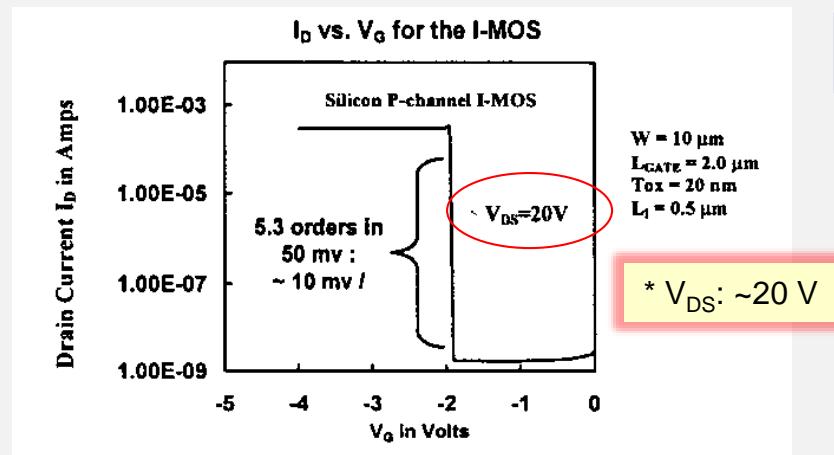
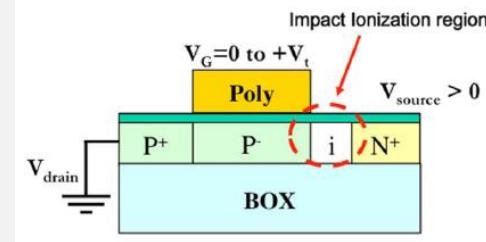
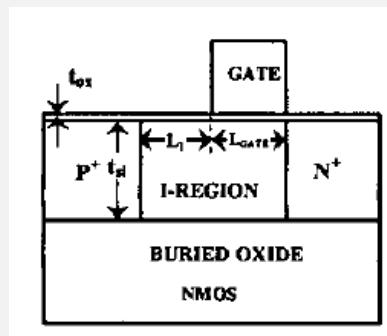


Challenge: adjustment of mask on top of minimum feature size Gate



Result:

- Impact Ionization can be realized easily, even in conventional MOSFETs
- Impact Ionization can be boosted by small variations in the design of conventional devices (MOS-gated pin-diodes)
- Achievement of  $S < kT/q$  MOSFET-limit is not a problem



2002 Plummer: Experimental V<sub>DS</sub> ~ 20 V

2009 EDL, Plummer et al.:

"A Novel Depletion-IMOS (DIMOS) Device with Improved Reliability and Reduced Operating Voltage"

\* normally-on device

\* Experimental V<sub>DS</sub> ~ 12 V

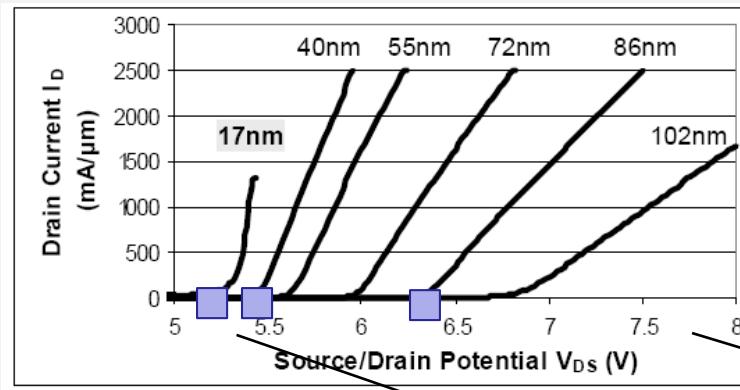
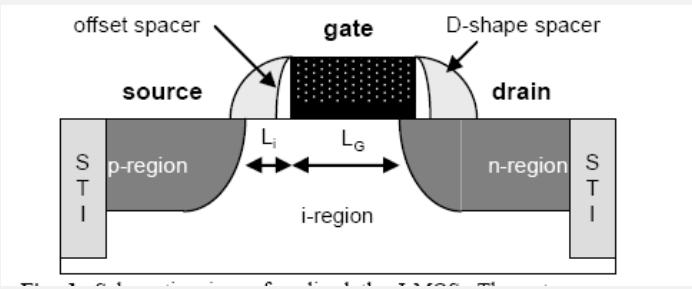


The operating voltage V<sub>DS</sub> still high (~12V)

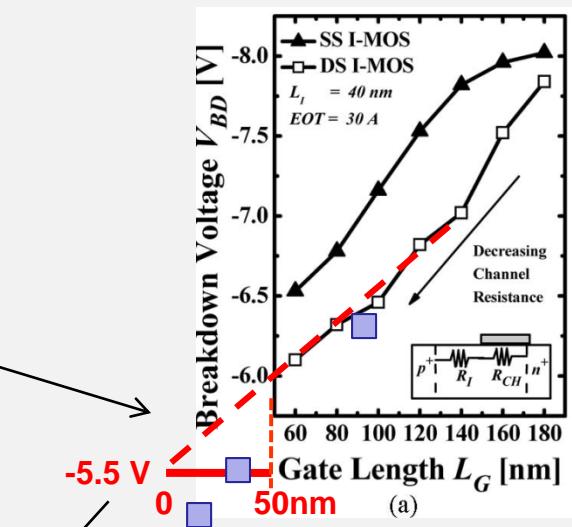
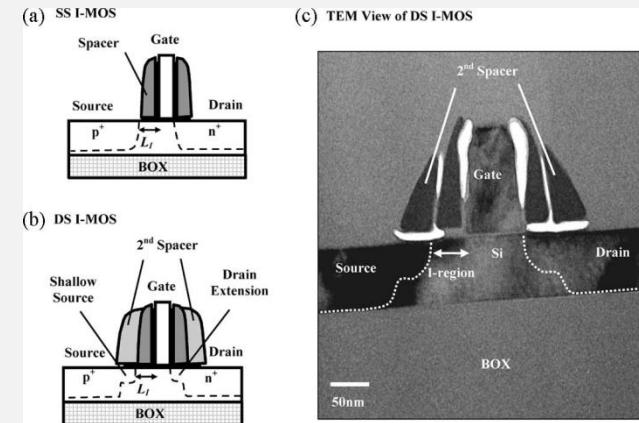


Where is the limit ?

2006 IEDM, STMicro, Skotnicki et al.



EDL 2008, NUS Singapore, Yeo



The operating voltage seems to saturate around 5-6  $V_{DS}$  for pin-IMOS with surface channel

Bulk Impact Model:

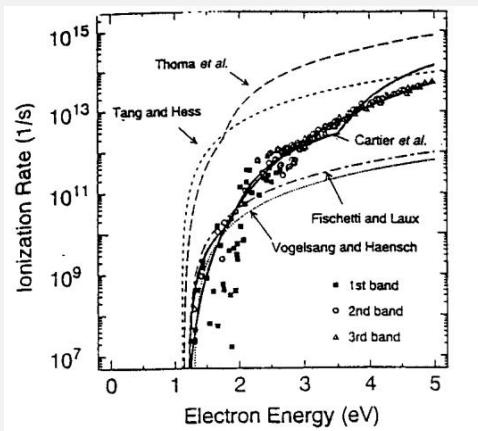
$$G = \alpha_n n v_n + \alpha_p p v_p$$

$$\alpha(\vec{E}) = \left( \frac{q\vec{E}}{Q_{ion,eff}} \right) \cdot \exp \left[ - \frac{\vec{E}_{is}}{\vec{E} \cdot \left( 1 + \frac{\vec{E}}{\vec{E}_{op}} \right) + \vec{E}_{kT}} \right]$$

$$\alpha(E) = A_n \cdot \exp \left[ - \frac{\vec{E}_{crit}}{\vec{E}} \right]$$

$$A_n \sim 7 * 10^5 \text{ cm}^{-1}$$

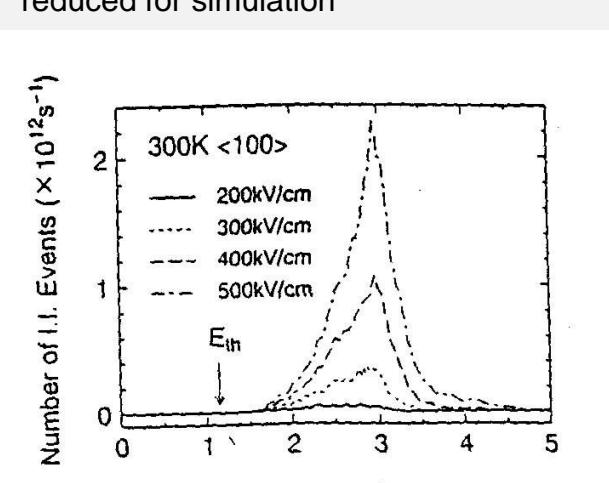
$$E_{crit} \sim 1.22 * 10^6 \text{ V/cm}$$



E: electrical field,  
 $E_{is}$ : threshold field for ionization scattering,  
 $E_{op}$ : threshold field for optical-phonon scattering,  
 $E_{kT}$ : threshold field for thermal scattering,  
 $Q_{ion,eff}$ : effective ionization energy  
[Si: ~3.6 eV for electrons]

Calculated impact ionization using various models

ionization threshold at electron energies  $> E_{gap}$



Independent of electric field the optimum energy for impact ionization is around 3 eV

Impact in regions of strong variations of electric fields (e.g. ...) non-local effects like velocity overshoot or dead space must be considered

Impact Ionization Energy:

$$W_{th}(e) \cong W_{gap} \cdot \left[ 1 + \frac{m_e^*}{m_e^* + m_h^*} \right]$$

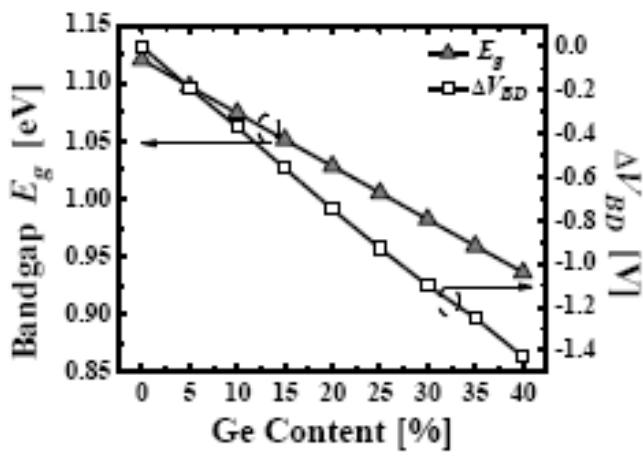
analog for holes



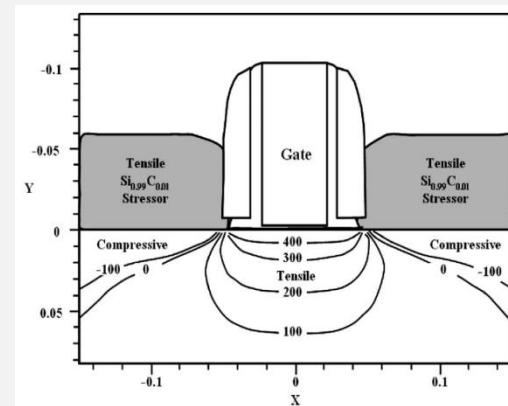
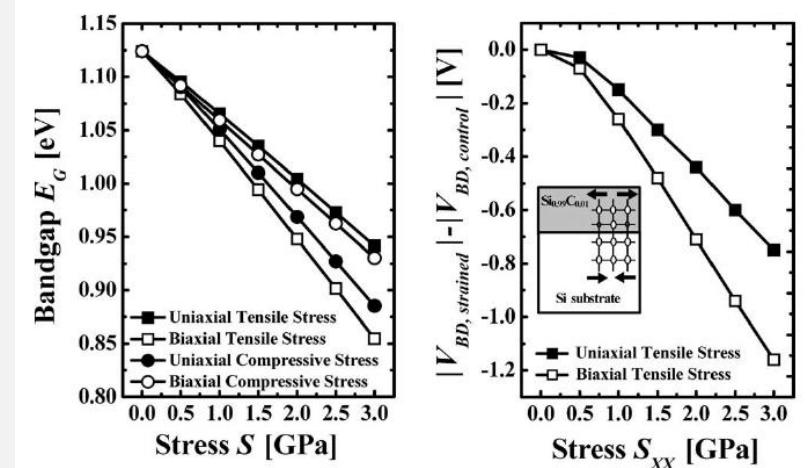
new materials with lower  $W_{gap}$  or smaller  $m^*$

bandstructure engineering by strain

reducing bandgap by changing material



changing bandstructure ( $E_{gap}$ ,  $m^*$ ) by strain



Many variations are possible:

- using SiGe  $\rightarrow$  Ge
- using strained Si on SiGe
- using strain liners (S/D, nitride cap)

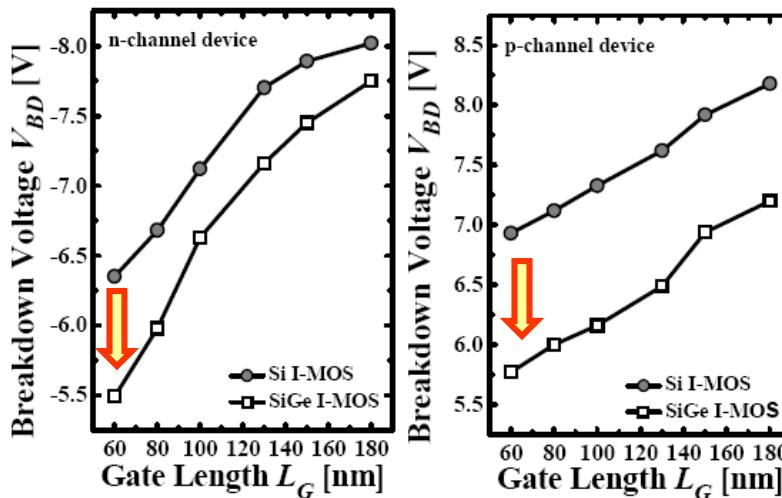
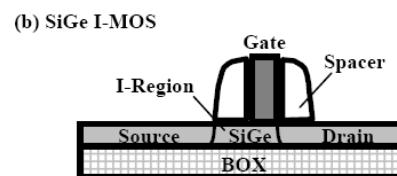
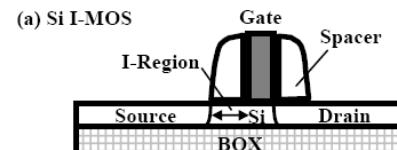
2007 DRC, NUS Singapore, Yeo et al.

Using  $\text{Si}_{0.75}\text{Ge}_{0.25}$

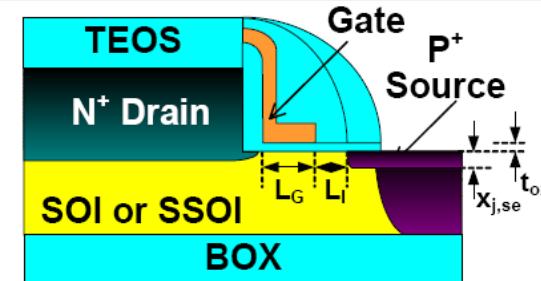


reduces bandgap by 0.1eV

Si: 1.1eV  
SiGe: 1.0eV



NMDC 2006, ISRC Korea, Park et al

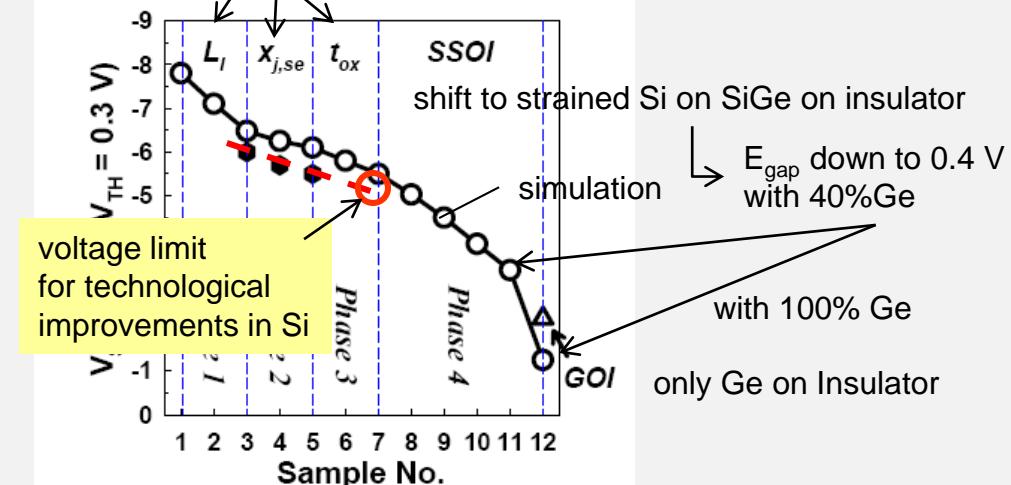


Proposing strained Si on SiGe



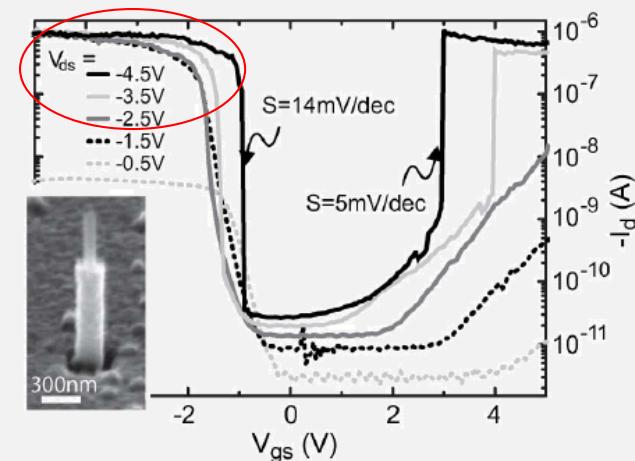
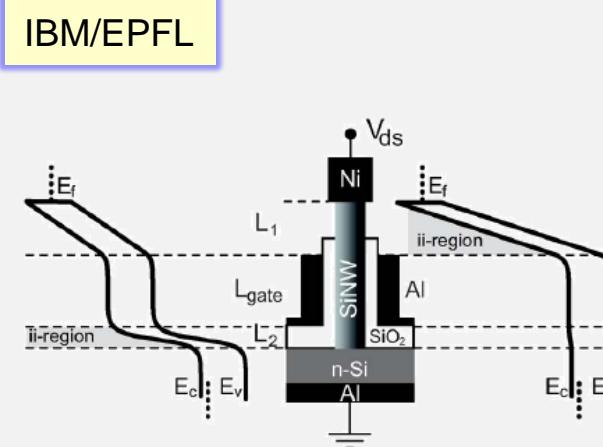
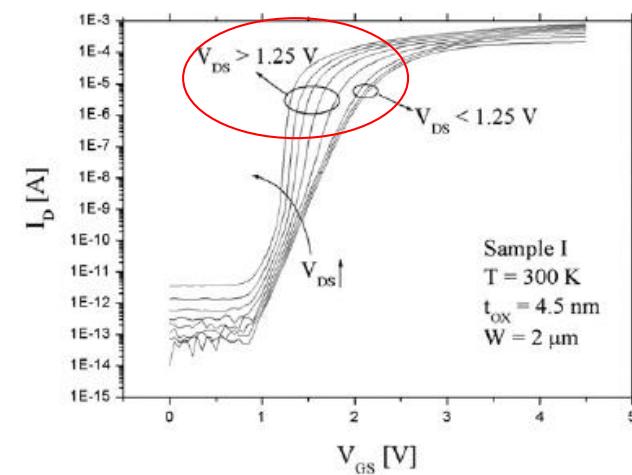
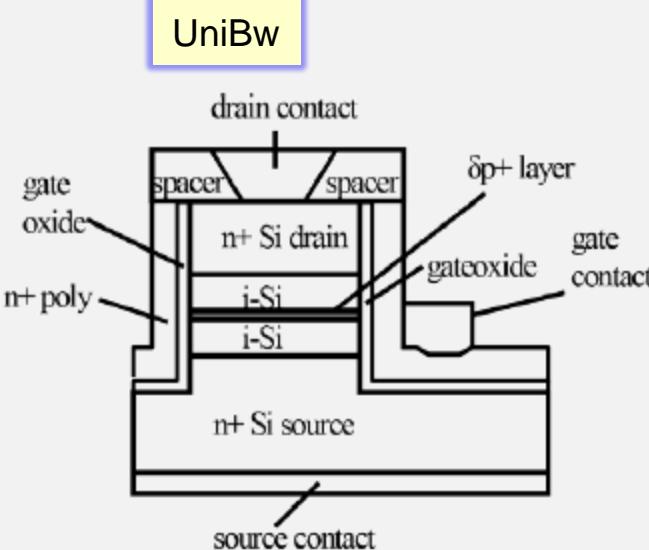
reduces bandgap down to 0.4eV

reduction of:



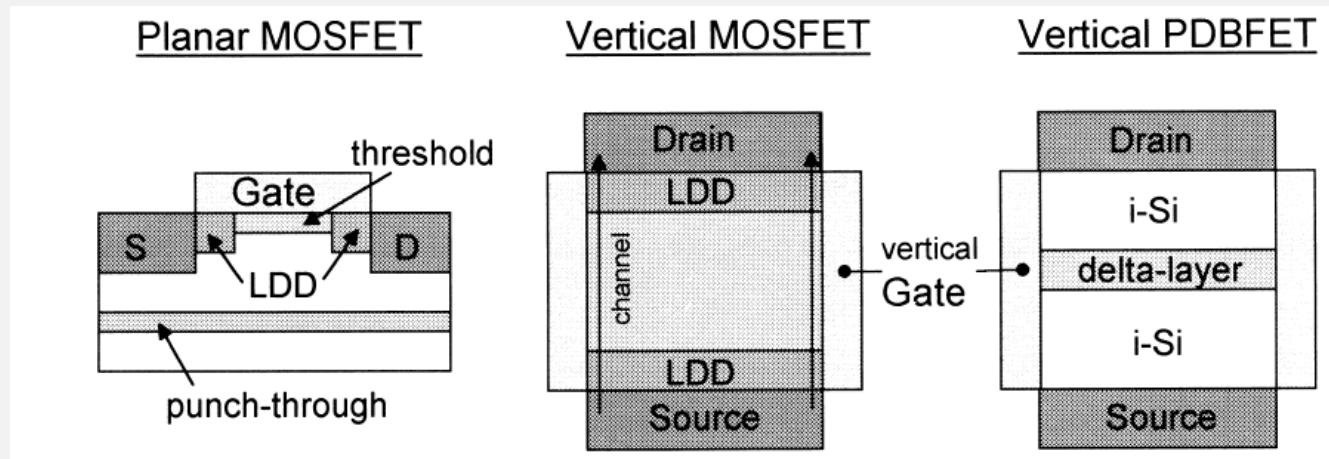
Simulations indicate for low bandgap materials like Ge (0.6eV) or s-Si on SiGe-On-Insulator (0.4eV)  $V_{DS}$  down to 1.3V



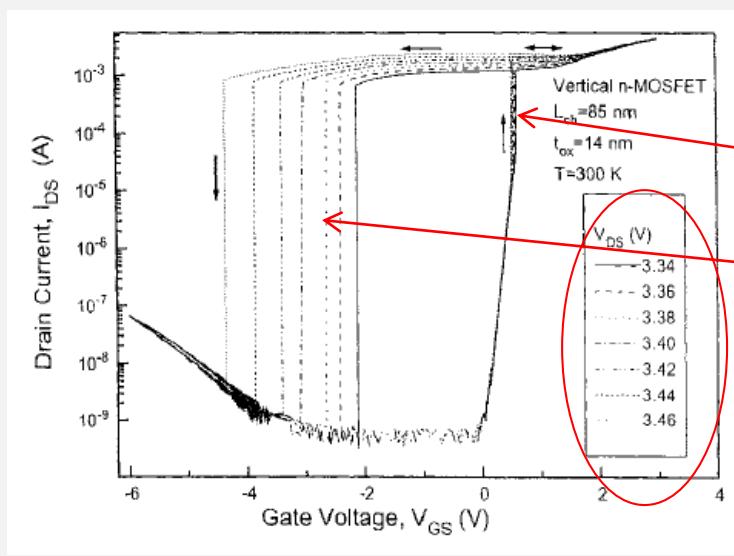
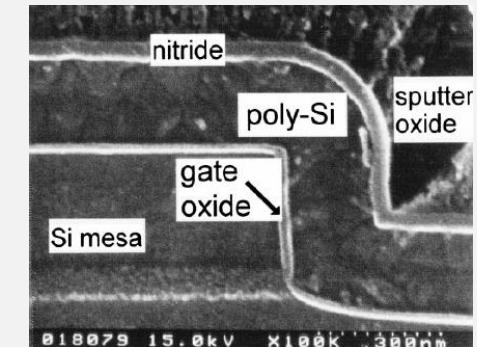


► Changing device layout enables benefits

1994 UniBw: Fabrication of vertical MOSFETs with channel length down to 50nm



1998 TSF, UniBw, Hansch et al.



Observation of:

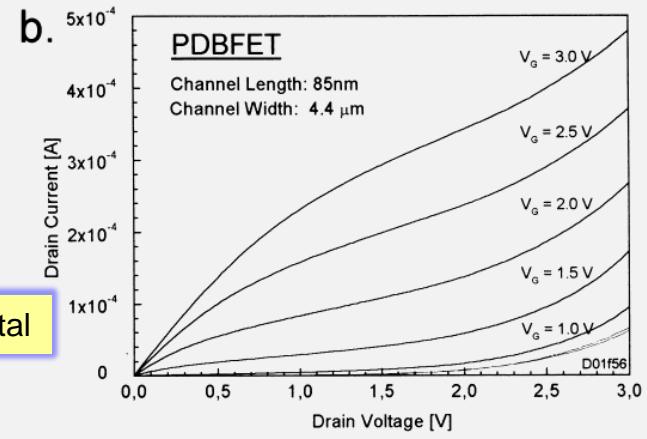
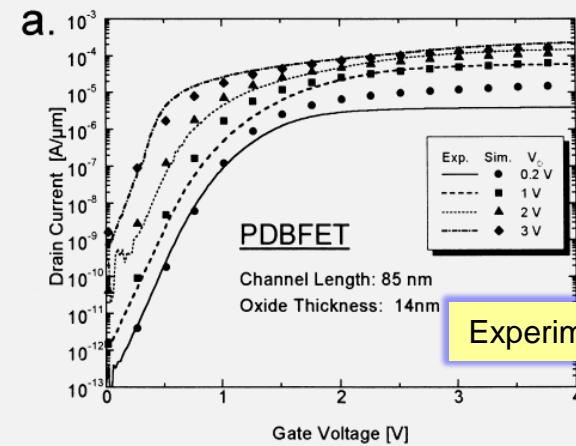
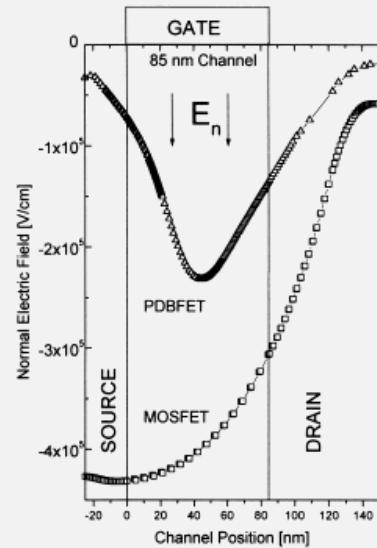
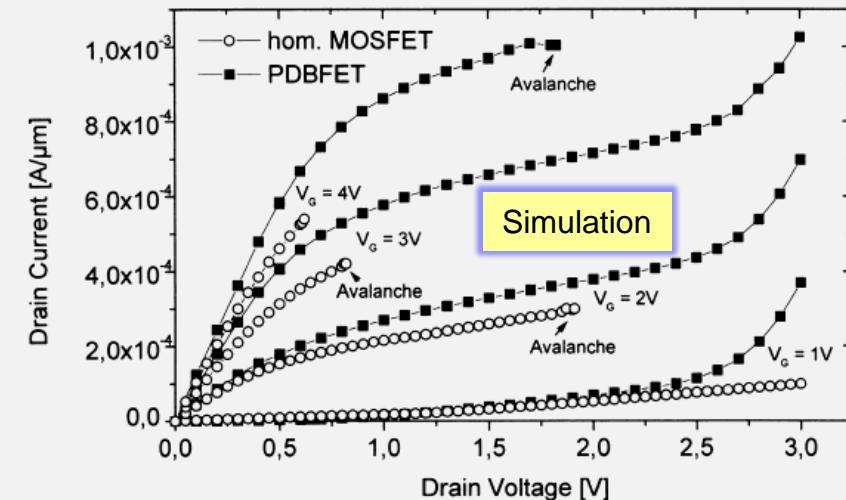
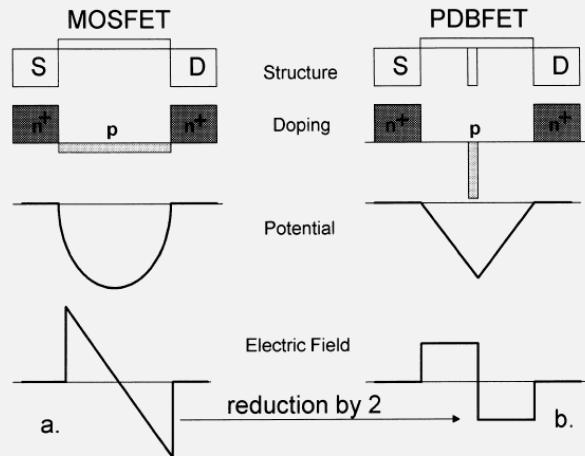
Impact Ionization at "high" voltages  $V_{DS} \sim 3\text{-}4\text{ V}$

Hysteresis behavior, dependent on  $V_{DS}$

This was a early SOI device

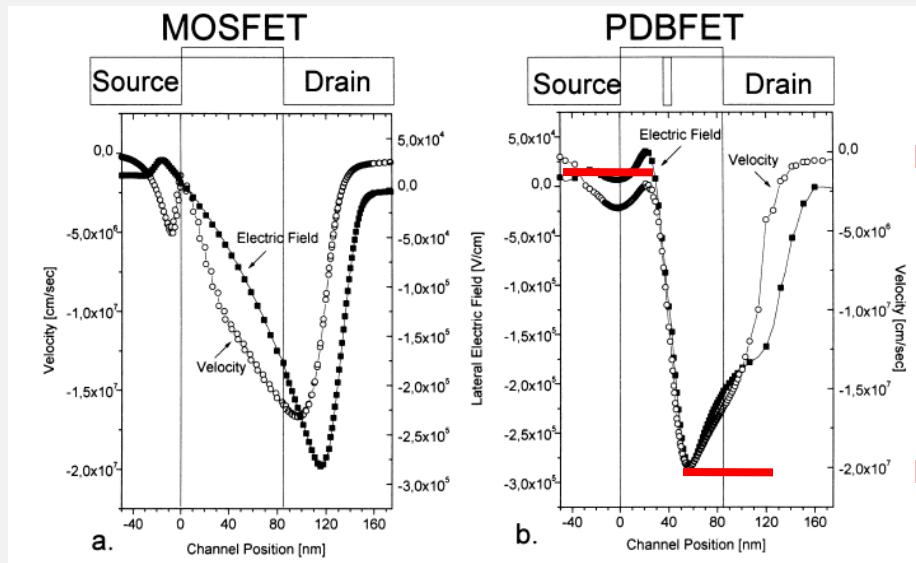
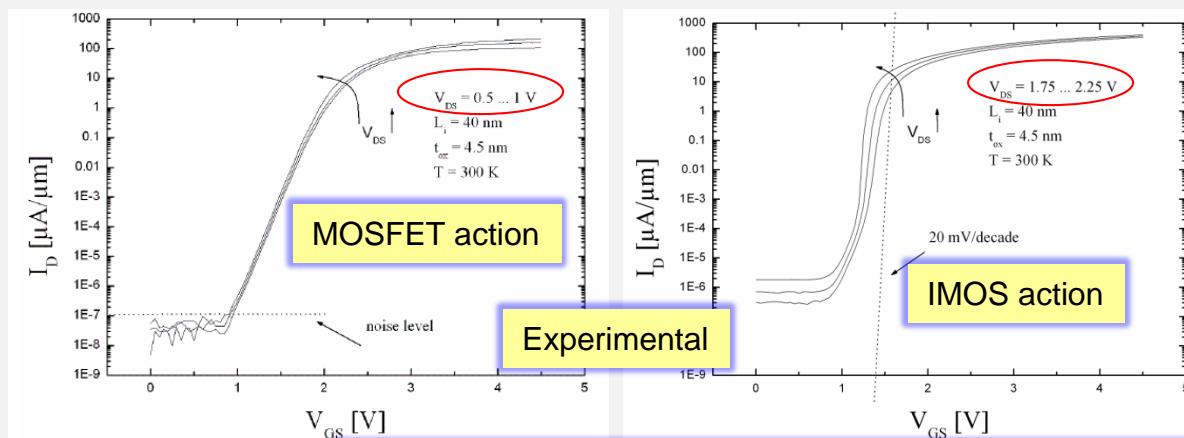
In this decade everybody was interested in suppressing "Short Channel Effects" like Impact Ionization

"Electric Field Tailoring" for suppression of Impact Ionization and Hysteresis



1998 Thin Solid Films, Hansch et al.

2006 UniBw, "Novel" Vertical IMOS

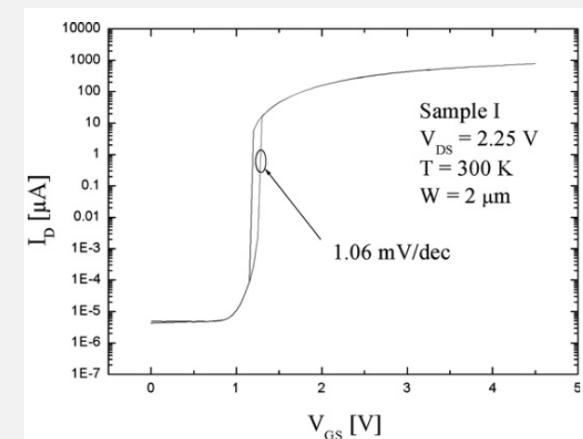
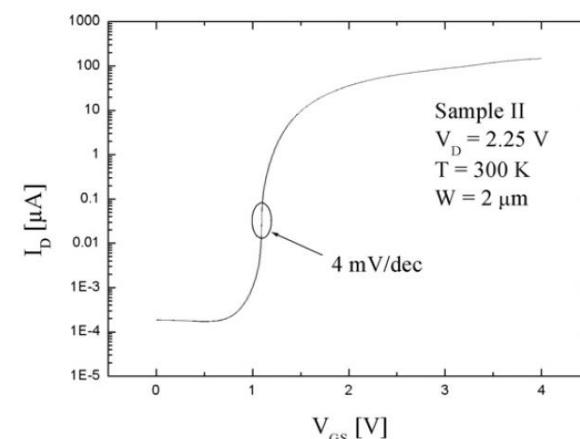
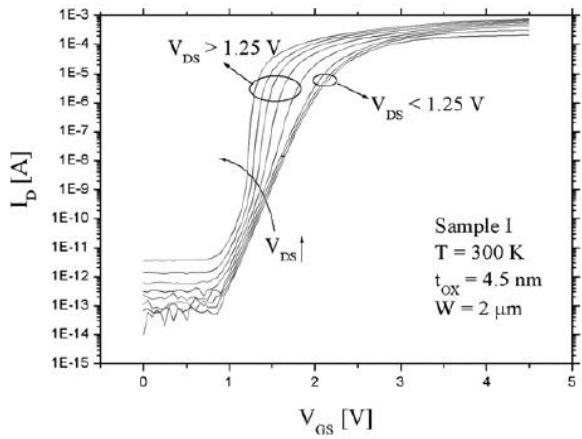
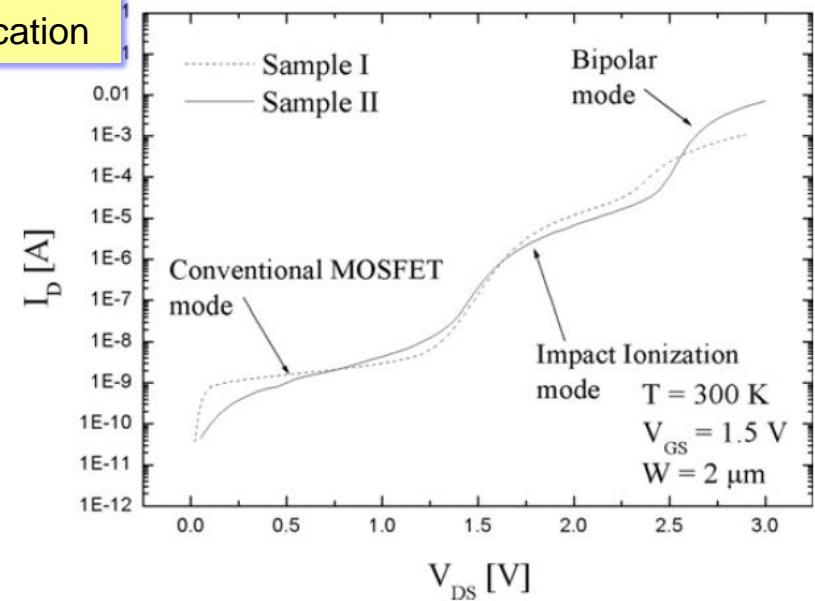
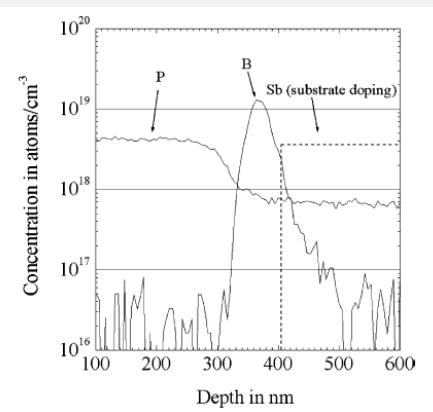
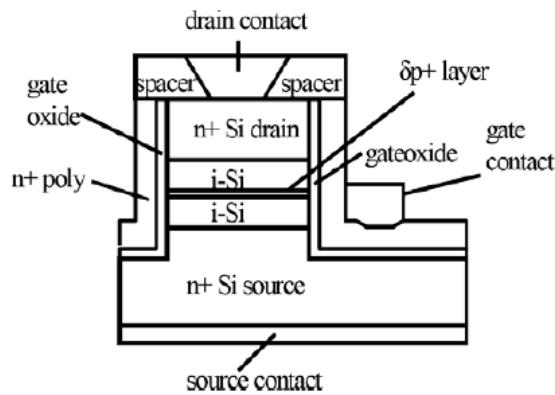
(inspired by IMOS Plummer, but there is the disadvantage of high voltages  $V_{DS} > 10$  V)Low electric field from Source to  $\delta$ -layer (about 50 nm)High electric field from  $\delta$ -layer to Drain (about 30 nm)

	Vertical I-MOS	[3]	[7]
Type	n	n/p	p
$L_{ch}$ (nm)	40	100	300
$V_{DSII}$ (V)	1.5	5.5	15
$I_{ON}/I_{OFF}$	$2.5 \times 10^8$	28.9/23	$10^5$
$I_{ON}$ (μA/μm)	500	81.1/78.2	$\sim 100$
S (mV/dec)	20	11.8	10

Proc. MIEL 2006, Abelein et al.

Steep S-slope < 20mV/dec can be realized at low voltages  $V_{DS} \sim 2$  V

Optimization of  $\delta$ -doping profile enables additional bipolar amplification



with bipolar action steep slopes and hysteresis is enabled

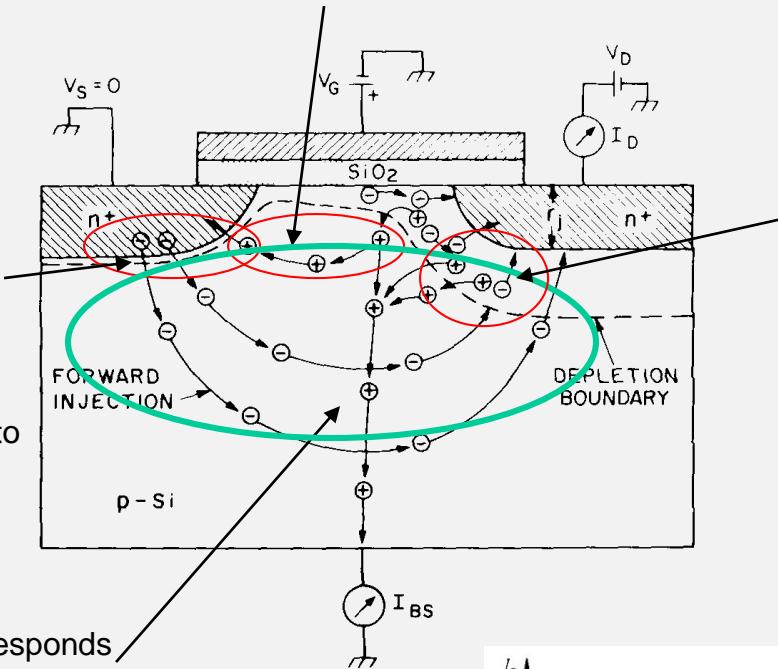
## Parasitic Bipolar Transistor

see chap.3

2 The existence of positively charged holes increases the substrate potential and lowers the junction barrier or even generate a forward biased junction for electrons

3 From the Source electrons are injected into the substrate and attracted by the positively charged Drain

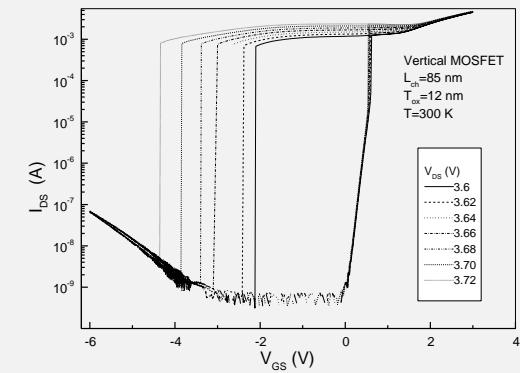
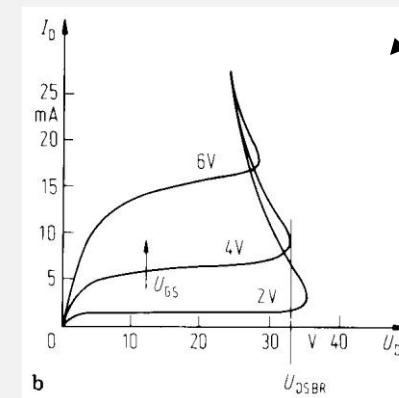
4 The resulting current increase corresponds to a „hidden“, **parasitic bipolar transistor**



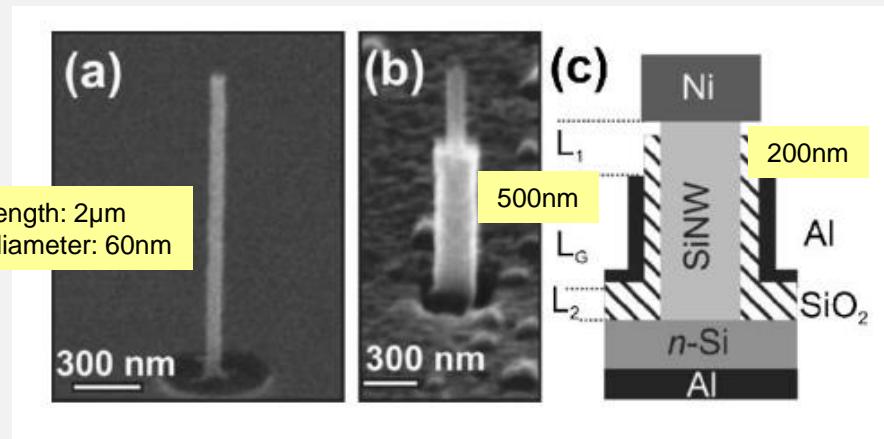
1 Some of the generated holes may be attracted by the negatively charged Source

5 Some of the electrons may generate additional e-h pairs, where the new holes support the the bipolar mechanism

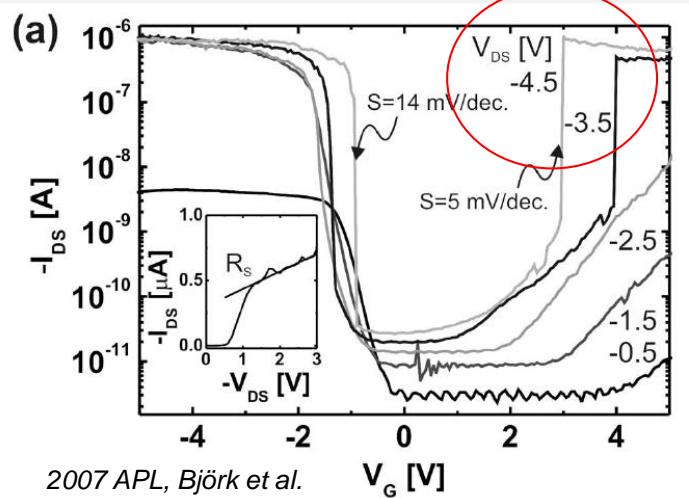
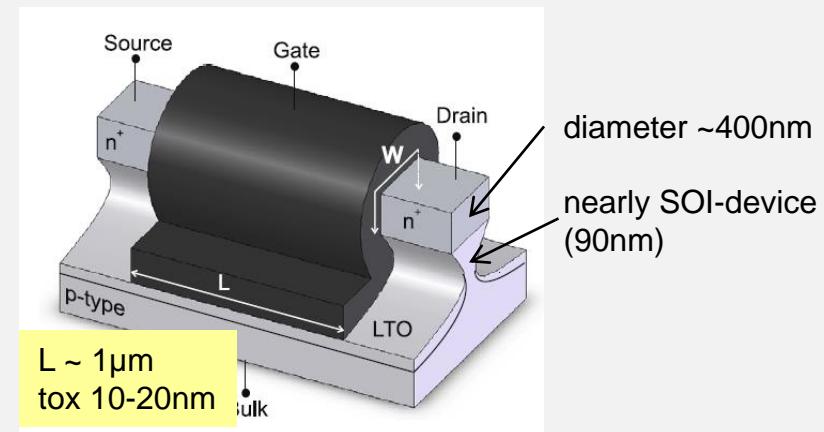
6 In consequence a self-controlling feed-back effect exists (**snap-back**)  
The gate voltage can be switched off, but current remains !



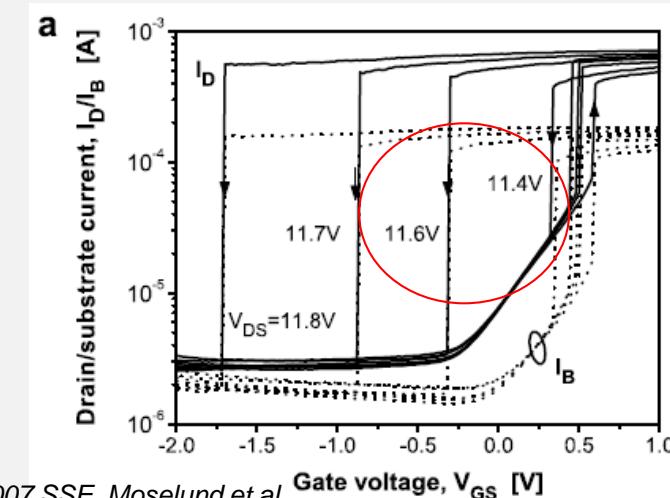
## 2007 IBM Swiss, Nanowire IMOS



## 2007 EPFL, PIMOS



Steep S-slope < 20mV/dec can be realized at low voltages  $V_{DS} \sim 2\text{V}$

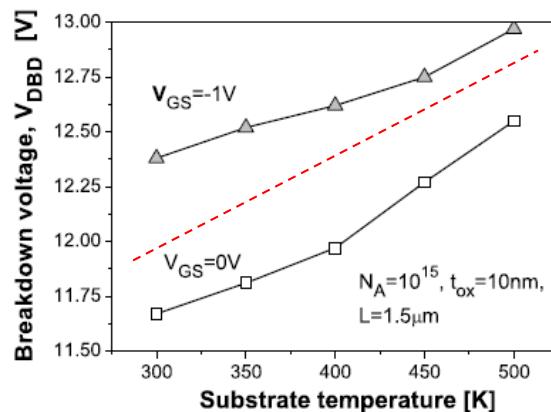


Steep S-slope < 20mV/dec and hysteresis can be realized at voltages  $V_{DS} \sim 11\text{V}$  due to long channel

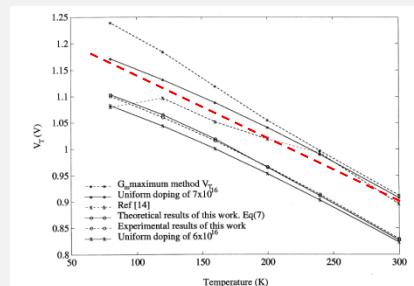
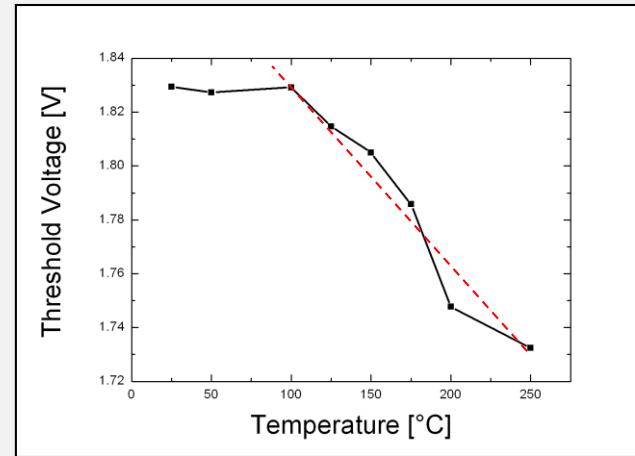
Dr.-Ing. J.Biba

AdMOS, 7-68

2007 EPFL, PIMOS



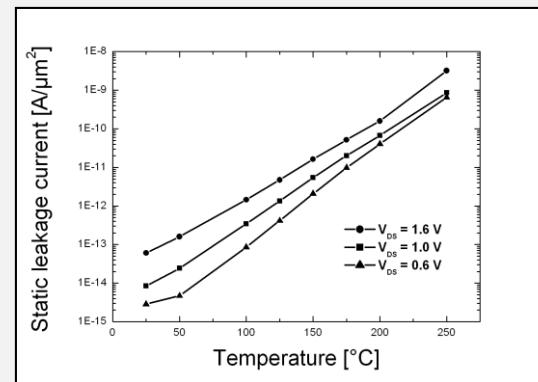
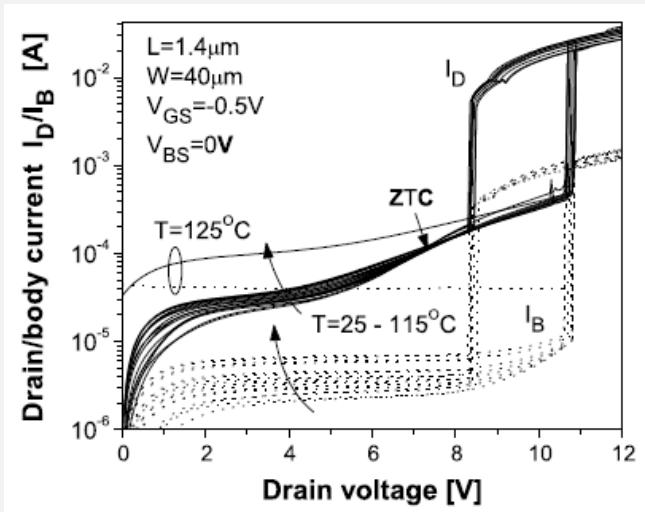
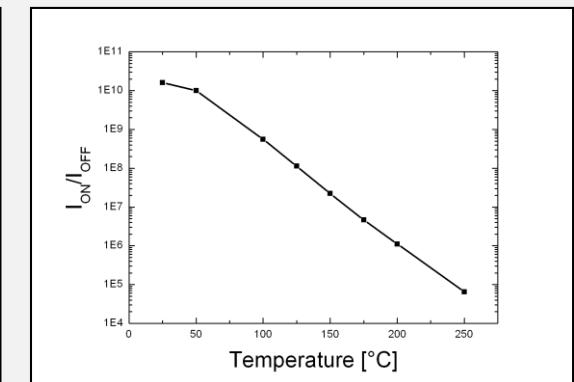
2008 UniBw



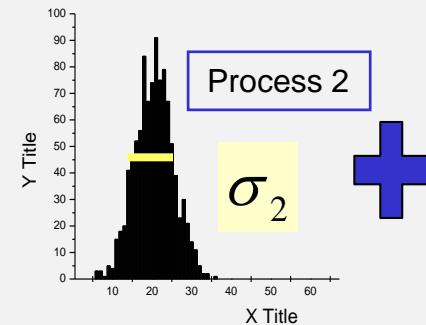
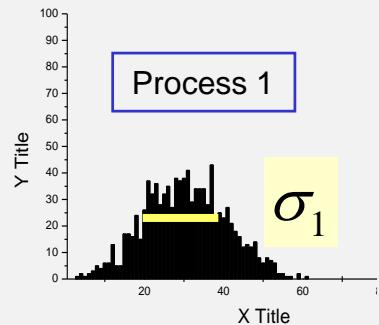
1998 SSE, Chen et al.

MOSFET.  $\sim 1\text{ mV/K}$ Threshold voltage dependence  $\sim 4\text{ mV/K}$ 

Threshold voltage reduction below 1mV/K

Drain source leakage current at 250°C:  $< 10^{-9}\text{ A}/\mu\text{m}^2$  $I_{ON}/I_{OFF}$  ratio at 250°C:  $> 10^5$

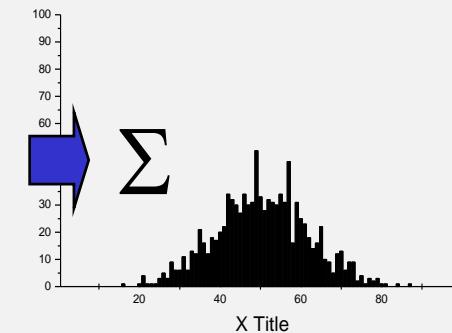
Remember: High-end CMOS exhibits about 25 mask steps, >500 process steps



**summing up:**

$$\frac{\sigma_{result}}{\mu_{result}} = \sqrt{\left(\frac{\sigma_1}{\mu_1}\right)^2 + \left(\frac{\sigma_2}{\mu_2}\right)^2 + \dots}$$

Three blue squares below the equation.



$$Y_R = Y_{Si} * Y_{poly} * Y_{m0} * Y_{m1} * Y_{m2} * \dots$$

With Steep-Slope devices like TFET, Nanowires, IMOS changing physics of carrier transport:



from "smooth" and "homogenizing" drift-diffusion

der Bundeswehr

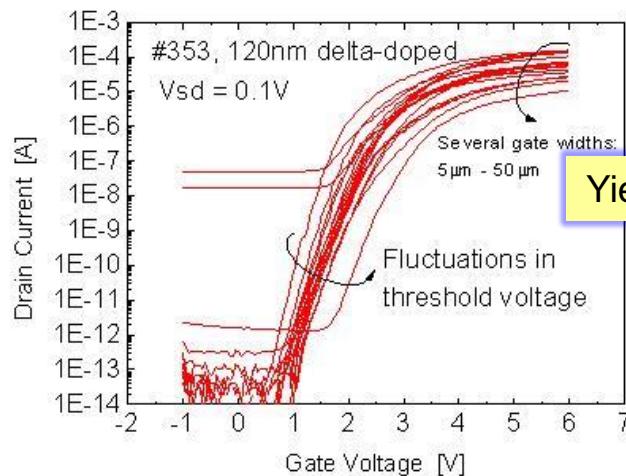


to

"extremely located" and "exponential wild" carrier generation

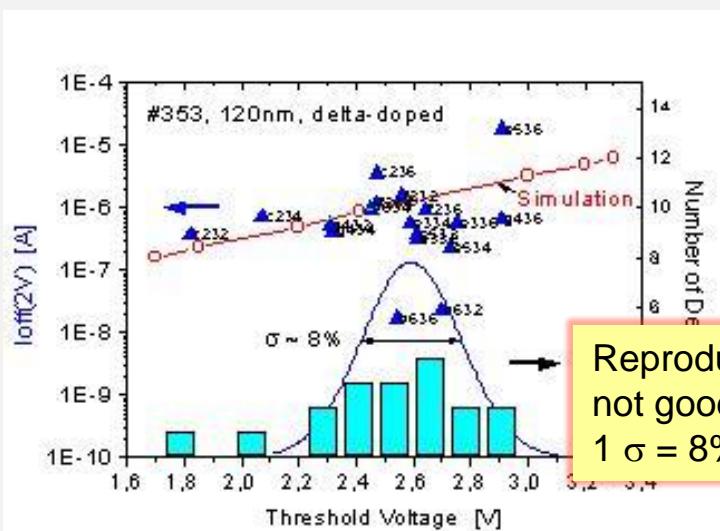
All groups no data !

### Old data on PDBFET, 1999 UniBw



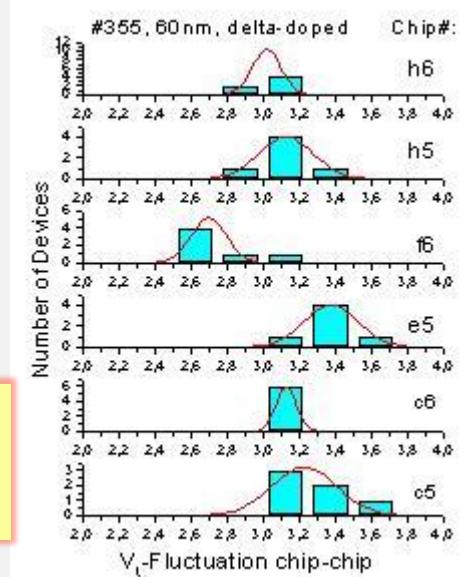
Yield = defect devices/ good devices =70-80%

(3"-wafer)



Requirement for 50nm MOSFET  
(ITRS):

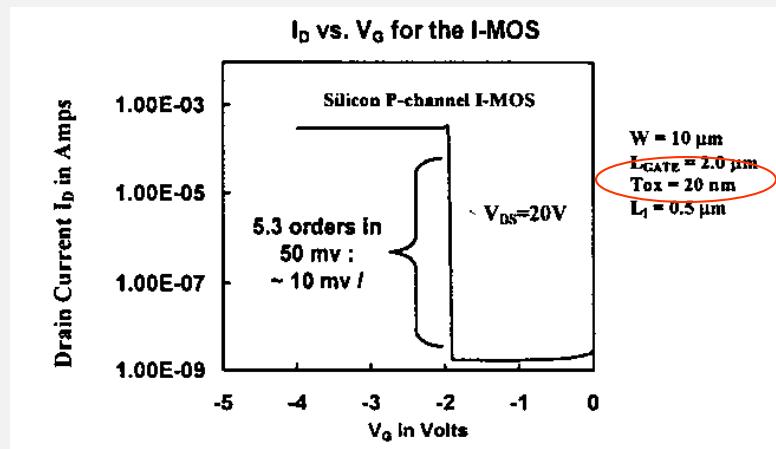
$3\sigma = 40 \text{ mV}$  at  $V_{th} = 0.3 \text{ V}$   
( $3\sigma \sim 15\%$ )



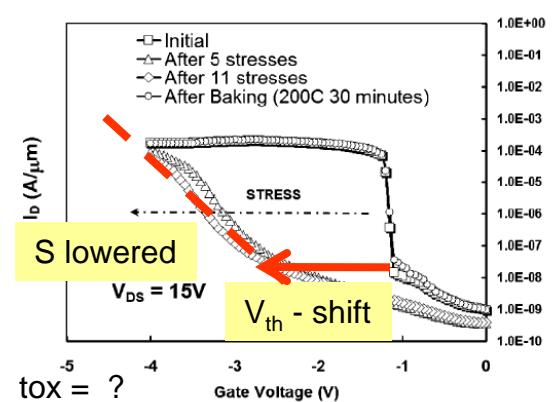
1999 ESSDERC, Hansch et al.

Reliability: what is the lifetime of the device ?

Lifetime is not time to complete breakdown,  
but time to leave parameters of about 10% from nominal value

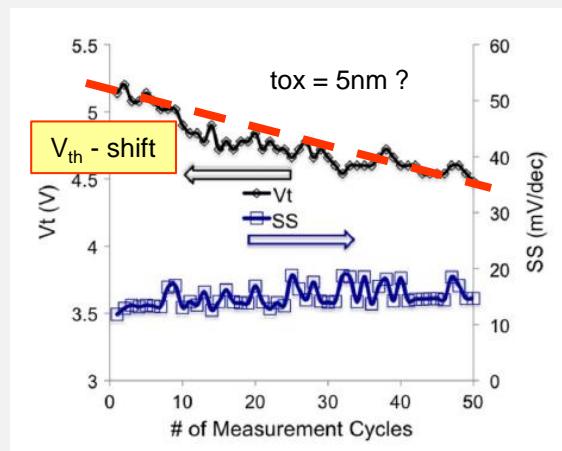


2002 Plummer: one-time device



2005 Plummer: several cycles

- large  $V_{\text{th}}$ -shift with every cycle
- loss of  $S < 60 \text{mV}$



2009 EDL, Plummer et al.:  
"A Novel Depletion-IMOS (DIMOS) Device with Improved Reliability and Reduced Operating Voltage"

- continuous  $V_{\text{th}}$ -shift with every cycle
- remaining of  $S < 60 \text{mV}$
- normally-on device

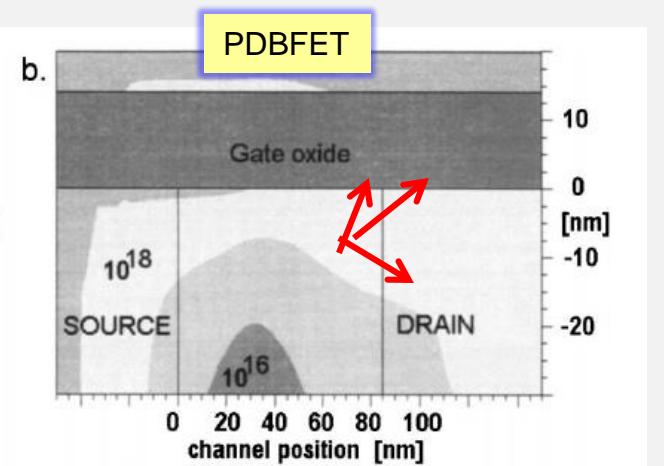
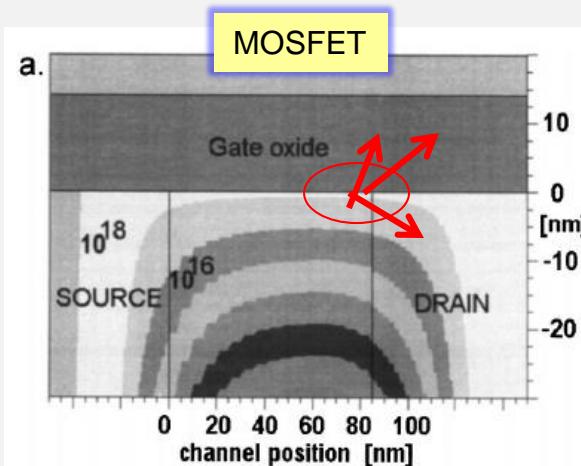
due to hot carriers degradation of the Gate oxide occurs

- shift of threshold voltage
- S is lowered

Why are some devices degrading, others not ?

Already in 2002 Plummer stated out, that the degradation by impact will be less by:

- very thin gate oxides (1-2nm)
- moving away impact region from gate



In a surface channel device the thickness of the channel is only a few nm, the location of impact region is very close to the gate oxide, scattering length of electrons in Si is about  $\lambda \sim 10\text{nm}$



Hot electrons  
- reach the Gate oxide  
- and are scattering within the Gate oxide



generation of oxide defects causes  $V_{th}$ -shift

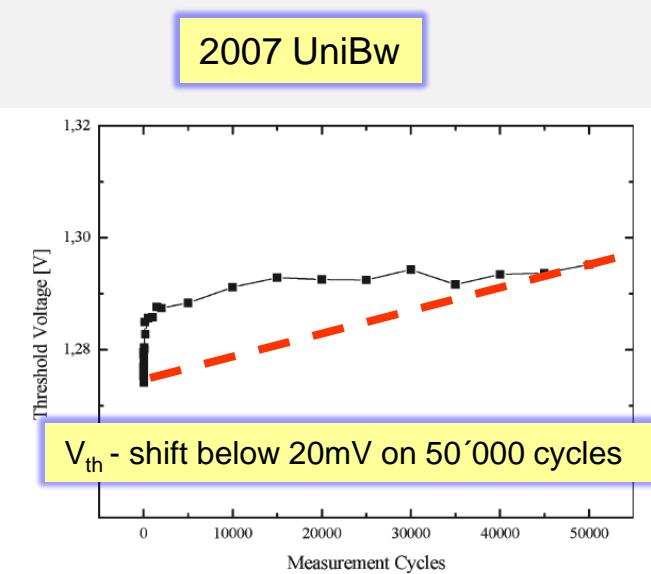
In a PDBFET the thickness of the channel is 10nm and more, the location of impact region is not close to the gate oxide



Hot electrons  
- merely reach the Gate oxide



Less generation of oxide defects, reduced  $V_{th}$ -shift, higher reliability



2007 EDL, Abelein et al.

Scalability: will smaller footprint devices (economics) -> leading to higher integration  
keeping or improving performance with less power consumption ?

In detail:

reduced geometries will:

- still guarantee proper device action
- allow reducing of  $V_{\text{supply}}$
- allow reducing  $I_{\text{off}}$
- allow reducing  $I_{\text{on}}$
- allow reducing circuit power consumption

} but footprints may be fixed by dimensions of contacts  
to achieve low serial resistance (like CMOS)



Proper device action

Impact ionization (and therefore basic I-V characteristics) is triggered by the strength of electric field E.

Electric field E will scale by:

$$E = \frac{V}{x} = \frac{V/S}{x/S} = E = \text{const}$$



reducing voltages and geometries  
will keep IMOS running



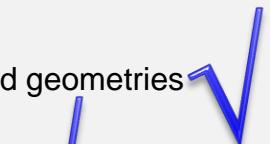
Reducing  $V_{\text{supply}}$ :

with smaller dimension x the  $V_{\text{supply}}$  may be reduced by the same factor S



Reducing  $I_{\text{on}}$ :

the impact region (surface or bulk) scales with channel width, so  $I_{\text{on}}$  will scale with reduced geometries



Reducing  $I_{\text{off}}$ :

Impact ionization takes place in an intrinsic region, so no conventional doping limitation.  
But parasitic effects like tunneling may increase  $I_{\text{off}}$

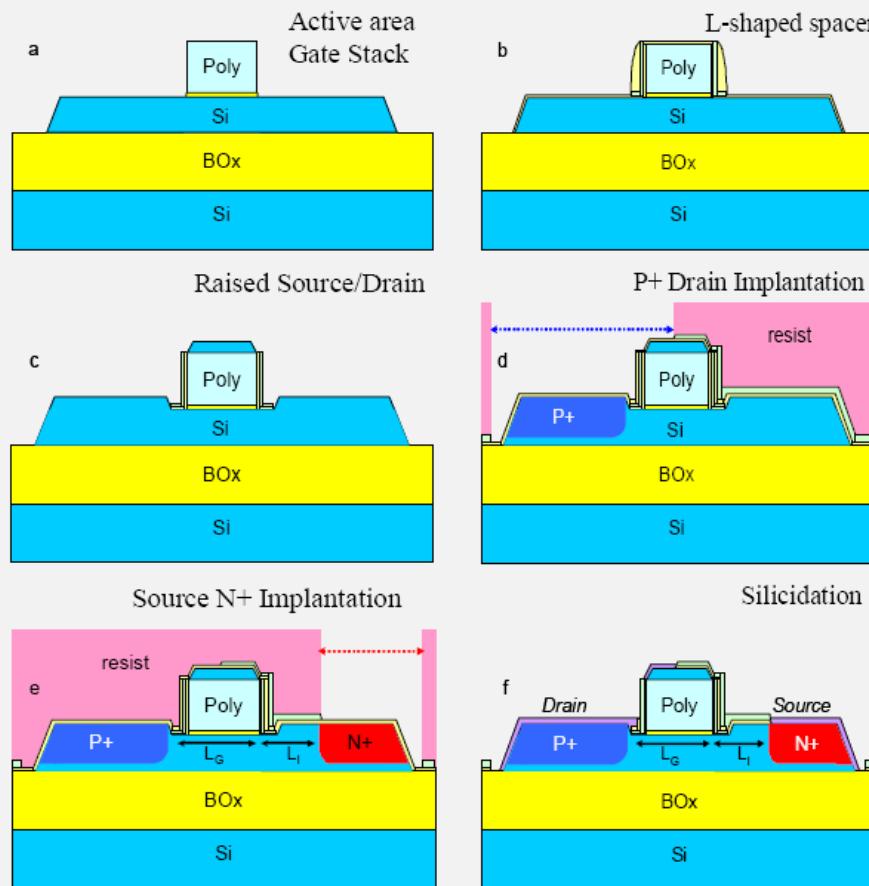
Circuit scalability:

questionable -> discussion

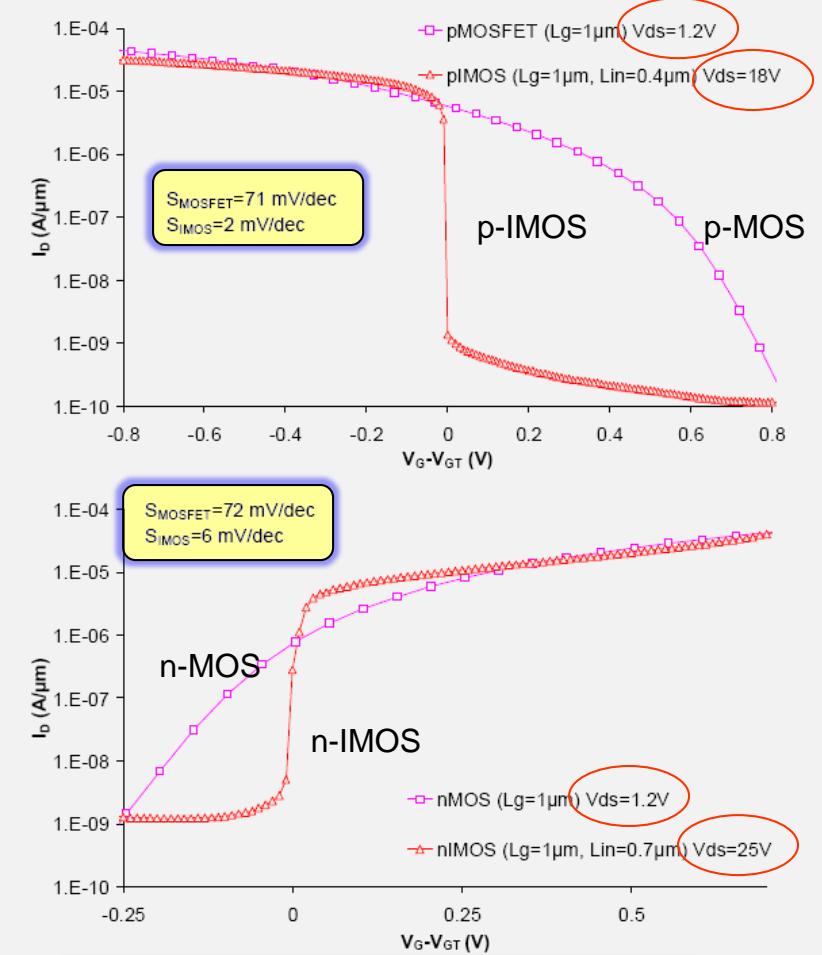


\* IEDM 2004, ISRC Korea, Park et al.

\* 2006 ESSDERC, LETI, Deleonibus et al.



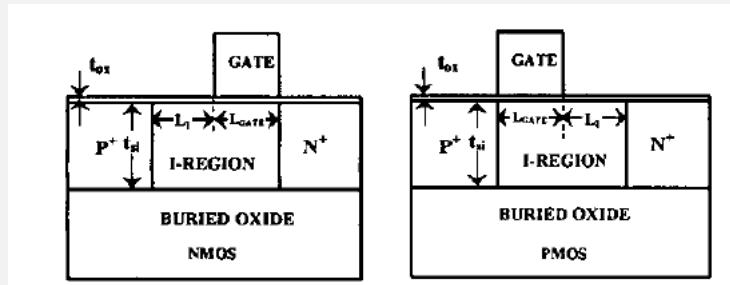
Conventional CMOS-flow with 2 additional masks for separate S/D doping



+ proper device function  
 - many supply voltages -> circuit design ?  
 - reproducibility, reliability, yield ?



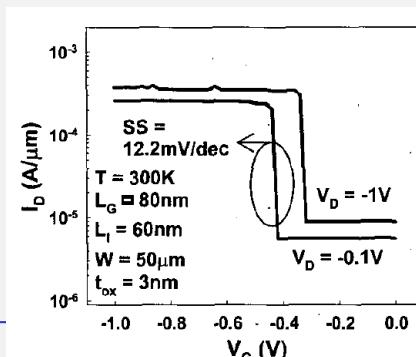
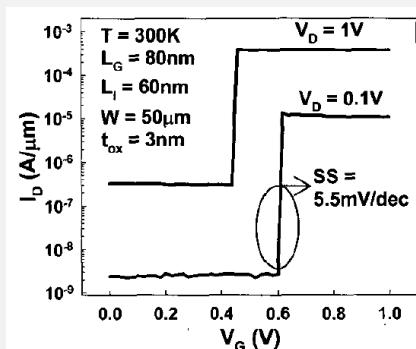
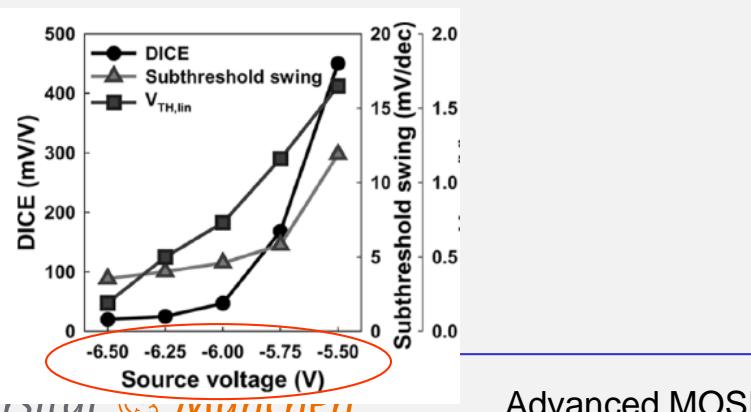
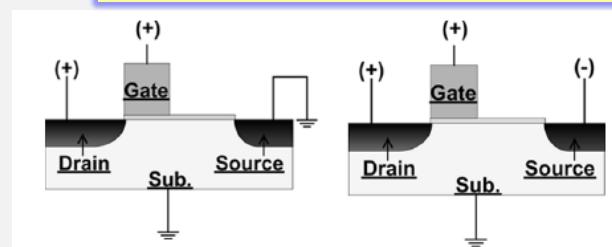
n-IMOS and p-IMOS can be fabricated easily by changing position of Gate



\* IEDM 2004, ISRC Korea, Park et al.  
\* 2006 ESSDERC, LETI, Deleonibus et al.



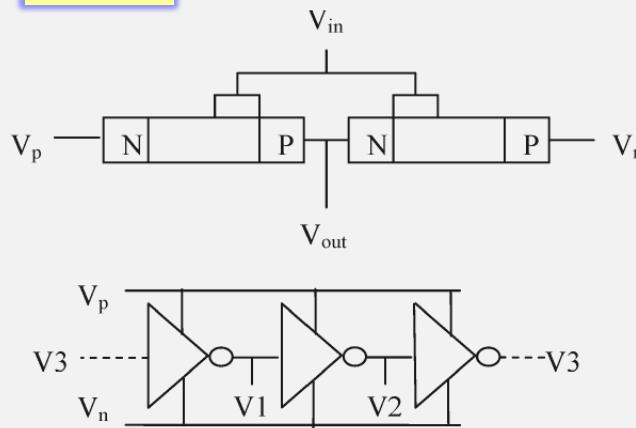
Biassing source separately (around 6V)  
the drain voltage can be kept low and fixed



- \* steep S
- \* high drive current  $I_{on}$
- \* high leakage current
- \*  $I_{on}/I_{off} < 3$  orders of magnitude
- \* different S for p-IMOS and n-IMOS
- \* still high voltages needed

## Inverter

2006 TED, LETI, Deleonibus et al.



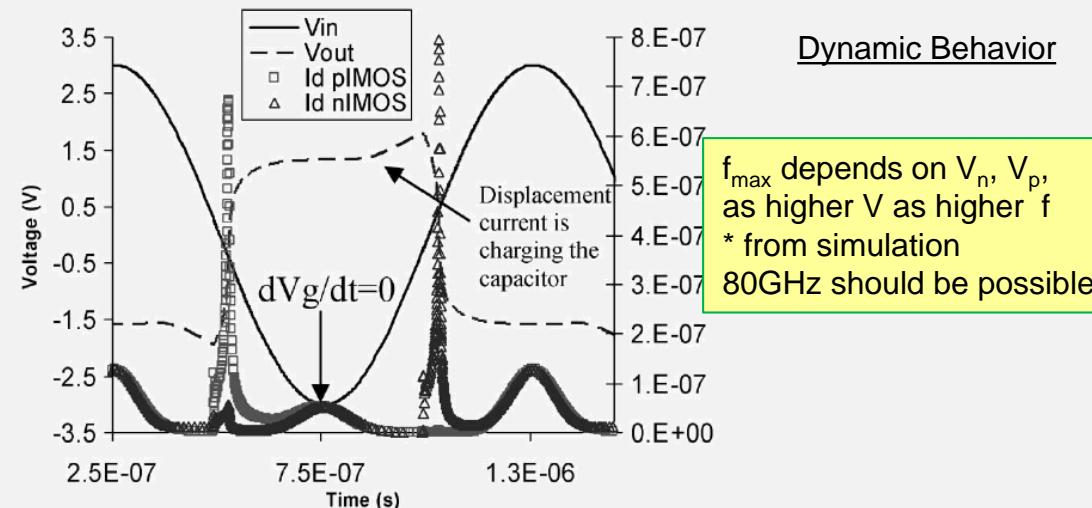
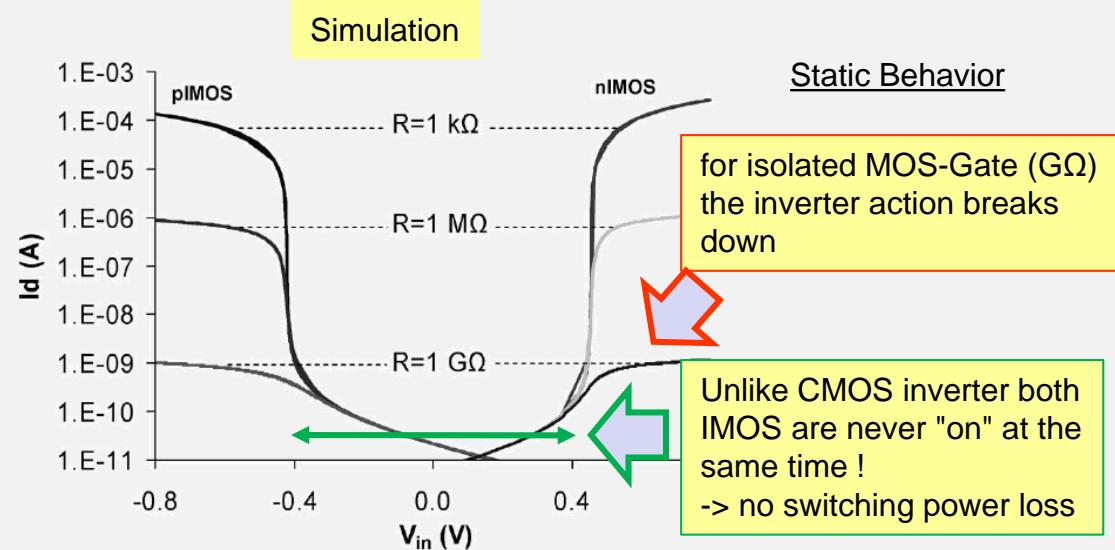
## Problem and Circuit design challenge:

- \* for inverter action one IMOS should be open and one be closed.

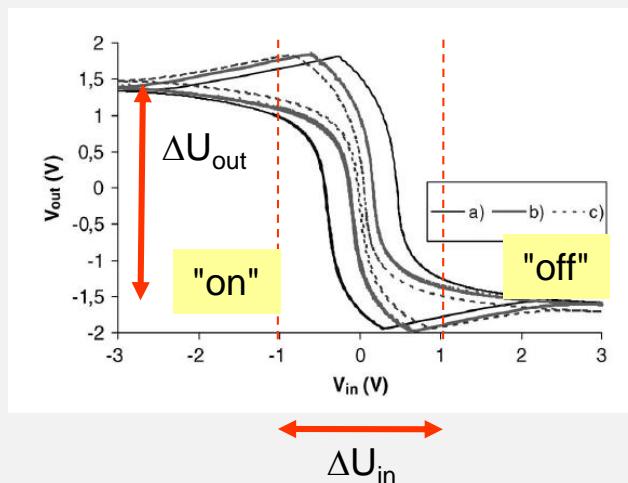
Because the open IMOS must remain with a S/D voltage difference to keep impact running, the output voltage is lower than the  $V_n$  or  $V_p$  supply.

- \* The on-current is generated by breakdown. If the current cannot flow, the IMOS cannot switch on. Using MOS-Gates the current will stop after loading the following Gate, the loading IMOS-inverter will not operate any longer.

To ensure stable action a parasitic resistor is needed.

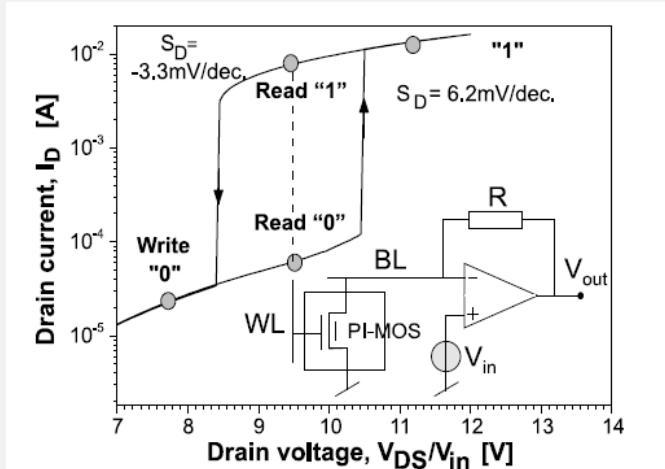


2006 TED, LETI, Deleonibus et al.



Inverter gain is achievable

2008 SSE, EPFL, Ionescu et al.



Using hysteresis memory and inverter are possible

but:

► Logic and memory circuits are in principle possible

► still high operational voltages and high reverse currents consume more power than CMOS

► many voltage levels and positioning devices in isolated wells each make circuit design more complex

Further work:

- still high voltages

(see MOSFET -> ~ 1.0 V)

Operating voltages seem to have an **experimental lower limit around 6 V** for surface channels whereas bulk pin-breakdown is around 3-4 V (Simulation and UniBw) (@~ 50nm pin-length)

- no data yet on reproducibility, yield and reliability

- no experimental data yet on dynamic switching

- noise

$\pm 1$  e/h-pair may generate  $\pm 100$  new impact electrons -> statistics  $\sqrt{n}$

- introducing new materials, new device layout, new effects

- takes time

- makes the devices more complex in:  
- technological realization  
- physical understanding (strain, defects, local effects)



- circuit technology with several voltages need more interconnects, need more chip area as MOSFETs

Don't forget:  
- steep-S devices are focused on lower power consumption for increasing high integration  
-> for industry we need smaller footprints (economics)

## 7.1 Motivation for Hot Carrier Devices

## 7.2 Overview of Hot Carrier Devices

Fabrication Technology: Epitaxy  
Examples of Hot Carrier Devices

## 7.3 The Planar-Doped Barrier FET (PDBFET)

Fabrication  
Electric Field Tailoring  
Modification of Charge Carrier Transport  
Experimental IV-Characteristics  
Low-temperature Physical Transport Effects

## 7.4 The Impact Ionization MOSFET (IMOS)

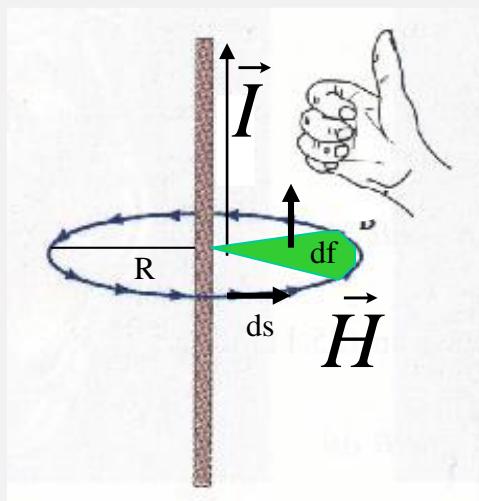
Advantage as Steep-Slope Device  
Working Principle  
Experimental Devices  
Circuit application  
Outlook

## 7.5 Spintronics

Spin Valve Transistor  
Magnetic RAM

Every stationary charge creates an electric field  $\vec{E}$ , every moving charge creates a magnetic field  $\vec{H}$

A current  $I$  moving through a long wire creates a magnetic field  $\vec{H}$ :



$$\text{rot } \vec{H} = \vec{j}$$

$$\text{rot } \vec{H} = \vec{\nabla} \times \vec{H} = \begin{pmatrix} \frac{\partial H_z}{\partial y} - \frac{\partial H_y}{\partial z} \\ \frac{\partial H_x}{\partial z} - \frac{\partial H_z}{\partial x} \\ \frac{\partial H_y}{\partial x} - \frac{\partial H_x}{\partial y} \end{pmatrix}$$

To solve the differential equation both sides are integrated:

$$\int \text{rot } \vec{H} \cdot d\vec{f} = \int \vec{j} \cdot d\vec{f} \xrightarrow{\text{Stokes}} \oint_{\text{circumference}} \vec{H} \cdot d\vec{s} = \int \vec{j} \cdot d\vec{f}$$



Because in the shown easy arrangement the magnetic field  $\vec{H}$  and  $d\vec{s}$  in the scalar product are parallel and  $\vec{j}$  and  $d\vec{f}$  as well, the vectors reduce to a scalar equation:

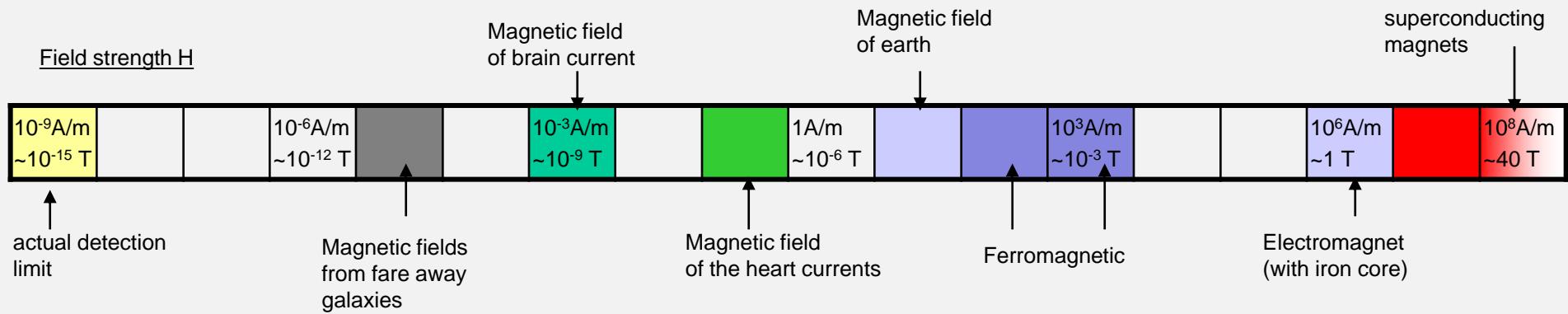
$$2\pi R \cdot H = I$$

or:

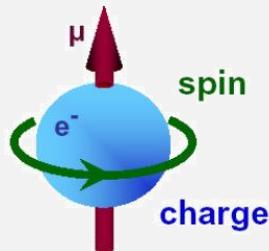
$$H = \frac{I}{2\pi R}$$

with increasing distance  $R$   
the strength of the created field  $H$   
is decreasing

The magnetic field strength belongs to the unit [A/m]



Definition	SI-units	cgs-units		transformation
Magnetic Flux Density B	Tesla $T = Vs/m^2$	Gauss	G	$1 \text{ T} = 10^4 \text{ G}$
Field Strength H	A/m	Oersted	Oe	$1 \text{ A/m} = 0,012566 \text{ Oe}$
Magnetization M	A/m	Oersted	Oe	$1 \text{ A/m} = 0,012566 \text{ Oe}$
Polarisation J	Tesla $T = Vs/m^2$	Gauss	G	$1 \text{ T} = 10^4 \text{ G}$
Magnetic Moment	Vsm	emu	$= G \text{ cm}^3$	$1 \text{ Vsm} = 10^{10} \text{ emu}$
Magnetic Flux $\Phi$	Weber $= Vs$	Maxwell	$= G \text{ cm}^2$	$1 \text{ Weber} = 10^8 \text{ Maxwell}$
Magn. Energy Density (BH)	J/m <sup>3</sup>	GOe		$1 \text{ J/m}^3 = 125,66 \text{ GOe}$ $1 \text{ kJ/m}^3 = 0,12566 \text{ MGOe}$
Permeability m	Vs / Am	G/Oe		$1 \text{ Vs/Am} = 7,958 \cdot 10^5 \text{ G/Oe}$
Magn. Tension Q	A	Gilbert	$= \text{Oe cm}$	$1 \text{ A} = 1,2566 \text{ Oe cm}$



electronics uses the elementary property : **charge e**

But there is another elementary property connected with the electron: **spin s**

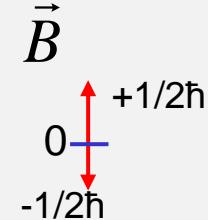
Spin is something like rotation of the electron (but it is only a model).

A moving (= rotating) charge induces a magnetic moment.

The magnetic moment of the electron can be arranged in an external magnetic field parallel or antiparallel to the magnetic field lines:



electron spin orientation in a magnetic field: magnetic quantum number  $m_s = \pm 1/2$



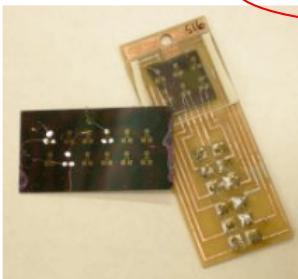
Spintronics is using the magnetic moment of the spin to influence charge transport

First experiments were done around 1980, when some high magnetoresistive effects were discovered

### Researchers aim to room-temperature spintronic computers

Researchers at the University of Utah utilize magnesium oxide to put a new spin on spintronic transistors, using them to align the magnetic spins of electrons for a record period of time in silicon chips at room temperature.

By Suzanne Deffree, Managing Editor, news – EDN, March 15, 2011



Researchers at the University of Utah have built spintronic transistors and used them to align the magnetic spins of electrons for a record period of time in silicon chips at room temperature.

"Electronic devices mostly use the charge of the electrons, a negative charge that is moving," Ashutosh Tiwari, an associate professor of materials science and engineering at the University of Utah, explained in a statement today. "Spintronic devices will use both the charge and the spin of the electrons. With spintronics, we want smaller, faster and more power-efficient computers and other devices."

The National Science Foundation-funded research saw electron spin aligned in a certain way injected into silicon chips and maintained for a record 276 trillionths of a second. In the study, researchers used electricity and magnetic fields to inject spin polarized carriers—namely, electrons with their spins aligned either all up or all down—into silicon at room temperature.

Magnesium oxide was used as a tunnel barrier to get the aligned electron spins to travel from one nickel-iron electrode through the silicon semiconductor to another nickel-iron electrode. Without the magnesium oxide, the spins would get randomized almost immediately, with half up and half down, explained Nathan Gray, a PhD student at the university.

A dozen three-contact nickel-iron transistors sit on a silicon chip coated with an ultra-thin film of magnesium oxide (left). A six-transistor chip attached to electrical contacts for experiments shows that the magnetic "spins" of electrons can be aligned as they travel through silicon at room temperature (right).

"Almost every electronic device has silicon-based transistors in it," Gray said. "The current thrust of industry has been to make those transistors smaller and to add more of them into the same device" to process more data.

"Instead of just making transistors smaller and adding more of them, we make the transistors do more work at the same size because they have two different ways [electron charge and spin] to manipulate and process data," said Gray.

Much of the previous research on spintronic transistors involved using optical radiation in the form of polarized light from lasers to orient the electron spins in non-silicon materials such as gallium arsenide or organic semiconductors at very cold temperatures.

"Optical methods cannot do that with silicon, which is the workhorse of the semiconductor and electronics industry, and the industry doesn't want to retool for another material," Tiwari said. "Spintronics will become useful only if we use silicon."

Tiwari pointed out that most of the devices in earlier studies have had to be cooled to very low temperatures. Indeed, previous experiments have focused on temperatures colder than 200 below zero Fahrenheit to align the electrons' spins either all up or all down. "Our new way of putting spin inside the silicon does not require any cooling," Tiwari said.

The experiment used a flat piece of silicon about 1-inch long, about 0.3-inches wide, and one-fiftieth of an inch thick. An ultra-thin layer of magnesium oxide was deposited on the silicon wafer. A dozen transistors were deposited on the silicon wafer so they could be used to inject electrons with aligned spins into the silicon and later detect them.

The researchers explained that each nickel-iron transistor had three contacts or electrodes: one through which electrons with aligned spins were injected into the silicon and detected, a negative electrode, and a positive electrode used to measure voltage.

During the experiment, the researchers sent direct current through the spin-injector electrode and negative electrode of each transistor. The current was kept steady, and the researchers measured variations in voltage while applying a magnetic field to the apparatus.

"By looking at the change in the voltage when we apply a magnetic field, we can find how much spin has been injected and the spin lifetime," Tiwari said.

During the new study, the electrons retained their spins for 276 picoseconds, or 276 trillionths of a second. Based on that lifetime, the researchers calculate the spin-aligned electrons moved through the silicon 328 nanometers.

"It's a tiny distance for us, but in transistor technology, it is huge," Gray said. "Transistors are so small today that that's more than enough to get the electron where we need it to go."

Tiwari added that the new study's use of electronic spin injection is much more practical than using optical methods such as lasers, as lasers are too big for chips in consumer electronic devices.

He added that spintronic computer processors require little power compared with electronic devices, so a battery that may power an electronic computer for eight hours might last more than 24 hours on a spintronic computer.

Tiwari and Gray report their creation of room-temperature, spintronic transistors on a silicon semiconductor this month in the journal *Applied Physics Letters*.

## Overview of magnetoresistive Effects

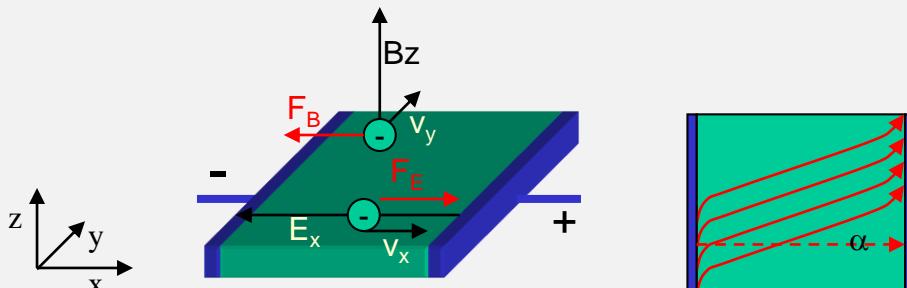
External magnetic field

Material does not change its internal magnetism

due to the Lorentz force the external magnetic field creates longer internal current paths  
-> measurable increase in resistance

- > the material must be conducting
- > all metals and semiconductors

Normal magnetoresistive effect



Material changes its internal magnetism

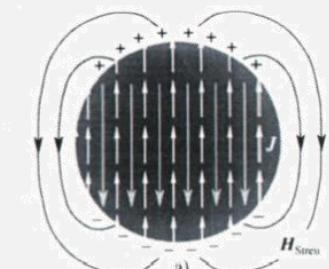
an internal magnetism can only exist in so-called Ferroelectrics (transition metals Fe, Ni, Co)

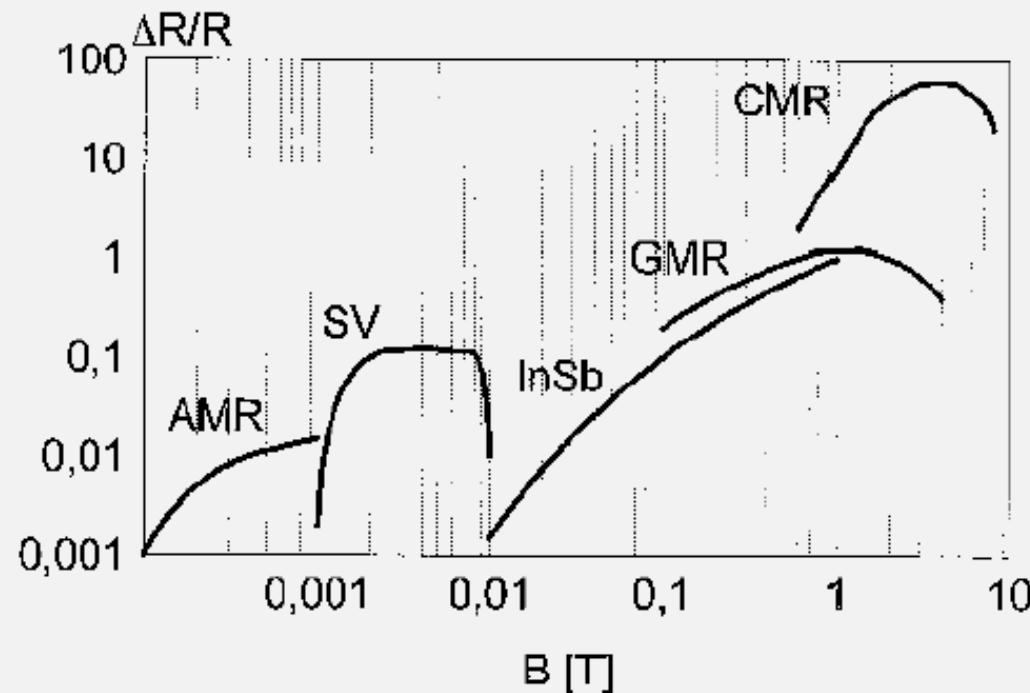
- Due to an external magnetic field the internal magnetic orientation will be changed
- > electrons with spin parallel or antiparallel to the internal magnetic orientation will be more or less scattered
- > the resistance changes in an external magnetic field

Abnormal (anisotropic) magnetoresistive effect  
AMR

Giant magnetoresistive effect  
GMR

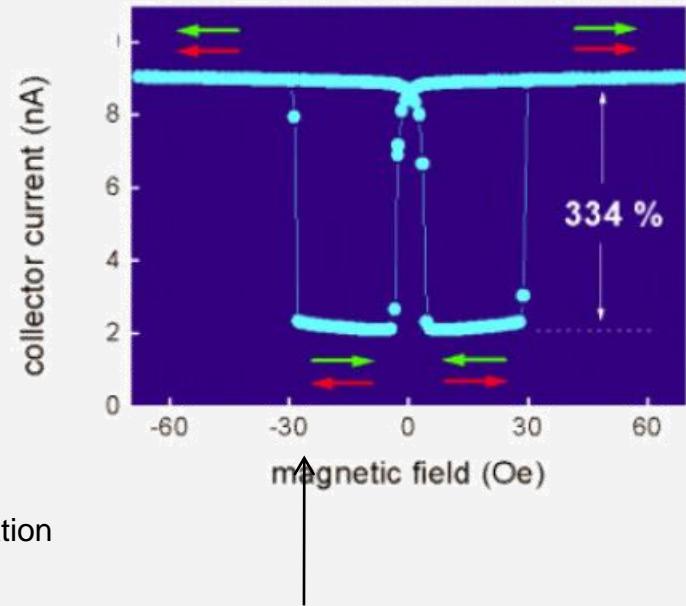
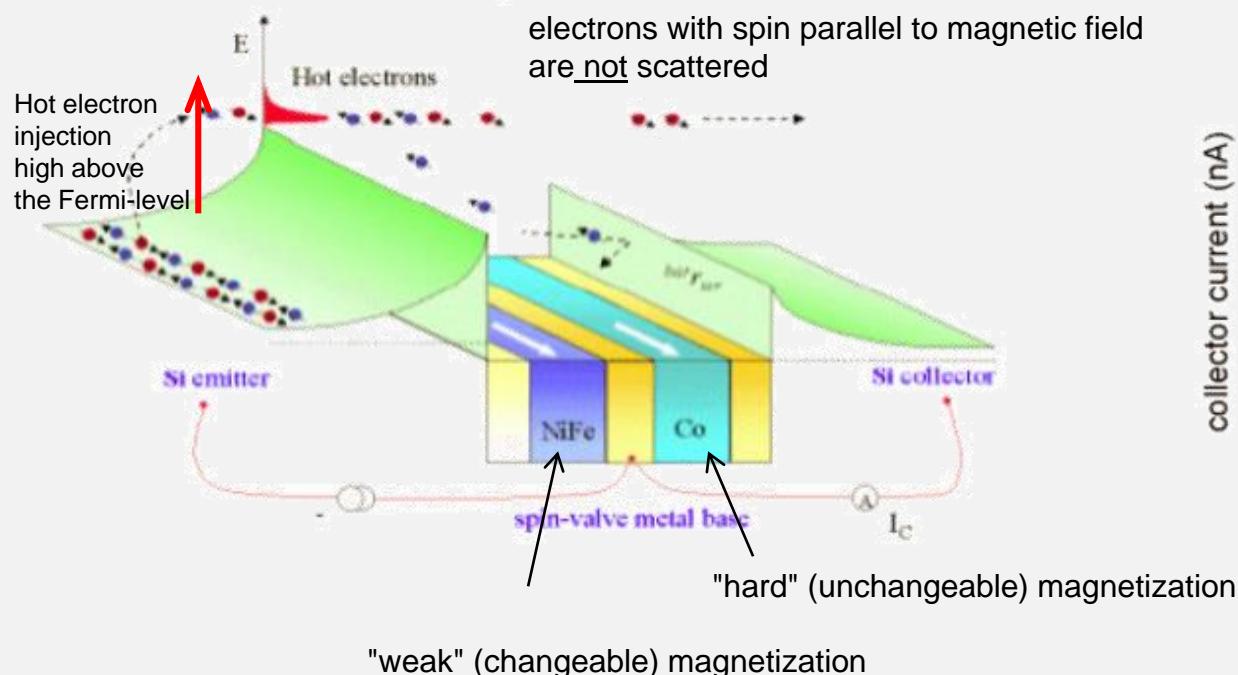
Colossal magnetoresistive effect  
CMR





**Figure 1.9** The typical field range of various magnetoresistive sensors – AMR: anisotropic magnetoresistance; SV: spin valve sensors; InSb: semiconductor magnetoresistors; GMR: multilayer GMR sensors; CMR: colossal magnetoresistance (Heremans 1993).

with Schottky-emitter:

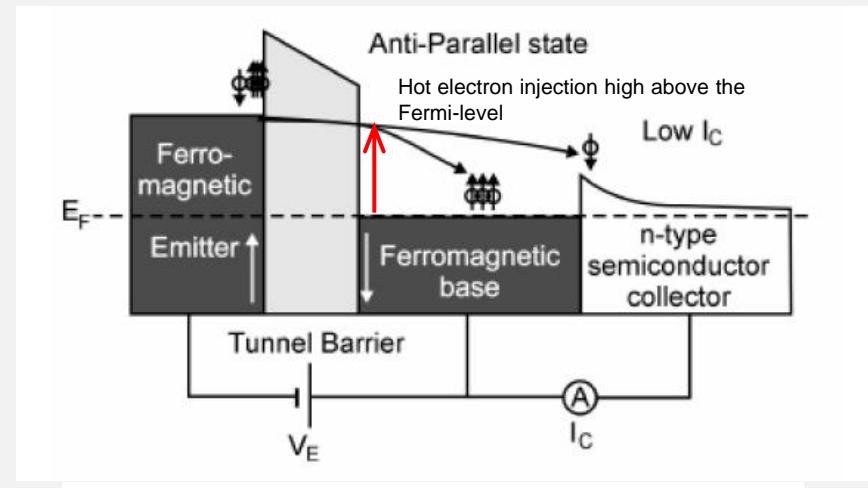
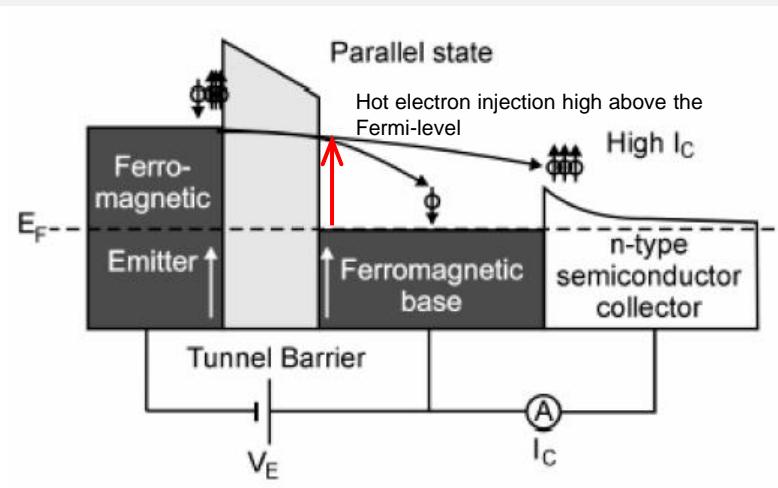


Magnetic field:  $30 \text{ Oe} = 3000 \text{ A/m}$   
 ~ magnetic strength of a magnet used at the front door of a refrigerator

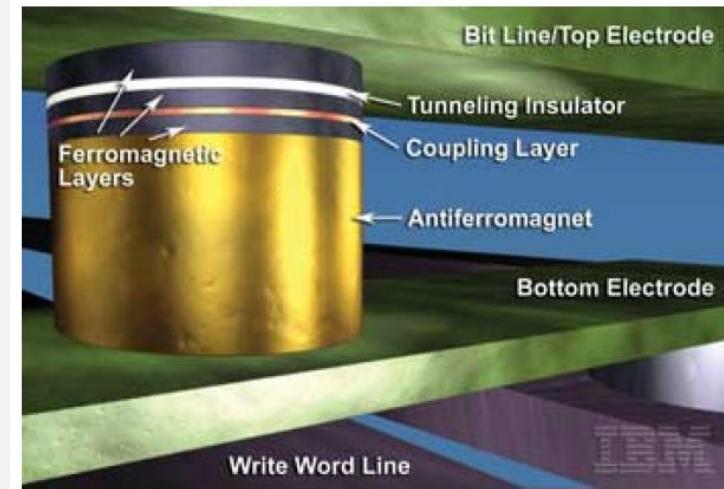
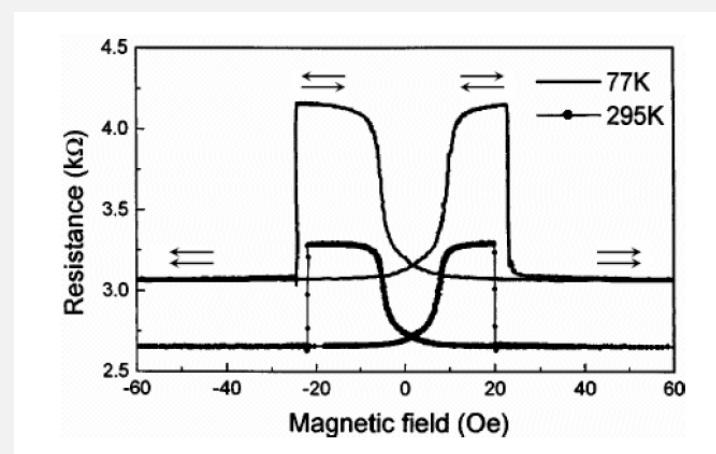
But: remember quantum-mechanical reflection on deep metal conduction band (like metal base transistor)

Introducing tunneling barriers in the working principle of hot electron transistors.  
Remember: Hot electrons mean energy above the Fermi-level.

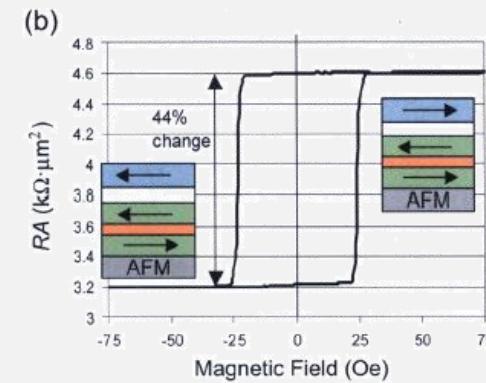
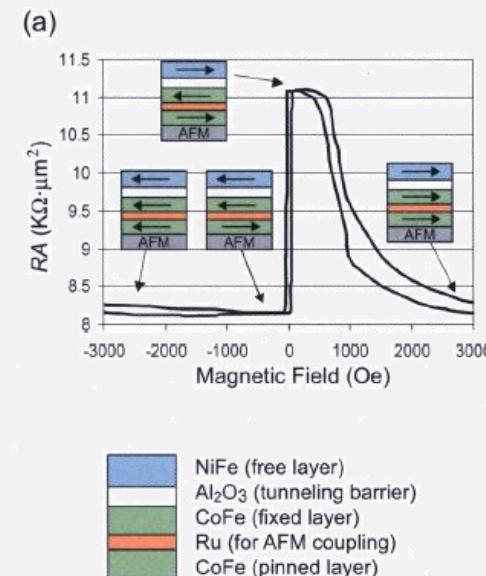
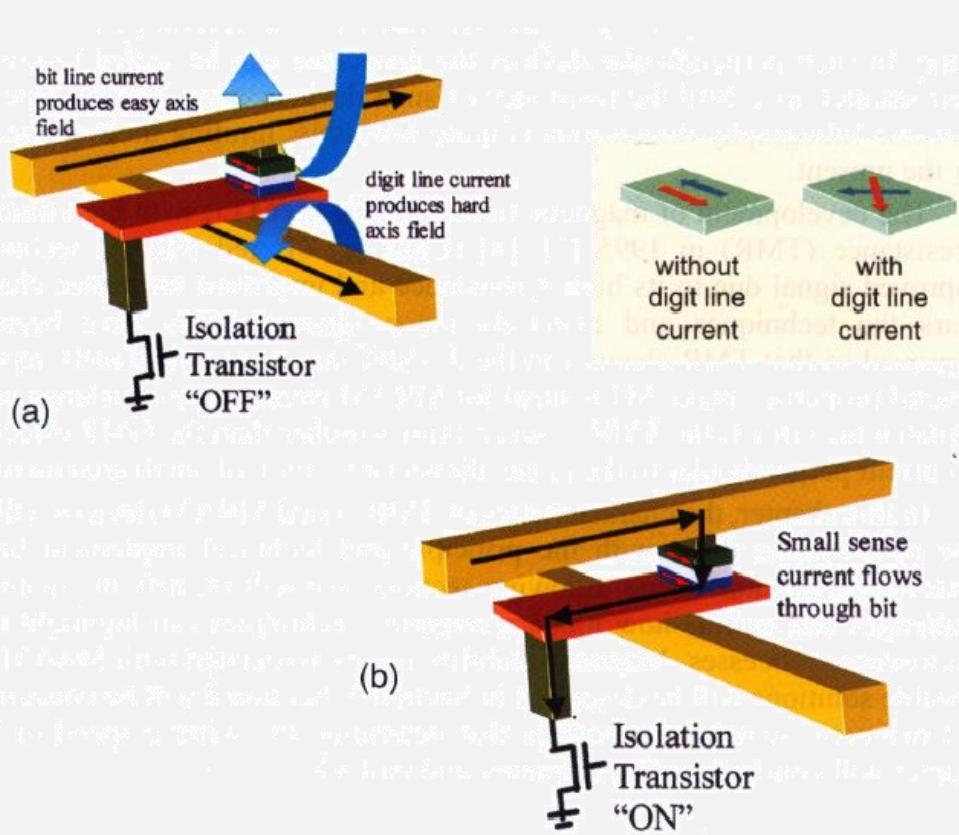
tunnel emitter with already polarized injection:



Magnetic Tunneling Junction



# MRAM



## MRAM

- \* non volatile
- \* fast access ~10nsec
- \* no boot time

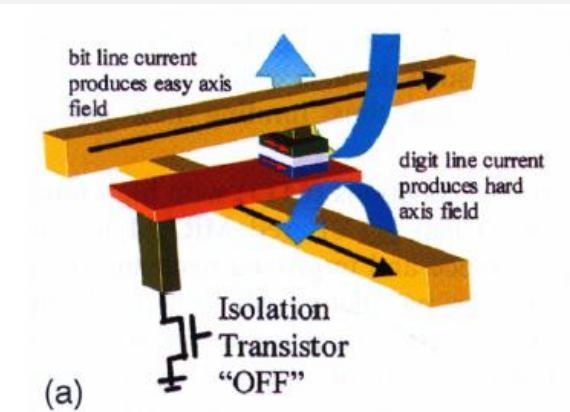
Writing:

With two currents the magnetic direction in the memory layers (base) are oriented  
 -> it can polarize or not through going electrons

currents are needed:

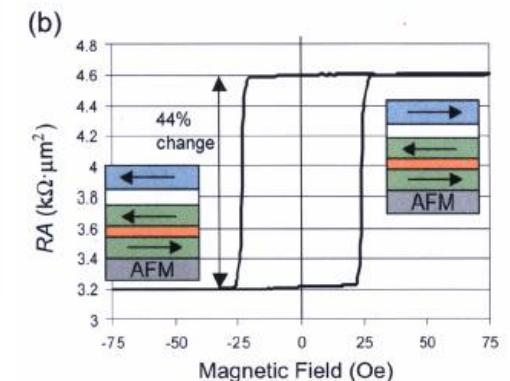
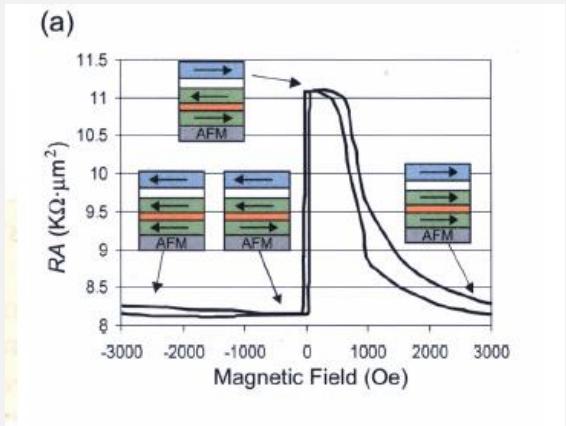
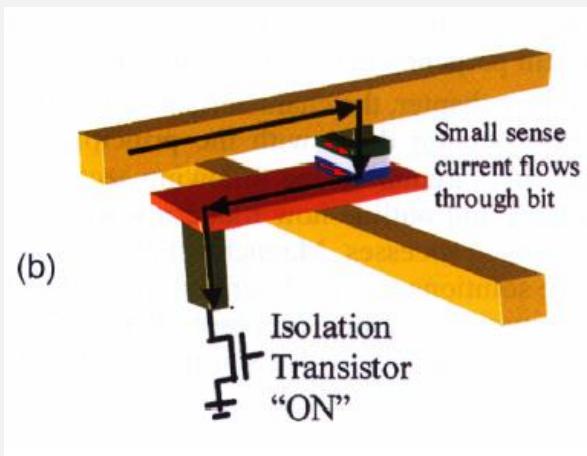
100nm distance:  $2\pi RH = I \rightarrow I = 0.1A$   
 (MOSFET: on-current:  $0.001A/\mu m$ )

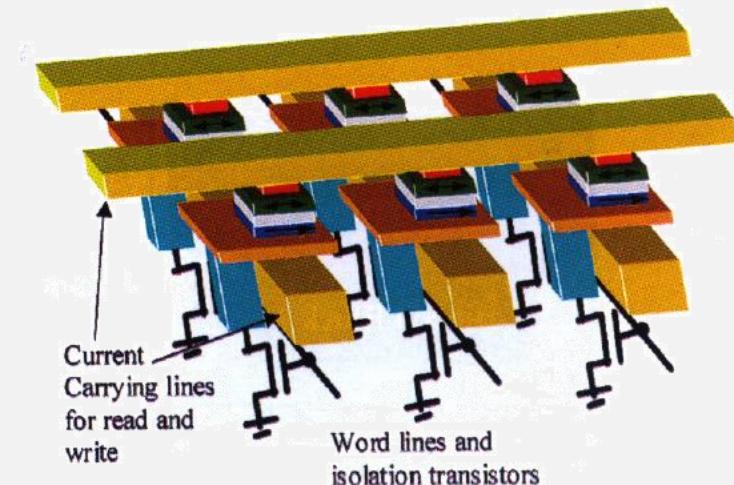
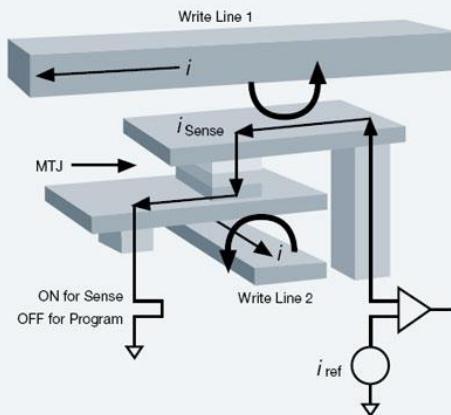
The sense transistor is off



Reading:

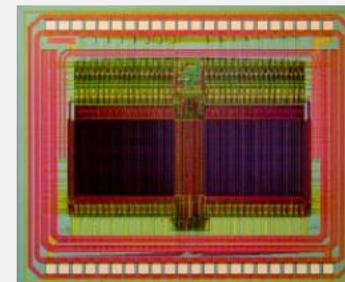
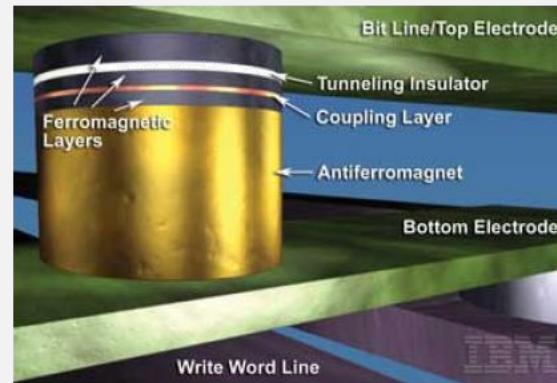
Small current runs through the base, the selection transistor is on and detects the level of current





## MRAM

Realization by IBM (2005) and Motorola (2004)



Advantages:

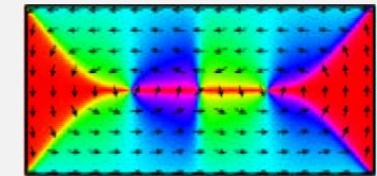
- \* non volatile
- \* fast access: ~10nsec
- \* lower soft error rates
- \* temperature stable (-40 - +150°C)
- \* integration in CMOS

Disadvantages:

- \* high writing currents needed (~0.1A)
- \* not scalable



as smaller the dimensions are shrunked,  
as more difficult -> higher currents  
are needed for writing



25nm

### Everspin Expands Toggle MRAM Product Portfolio

Adds 2Mb, 8Mb and 32Mb capacities to its industry-leading Toggle MRAM product family, offering replacements for legacy SRAM sockets

**Chandler, AZ – October 29, 2019** — [Everspin Technologies, Inc.](#), (NASDAQ: MRAM), the world's leading developer and manufacturer of Magnetoresistive RAM (MRAM) persistent memory solutions, announced the world's first 32Mb Toggle MRAM product. Everspin's new 32Mb Toggle MRAM (MR5A16A) provides twice the capacity of its current 16Mb solution and enables critical applications, such as storing configurations and setup and data logging in embedded systems that need a higher density option, while also providing the proven benefits of Everspin's Toggle MRAM.



[https://www.everspin.com/sites/default/files/pressdocs/MRAM-Toggle\\_Family\\_Release.pdf](https://www.everspin.com/sites/default/files/pressdocs/MRAM-Toggle_Family_Release.pdf)



### Freescale Pushing MRAM Technology Toward Automotive Goal

**David Lammers, News Editor -- Semiconductor International,**  
**2/28/2008 7:41:00 AM**

<http://www.semiconductor.net/article/CA6536292.html?nid=3572>



Freescale Semiconductor Inc.(Austin, Texas) is continuing its push to bring magneto-resistive random access memory (MRAM) technology to the marketplace, emphasizing the reliability of the new memory technology.

Freescale's 4 Mb MRAM has much **higher soft error rate (SER) immunity** than conventional SRAMs, with a failure in time (FIT) rate of one soft error in  $10^7$  device hours, said MRAM marketing manager David Bondurant.

Freescale's goal is to introduce MRAM to its lineup of automotive controllers. To that end, the company is developing a **16 Mb MRAM** based on **130 nm design rules**, and will port its MRAM technology to the company's automotive-grade 130 nm process, SMOS 10.

The 4 Mb device, with a **35 nsec read and write time**, was priced at \$25 in 2006 when it first went on sale. Bondurant said Freescale has recently reduced the **price to \$15**, adding that "we do plan to keep bringing the price down to make MRAM more competitive with SRAM prices."



2008 EverSpin was founded by Freescale and is doing now the MRAM technology

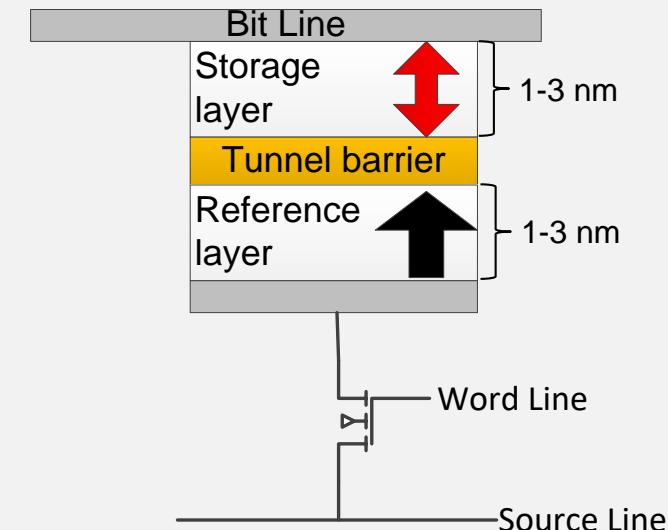
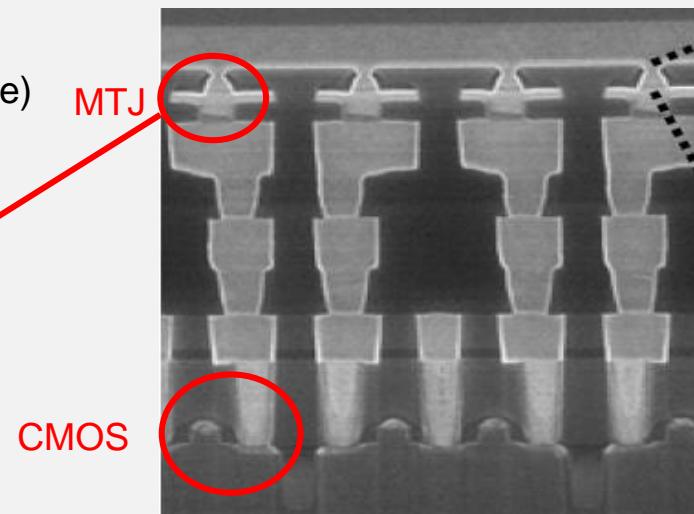
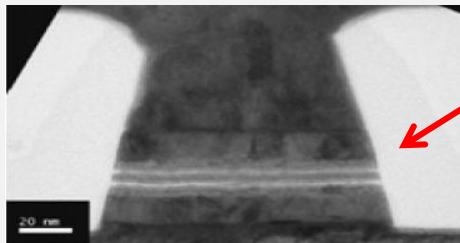


2019 EverSpin announced to produce a 32Mb Toggle MRAM



Difficulties in scaling and the high writing current in Toggle MRAMs lead to the development of Spin-Torque MRAMs (ST-MRAM)

- Device structure consists of a Transistor and a Magnetic Tunnel Junction (MTJ)
- Magnetic Tunnel Junction (MTJ):
  - Reference layer with fixed magnetic polarization
  - Tunnel barrier
  - Storage layer which switches between two stable magnetic polarization states (free layer)
- Two states:
  - High resistance
    - Magnetic polarization of storage layer is opposite to reference layer
  - Low resistance
    - Magnetic polarization of storage layer is aligned to reference layer
- Switching
  - Current flows directly through MTJ
  - Writing current  $I \sim 80\mu A$  (40nm node)

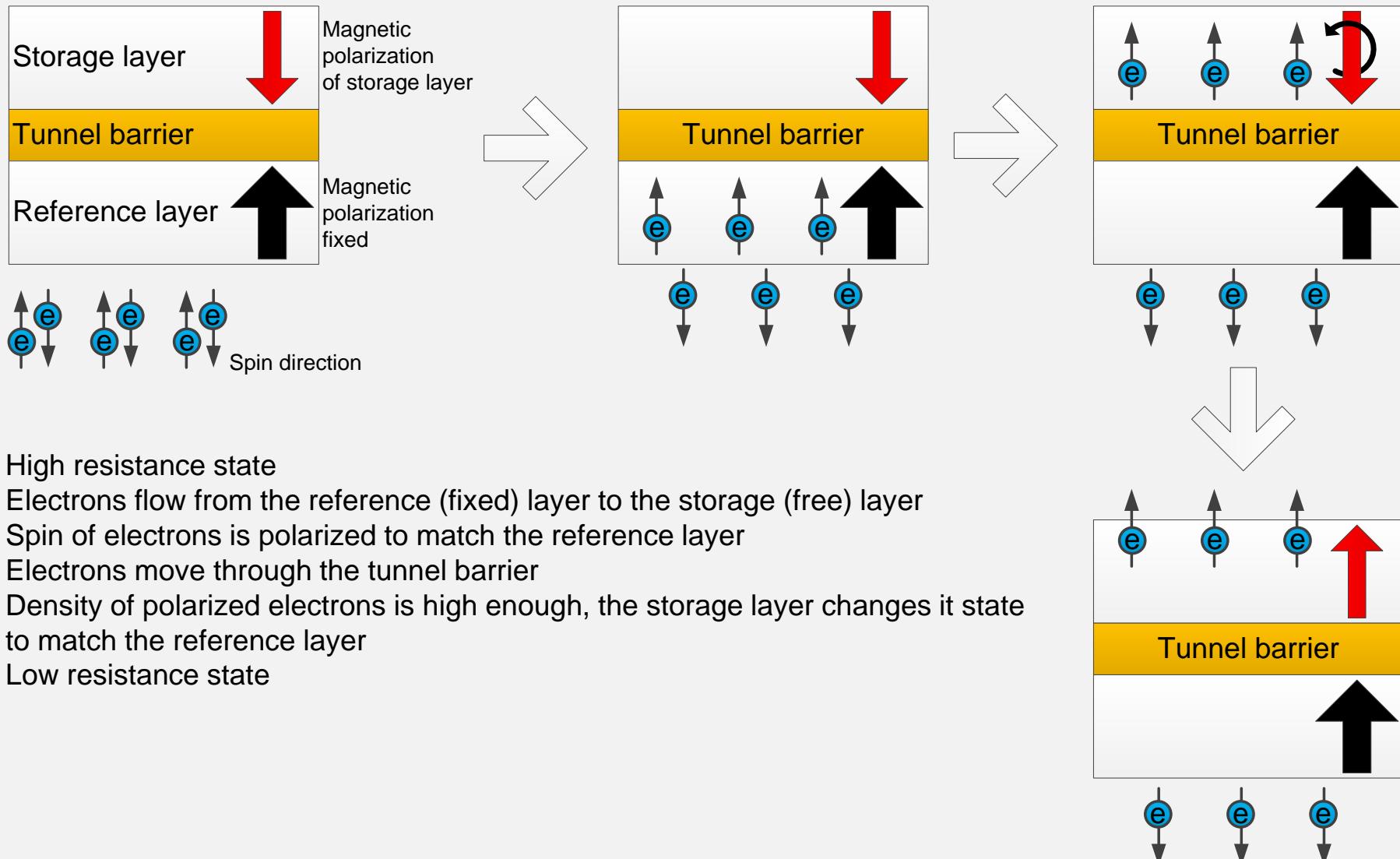


Source: T. Andre, ST-MRAM Fundamentals, Challenges, and Outlook  
IEEE 2017

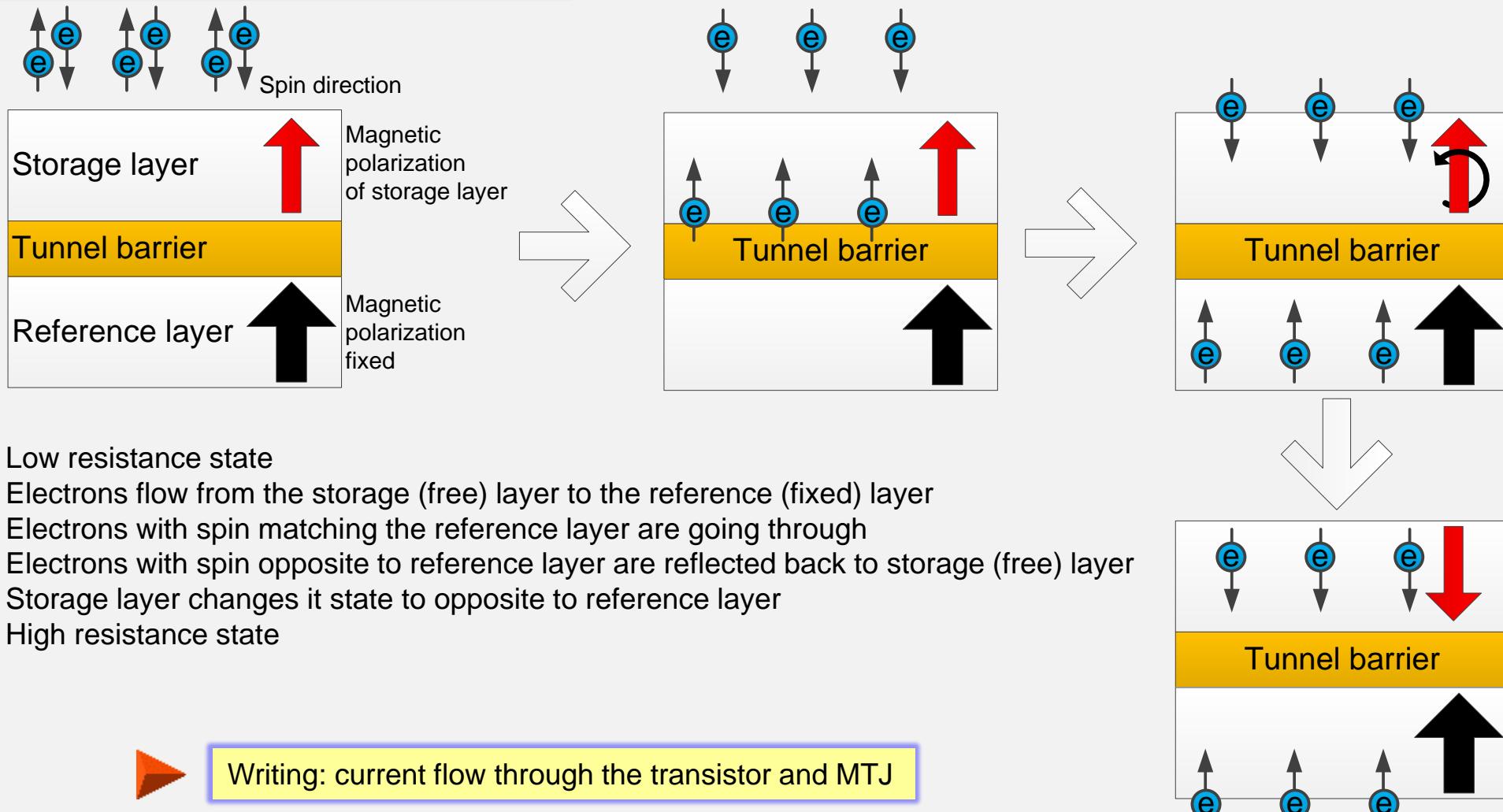
Source: T. Andre, ST-MRAM Fundamentals, Challenges, and Applications  
IEEE 2013

Source: Driskill-Smith, Latest Advances and Future Prospects of STT-RAM, Non-Volatile Memories Workshop 2010

Switching from high resistance to low resistance

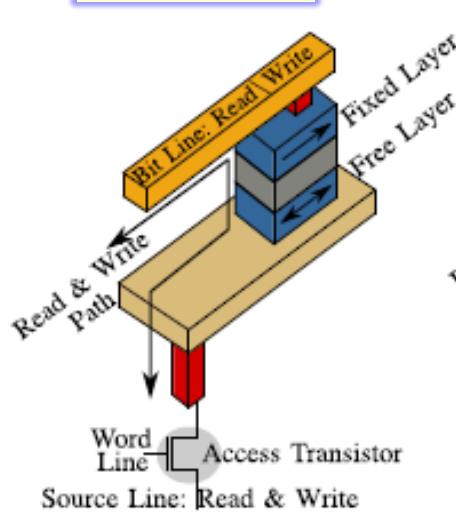


Switching from low resistance to high resistance



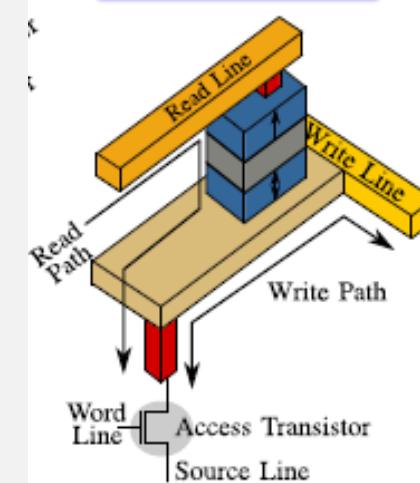
The writing current through a MTJ-cell in a ST-MRAM reduces the lifetime of the cell

ST-MRAM



- One path for reading and writing the cell
- Higher stress for the cell
- Higher degradation

SOT-MRAM



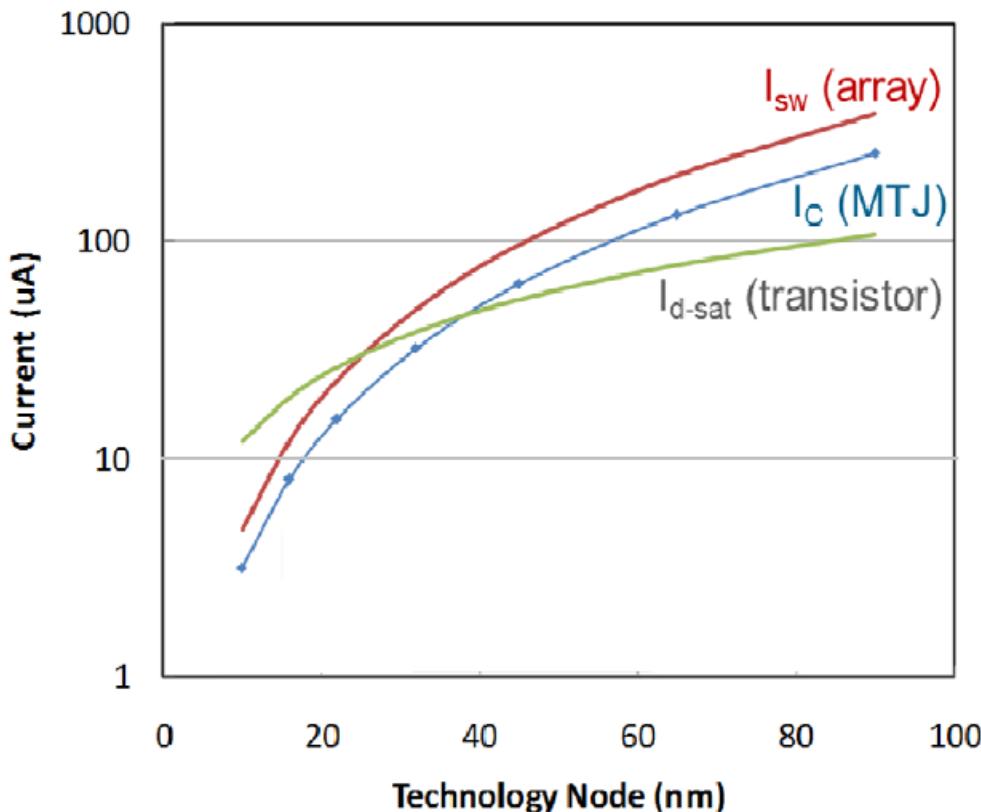
- Separate read and write line
- Faster access time
- Lower energy consumption

Source: F. Oboril et al., Evaluation of Hybrid Memory Technologies Using SOT-MRAM for On-Chip Cache Hierarchy, IEEE TRANSACTIONS ON COMPUTER-AIDED DESIGN OF INTEGRATED CIRCUITS AND SYSTEMS, VOL. 34, NO. 3, MARCH 2015

Writing: current flow does not go through MTJ

Reading: low voltage to avoid disturbing the state of the MTJ

Calculated



$I_c$ (MTJ): average current required to switch an MTJ  
 $I_{sw}$ (array): current to switch the distribution of MTJ in an array  
 $I_{d\text{-sat}}$ (transistor): saturation current of the CMOS-transistor

Main challenges are:

- Reduce  $I_{sw}$
- Data Retention

Source: T. Andre, ST-MRAM Fundamentals,  
Challenges, and Applications  
IEEE 2013



To achieve this the critical current density for ST-switching must be held constant

## FEATURES

- Non-volatile 256Mb (32Mb x 8, 16Mb x 16) DDR3
- Supports standard DDR3 SDRAM features
- $V_{DD} = 1.5v \pm 0.075v$
- Up to 667MHz fCK (1333MT/sec/pin)
- Page size of 512 bits (x8) or 1024 bits (x16)

256Mb ST-DDR3 Spin-transfer Torque  
MRAM



Source: <https://www.everspin.com>

Everspin Ships the World's First Pre-Production 28 nm 1 Gb STT-MRAM Customer Samples

*Next generation product family expands portfolio of non-volatile persistent memory solutions.*

**Chandler, AZ, January 8, 2019** — Everspin Technologies, Inc. (NASDAQ: MRAM), the world's leading developer and manufacturer of Magnetoresistive RAM (MRAM), today announces that it commenced shipment of pre-production customer samples of its 28 nm 1-Gigabit (Gb) Spin Torque Transfer Magnetoresistive Random Access Memory (STT-MRAM) product in December 2018. This achievement follows Everspin's successful commercialization of its 40 nm 256 Mb STT-MRAM and builds upon months of close work with customers and manufacturing partners to mature this product technology. These are the world's first 1 Gb STT-MRAM parts that meet customer specifications for endurance, performance and reliability in persistent write buffer applications.

**Everspin Begins 40nm STT-MRAM Volume Production**

**Chandler, AZ, January 17, 2018** — Everspin Technologies, Inc., the world's leading developer and manufacturer of discrete and embedded MRAM, today announced the Company recorded revenue for its first 40nm 256Mb STT-MRAM products in the fourth quarter of 2017 and is in the process of ramping its volume production in 2018. This achievement represents an important milestone for STT-MRAM as it is the enabling step for bringing the persistent memory to market.



1Gb ST-MRAM (28nm node) risk production started in 2019



256 Mb ST-MRAM (40nm node) volume production started in 2018

IEDM 2018: Three companies present embedded MRAM

## Demonstration of Highly Manufacturable STT-MRAM Embedded in 28nm Logic



Y. J. Song<sup>1,a</sup>, J. H. Lee<sup>1</sup>, S. H. Han<sup>1</sup>, H. C. Shin<sup>1</sup>, K. H. Lee<sup>1</sup>, K. Suh<sup>1</sup>, D. E. Jeong<sup>1</sup>, G. H. Koh<sup>1</sup>, S. C. Oh<sup>1</sup>, J. H. Park<sup>1</sup>, S. O. Park<sup>1</sup>, B. J. Bae<sup>1</sup>, O. I. Kwon<sup>1</sup>, K. H. Hwang<sup>1</sup>, B.Y. Seo<sup>2</sup>, Y.K. Lee<sup>2</sup>, S. H. Hwang<sup>2</sup>, D. S. Lee<sup>2</sup>, Y. Ji<sup>2</sup>, K.C. Park<sup>2</sup>, G. T. Jeong<sup>2</sup>, H. S. Hong<sup>1</sup>, K. P. Lee<sup>1</sup>, H. K. Kang<sup>1</sup>, and E. S. Jung<sup>2</sup>

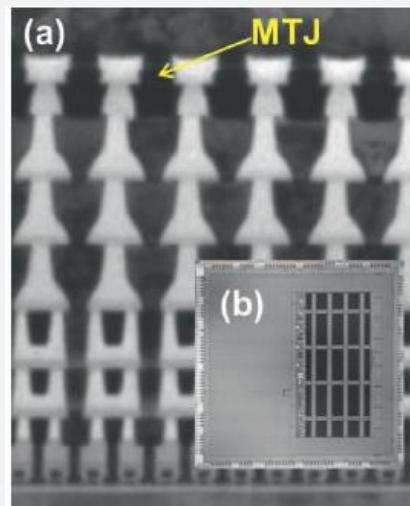
<sup>1</sup>R&D Center, Samsung Electronics Co., Hwasung, Korea, <sup>a</sup>email: [yoonjiong.song@samsung.com](mailto:yoonjiong.song@samsung.com), Tel.: (82)31-325-9319

<sup>2</sup>Foundry Business, Samsung Electronics Co., Kihueung, Korea

## 22-nm FD-SOI Embedded MRAM Technology for Low-Power Automotive-Grade-1 MCU Applications



K. Lee, Senior Member, R. Chao, K. Yamane, V. B. Naik, H. Yang, J. Kwon, N. L. Chung, S. H. Jang, B. Behin-Aein, J. H. Lim, S. K. B. Liu, E. H. Toh, K. W. Gan, D. Zeng, N. Thiagarajah, L. C. Goh, T. Ling, J. W. Ting, J. Hwang, L. Zhang, R. Low, R. Krishnan, L. Zhang, S. L Tan, Y. S. You, C. S. Seet, H. Cong, J. Wong, S. T. Woo, E. Quek, S. Y. Siah  
GLOBALFOUNDRIES, Singapore, email: [kangho.lee@globalfoundries.com](mailto:kangho.lee@globalfoundries.com)



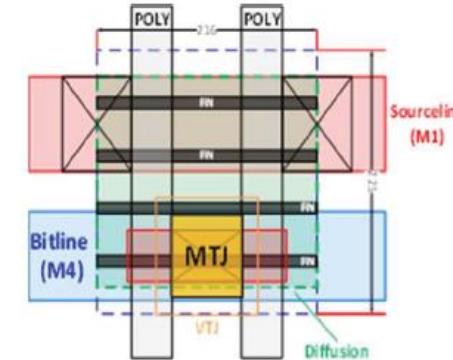
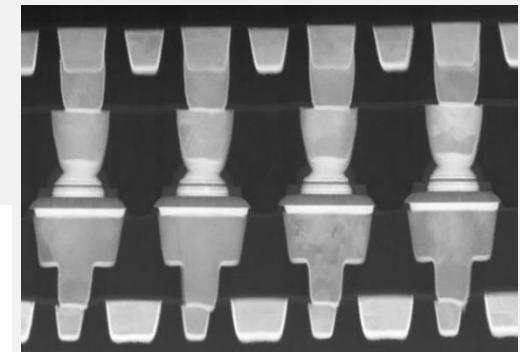
All four show working MRAM cells

No proof that the transistors are working

## MRAM as Embedded Non-Volatile Memory Solution for 22FFL FinFET Technology

O. Golonzka, J. -G. Alzate, U. Arslan, M. Bohr, P. Bai, J. Brockman, B. Buford, C. Connor, N. Das, B. Doyle, T. Ghani, F. Hamzaoglu, P. Heil, P. Hentges, R. Jahan, D. Kencke, B. Lin, M. Lu, M. Mainuddin, M. Meterelliyoz, P. Nguyen, D. Nikonorov, K. O'brien, J. O'Donnell, K. Oguz, D. Ouellette, J. Park, J. Pellegren, C. Puls, P. Quintero, T. Rahman, A. Romang, M. Sekhar, A. Selarka, M. Seth, A. J. Smith, A. K. Smith, L. Wei, C. Wiegand, Z. Zhang and K. Fischer

Intel Corporation, Santa Clara, CA, USA, email: [oleg.golonzka@intel.com](mailto:oleg.golonzka@intel.com)



## IEDM 2019: TSMC embedded MRAM

22nm STT-MRAM for Reflow and Automotive Uses  
with High Yield, Reliability, and Magnetic Immunity  
and with Performance and Shielding Options

W.J. Gallagher\*, Eric Chien, Tien-Wei Chiang, Jian-Cheng Huang, Meng-Chun Shih, C.Y. Wang, Chih-Hui Weng, Sean Chen, Christine Bair, George Lee, Yi-Chun Shih, Chia-Fu Lee, Po-Hao Lee, Roger Wang, Kuei-Hung Shen, J.J. Wu, Wayne Wang, and Harry Chuang  
Taiwan Semiconductor Manufacturing Company, Hsinchu, Taiwan, \*gallagh@tsmc.com



### RAID-on-Chip Journal Memory



Dell Computer selected Everspin MRAM because MRAM fast Write and non-volatility supports enhanced data center fault recovery without requiring wear leveling or ECC overhead. This reduced system downtime and lowered their total cost of ownership.



See a full Case Study under Applications/ RAID on our web site.

### Industrial Grade Memory Module

The Advantech PCM-23 memory module is an optional extended



memory used to store critical data in an event log. For their non-volatile memory requirement, Advantech chose an Everspin 16Mb MRAM because it provides two megabytes of non-volatile, reliable data storage, with 20 years of data retention.



Source: <https://www.everspin.com>

### Direct Logic 205 PLC



Koyo Electronics Industries' new Direct Logic 205 PLC utilizes a 1Mb Everspin MRAM, which enables data integrity and reliability in harsh environments, and instant event save in the event of a power loss - without the need for a battery.



See a full Case Study under Applications/ Factory Automation on our web site.

### Engine Control Module



BMW Motorsport selected Everspin's 4Mb MRAM in the AEC-Q100 Grade 1 qualified option for their 1000RR Superbike because it was rugged enough to operate within the very high temperature environments encountered in a motorcycle race, fast enough to read or write data in real time during a race, yet always be non-volatile.



- Aerospace
- Automotive
- Data Storage
- Factory Automation
- Industrial Computing
- Medical



Used when high robustness, speed and non-volatility is needed

### Prices DRAM vs MRAM (12.02.2020)



#### DRAM 16Mb



AS4C4M16S Series 16 Mb (1 M x 16)  
143 MHz CMOS Synchronous DRAM  
TSOP II-50

Quantity

Total: \$1.37



List

Add to Cart

<http://www.futureelectronics.com/en/technologies/semiconductors/memory/dram/component-dram/Pages/3026786-AS4C1M16S-7TCN.aspx?IM=0>

#### Toggle MRAM 16Mb



MR4A16B Series 16 Mb (1 M x 16) 3.6 V 35 ns Asynchronous MRAM Memory - TSOP2-54

Quantity

Total \$32.18 USD

ADD TO CART

≡

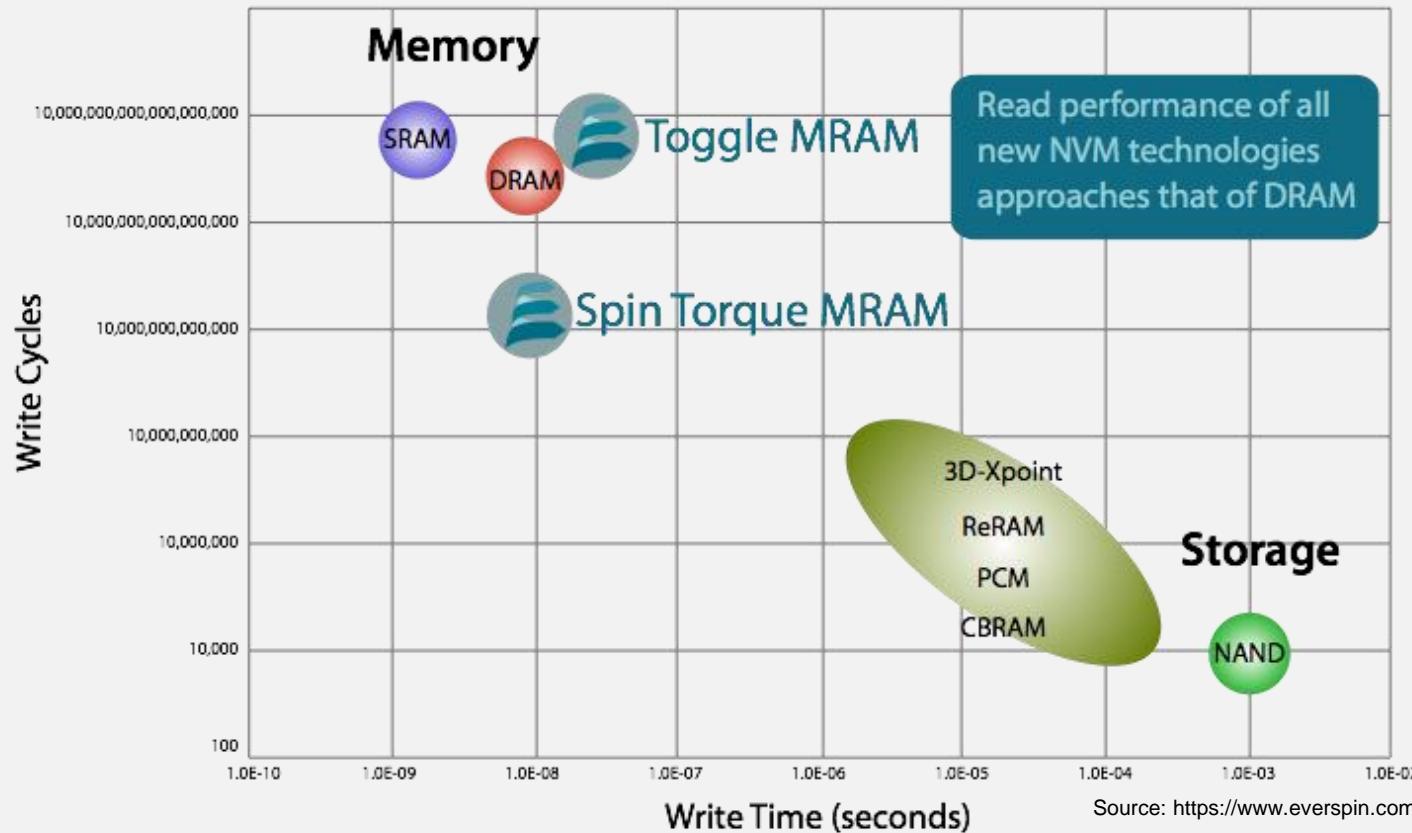
<http://www.futureelectronics.com/en/technologies/semiconductors/memory/mram/Pages/1002867-MR4A16BCYS35.aspx?IM=0>

► ST-MRAM coming to the market

► Today (2020) there seems no chips on the high volume market.

► Toggle MRAM is about 30 times more expensive than DRAM

► In 2017 the MRAM market was \$36 million, in 2020 should reach \$325 million



- ▶ ST-MRAM seems to be a good candidate to replace DRAM/SRAM, because it is non-volatile and scalable
- ▶ RRAM/PCM seems a good candidate for Storage

## 7.1 Motivation for Hot Carrier Devices

## 7.2 Overview of Hot Carrier Devices

Fabrication Technology: Epitaxy and ALD

Examples of Hot Carrier Devices

## 7.3 The Planar-Doped Barrier FET (PDBFET)

Fabrication

Electric Field Tailoring

Modification of Charge Carrier Transport

Experimental IV-Characteristics

Low-temperature Physical Transport Effects

## 7.4 The Impact Ionization MOSFET (IMOS)

Advantage as Steep-Slope Device

Working Principle

Experimental Devices

Circuit application

Outlook

## 7.5 Spintronics

Spin Valve Transistor

Magnetic RAM

End  
of  
Chapter 7