

## 8.1 Introduction

Overview of Tunneling Transistors  
Tunneling in MOSFETs

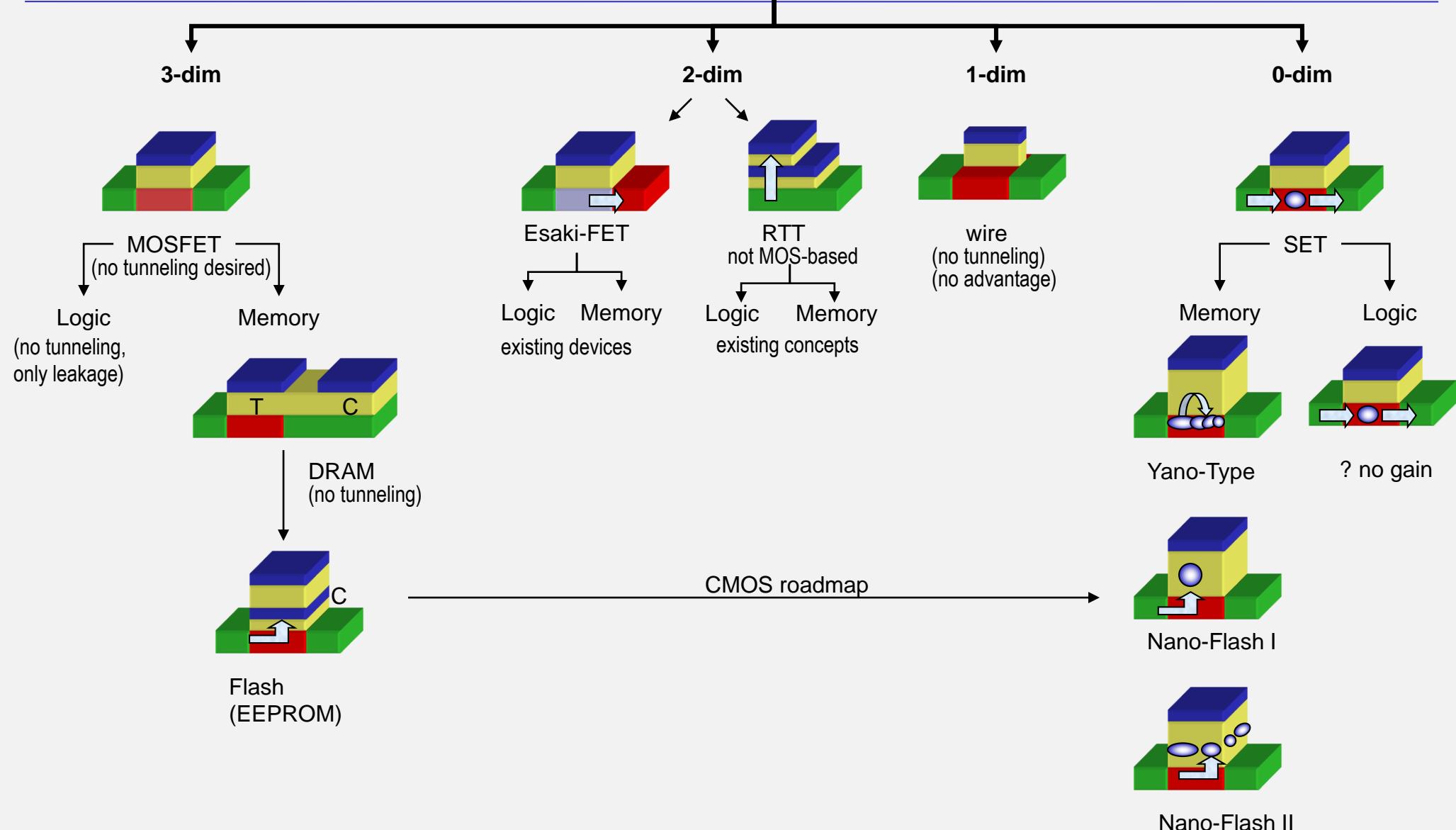
## 8.2 The Esaki-Tunneling MOSFET

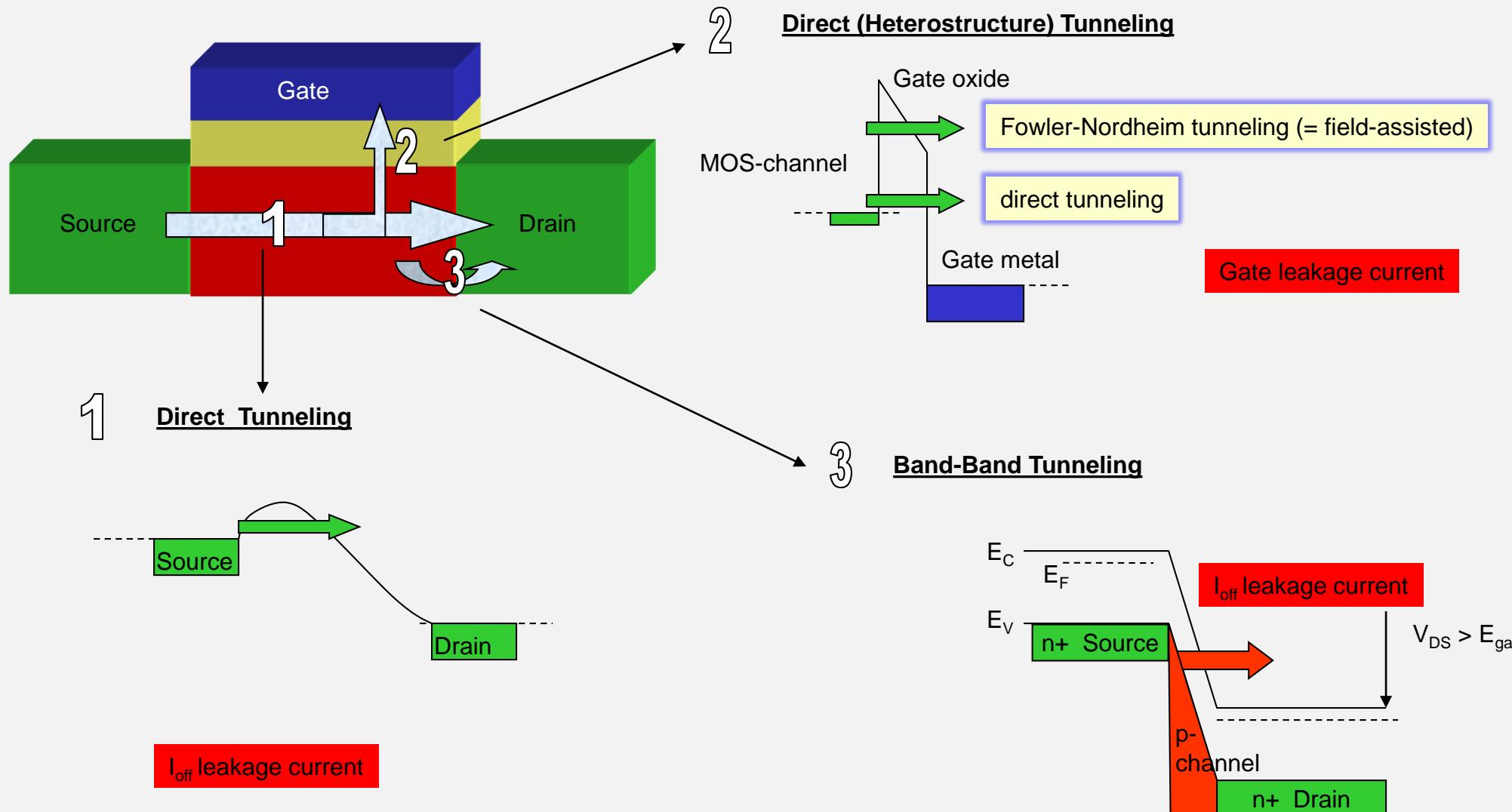
Esaki-Tunneling, Esaki-Diode  
Esaki-Tunneling MOSFET

## 8.3 Coulomb Blockade Devices

CMOS Roadmap to Single-Electron MOSFETs  
Nanotechnology  
Physics of Coulomb Blockade  
Coulomb Blockade Devices  
Single Electron Transistor  
Single Electron Memory and Logic

## Overview of Tunneling Devices





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Tunneling in MOSFETs

## 8.2 The Esaki-Tunneling MOSFET

Esaki-Tunneling, Esaki-Diode  
Esaki-Tunneling MOSFET

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1

tunneling gate leakage current due to scaling

since 2000 (180 nm node) it was recognized that further scaling will increase tunneling through gate oxide to an unacceptable level. The solution was the use of high-k oxides first with 65 nm in 2007.

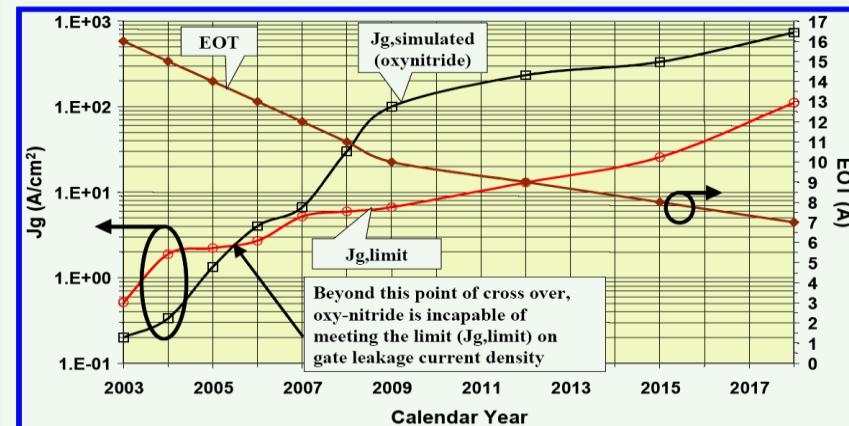
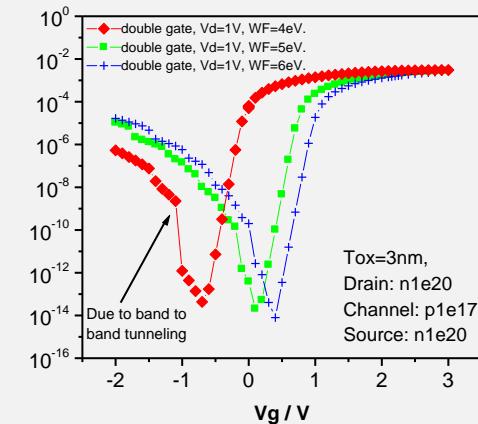
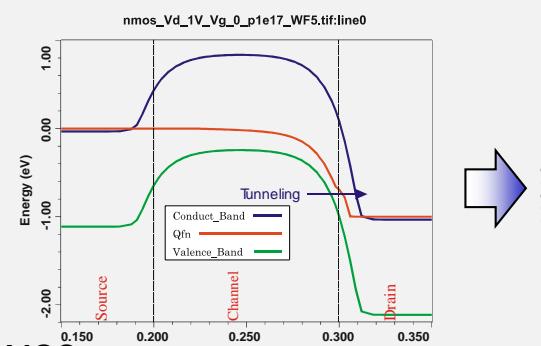


Figure 24 LOP Logic Scaling-up of Gate Leakage Current Density Limit and of Simulated Gate Leakage due to Direct Tunneling [UPDATED](#)

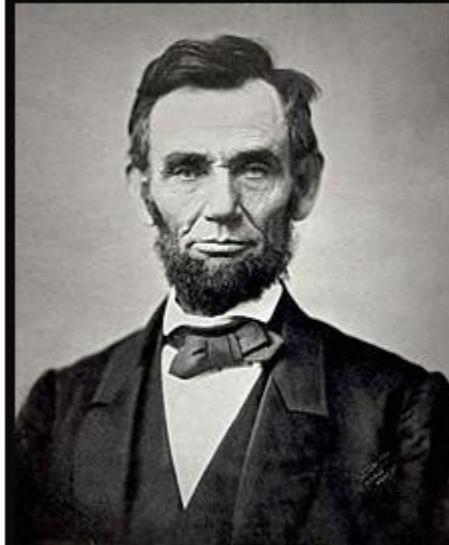
2

tunneling S/D tunneling due to supply voltage

without possibility to reduce  $V_{DS}$  in reverse direction (which means negative bias on a n-FET or positive bias on an p-FET, as it is used in any CMOS inverter) the high drain bias ( $\sim 1V$ ) will induce band-band tunneling. This reverse current will make always one FET in the inverter not closing current perfectly -> lose of advantage of low-power CMOS



So, why not to try to make your enemy your friend ?



The best way to destroy an enemy is to make him a friend.

(Abraham Lincoln)

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can we use unavoidable tunneling currents for active device operation ?



yes, we can

# Discovery of Esaki-Tunneling

## Esaki-Tunneling: Band-Band-Tunneling without High Electric Fields, due to abrupt, highly doped junctions

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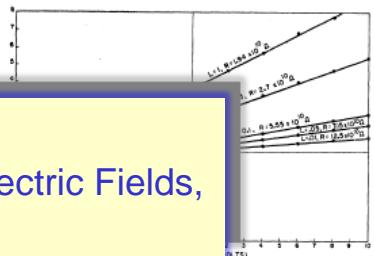


FIG. 3. Current through film vs applied voltage. Relative light intensities and corresponding film resistances are as shown. Intercepts on the ordinate and the abscissa are the short-circuit current and the open-circuit voltage, respectively.

with the space charge layers at grain boundaries. Whatever their location, however, the crystallographic ordering process which produces the additive arrangement of these elements is a major factor yet to be explained.

<sup>†</sup>This work was supported by the Evans Signal Corps Laboratories.

<sup>1</sup>L. Penson, Phys. Rev. **109**, 601 (1958), preceding letter.

<sup>2</sup>M. B. Prince, J. Appl. Phys. **26**, 534 (1955).

<sup>3</sup>J. J. Loferski, J. Appl. Phys. **27**, 777 (1956).

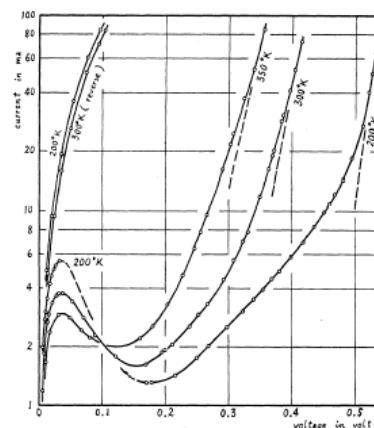


FIG. 1. Semilog plots of the measured current-voltage characteristic at 200°K, 300°K, and 350°K.

in which no voltage is applied to the junction, though the band scheme may be, at best, a poor approximation for such a narrow junction. (The remarkably large values observed in the capacity measurement indicated that the junction width is approximately 150 angstroms, which results in a built-in field as large as  $5 \times 10^5$  volts/cm.)<sup>2</sup> In the reverse direction and even in the forward direction for low voltage, the current might be carried only by internal field emission and the possibility of an avalanche might be completely excluded because the breakdown occurs at much less than the threshold voltage for electron-hole pair production.<sup>3</sup> Owing to the large density of electrons and holes, their distribution should become degenerate; the Fermi level in the p-type side will be 0.06 ev below the top of the valence band,  $E_v$ , and that in the n-type side will lie above the bottom of the conduction band,  $E_c$ . At zero bias, the field emission current  $I_{e \rightarrow v}$  from the valence band to the empty state of the conduction band and the current

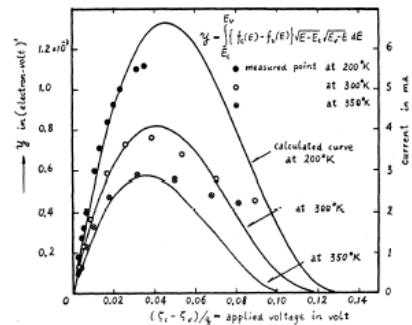


FIG. 3. Comparison of the current-voltage curves calculated with the measured points at 200°K, 300°K, and 350°K.

$I_{e \rightarrow v}$  from the conduction band to the empty state of the valence band should be detail-balanced. Expressions for  $I_{e \rightarrow v}$  and  $I_{v \rightarrow e}$  might be formulated as follows:

$$I_{e \rightarrow v} = A \int_{E_v}^{E_c} f_e(E) \rho_v(E) Z_{e \rightarrow v} \{1 - f_v(E)\} \rho_e(E) dE,$$

$$I_{v \rightarrow e} = A \int_{E_v}^{E_c} f_v(E) \rho_e(E) Z_{v \rightarrow e} \{1 - f_e(E)\} \rho_v(E) dE,$$

where  $Z_{e \rightarrow v}$  and  $Z_{v \rightarrow e}$  are the probabilities of penetrating the gap (these could be assumed to be approximately equal);  $f_e(E)$  and  $f_v(E)$  are the Fermi-Dirac distribution functions, namely, the probabilities that a quantum state is occupied in the conduction and valence bands, respectively;  $\rho_v(E)$  and  $\rho_e(E)$  are the energy level densities in the conduction and valence bands, respectively.

When the junction is slightly biased positively and negatively, the observed current  $I$  will be given by

$$I = I_{e \rightarrow v} - I_{v \rightarrow e} = A \int_{E_v}^{E_c} \{f_e(E) - f_v(E)\} Z \rho_e(E) \rho_v(E) dE.$$

From this equation, if  $Z$  may be considered to be almost constant in the small voltage range involved, we could calculate fairly well the current-voltage curve at a certain temperature, indicating the dynatron-type characteristic in the forward direction, as shown in Fig. 3.

Further experimental results and discussion will be published at a later time. The author wishes to thank Miss Y. Kurose for assistance in the experiment and the calculations.

<sup>1</sup>A. H. Wilson, Proc. Roy. Soc. (London) **A136**, 487 (1932); J. Frenkel and A. Joffe, Physik Z. Sowjetunion **1**, 60 (1932); L. Nordheim, Z. Physik **75**, 434 (1932).

<sup>2</sup>McAfee, Ryder, Shockley, and Sparks, Phys. Rev. **83**, 650 (1951); C. Zener, Proc. Roy. Soc. (London) **145**, 523 (1934).

<sup>3</sup>S. L. Miller, Phys. Rev. **99**, 1234 (1955); A. G. Chynoweth and K. G. McKay, Phys. Rev. **106**, 418 (1957).

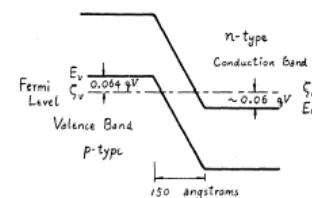
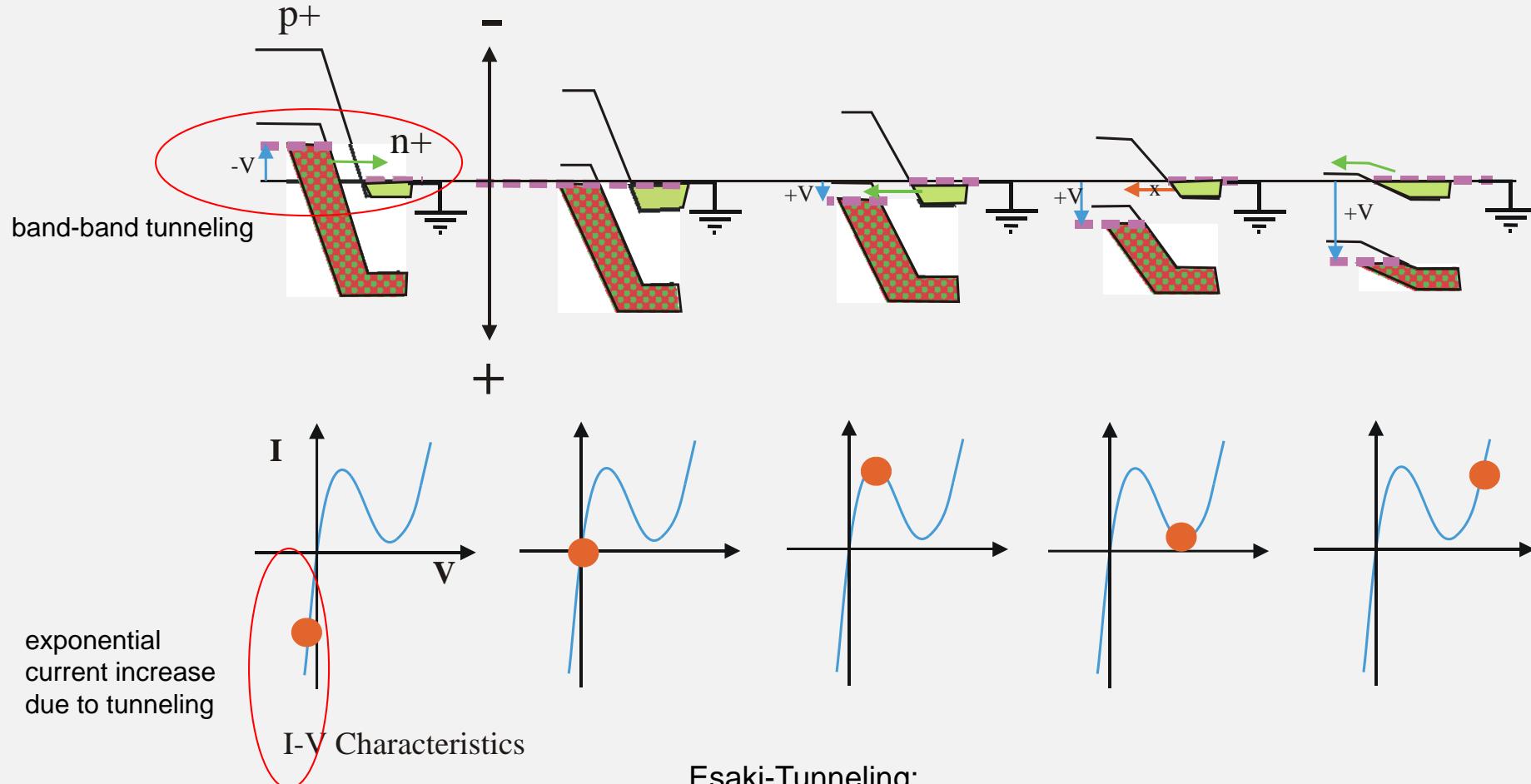


FIG. 2. Energy diagram of the p-n junction at 300°K and no bias voltage.

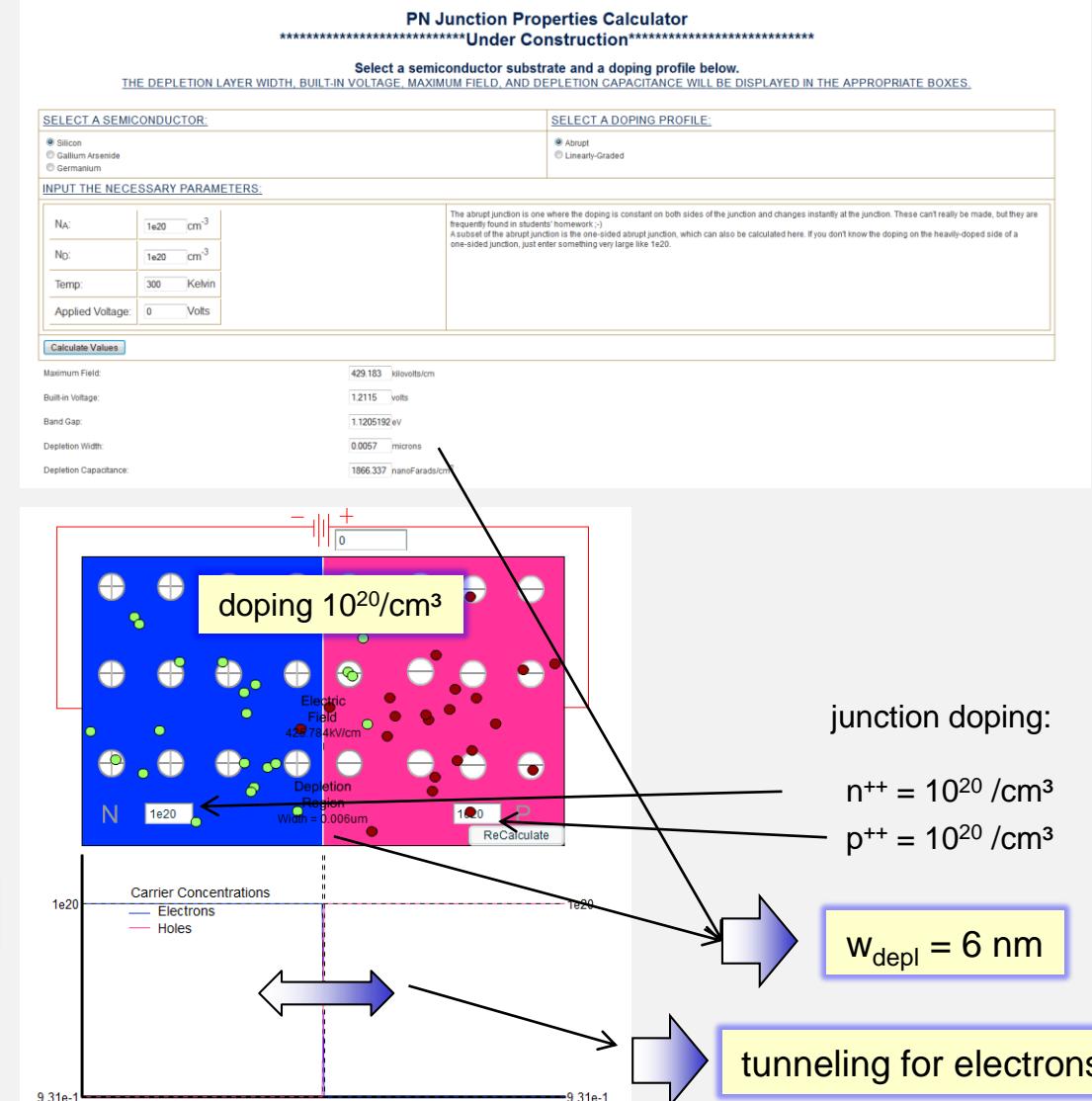
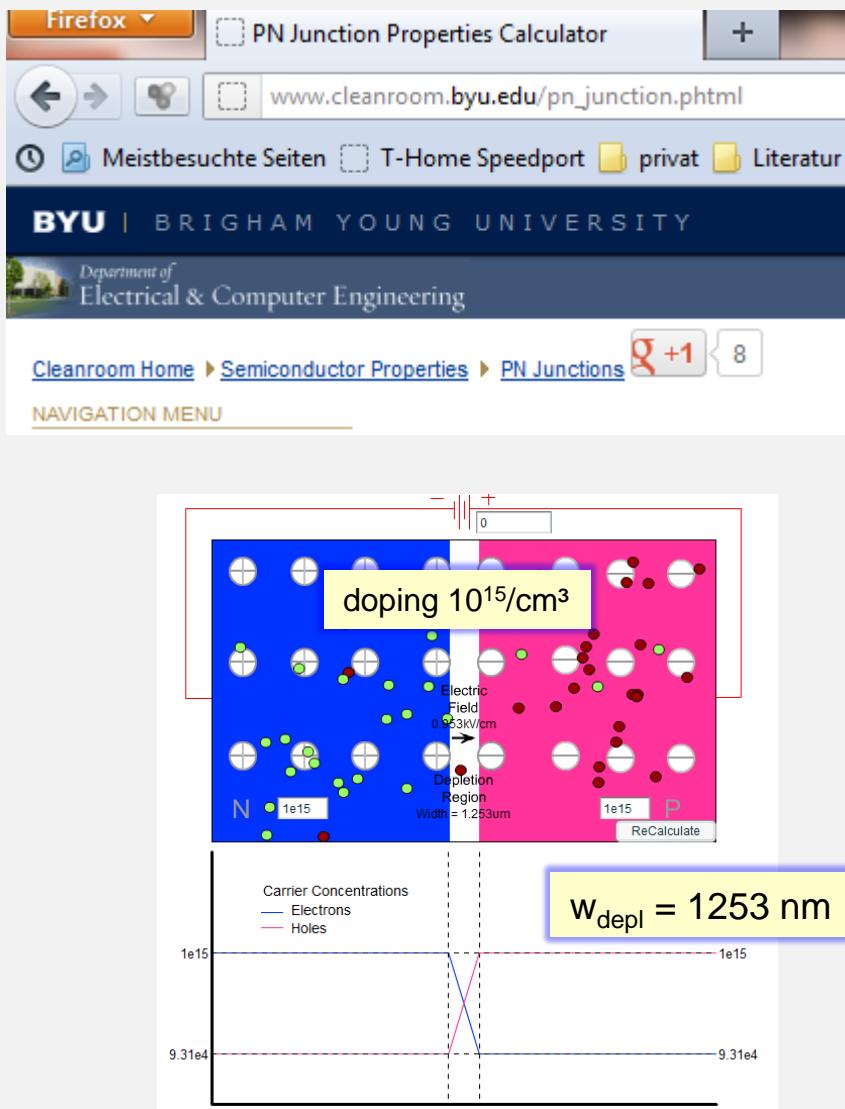
Electron Energy Band Diagram:



### Esaki-Tunneling:

In extreme highly-doped  $n^{++}/p^{++}$  semiconductor junctions:

- 1) the Fermi-level may be up to 0.1 eV within the conduction and valence band
- 2) the depletion zone is only a few nanometers (= electron tunneling distance)



First fabricated vertical Esaki-Tunneling-FET



*Thin Solid Films* 369 (2000) 387–389



A vertical MOS-gated Esaki tunneling transistor in silicon

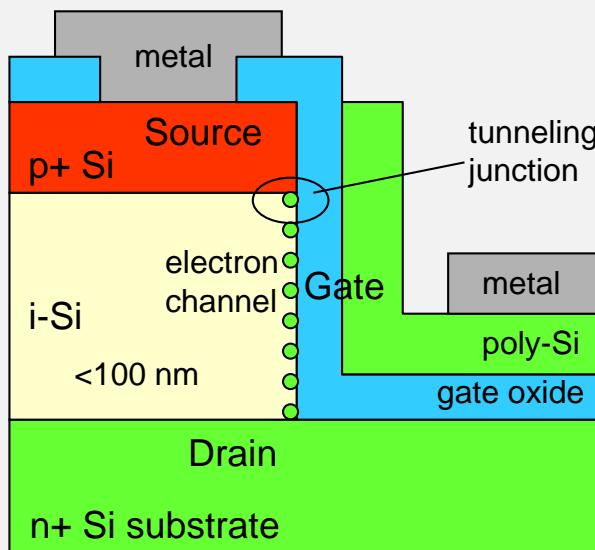
W. Hansch\*, C. Fink, J. Schulze, I. Eisele

Universität der Bundeswehr München, Institut für Physik, D-85577 Neubiberg, Germany

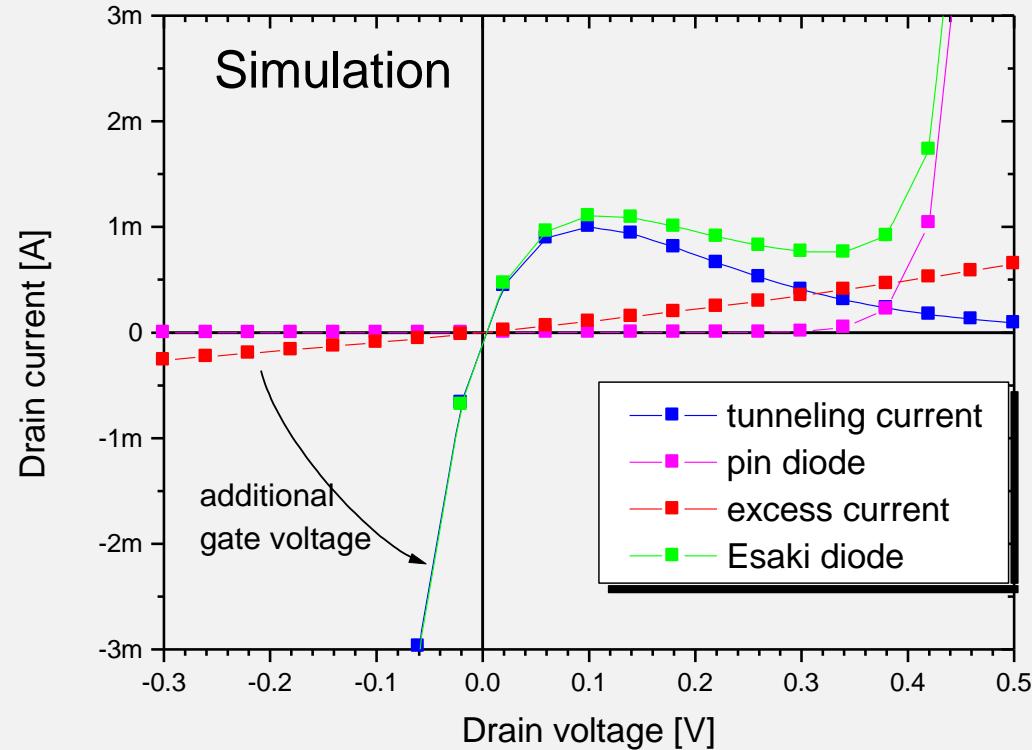
Abstract

For the first time a vertical, MOS gated tunneling transistor in silicon is fabricated. The necessary sharp doping profile structure is created by means of MBE. Pronounced transistor action due to Esaki tunneling is demonstrated at room temperature. At a low supply voltage of  $-0.2$  V a current gain of three magnitudes with saturation behaviour is achieved. MOS-gate, low supply voltage and exponential current increase make this device attractive for ULSI applications. © 2000 Elsevier Science S.A. All rights reserved.

Keywords: Molecular beam epitaxy; Vertical tunneling device; Esaki diode



The Esaki-Tunneling MOSFET looks like a vertical MOSFET, but the drain is oppositely doped as the source.



In the reverse-biased pin-diode the current can be switched on and off by creating a MOS-channel

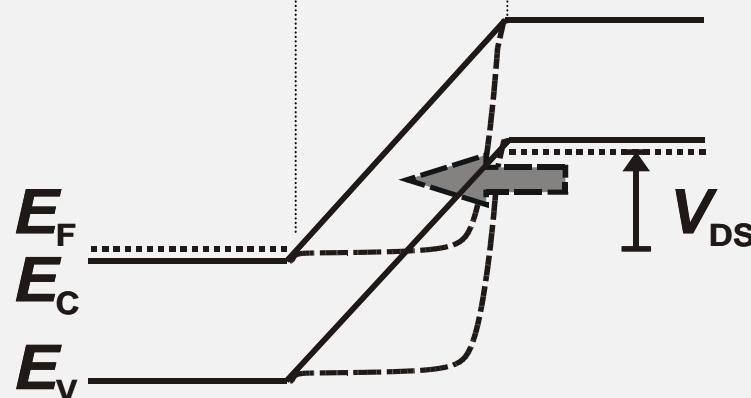
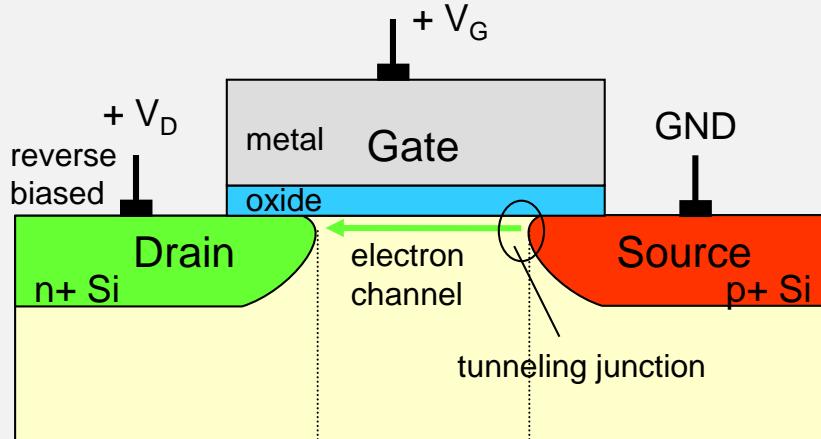
## NTFET

### Off-state:

Device behaves like a reverse biased *pin*-diode

### On-state:

Positive  $V_{GS}$  induces an electron channel. The band bending allows interband tunneling at the source channel interface

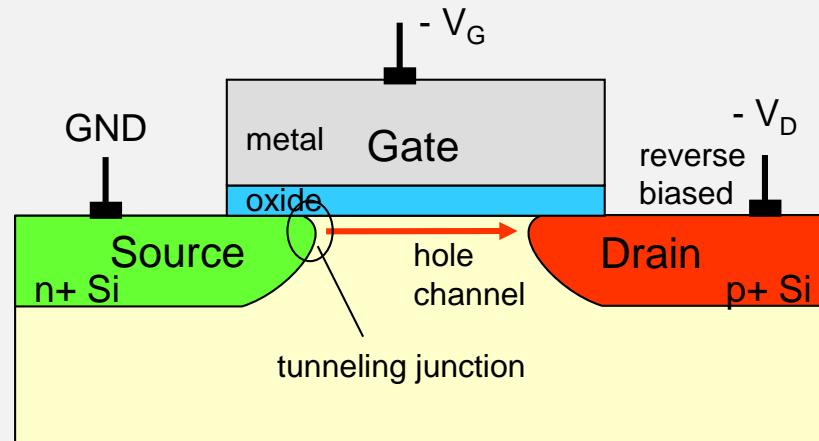


→ gate controlled interband tunneling

## PTFET

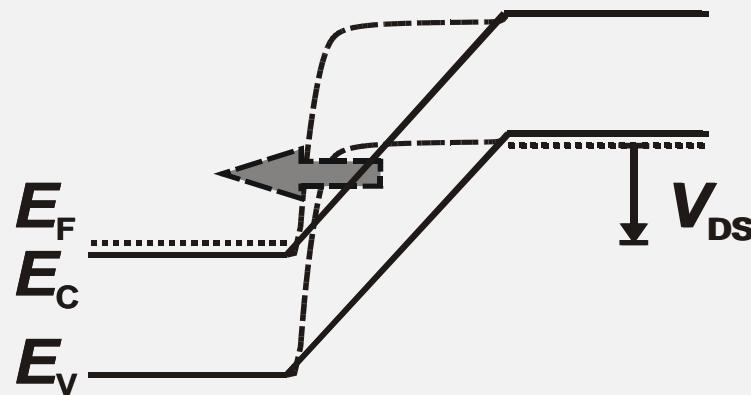
### Off-state:

Device behaves like a reverse biased *pin*-diode



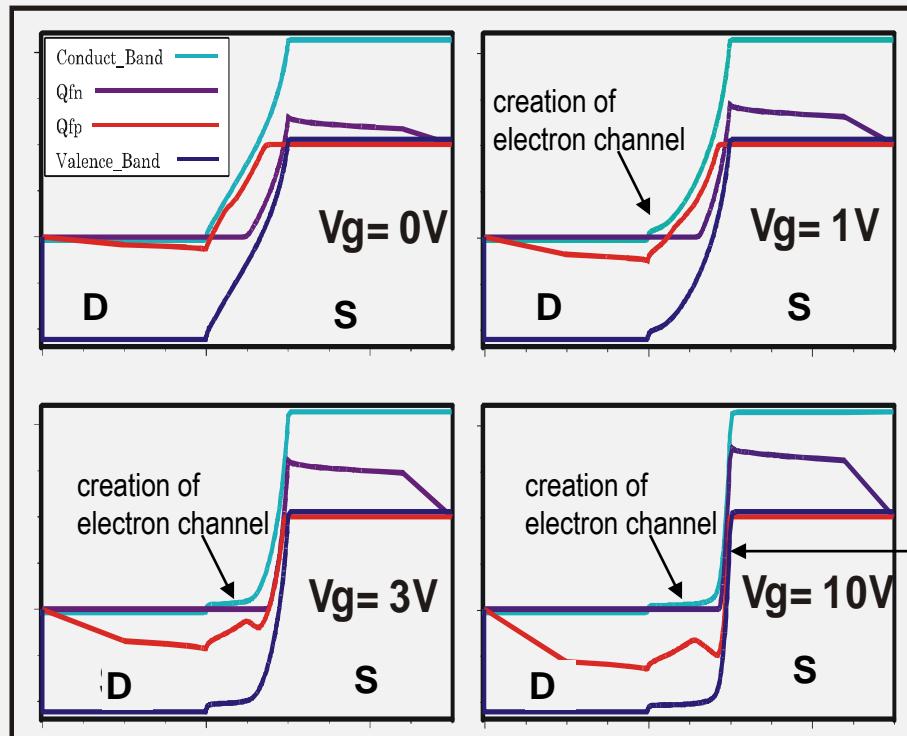
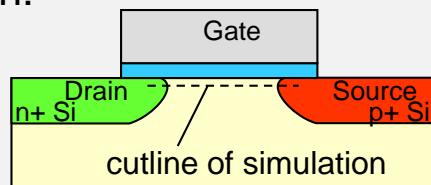
### On-state:

Negative  $V_{GS}$  induces a hole channel. The band bending allows interband tunneling at the source channel interface



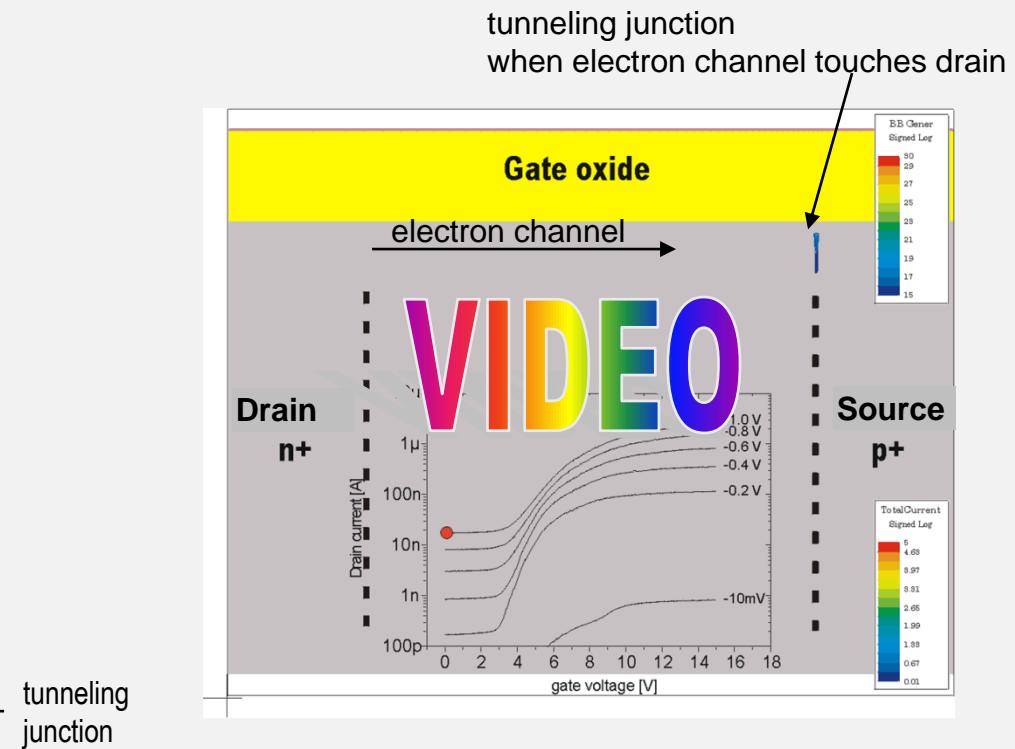
→ complementary devices exist

Simulation:

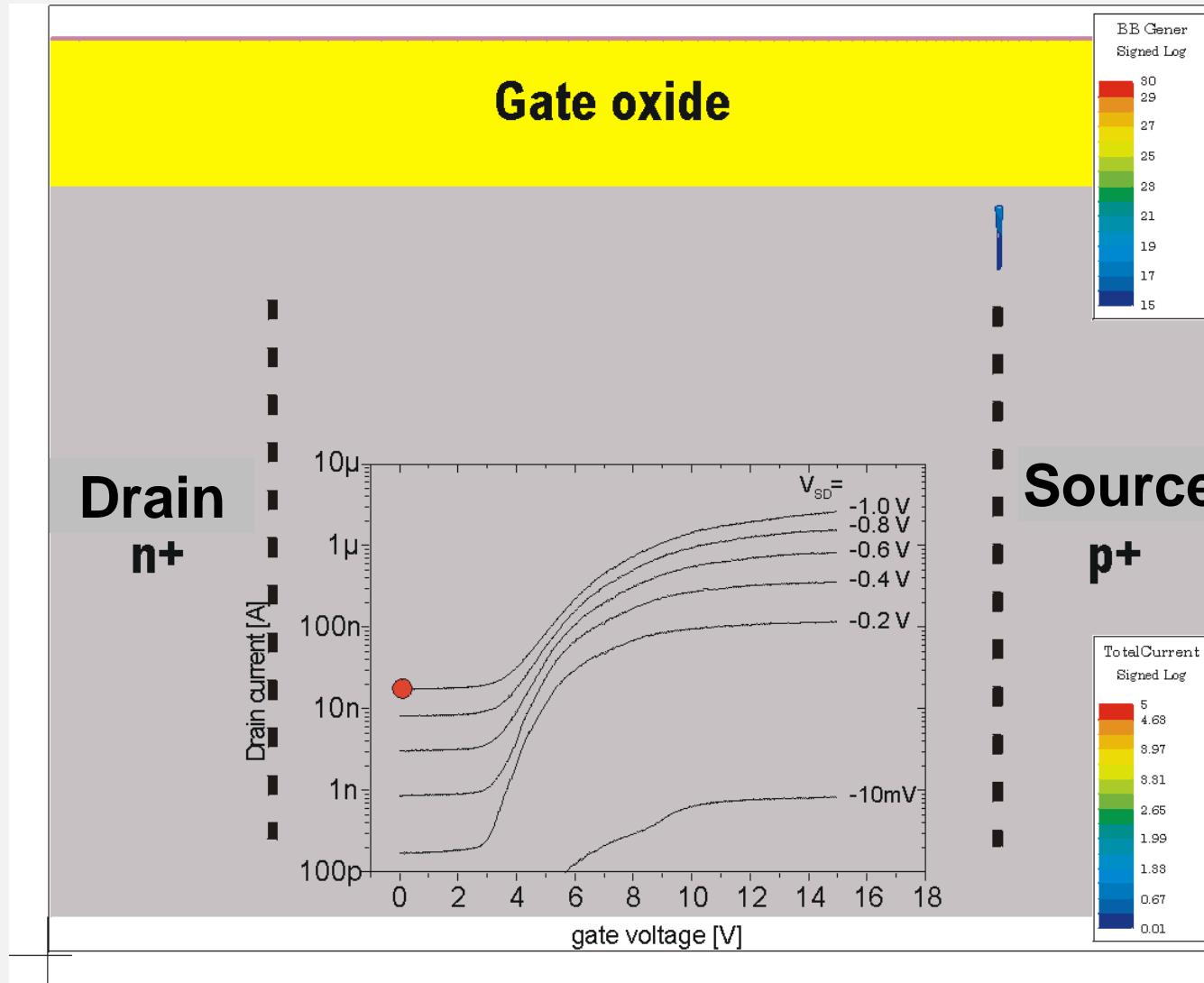


Band diagrams at the silicon surface  
with various gate voltages ( $V_{\text{Drain}}$  is fixed at -1V)

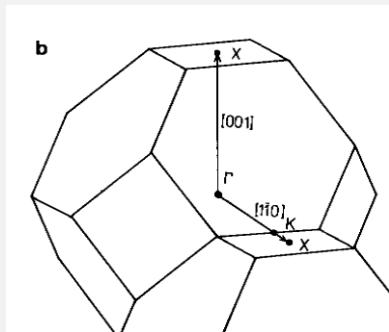
Simulator: MEDICI of TAURUS (TMA)



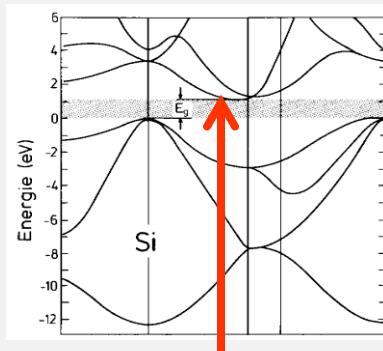
Tunneling can be controlled by gate voltage



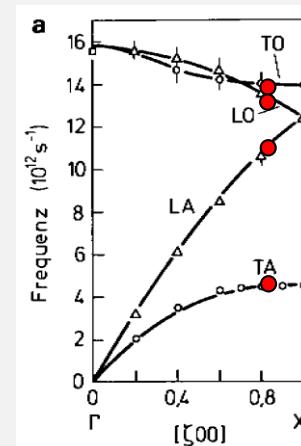
## Theory:



Brillouin-zones in Si



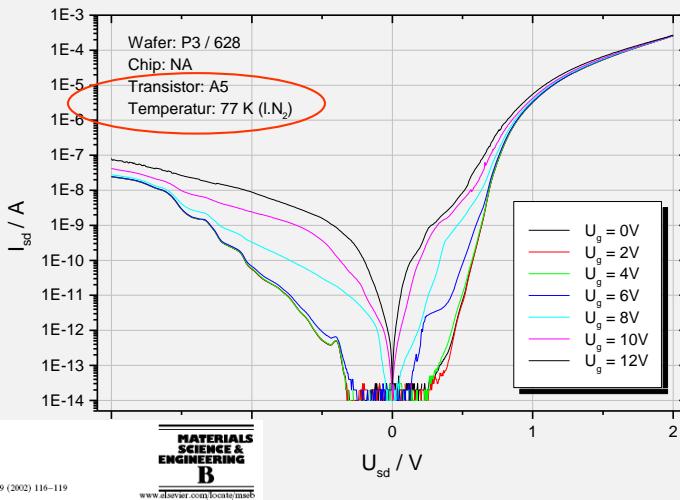
Bandstructure of silicon  
-> Minimum-Gap at  $\sim 0.8 \text{ \AA}^{-1}$  in X-direction



At wave vector  $q = 0.8 \text{ \AA}^{-1}$   
the phonon energies are:  
( $1 \text{ eV} = 2.42 \times 10^{14} \text{ Hz}$ )

- TO:  $\sim 59 \text{ meV}$
- LO:  $\sim 53 \text{ meV}$
- LA:  $\sim 44 \text{ meV}$
- TA:  $\sim 18 \text{ meV}$

## Experiment:



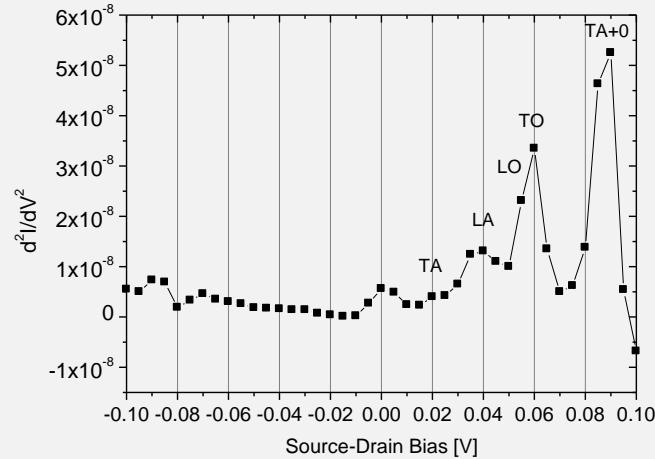
Experimental IV-characteristics at 77K

Phonon assisted tunneling in gated p-i-n diodes

S. Sedlmaier <sup>a,\*</sup>, J. Schulze <sup>a</sup>, T. Sulima <sup>a</sup>, C. Fink <sup>a</sup>, C. Tolksdorf <sup>a</sup>, A. Bayerstadler <sup>a</sup>, I. Eisele <sup>a</sup>, P.-F. Wang <sup>b</sup>, K. Hilsenbeck <sup>b</sup>, W. Hansch <sup>b</sup>

<sup>a</sup>Institute of Physics, Universität der Bundeswehr München, 85577 Neubiberg, Germany

<sup>b</sup>Institute of Technical Electronics, Technische Universität München, 80333 Munich, Germany



2. derivative of I-V,  $V_g=12\text{V}$



Proof of phonon-assisted band-band tunneling of electrons



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Solid-State Electronics 47 (2003) 1187–1192

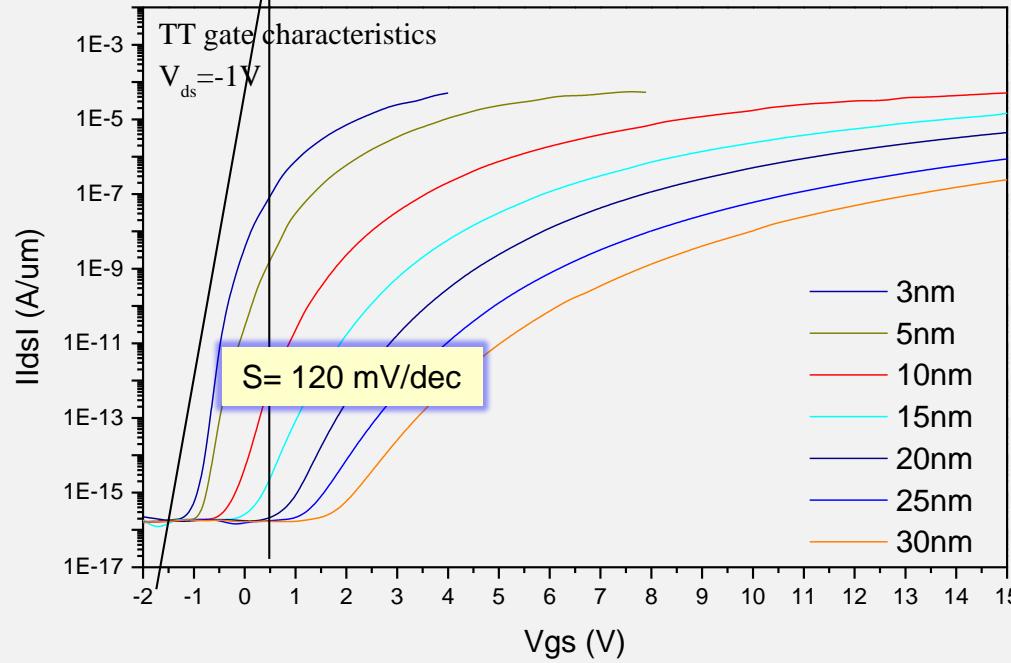
PERGAMON

### Simulation of the Esaki-tunneling FET

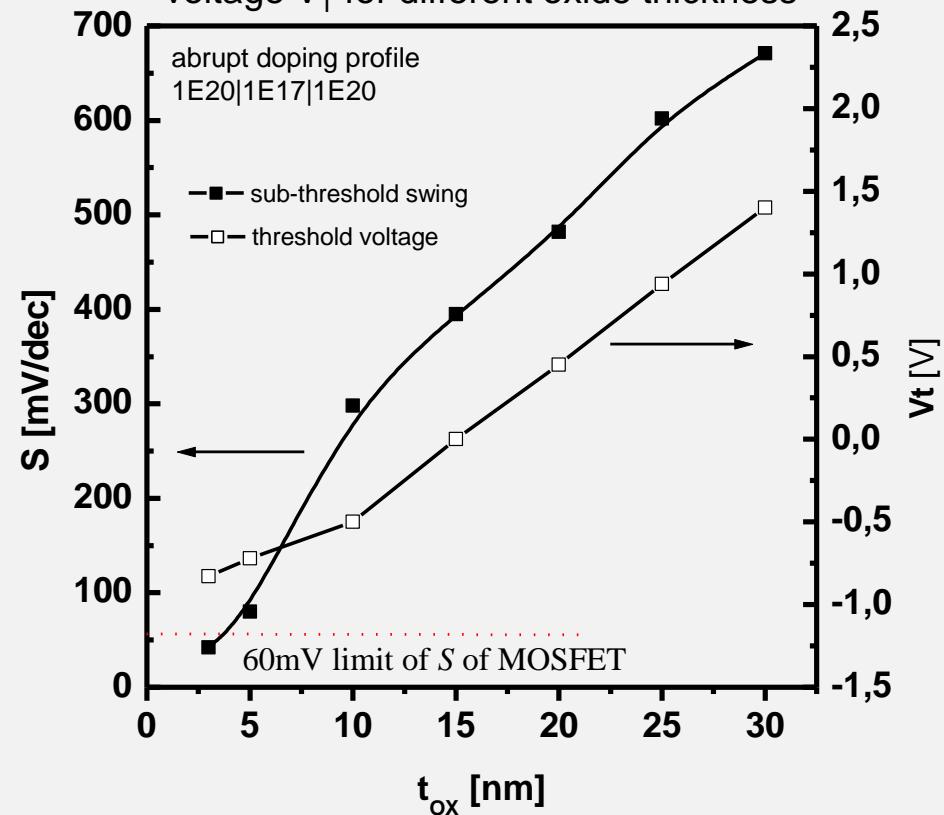
Peng-Fei Wang \*, Thomas Nirschl, Doris Schmitt-Landsiedel, Walter Hansch

Institute for Technical Electronics, Technical University Munich, Arcistr. 21, 80333 Munich, Germany

### Transfer characteristics for different oxide thickness

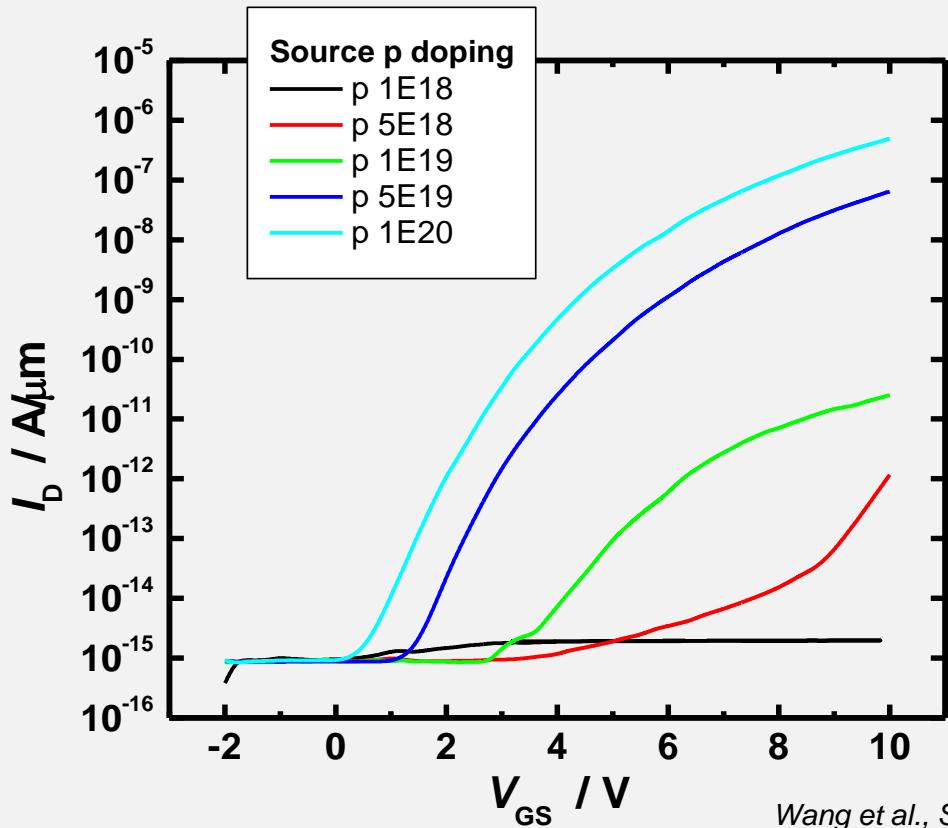


Subthreshold slope S and threshold voltage V<sub>T</sub> for different oxide thickness

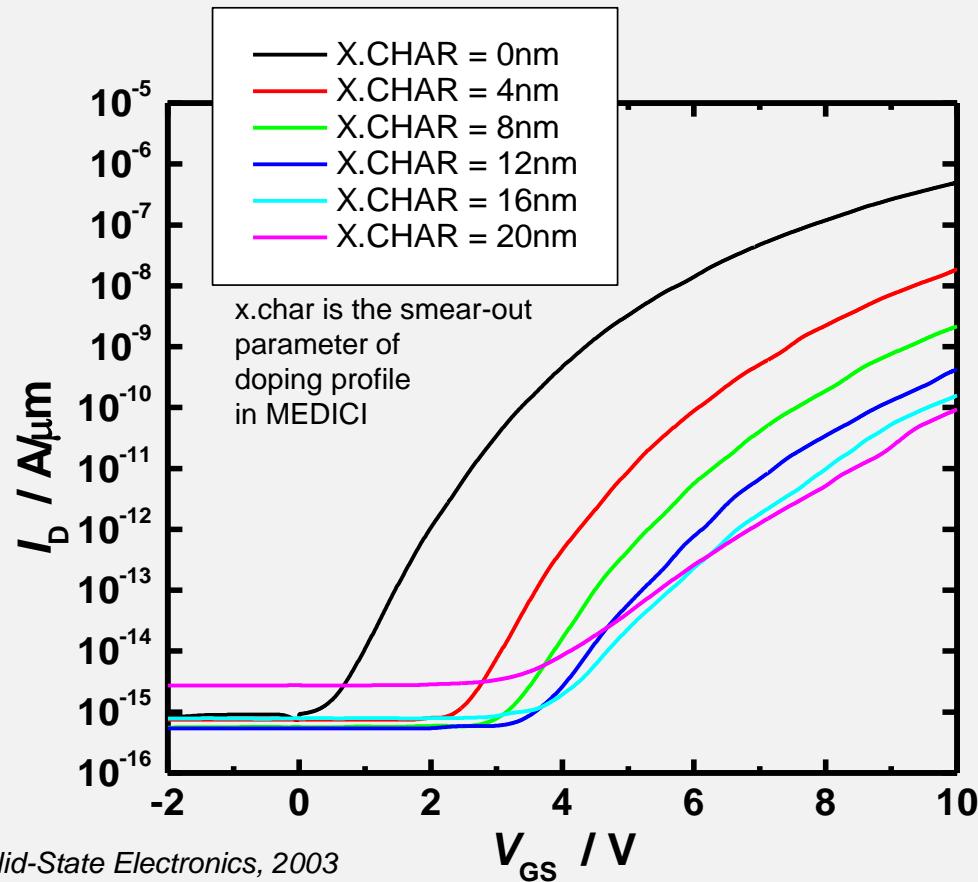


Subthreshold slope below 60 mV/dec possible !!!

Transfer characteristics  
for various source dopings and various doping profiles at the source-channel interface



Wang et al., Solid-State Electronics, 2003

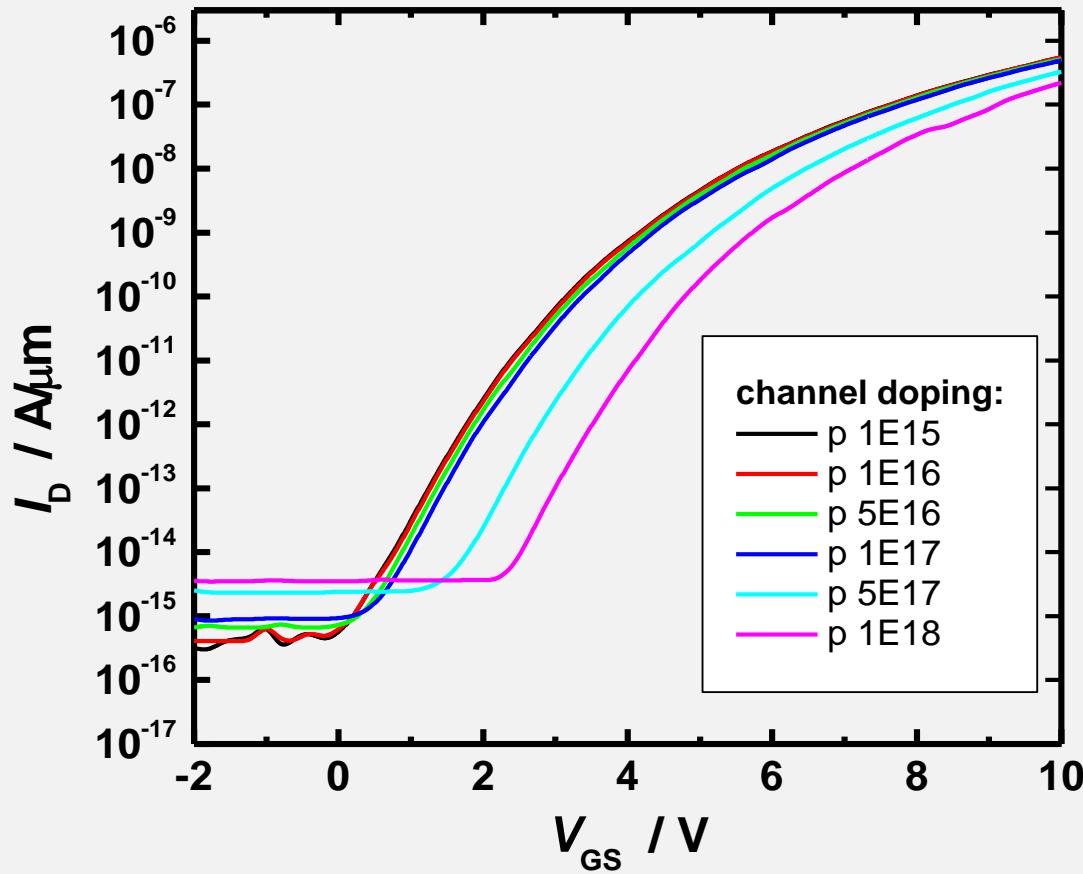


as higher the Source doping as steeper the SS



as more abrupt the Source doping as steeper the SS

Transfer characteristics  
for different channel dopings



**Important design parameters:**

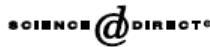
- High source doping
- Steep doping gradients at the source channel interface
- Thin gate oxide (but requirements are not as high as for the MOSFET)
- Channel doping has hardly any effect as long as it is below  $10^{17} \text{ cm}^{-3}$

Undoped channels (no threshold fluctuations) keep the S constant





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Solid-State Electronics 48 (2004) 2281–2286

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## Complementary tunneling transistor for low power application

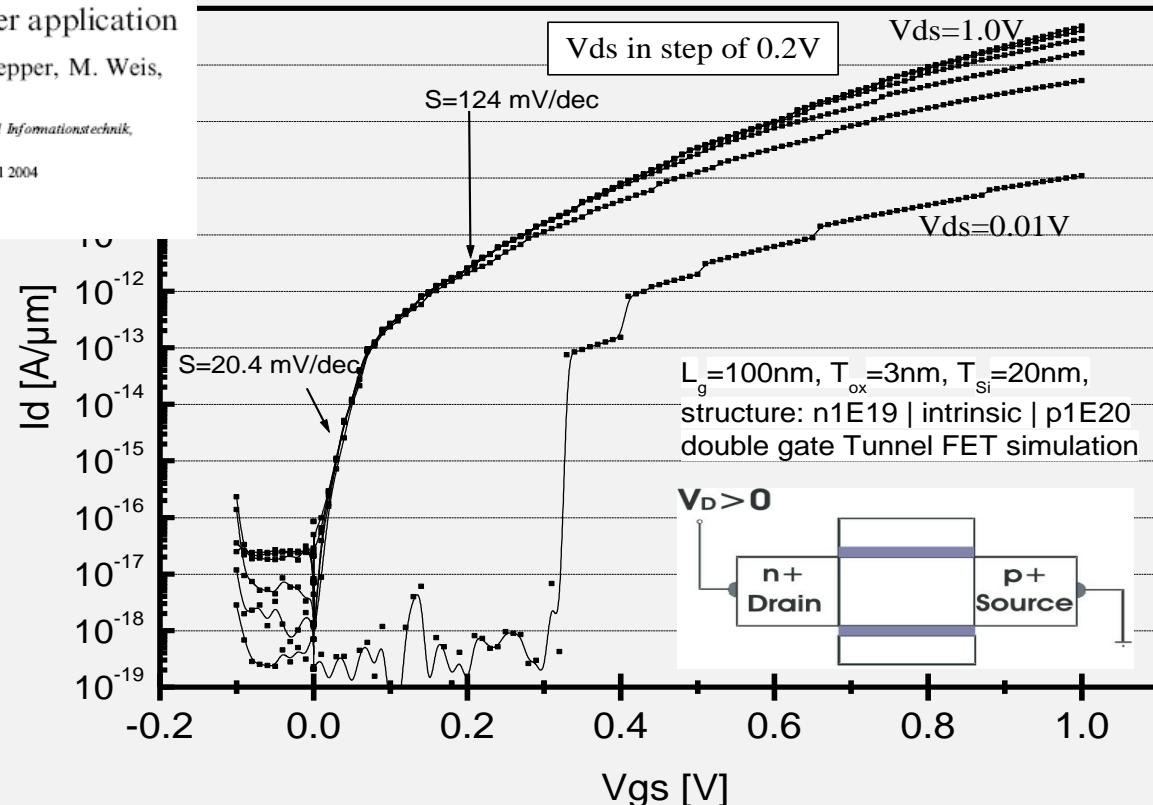
P.-F. Wang \*, K. Hilsenbeck, Th. Nirschl, M. Oswald, Ch. Stepper, M. Weis,  
D. Schmitt-Landsiedel, W. Hansch

Institute for Technical Electronics, Technical University Munich, Fakultät für Elektrotechnik und Informationstechnik,  
Arcisstr. 21, 80333 Munich, Germany

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Available online 6 May 2004

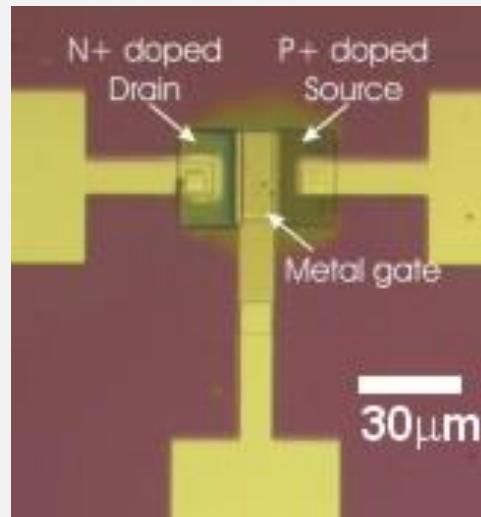
The review of this paper was arranged by Prof. S. Cristoloveanu



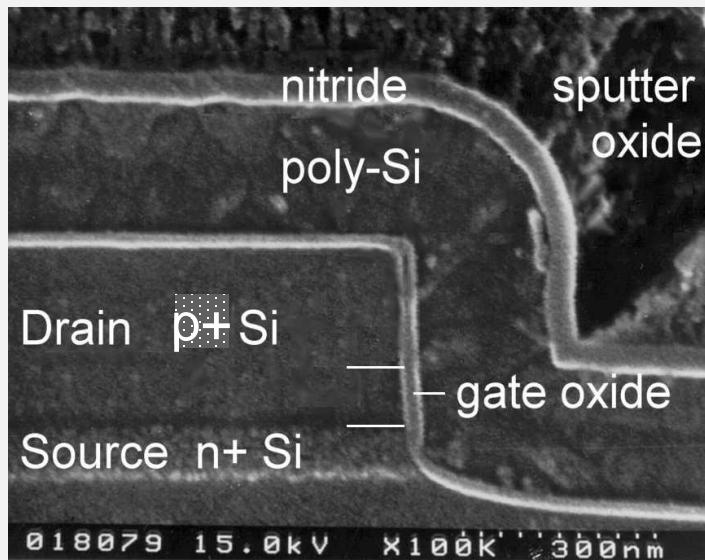
S is not limited by  $\ln(10) \cdot kT/q \sim 60 \text{ mV/dec}$  as in a MOSFET

-> still simulation and design work necessary

Top view of a long channel planar ETFET



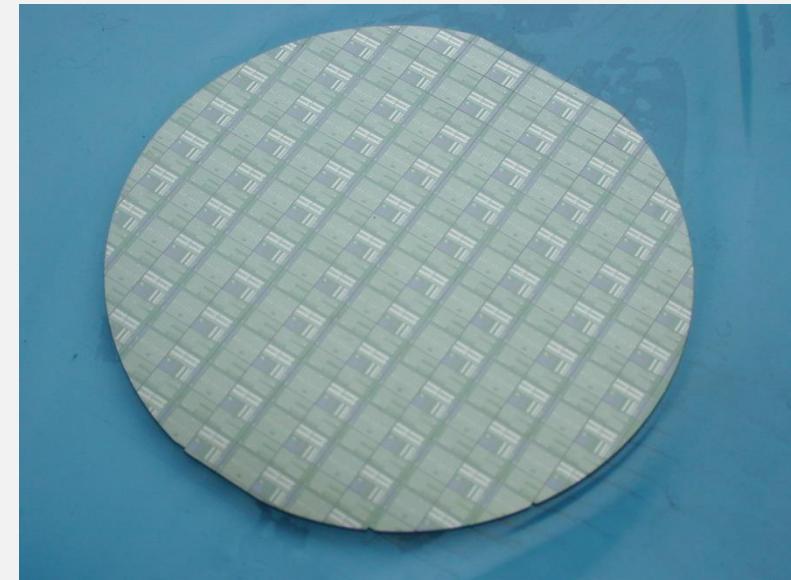
SEM picture of a vertical ETFET



Fabrication of planar TFETs at TUM in 2004

Hansch et al., IEDM, 2004

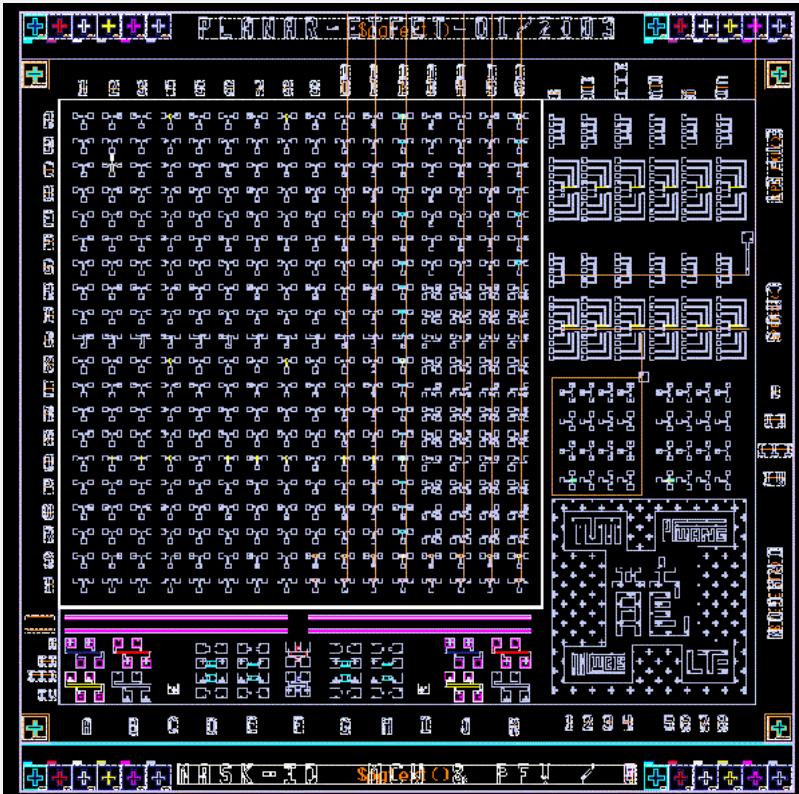
Processed wafer



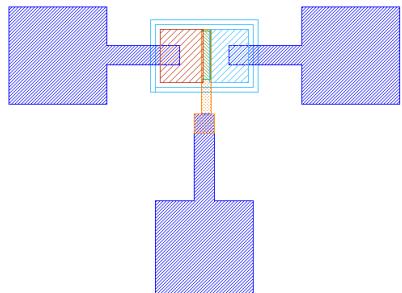
Fabrication of vertical TFETs at UniBw Munich in 1998

Hansch et al., Thin Solid Films, 1998

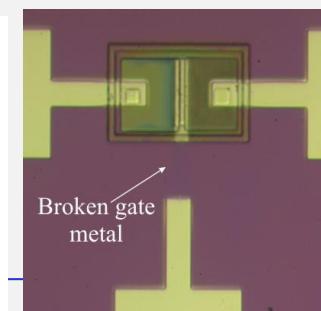
### Mask layout



TFET in mask

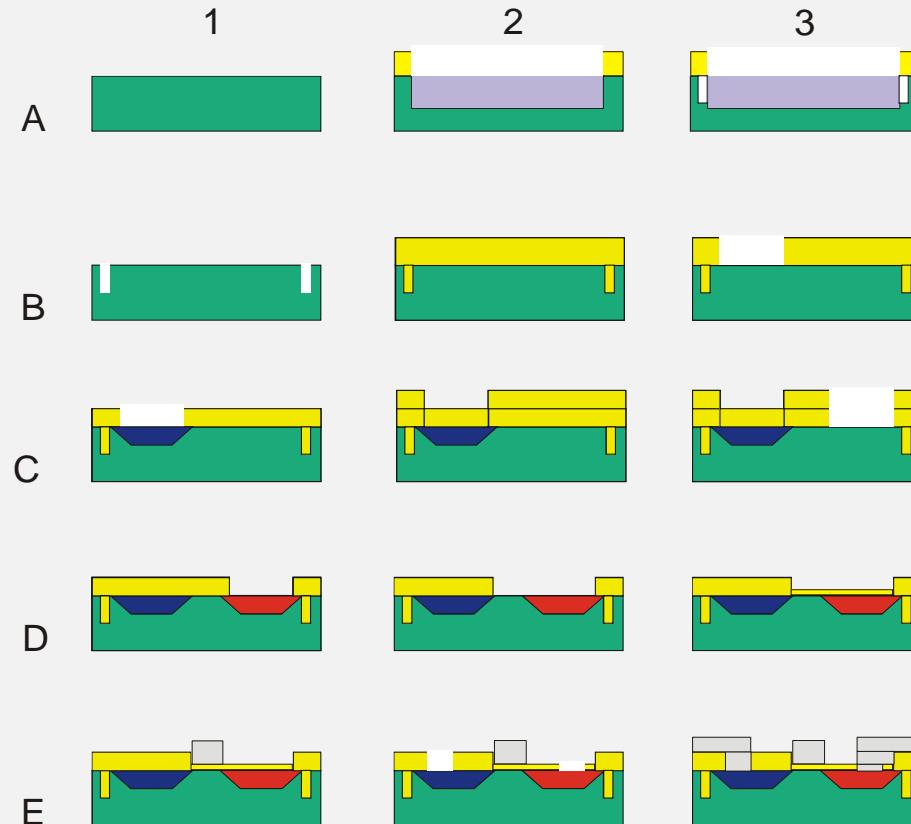


Fabricated TFET



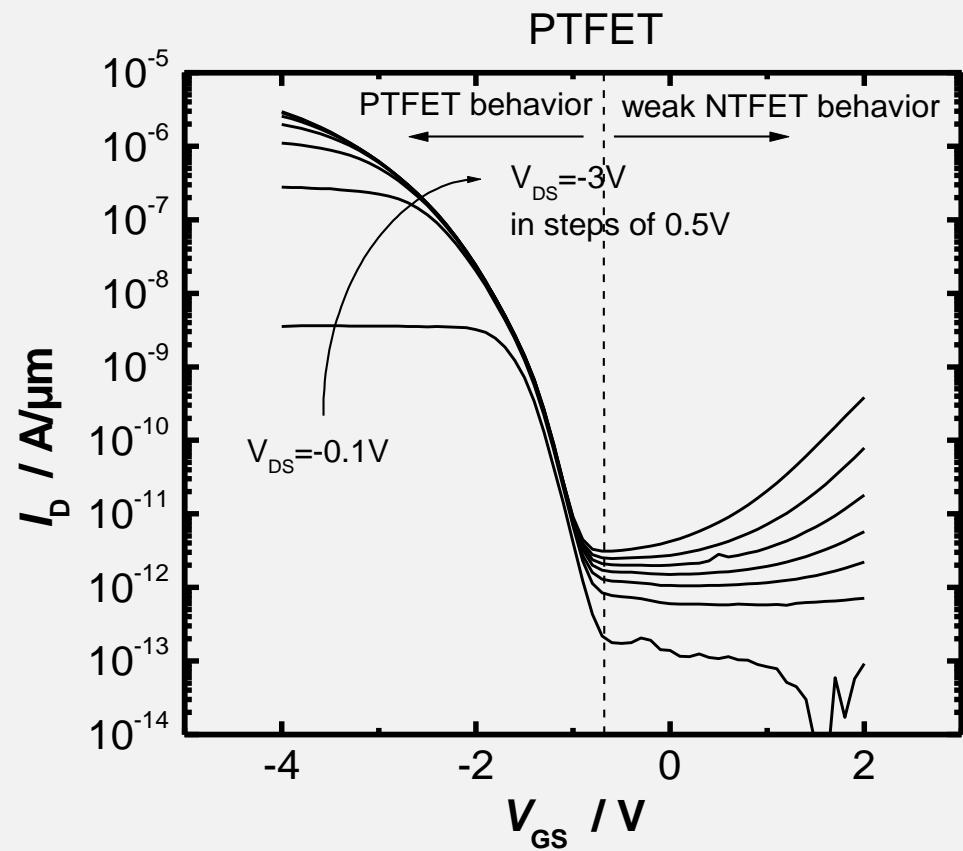
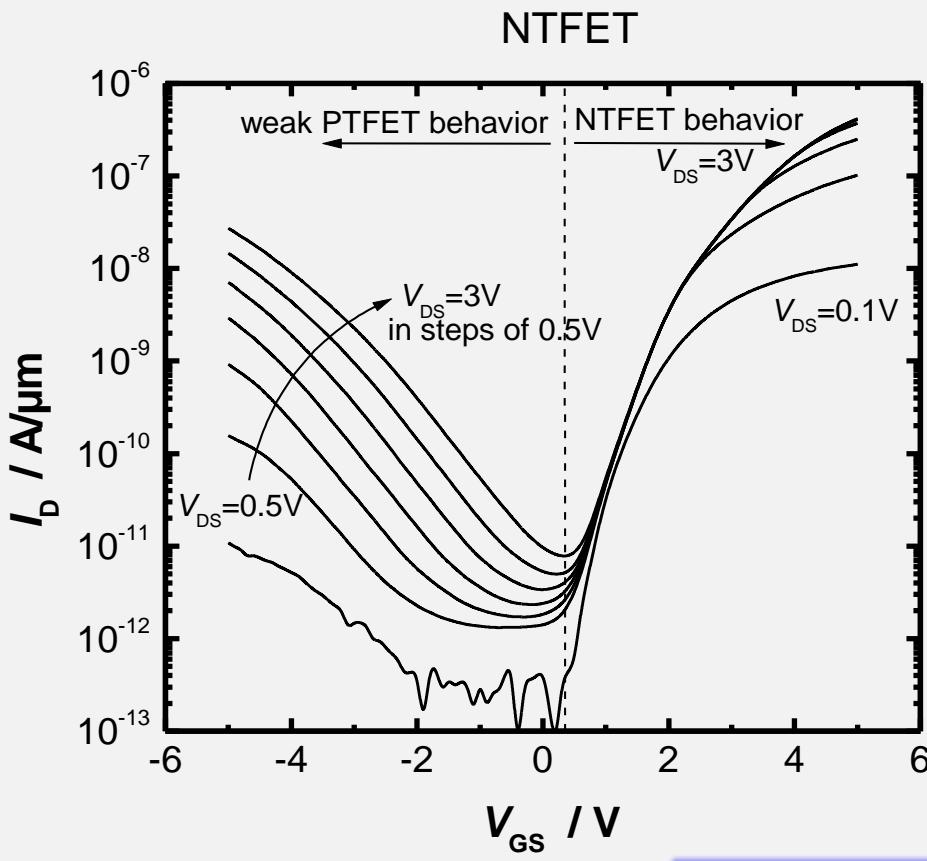
Advanced MOSFETs and Novel Devices

### Process sequence



<ul style="list-style-type: none"> <li>■ p well</li> <li>■ n+ doping</li> <li>■ p+ doping</li> </ul>	<ul style="list-style-type: none"> <li>■ SiO<sub>2</sub></li> <li>■ Al</li> <li>■ Si</li> </ul>
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## Transfer Characteristics



Experimental proof of complementary behaviour

Improvements for on-current necessary (e.g. SiGe)

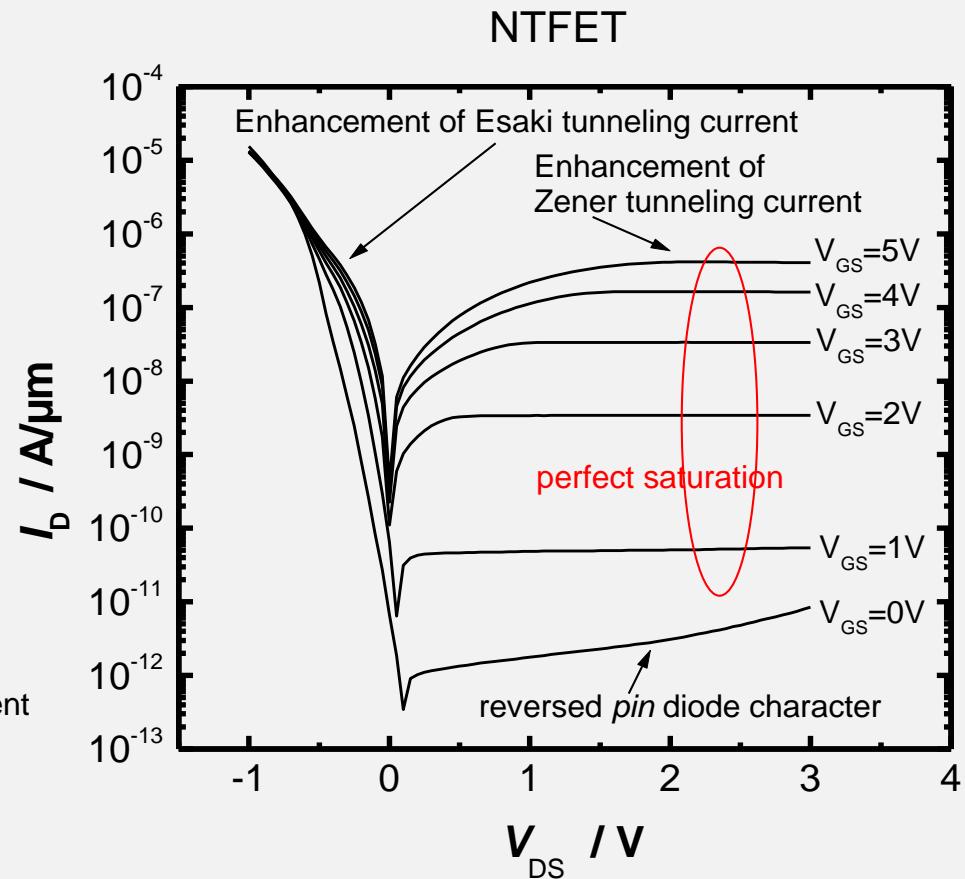
- Experimental proof of complementary behaviour
- $I_{on} / I_{off}$  up to 6 orders of magnitude
- Very good saturation behaviour
- Proof of working principle:  $I_D$  is enhanced in both the forward and the backward biased *pin*-structure



Combines the advantages of

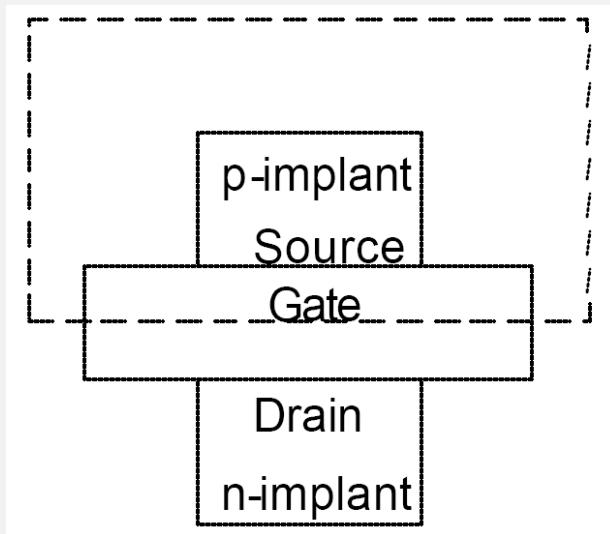
Bipolar - exponential increase in current  
MOS - no static power consumption

### Output Characteristics

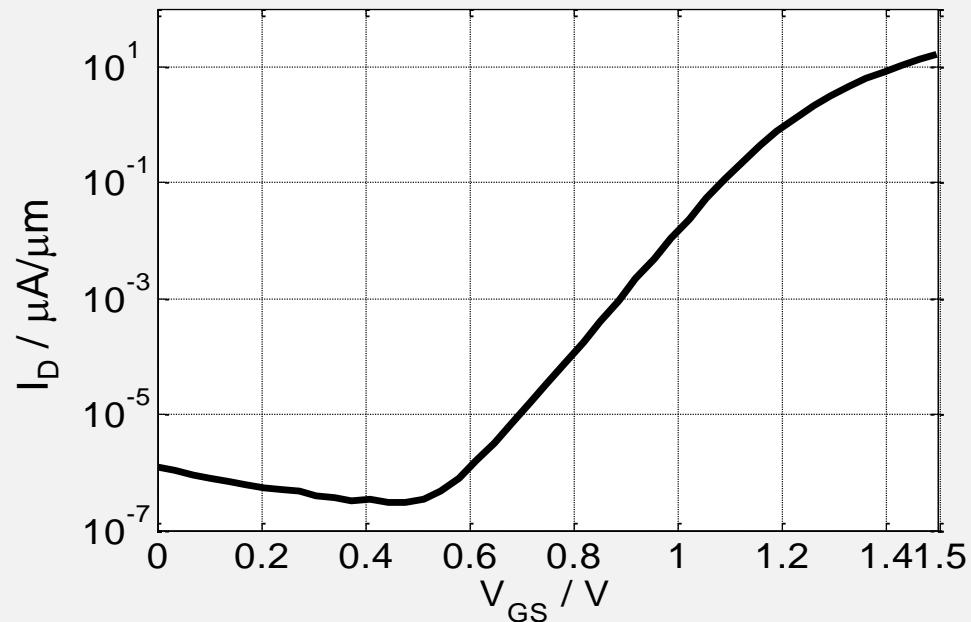


Ideal candidate for post silicon MOSFET era

- Infineon's standard CMOS process flow without any modifications was used for the fabrication of a tunneling device
- By shifting the p+ implant for the contact of the p-well over one half of a NMOSFET a diode is formed



transfer characteristic of the tunneling device fabricated in the 130nm technology

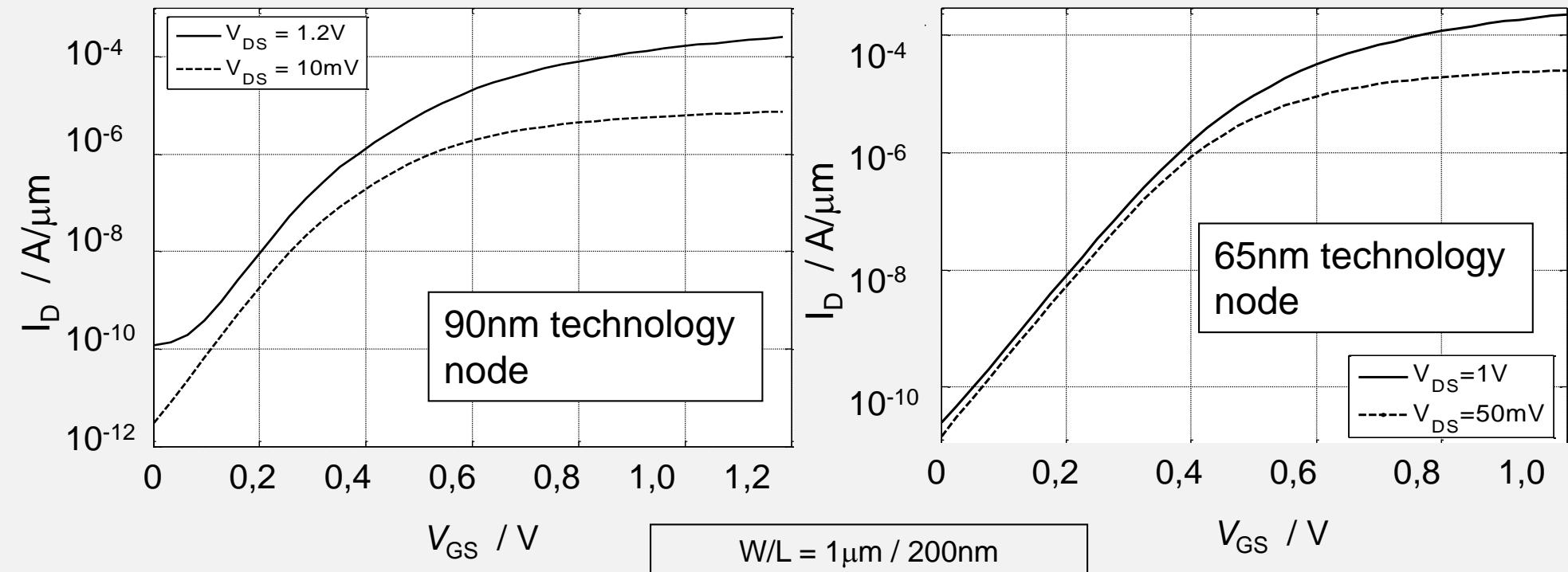


$W/L=1\mu\text{m}/300\text{nm}$ ,  $V_{DS}=V_{DD}=1.5\text{V}$



Never stop thinking

First prototypes show competitive  $I_{on}$  and lower leakage than the reference MOSFETs. The drain induced barrier lowering (DIBL) is also reduced substantially.

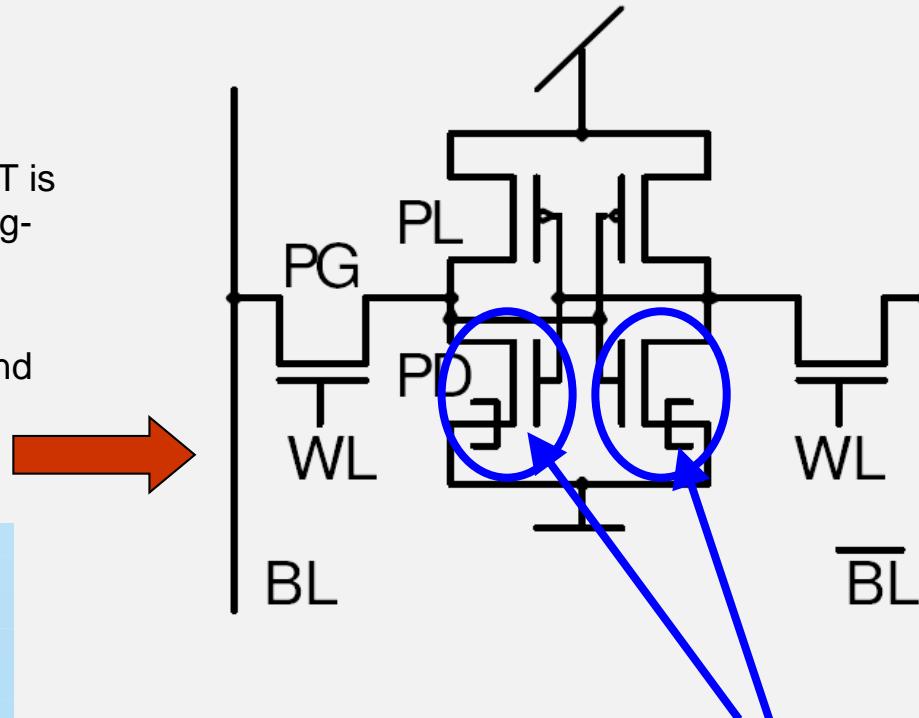


BUT:

Due to technological problems no gate controlled tunneling could be realized by the industrial processes.

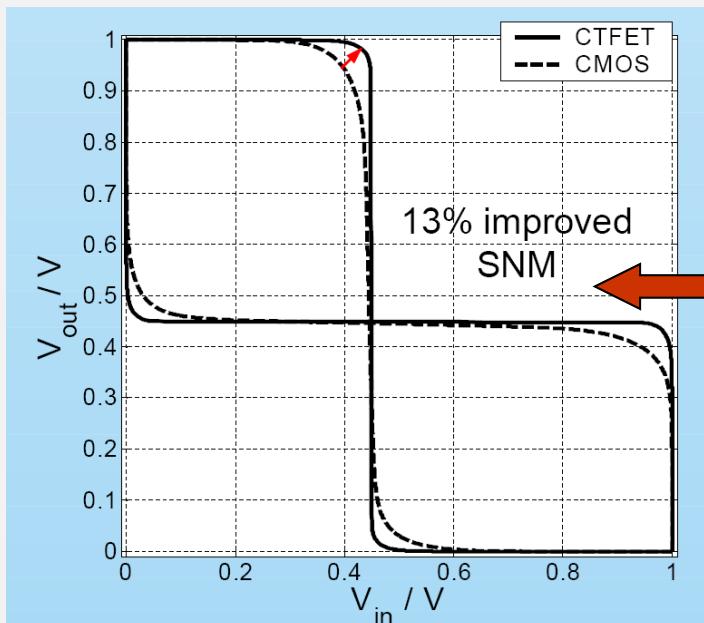
## Low Power Digital Circuits SRAM Cell

- Due to its extremely low leakage current the TFET is suitable for low standby-power and low operating-power circuits.
- A 6T SRAM cell consisting of both MOSFETs and TFETs combines the powers of both devices in today's technology.



Pull-down device replaced by TFET:

- smaller leakage current
- smaller area
- larger static noise margin



The Tunneling Field Effect Transistor (TFET) as an Add-on for Ultra-Low-Voltage Analog and Digital Processes

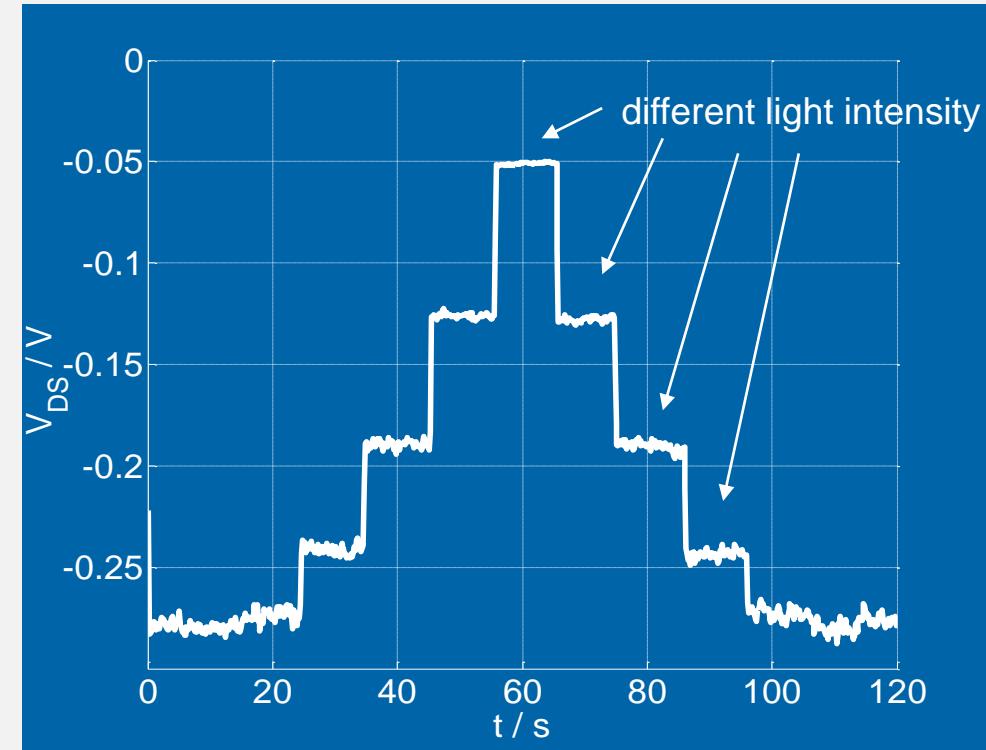
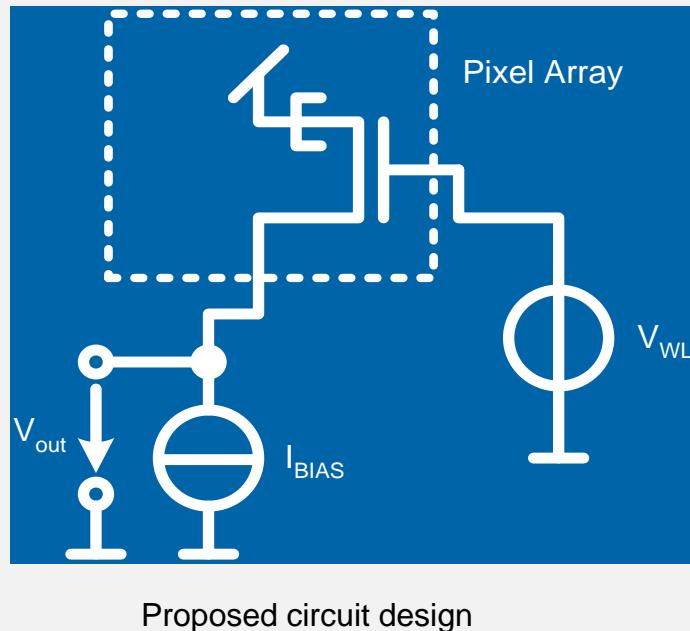
Th. Nirschl<sup>1,2</sup>, P.-F. Wang<sup>1,2</sup>, C. Weber<sup>3</sup>, J. Sedlmeir<sup>3</sup>, R. Heinrich<sup>3</sup>, R. Kakoschke<sup>4</sup>, K. Schräfer<sup>4</sup>, J. Holz<sup>4</sup>, C. Pacha<sup>5</sup>, T. Schulz<sup>5</sup>, M. Ostermayer<sup>2</sup>, A. Olbrich<sup>2</sup>, G. Georgakos<sup>2</sup>, E. Ruderer<sup>6</sup>, W. Hansch<sup>1</sup>, D. Schmitt-Landsiedel<sup>1</sup>

<sup>1</sup>Institute for Technical Electronics, Technical University Munich, Germany  
Theresienstrasse 90, 80290 Munich, Germany, Thomas.nirschl@tum.de, Tel.: +49 89 289 22908, Fax.: +49 89 289 22938  
<sup>2</sup><sup>4</sup>Infineon Technologies AG, Munich Germany

<sup>3</sup>Corporate Logic, <sup>5</sup>Parameter Extraction, <sup>6</sup>Technology Pre-Development, <sup>5</sup>Corporate Research, <sup>6</sup>Technology Integration

## 1 Transistor Photo Pixel Cell suitable for low cost applications:

- Due to the pin structure of the device it is very sensitive to ambient light, therefore the ETFET can be used as a photo detector and for addressing itself within a pixel array at the same time.
- The evaluated signal is  $V_{DS}$ , which changes with a change in illumination.



## Simulation of optimized structure

similar technological requirements as double gate MOSFETs:

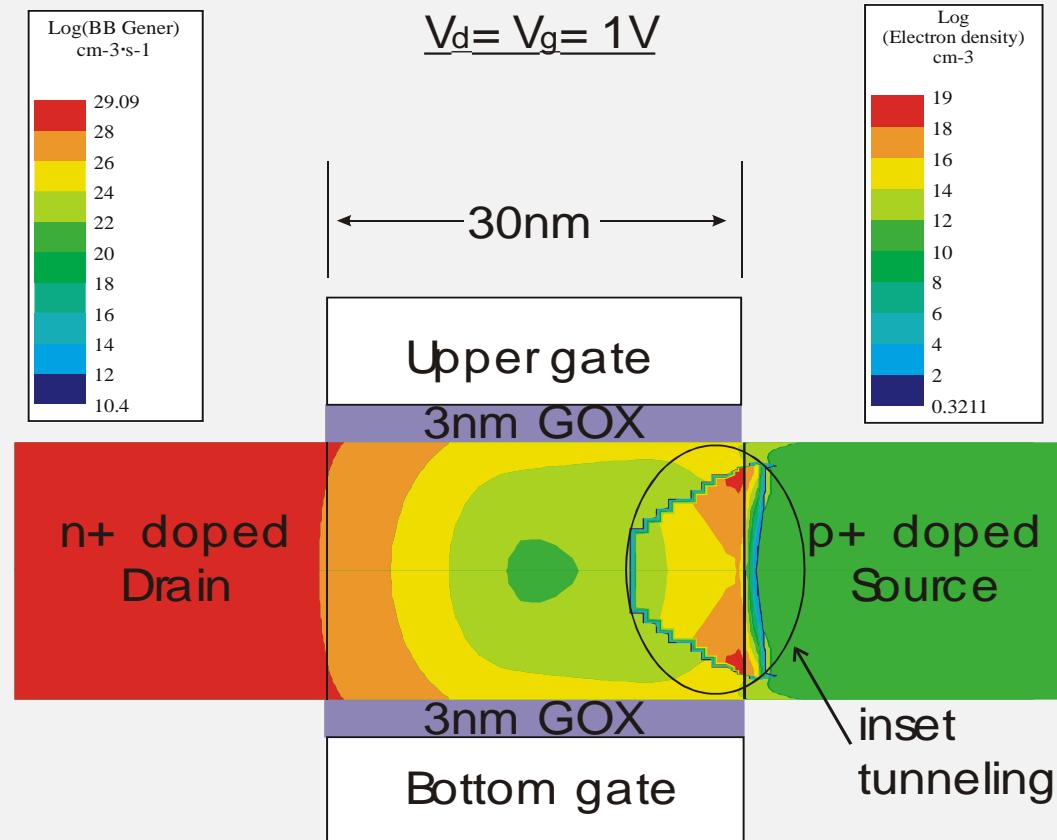
- abrupt doping profiles
- thin gate oxide
- thin silicon film

$T_{Si}$  is 20 nm,  $T_{ox}$  is 3 nm, and  $L_g$  is 30 nm.

Source:  $p^+ 1 \times 10^{20} \text{ cm}^{-3}$ .

Drain:  $n^+ 1 \times 10^{19} \text{ cm}^{-3}$ .

Channel: intrinsic silicon



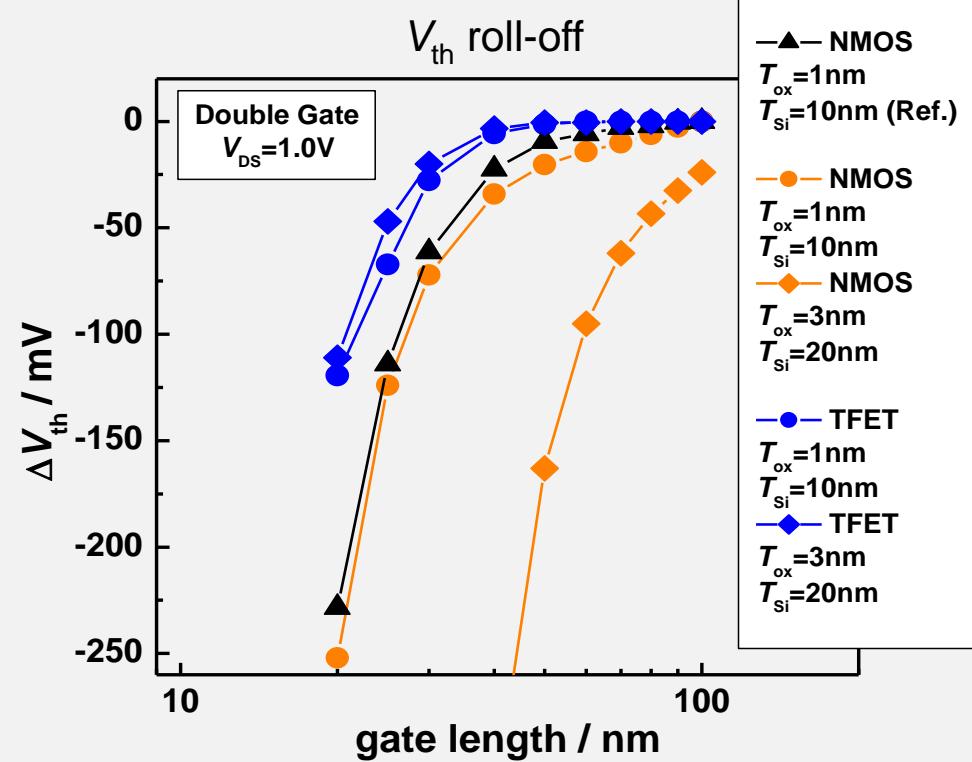
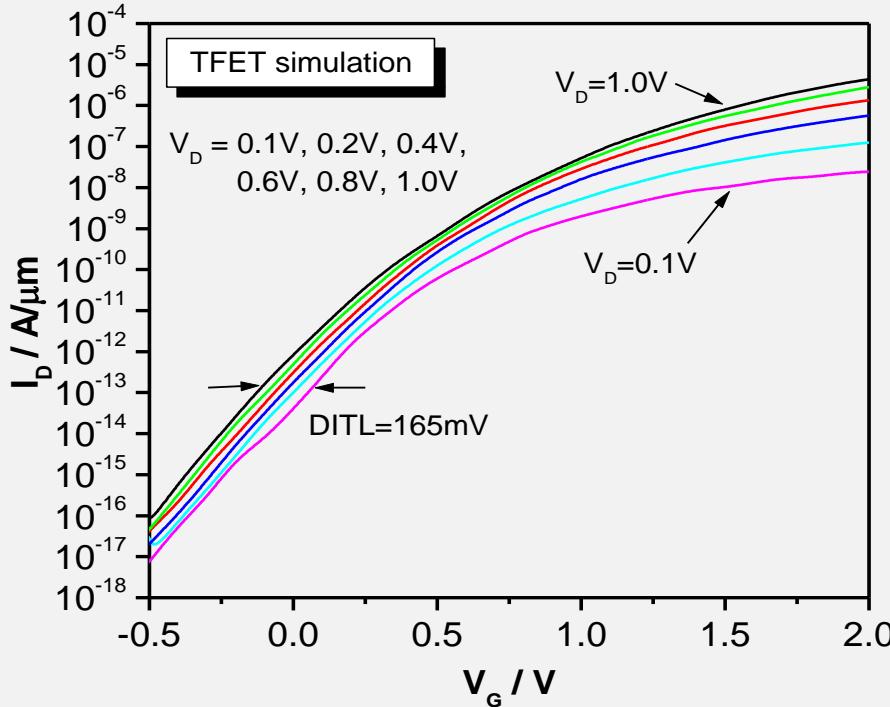
Wang et al., Solid-State Electronics, 2003

$T_{Si}$  is 20 nm,  $T_{ox}$  is 3 nm, and  $L_g$  is 30 nm.

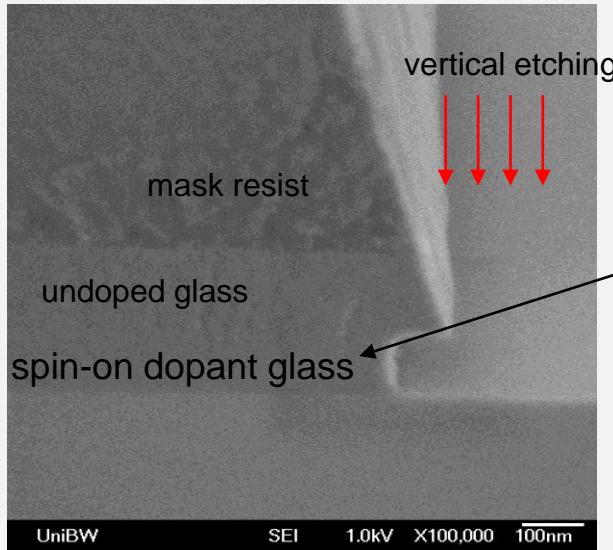
Source:  $p^+ 1 \times 10^{20} \text{ cm}^{-3}$ .

Drain:  $n^+ 1 \times 10^{19} \text{ cm}^{-3}$ .

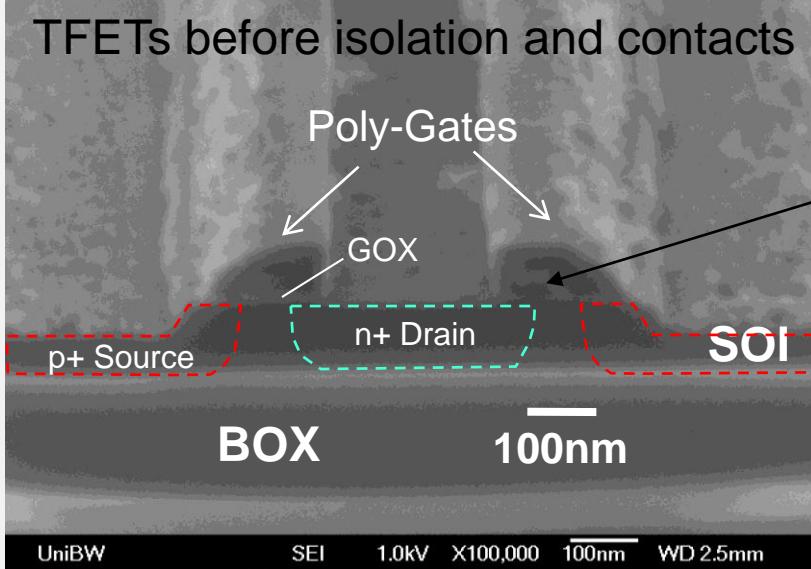
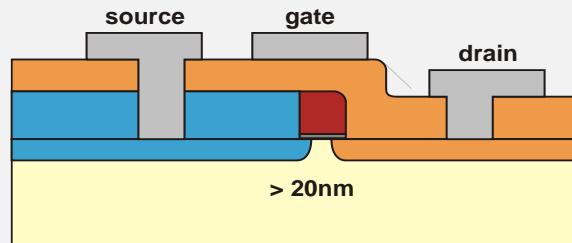
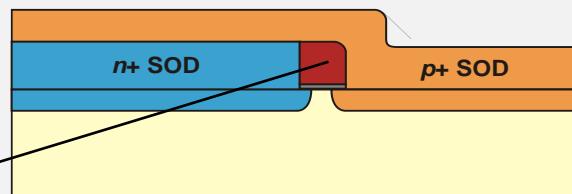
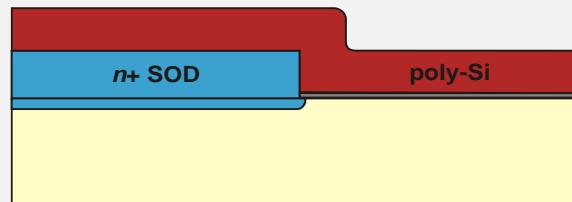
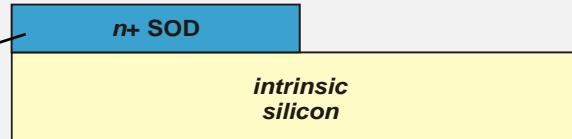
Channel: intrinsic silicon



- Low  $I_{off}$  with  $L_g = 30 \text{ nm}$
- Reduced  $V_{th}$  roll-off (no high- $k$  needed)



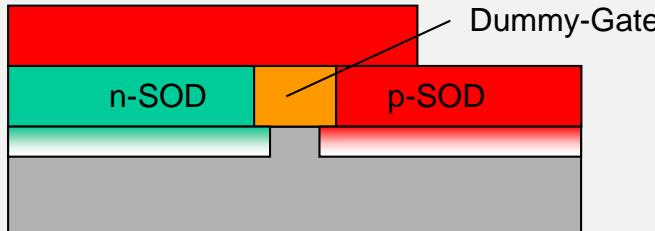
Spacer-Gate Technology:



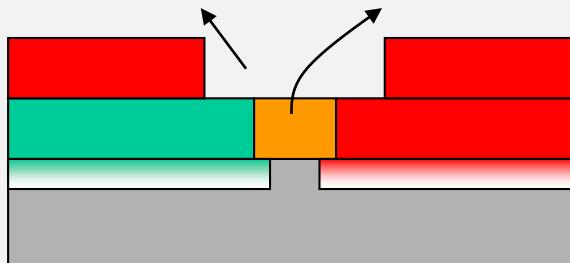
Channel length adjustable by process parameters down to 0 nm

### Replacement-Gates

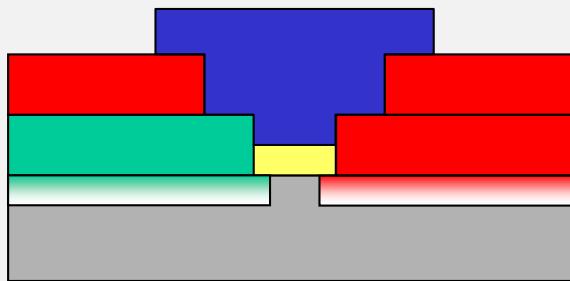
with SOD  
or etching  
+ new isolation



etch or CMP  
+  
sel. etching  
of Dummy-Gate



Fill-in  
Gate dielectrics  
(SiO2, high-k)  
+ metal



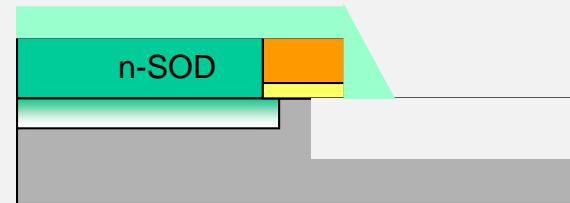
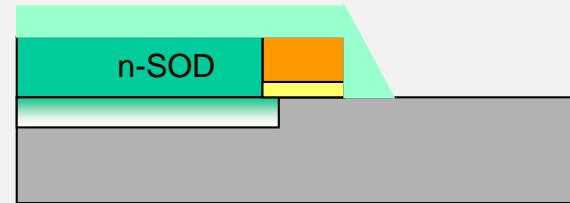
Reduction of thermal budget

new high-k

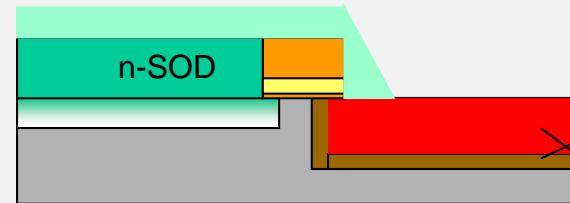
new Gate Metals

### $I_{on}$ - improvement

masked spacer deposition  
(Nitrid)



isotropical  
backetch



CVD (e.g. selective epitaxy)  
low doped SiGe  
+  
CVD high doped p-Si

SiGe at tunneling position

abrupt doping profil

high n+/p+ Si-barrier

**SEMICONDUCTOR FABTECH**  **TOKYO ELECTRON**

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**infineon**  
Never stop thinking

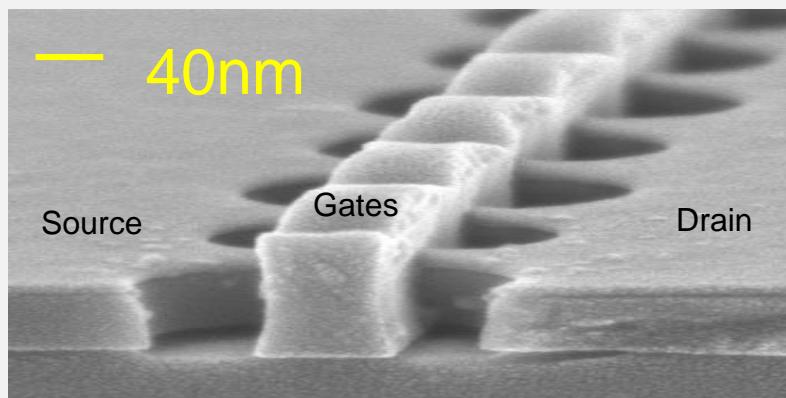
Sections  
Special Features  
Job Management

**Infineon demonstrated new tunneling Field Effect Transistors**

Friday, 04 February 2005

At the 2004 IEEE International Electron Devices Meeting (IEDM) in San Francisco (December 13 - 15, 2004) scientists from Infineon Technologies AG (FSE/NYSE: IFX) introduced several papers representing outstanding achievements each. Together with the Technical University of Munich the company presented a new scalable transistor concept enabling low voltage digital and analog circuits. For the first time ever, complementary Tunneling Field Effect Transistors (TFETs) are fabricated in a standard silicon process with good performance for static and dynamic parameters. "This is an important milestone on the way to transfer TFET research results into industrial products," says Dr. Michael Riehn, Vice President of Technology at Infineon.

Print E-mail



## Fabrication, Optimization and Application of Complementary Multiple-Gate Tunneling FETs

M. Fulde\*, A. Heigl†, M. Weis\*, M. Wirschofer\*, K. v. Arnim‡, Th. Nirschl‡, M. Sterkel\*, G. Knoblinger§, W. Hansch\*, G. Wachutka† and D. Schmitt-Landsiedel\*

\*Institute for Technical Electronics, Technical University Munich, Germany

†Institute for Physics of Electrotechnology, Technical University Munich, Germany

‡Infineon Technologies AG, Neuberg, Germany

§Infineon Technologies AG, Villach, Austria

Email: fulde@tum.de

TFET Multi-Gate devices,  
fabricated at IMEC in 2006



Note: !!! FinFET used by INTEL in 2011 !!!

## Fabrication, Optimization and Application of Complementary Multiple-Gate Tunneling FETs

M. Fulde\*, A. Heigl†, M. Weis\*, M. Wirnhofer\*, K. v. Arnim†, Th. Nirschl‡, M. Sterkel\*, G. Knoblinger§, W. Hansch\*, G. Wachutka† and D. Schmitt-Landsiedel\*

\*Institute for Technical Electronics, Technical University Munich, Germany

†Institute for Physics of Electrotechnology, Technical University Munich, Germany

‡Infineon Technologies AG, Neubiberg, Germany

§Infineon Technologies AG, Villach, Austria

Email: fulke@tum.de

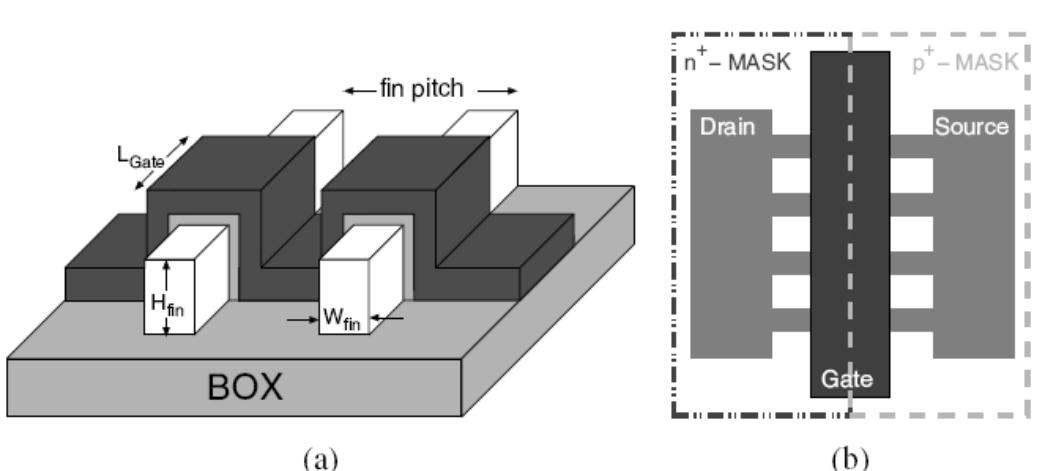


Fig. 2. Schematic view of MuGFET structure and MuGTFET implementation.

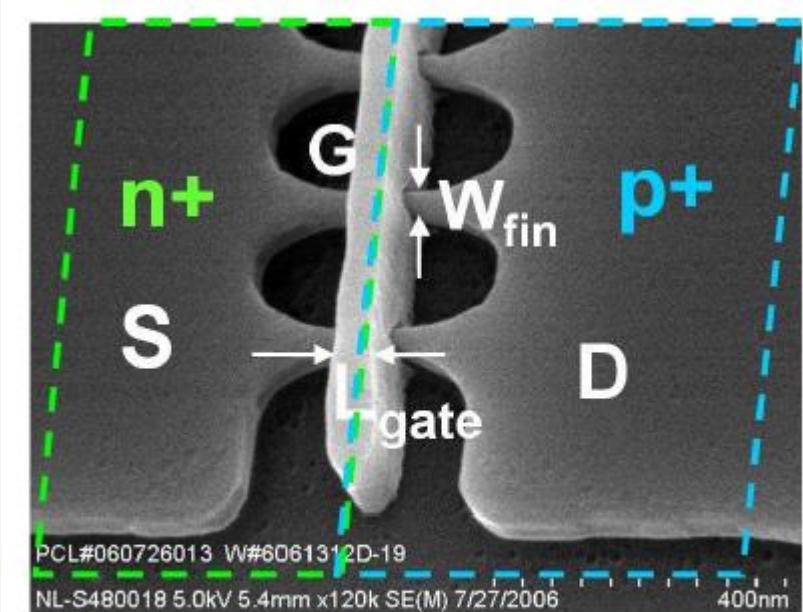
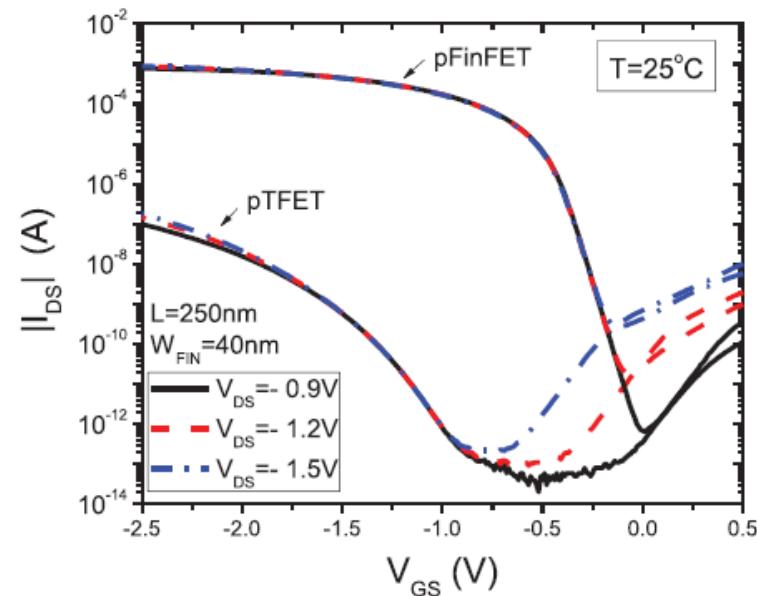


Fig. 3. SEM picture of realized T-MuGFET

## Experimental Comparison Between Trigate p-TFET and p-FinFET Analog Performance as a Function of Temperature

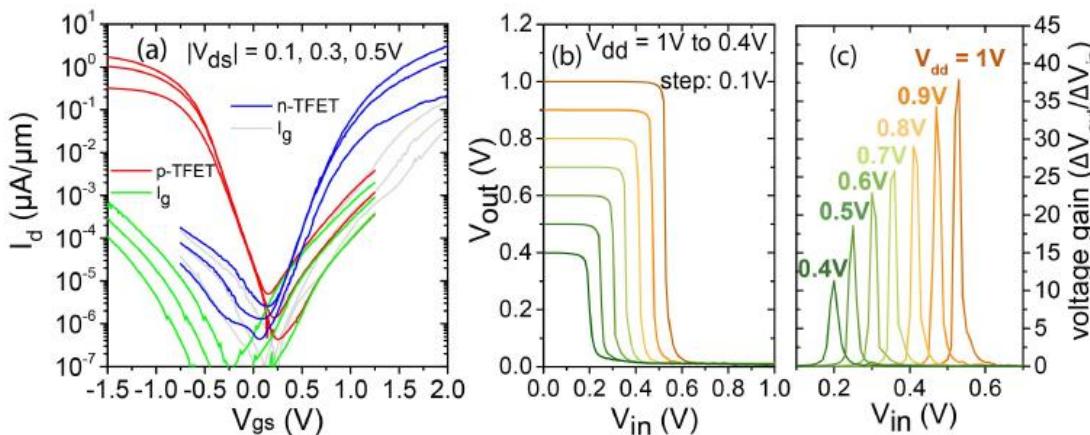
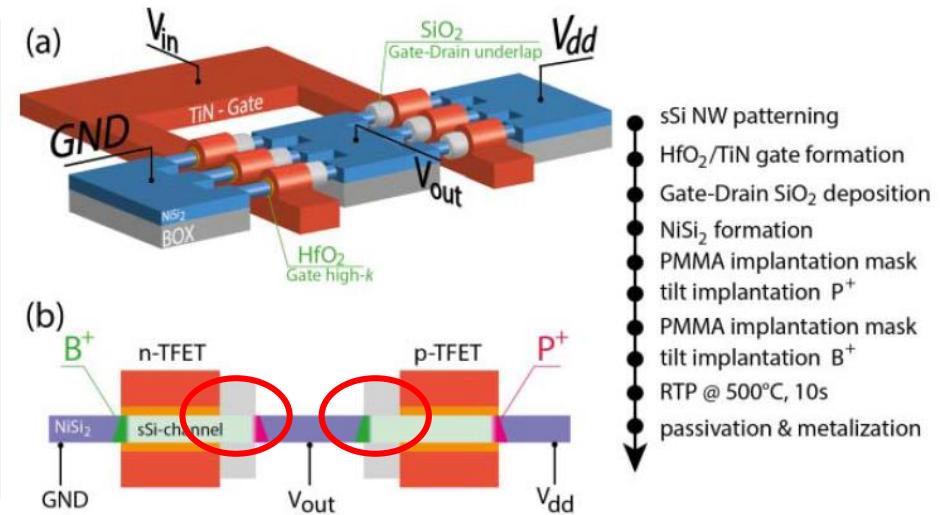
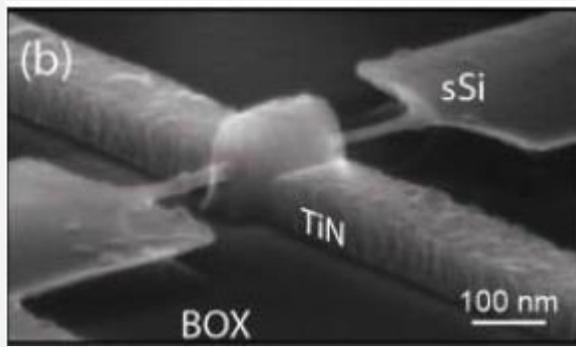
Paula Ghedini Der Agopian, *Member, IEEE*, João Antonio Martino, *Senior Member, IEEE*, Rita Rooyackers, Anne Vandooren, Eddy Simoen, and Cor Claeys, *Fellow, IEEE* 2013



- Both transistors fabricated in the same technology node
- TFET has a low on-current compared to the FinFET
- More investigation needed to get a higher on-current, suppression of ambipolarity
- If TFET will come then as Gate-All-Around-FET or in Monolithic 3D-Integration

# Complementary Strained Si GAA Nanowire TFET Inverter With Suppressed Ambipolarity

G. V. Luong, K. Narimani, A. T. Tiedemann, P. Bernardy, S. Trellenkamp,  
Q. T. Zhao, Member, IEEE, and S. Mantl, Member, IEEE 2016

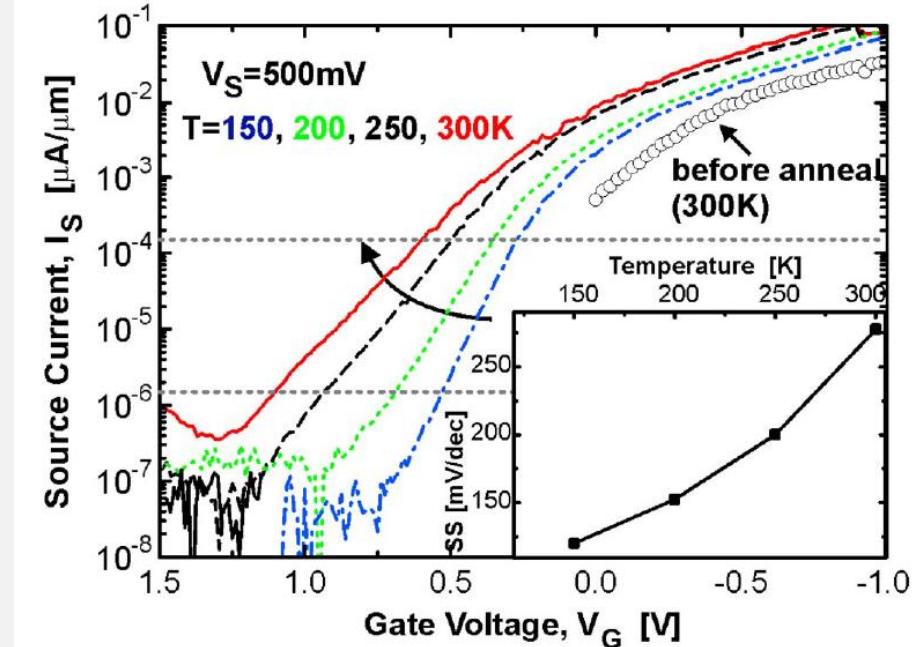
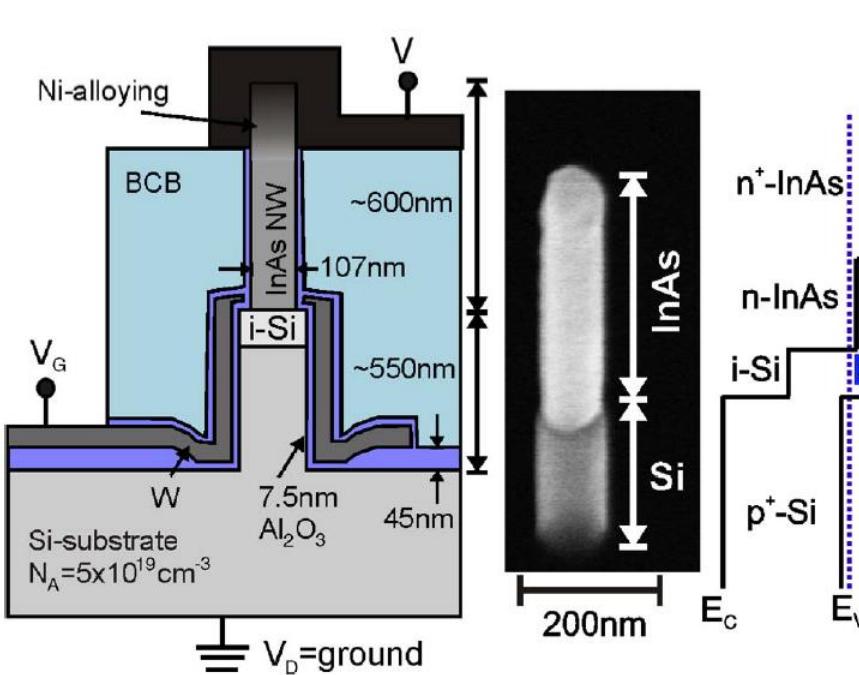
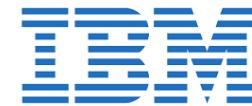


- CTFET as Gate-All-Around-FET
- Inverter shows good characteristics
- On-current still too low (50 NWs)

# InAs–Si Nanowire Heterojunction Tunnel FETs

K. E. Moselund, *Member, IEEE*, H. Schmid, *Member, IEEE*, C. Bessire, M. T. Björk,  
H. Ghoneim, *Student Member, IEEE*, and H. Riel, *Senior Member, IEEE*

2012



Vertical Nanowire with Gate-All-Around



InAs in the Source to achieve higher on-currents



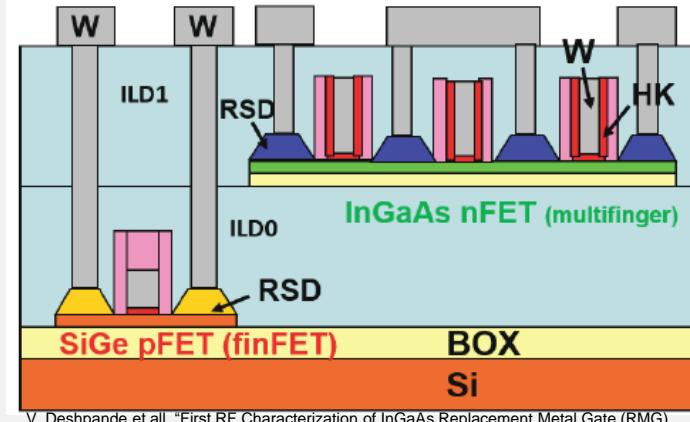
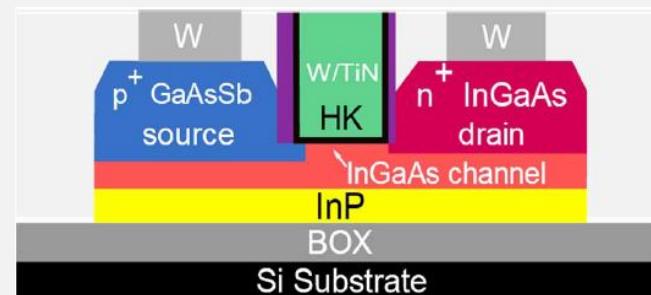
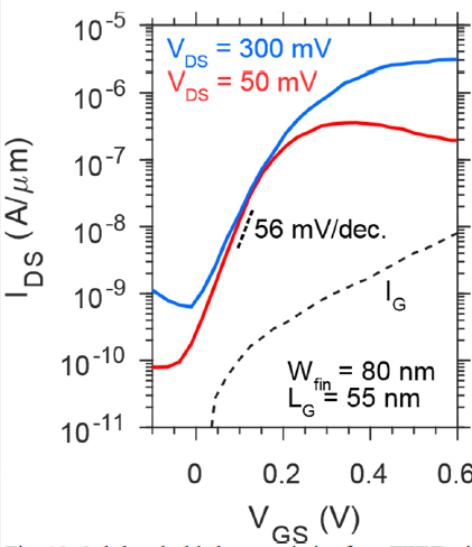
Vertical Gate-All-Around TFETs are working but the current is still low

## Sub-Thermionic Scalable III-V Tunnel Field-Effect Transistors Integrated on Si (100) IEE 2019

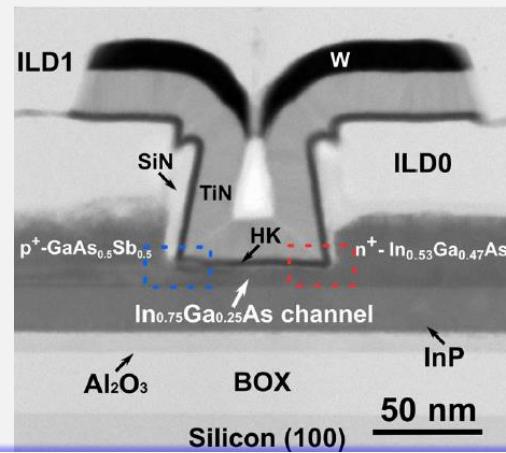
C. Convertino<sup>1</sup>, C. B. Zota<sup>1</sup>, Y. Baumgartner<sup>1</sup>, P. Staudinger<sup>1</sup>, M. Sousa<sup>1</sup>, S. Mauthe<sup>1</sup>, D. Caimi<sup>1</sup>, L. Czornomaz<sup>1</sup>, A. M. Ionescu<sup>2</sup> and K. E. Moselund<sup>1</sup>

<sup>1</sup> IBM Research Zurich, Saumerstrasse 3, Ruschlikon, Switzerland, email: [ino@zurich.ibm.com](mailto:ino@zurich.ibm.com)

<sup>2</sup>École polytechnique fédérale de Lausanne EPFL, Switzerland



V. Deshpande et al., "First RF Characterization of InGaAs Replacement Metal Gate (RMG) nFETs on SiGe-OI FinFETs Fabricated by 3D Monolithic Integration, IEEE 2016



III-V materials have the advantage of high tunneling efficiency (direct band gap, small effective mass)

Process can be used for monolithic 3D-Integration

Low subthreshold slope, low on-current

- ***Working principle of TFET:***
  - Gate controlled band to band tunneling
- ***Conditions for the high performance TFET:***
  - Sharp doping profile
  - Thin gate oxide/high-k
  - High drain doping level
- ***Performance of the optimized structure:***
  - Sub-threshold swing  $\sim 60$  mV / dec with 3 nm gate oxide
  - 8 orders of magnitude current gain at -0.5V supply voltage
  - low leakage current  $\sim 10^{-15}$  A/ $\mu$ m
- ***Problem to be solved***
  - further increase of  $I_{on}$
  - Gate delay scales with  $CV / I$
  - > gate capacitance must be reduced for low current and voltages
  - Ambipolarity

## 8.1 Introduction

Overview of Tunneling Transistors  
Tunneling in MOSFETs

## 8.2 The Esaki-Tunneling MOSFET

Esaki-Tunneling, Esaki-Diode  
Esaki-Tunneling MOSFET

## 8.3 Coulomb Blockade Devices

CMOS Roadmap to Single-Electron MOSFETs  
Nanotechnology  
Physics of Coulomb Blockade  
Coulomb Blockade Devices  
Single Electron Transistor  
Single Electron Memory and Logic

Looking at the CMOS future:

[http://public.itrs.net/files/1999\\_SIA\\_roadmap/home.htm](http://public.itrs.net/files/1999_SIA_roadmap/home.htm)

**MEMORY AND LOGIC**

Table 28a Memory and Logic Technology Requirements—Near Term      Logic Technology Requirements—Long Term

	YEAR TECHNOLOGY NODE	1999 180 nm	2000	2001	2002 130 nm	2003	2004	2005 100 nm	2008 70 nm	2011 50 nm	2014 35 nm	DRIVER
1	DRAM $\frac{1}{2}$ Pitch (nm)	180	165	150	130	120	110	100	70	50	35	
2	MPU Gate Length (nm)	140	120	100	85	80	70	65	45	32	22	
3	MPU / ASIC $\frac{1}{2}$ (nm)	230	210	180	160	145	130	115	80	55	40	
4	ASIC Gate Length (nm)	180	165	150	130	120	110	100	70	50	35	
5	Minimum logic $V_{dd}$ (V) (desktop)	1.5–1.8	1.5–1.8	1.2–1.5	1.2–1.5	1.2–1.5	0.9–1.2	0.9–1.2	0.6–0.9	0.5–0.6	0.3–0.6	M Gate
6	$T_{ox}$ equivalent (nm)	1.9–2.5	1.9–2.5	1.5–1.9	1.5–1.9	1.5–1.9	1.2–1.5	1.0–1.5	0.8–1.2	0.6–0.8	0.5–0.6	M Gate
7	Nominal $I_{on}$ at 25 °C ( $\mu$ A/ $\mu$ m) [NMOS/PMOS] high performance	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350	750/350	M Gate
8	Maximum $I_{off}$ at 25 °C (nA/ $\mu$ m) (For minimum L device) high performance	5	7	8	10	13	16	20	40	80	160	M Gate
9	Gate delay metric CV/I (ps) high-performance	11	9.4	8.6	7.3	6.9	6.1	5.7	3.7	2.6	2.4	
10	Percent static power reduction necessary due to innovative circuit/system design	0	33	48	55	71	77	81	M GATE M & A $\frac{1}{2}$			
11	Nominal $I_{on}$ at 25 °C ( $\mu$ A/ $\mu$ m) [NMOS/PMOS] low power	490/230	490/230	490/230	490/230	490/230	490/230	490/230	A GATE			
12	Maximum $I_{off}$ at 25 °C (pA/ $\mu$ m) (For minimum L device) low power	5	7	8	10	13	16	20	A GATE			
13	Gate delay metric CV/I (ps) low power	18	16	13	11.2	10.7	8.8	8.2				

The on-current of CMOS will stay constant at 750 $\mu$ A/ $\mu$ m gate width.

Why ?

\* Scaling devices by a factor  $S > 1$  results in scaled geometries  $L' = L / S$  and as a result absolute drain current scales the same  $I_D' = I_D / S$   
 -> in a scaled device the drain current per gate length  $w$  will keep constant:  $(I_D/w)' = (I_D/S) / (w/S) = I_D / w$

\* The absolute value of 750 $\mu$ A/ $\mu$ m (n-MOS) is a trade-off between high drive capability and power consumption

What is the extrapolation when keeping  $750\mu\text{A}/\mu\text{m}$  and shrinking dimensions ?



- 1 A MOS-channel may be fabricated with minimum feature size F.  
The geometry of the channel will be: channel length  $L=F$ , channel width  $w=F$

- 2 Electrons move in a MOS-channel with maximum velocity  $\sim 10^7\text{cm/sec}$

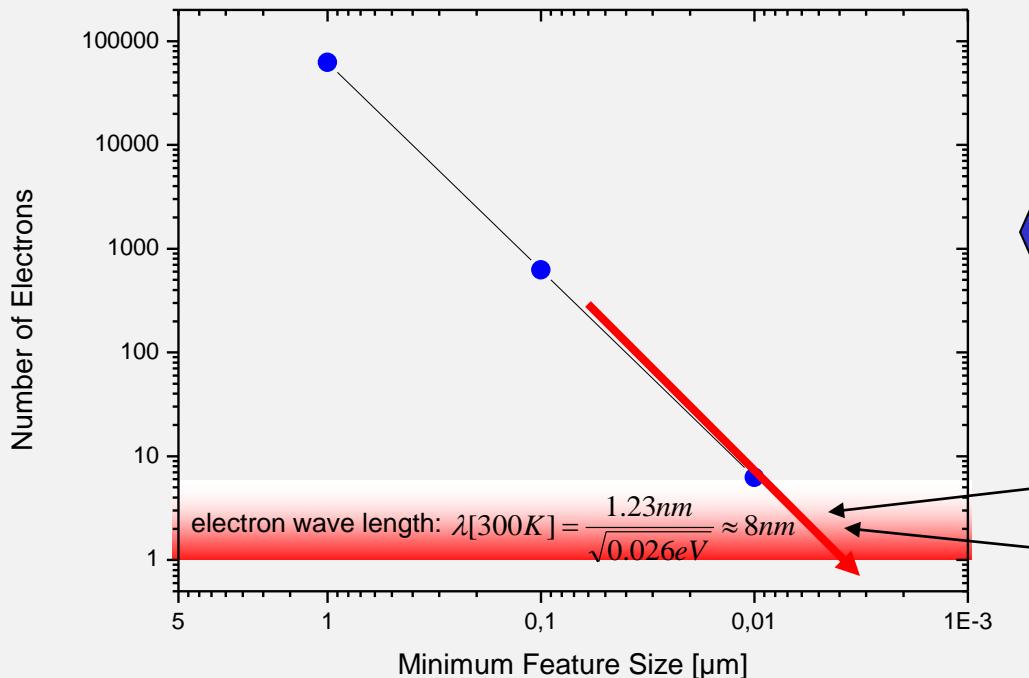
3 the transit time for an electron:

$$t_{\text{transit}} = \frac{L}{v} = \frac{L}{10^7\text{cm/sec}}$$

- 4 The moved charge can be calculated from the current:

$$Q = I \cdot t_{\text{transit}}$$

- 5 Calculating the number of channel electrons:



$L$	$t_{\text{transit}}$ [sec]	$Q=I \cdot t$ [Cb]	Number of electrons
$1\mu\text{m}$	$10^{-11}$	$7.5 \cdot 10^{-15}$	46'875
$100\text{ nm}$	$10^{-12}$	$7.5 \cdot 10^{-17}$	468
$10\text{ nm}$	$10^{-13}$	$7.5 \cdot 10^{-19}$	4.7

With feature size  $\sim 10\text{nm}$  we reach:

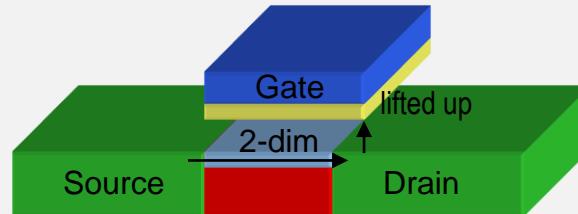
\* region of single-electron transport  
  
 \* Quantum mechanics  
 (feature size  $\sim$  wave length of electrons)

With the development of **electron-beam lithography** research labs start to investigate **low-dimensional systems** (~1980).

Starting point:

We need geometries of a few Nanometer !

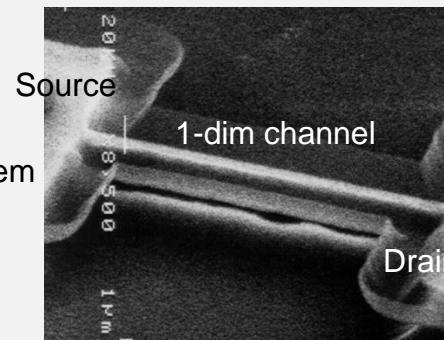
2-dim



A conventional MOSFET already inhibits a 2-dim electron gas  
-> the channel with a thickness of ~ 5nm

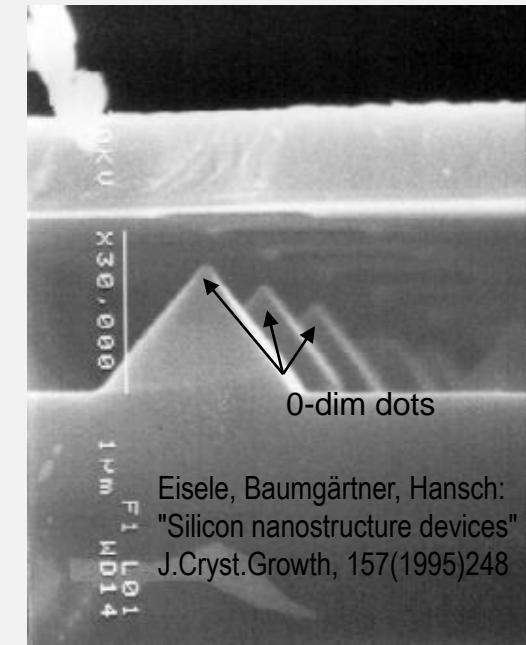
1-dim

Just reducing width is easy by e-beam,  
relaxed adjustment and no contact problem



0-dim

Reducing length and width to receive dot structures  
is really difficult because of adjustment and contacts



Eisele, Baumgärtner, Hansch:  
"Silicon nanostructure devices"  
J.Cryst.Growth, 157(1995)248

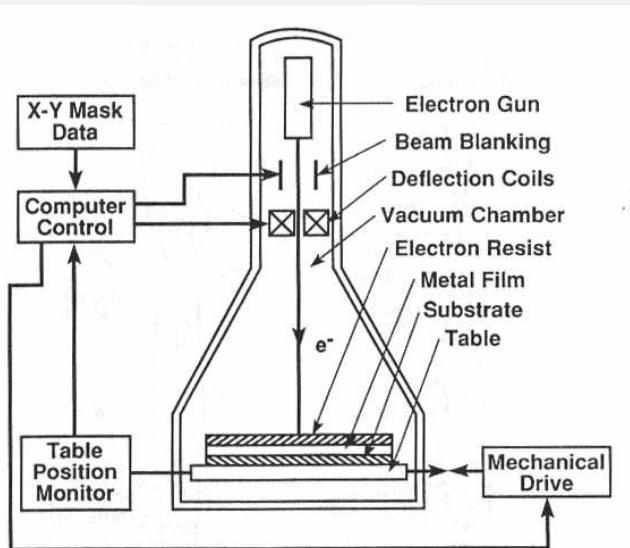


Figure 67. Schematic of an electron-beam exposure system.

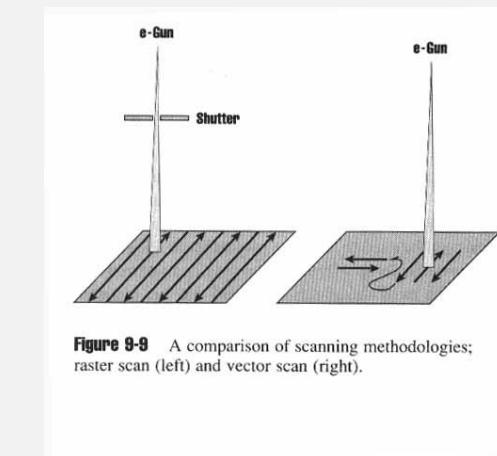
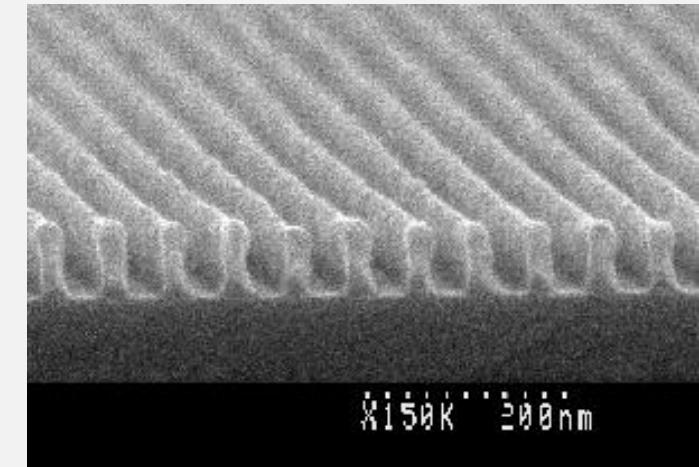


Figure 9-8 A comparison of scanning methodologies; raster scan (left) and vector scan (right).



[www.elec.gla.ac.uk/knt/kntbeam\\_examples.html](http://www.elec.gla.ac.uk/knt/kntbeam_examples.html)

Year 2010 :

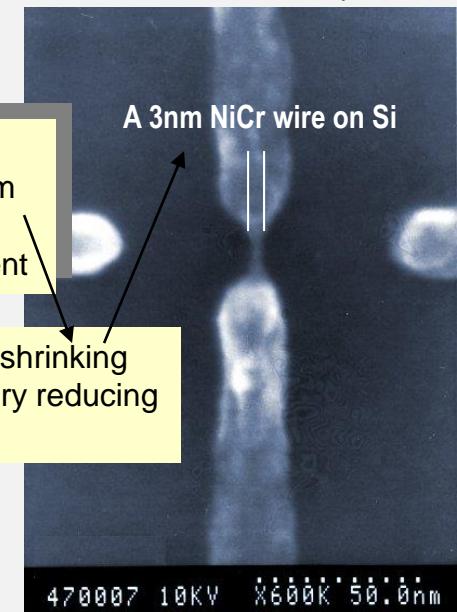
- \* minimum feature size in industrial application is ~ 30nm
- \* writing of one layer of 30nm pattern in  $10^9$  devices  
-> 100 sec / layer may be ok, but no time for adjustment

E-beam lithography system  
LEICA EBMF

- > 80nm structures
- > maximum writing speed: 10MHz ->  $10^{-7}$  sec/point

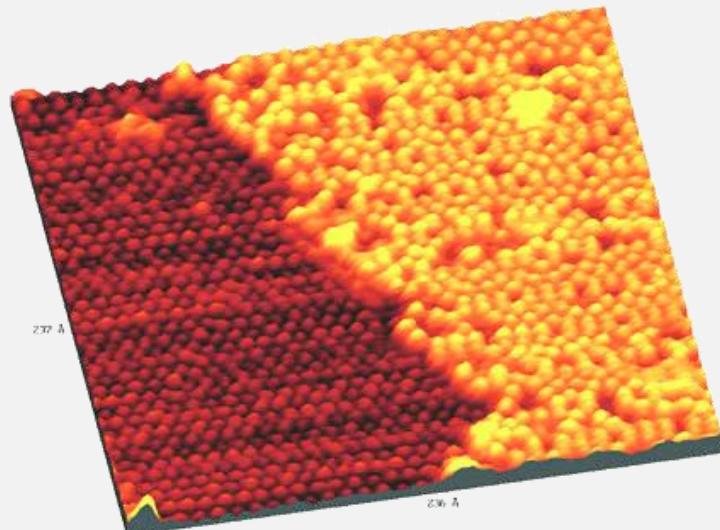
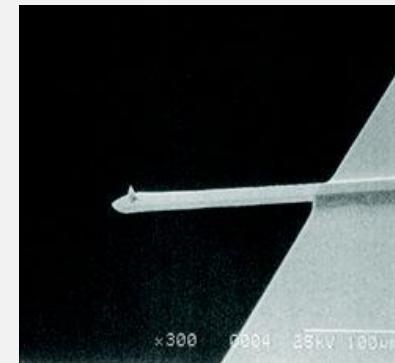
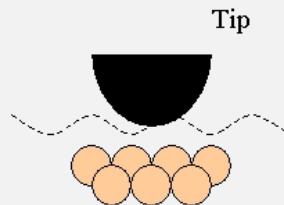
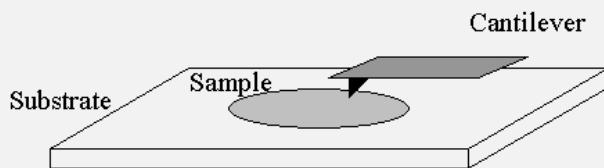
[www.micro.uiuc.edu/equipmentdescriptions/](http://www.micro.uiuc.edu/equipmentdescriptions/)

Additional shrinking  
by geometry reducing  
processes

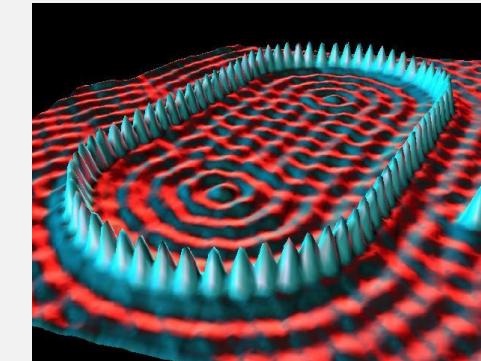
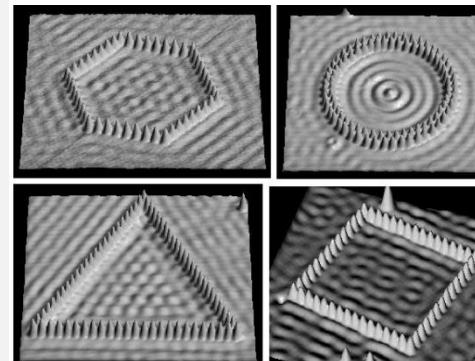


470007 10KV x600K 50.0nm

Tunneling Microscopy: 1986 by IBM



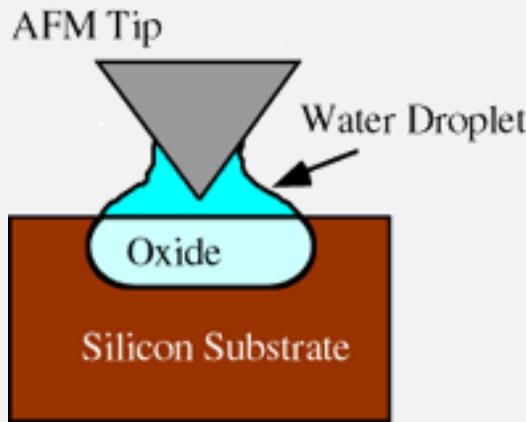
UHV STM image of iron silicide on Si(111)  
([www.rhk-tech.com/hall/ironsilicide.html](http://www.rhk-tech.com/hall/ironsilicide.html))



Artificial "corrals" of Fe-atoms on Cu(111) using STM  
Image originally created by IBM Corporation



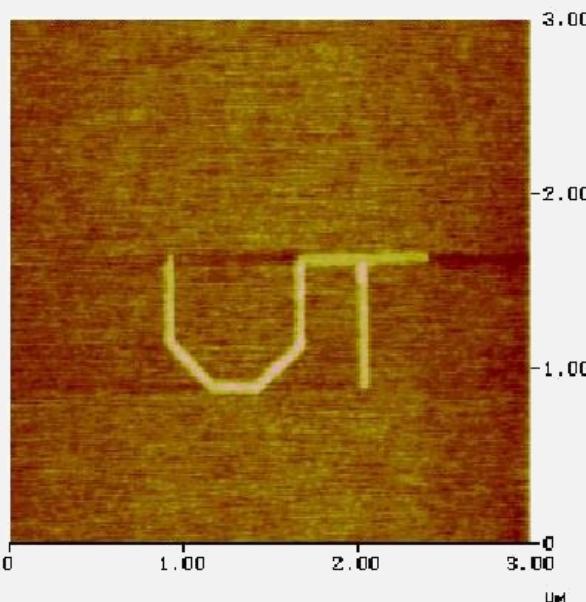
With STM (and followers like AFM) single atom resolution and positioning was achieved



In 1990, J.A. Dagata et al.(Appl. Phys. Lett 56, 2001 (1990)), reported that an electrical bias placed on an STM tip could oxidize hydrogen passivated silicon. Since then it has been shown that a conducting AFM tip under electrical bias could oxidize silicon as well, and that both methods could oxidize metal films such as Ti, Al, and Nb.

These oxides have since been used as a lithography mask or as current transport barriers to form electron devices with dimensions as small as 10nm.

With these small dimensions it has been possible to create single electron transistors operating at room temperature, the first group to do this was K. Matsumoto et al. in 1995 using Ti films (Appl. Phys. Lett 68, 34 (1996)).



Oxidation lines on Si by Atomic Force Microscope  
(the lines are ~ 50nm width)

[www.ph.utexas.edu/~nemrg/nanolith.html](http://www.ph.utexas.edu/~nemrg/nanolith.html)

Year 2013:  
\* minimum feature size: ~ 20nm  
width of contacts ~ 50nm

VOLUME 62, NUMBER 5

PHYSICAL REVIEW LETTERS

30 JANUARY 1989

**Conductance Oscillations Periodic in the Density of a One-Dimensional Electron Gas**

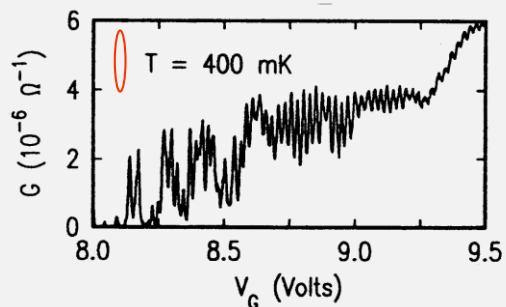
J. H. F. Scott-Thomas,<sup>(a)</sup> Stuart B. Field,<sup>(a)</sup> M. A. Kastner,<sup>(a)</sup> Henry I. Smith,<sup>(b)</sup> and D. A. Antoniadis<sup>(b)</sup>

Research Laboratory of Electronics, Massachusetts Institute of Technology, Cambridge, Massachusetts 02139  
(Received 18 November 1988)

By use of x-ray lithography Si inversion layers have been fabricated with width  $\sim 25$  nm and mobility  $\sim 15\,000 \text{ cm}^2/\text{V s}$ . These display oscillations in their conductance that are periodic in the number of electrons per unit length, even in zero magnetic field. The oscillations reflect an oscillatory activation energy of the conductance and are accompanied by unusual nonlinearities suggestive of pinned charge-density waves.

PACS numbers: 73.20.Dx, 71.45.Lr, 72.15.Ni

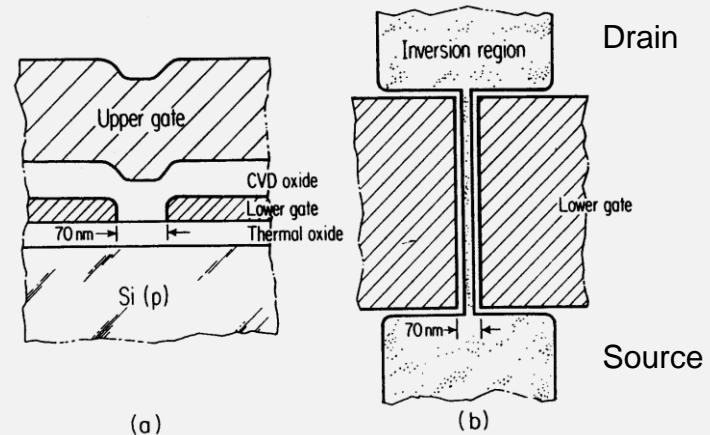
- 2 At extreme low temperatures ( $T < 1\text{K}$ ) equidistant oscillations in channel conductance were observed.



-> The authors believed in a Wigner-crystal (see chap. 7)

1

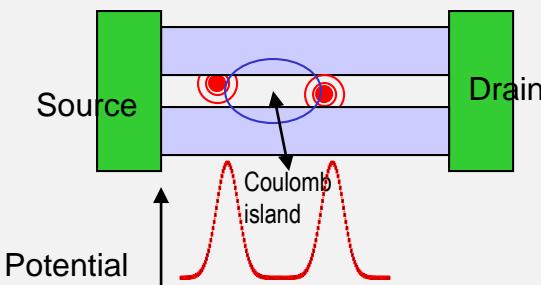
A MOSFET with a very narrow channel ( $w=25\text{nm}$ ) was fabricated.  
This results in a quasi 1d- inversion channel



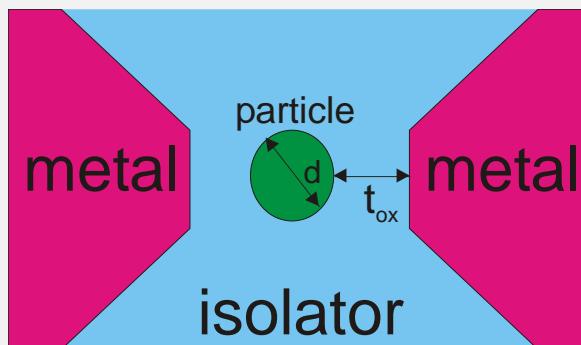
3

From Likharev et al. the correct interpretation was given:

Due to oxide charges ( $\sim 10^{10}\text{cm}^{-2}$ ) potential constrictions (= random tunnel barriers) were created



Principle:



A small particle is embedded in a isolator between two metal plates

Looking at the particle:

1

the particle forms a self-capacitance:

$$C = 2\pi\epsilon_0\epsilon \cdot d$$

for a spheric particle

2

if the capacitor is charged with  $Q$ , it creates a potential difference  $\Delta\varphi$  with the surroundings:

$$C = \frac{Q}{\Delta\varphi} = \frac{Q}{V}$$

3

the **electrostatic Coulomb-energy** of a charged capacitor is:

$$E_{coul} = \frac{1}{2}CV^2$$

Using eqs.2,3 the Coulomb-energy of a capacitor can be expressed:

$$E_{coul} = \frac{Q^2}{2C}$$



**the Coulomb-energy of a capacitor, charged with a single-electron is:**

$$E_{coul} = \frac{e^2}{2C}$$

If the charging of a capacitor should be controlled by a voltage of  $\sim 1V$  with single-electron precision, eq.2 delivers:

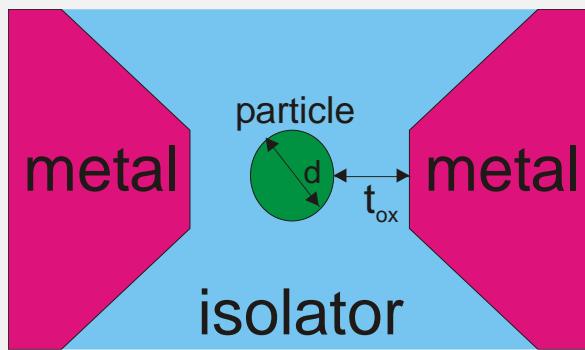
$$C = \frac{e}{V} = \frac{1.6 \cdot 10^{-19} As}{1V} \approx 10^{-19} F \approx 0.1 aF$$

With this capacitance the particle exhibits a diameter of (eq.1):

$$d = \frac{C}{2\pi\epsilon_0\epsilon} \approx \frac{10^{-19} F}{2\pi \cdot 8.85 \cdot 10^{-14} F/cm} \approx 10^{-7} cm \approx 1 nm$$



Single-electron handling requires nanometer particles with attoFarad (at  $\sim 1 V$  !)



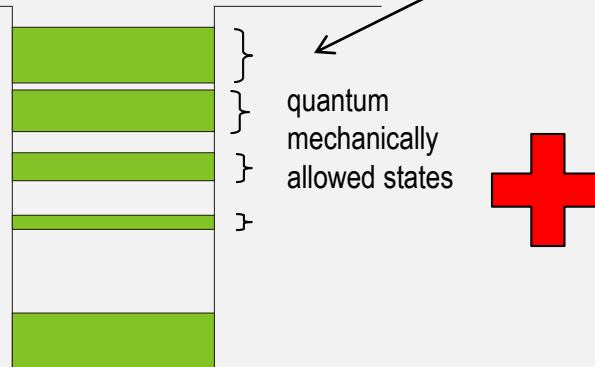
The energy of the particle (called **Coulomb-island**):

- 1 If the particle (with capacitance C) is charged with individual electrons, only discrete values of energy are allowed ( $n=1$  electron, 2 electrons, 3,...)

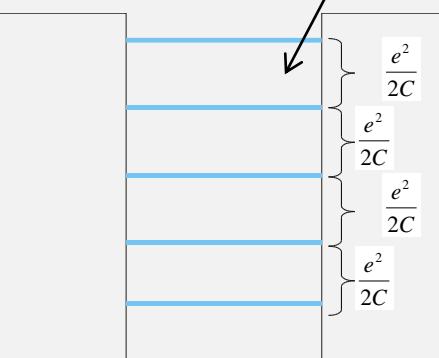
$$E_{coul} = n \cdot \frac{e^2}{2C}$$

These energy levels are **equidistant**

- 2 Because Coulomb-particles are very small (nm) an additional quantum-mechanical size quantization exists:



Quantum-mechanically  
size quantization  
**non-equidistant levels**

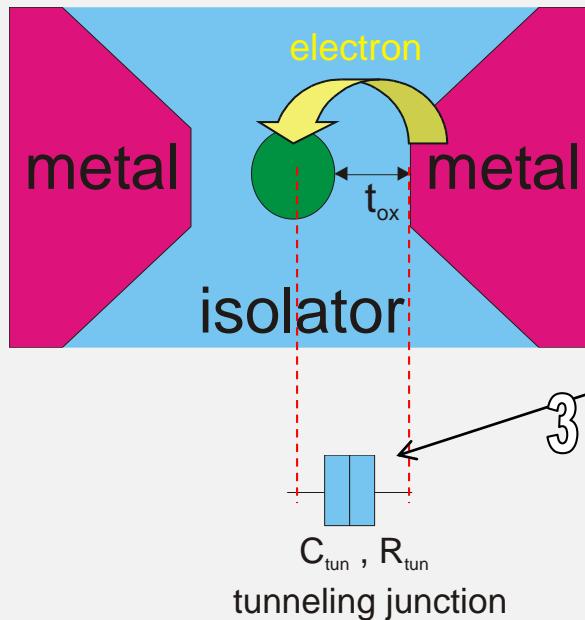


"Classical" energy separation due  
to electron charge quantization  
**equidistant levels**



result may be non-equidistant  
energy levels

In small particles a classical, equidistant Coulomb-ladder exists, which is usually overlaid by quantum-mechanically energy levels



1

Looking at the junction:  
if an electron should tunnel from the metal to the particle the tunneling barrier must be thinner than the electron wavelength:

$$\lambda = \frac{h}{p}$$

$$E_{kin} = \frac{1}{2}mv^2 = \frac{p^2}{2m} \approx kT = E_{therm}$$

$$\lambda(300K) \approx nm$$

2

the tunnel junction is described as a capacitor  $C_{tun}$  with an tunneling resistance  $R_{tun}$

3

Classically forbidden processes are possible due to Heisenberg's uncertainty relation:

$$\Delta E \cdot \Delta t > \frac{\hbar}{2}$$

for a charge fluctuation the characteristic time is about:

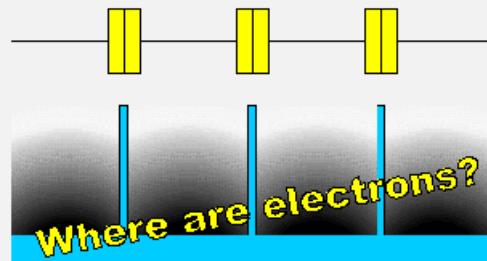
$$\Delta t \approx R_{tun} C_{tun}$$

$$\text{With: } \Delta E = \frac{e^2}{2C}$$

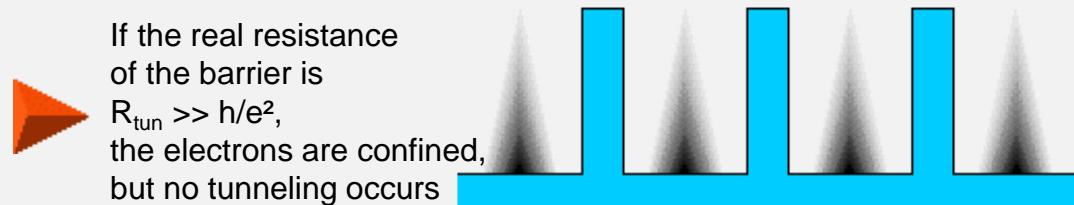
Using above equations the **universal resistance** of a tunneling junction is:

$$R_{tun} \geq \frac{\hbar}{e^2} = 25,8 \text{ k}\Omega$$

If the real resistance of the barrier is  $R_{tun} < h/e^2$ , no confinement exists



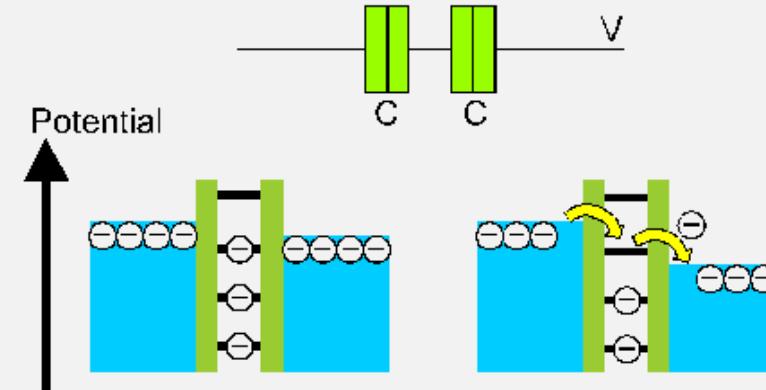
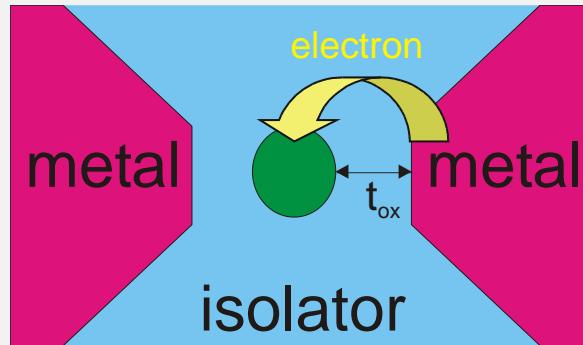
If the real resistance of the barrier is  $R_{tun} \gg h/e^2$ , the electrons are confined, but no tunneling occurs



The tunneling resistance must exceed the fundamental value of  $h/e^2$  to ensure confinement of the electrons

Double junction with Coulomb-island:

1



In a double-junction arrangement electrons can tunnel into the Coulomb-island if the energy levels are adjusted. Between the levels the electron tunneling is blockaded, this effect is called:

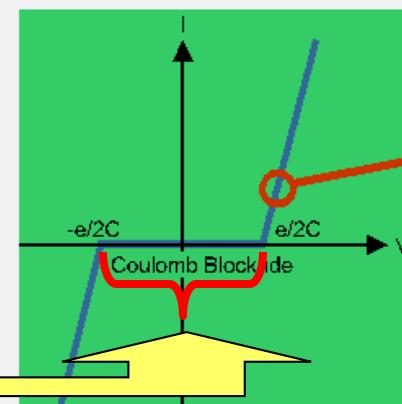
2

Coulomb-blockade results in

Tunneling of electrons change the potential right and left from the Coulomb-particle by:

$$\Delta V = \frac{\Delta Q}{C} = n \cdot \frac{e}{C}$$

### Coulomb-Blockade



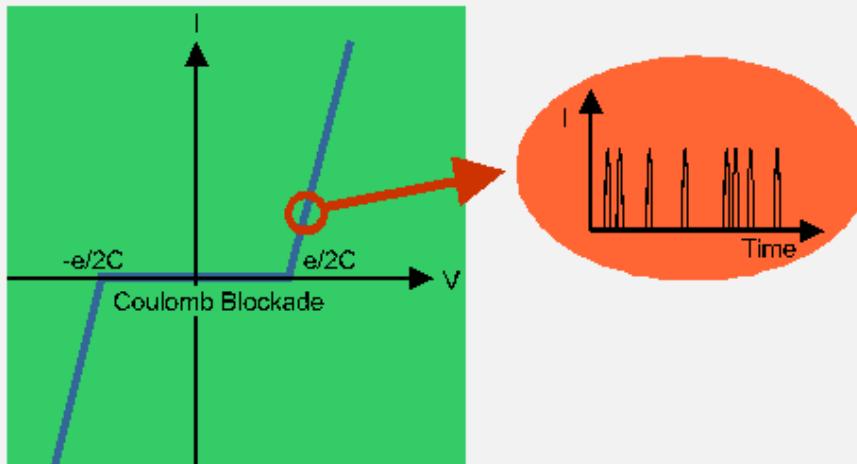
The average (time independent) tunneling rate:

$$\Gamma = \frac{\Delta E}{e^2 \cdot R_T \left[ 1 - \exp\left(-\frac{\Delta E}{kT}\right) \right]}$$

where the individual events are random distributed:

$$t_i = -\frac{1}{\Gamma} \cdot \ln(i)$$

i: random number (0 < i < 1)



Tunneling characteristics between two Coulomb-levels:

1) no current between

2) if level arrangement is achieved electron tunneling events take place.

The tunneling events are random in time.

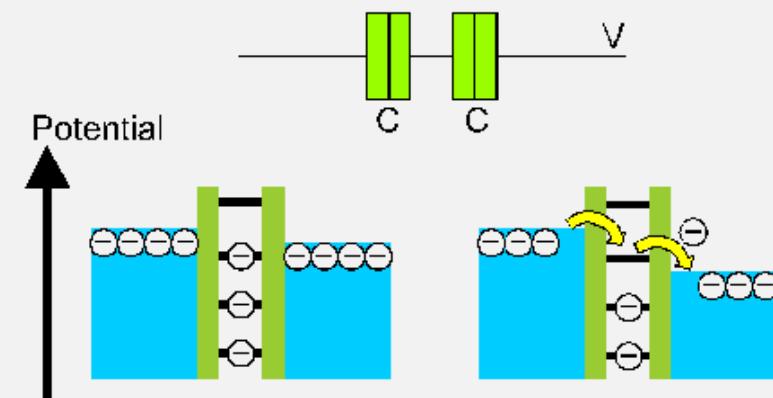
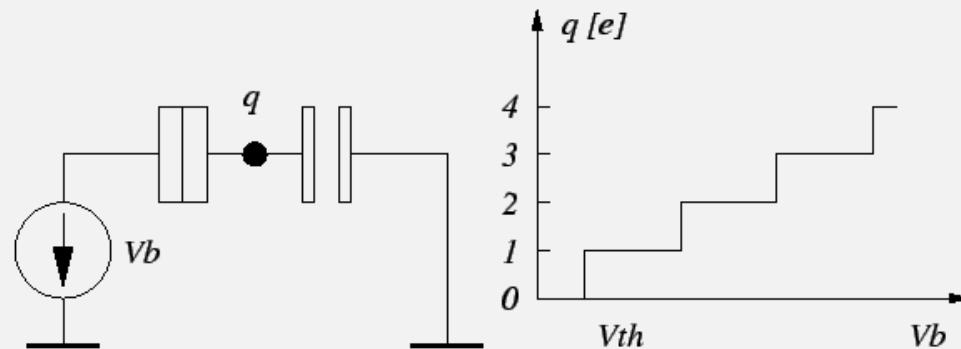
The mean time is dependent on the tunneling resistance.

If one electron tunnels out on one junction from the other junction another electron tunnels in immediately ( $10^{-14}$  sec).

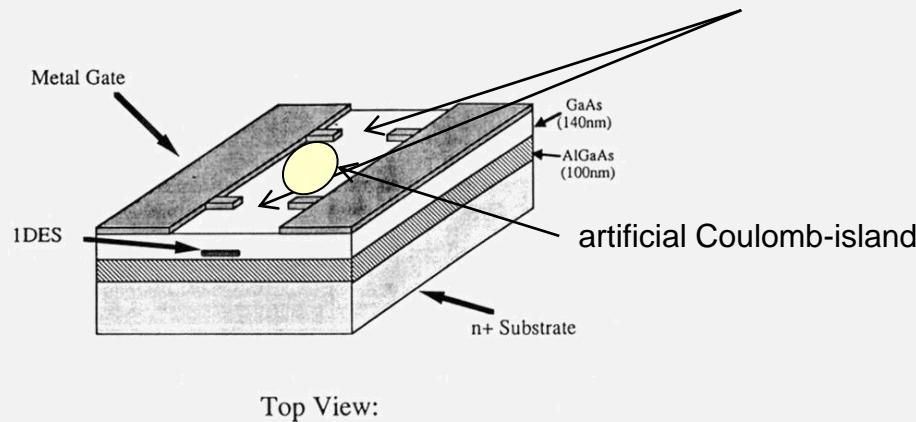


Although only one electron may be allowed in the Coulomb-island a high current may be possible

If the bias change covers sequentially various Coulomb-levels a staircase in current is the consequence.



A simple Coulomb-blockade devices exhibit only 2 tunnelling junctions:



Planar electrodes on GaAs, using 2-Dim electron gas (2DEG)

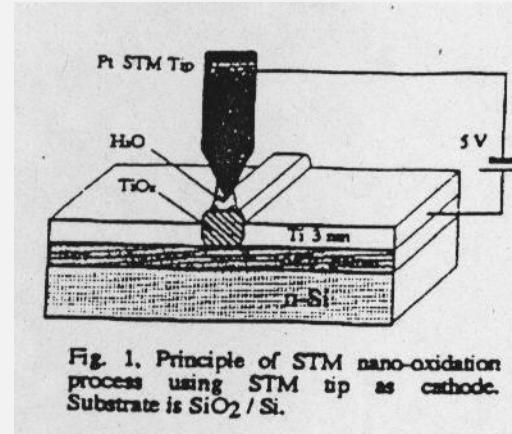
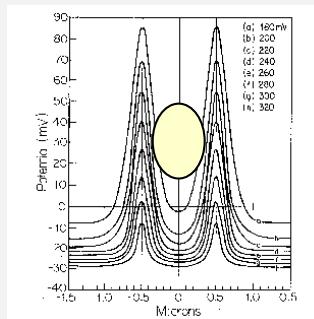
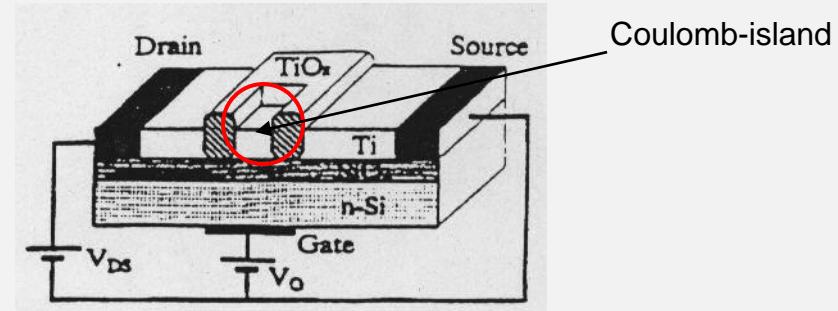
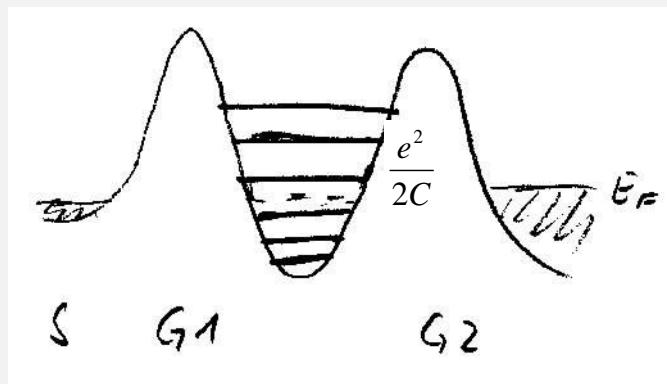


Fig. 1. Principle of STM nano-oxidation process using STM tip as cathode. Substrate is SiO<sub>2</sub> / Si.

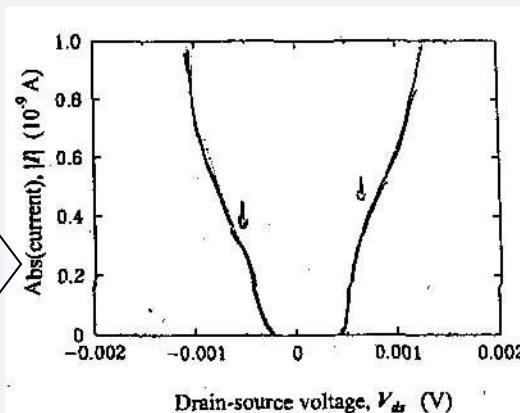


Creation of tunnel-junctions using scanning tunneling microscope STM

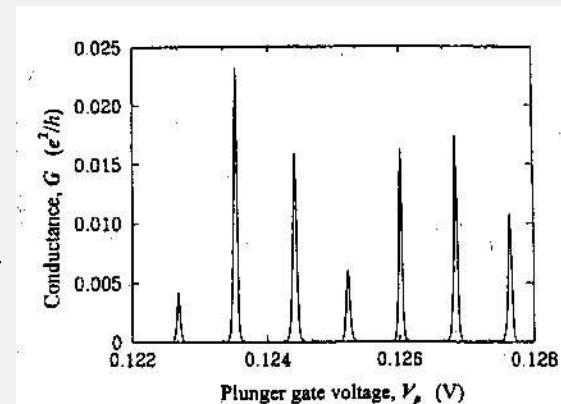
In these devices the so-called gate is needed to create an artificial Coulomb island. The gate cannot shift the potential of the island. These devices are not transistors ! These devices are used for spectroscopy of quantum states and general behavior.

"Large" Coulomb-island

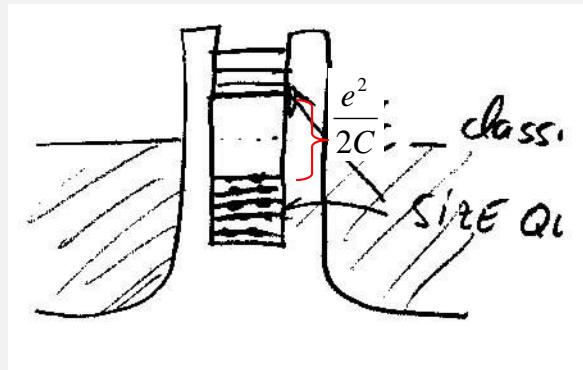
- > no size quantization (continuum)
- > only Coulomb quantization exists



**Figure 3.** The nonlinear conductance of a planar QD. The absolute value of the current is plotted against the drain-source bias,  $V_{ds}$ , at fixed gate voltages. A distinct threshold voltage is associated with the Coulomb blockade.

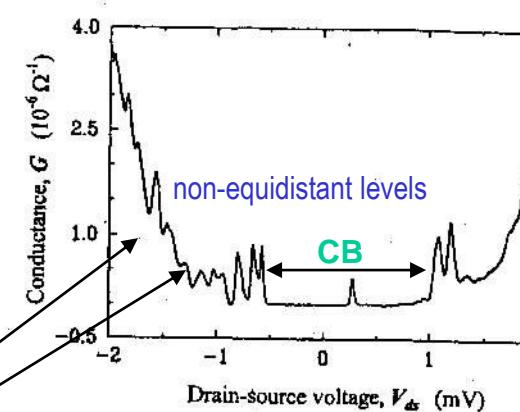


**Figure 2.** Representative data showing the conductance of a planar QD versus plunger gate voltage, at very low temperature (about 0.1 K). The conductance shows sharp peaks which are approximately equally spaced.

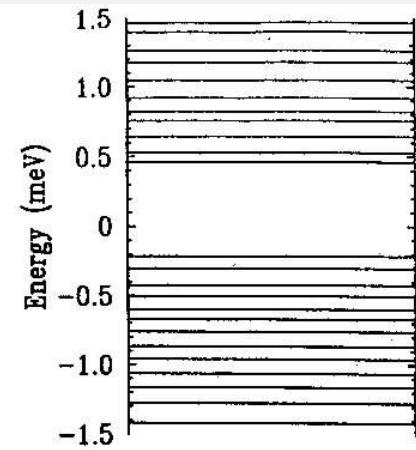
"Small" Coulomb-island

- > size quantization exists
- > and Coulomb quantization

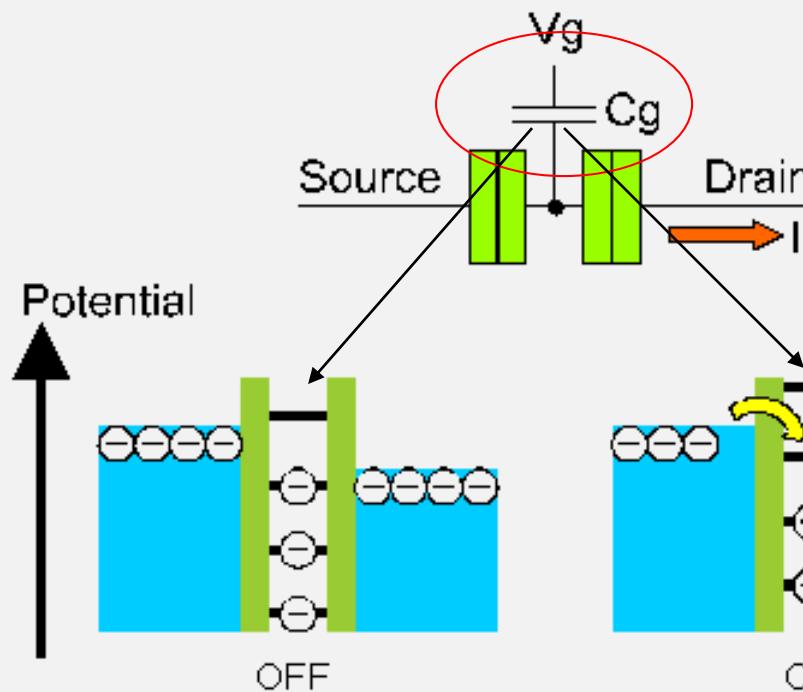
der Bundeswehr



**Figure 12.** The differential conductance  $G = dI/dV_{ds}$  as a function of  $V_{ds}$  measured in a planar QD [23]. The peaks are associated with the excited electron states in the QD, appearing whenever such an excitation is aligned with the Fermi level of one of the leads.



**Figure 14.** The experimental excitation spectrum of a QD extracted directly from the data of figure 12, with appropriate scaling of voltage to energy as discussed in the text. Note the two characteristic energy scales, the Coulomb gap and the discrete level spacing.



### Working principle:

- with a gate voltage the potential of the Coulomb-island can be influenced. The Coulomb-levels will be shifted up and down
- if the Source/Drain contacts are biased with a small voltage, no current flows. With varying gate voltage the Coulomb-levels can be shifted and tunneling can take place.  
Due to the discreteness of the tunneling ladder, the output current becomes a periodic function of the gate voltage.

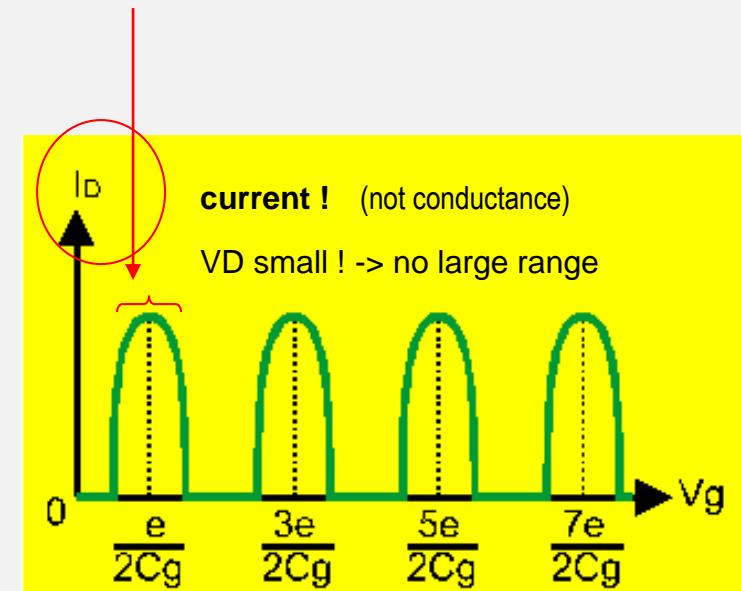
The **single-electron transistor** consists:

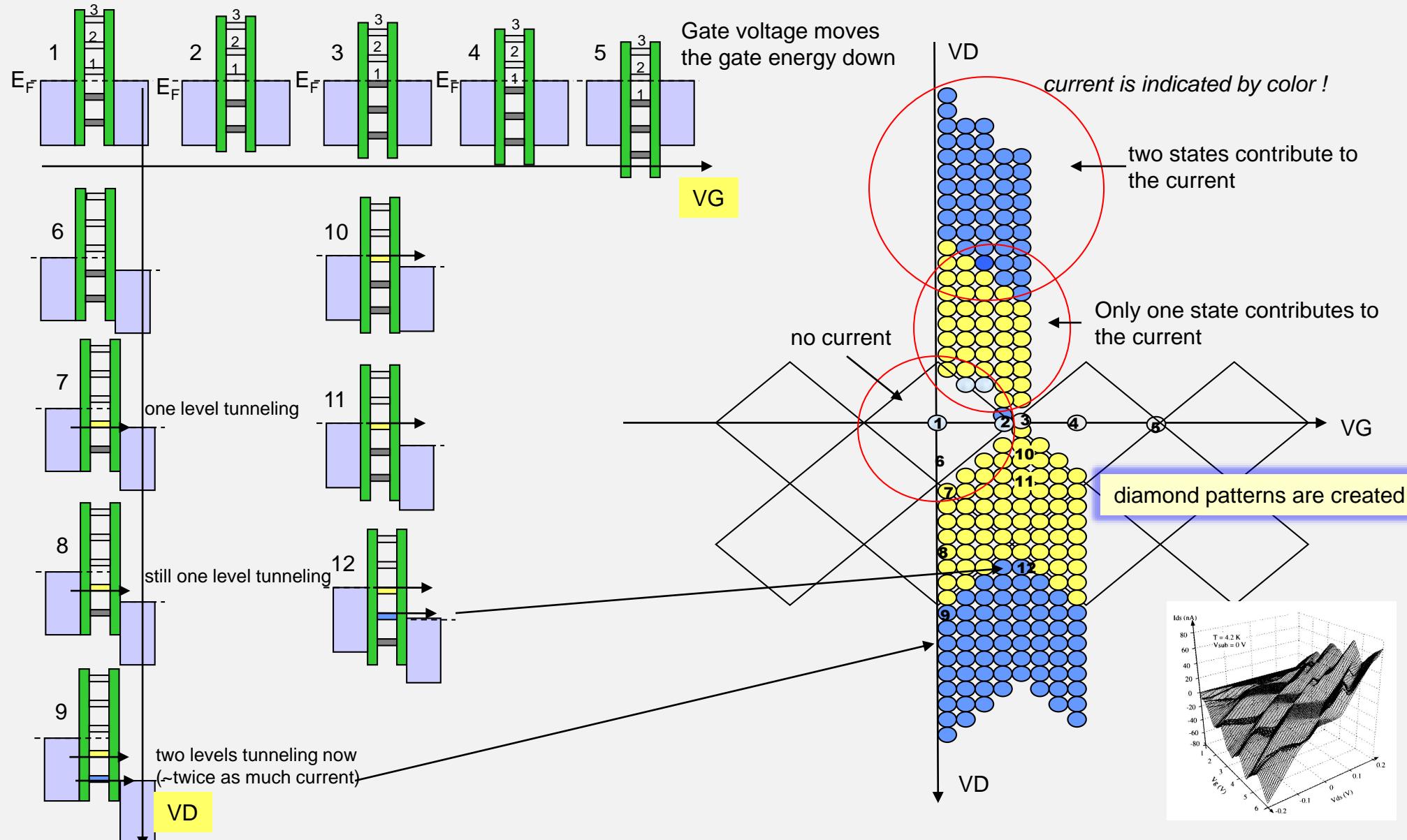
- a double-tunnel junction

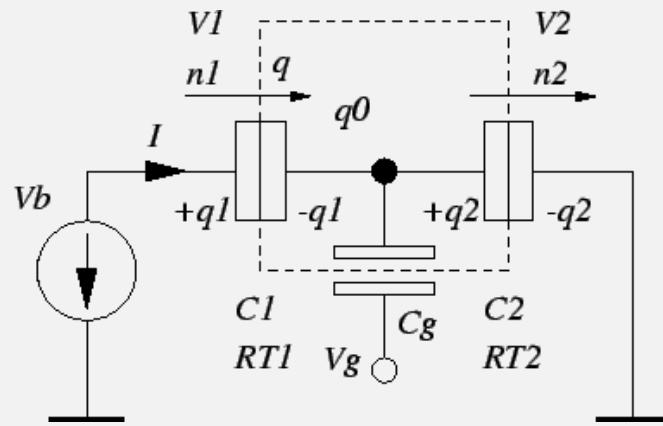


- the Coulomb-island capacitively coupled to a gate electrode

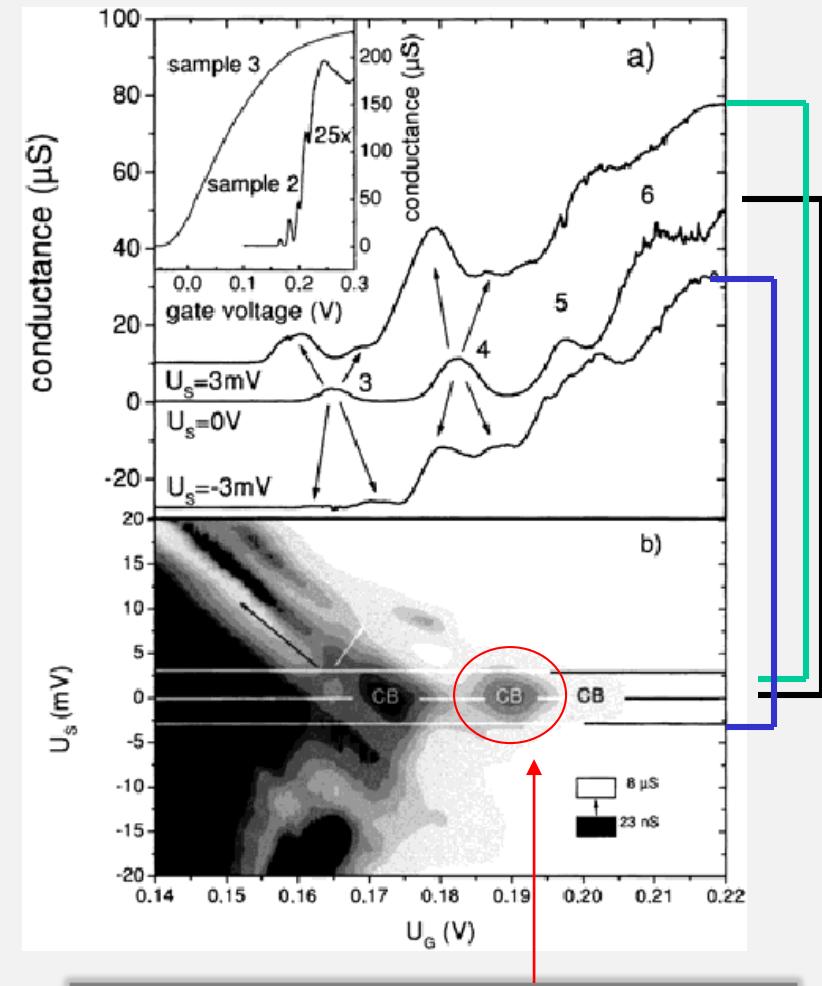
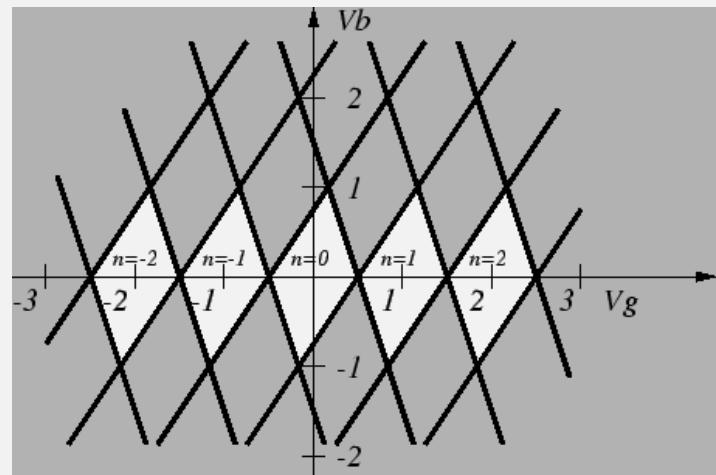
current range for one level





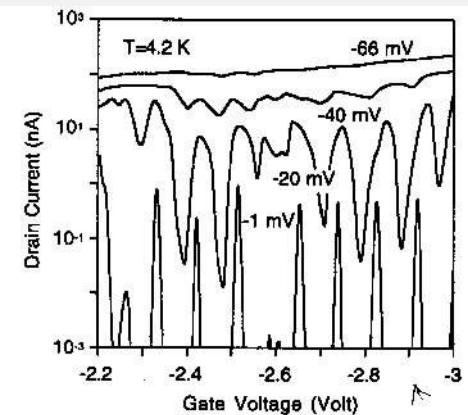
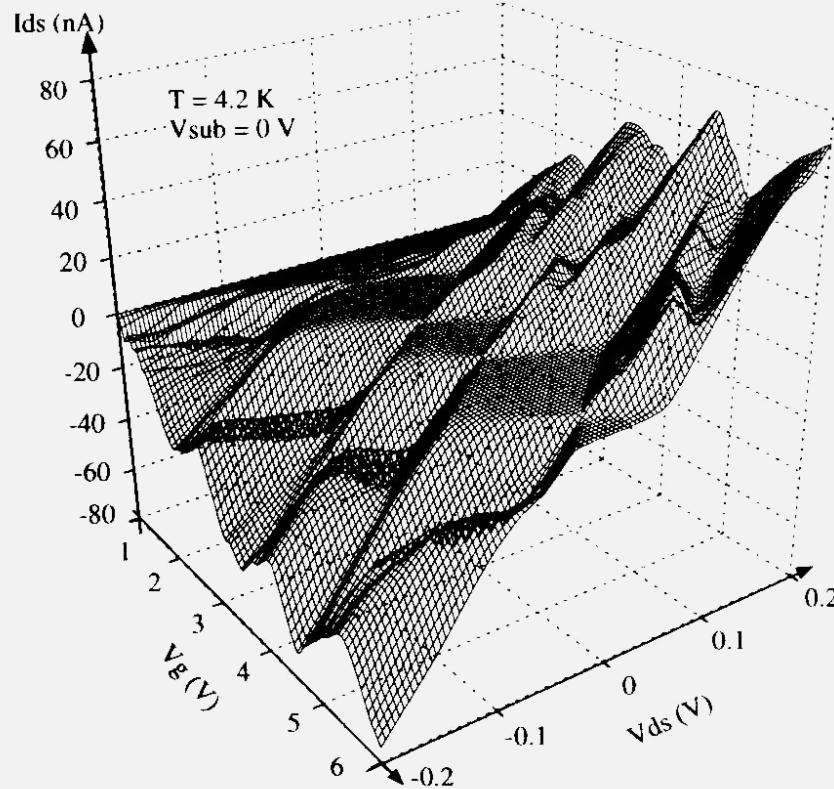


Equivalent circuit of a SET

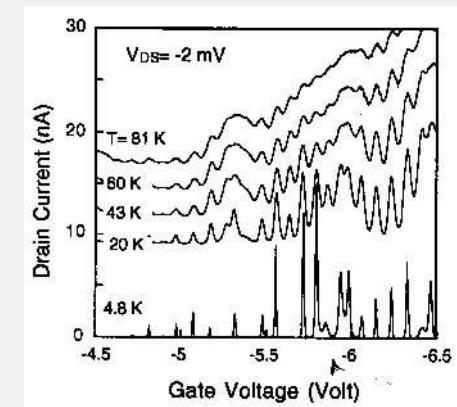


Coulomb islands are only a few mV in  $V_D$  and  $V_G$

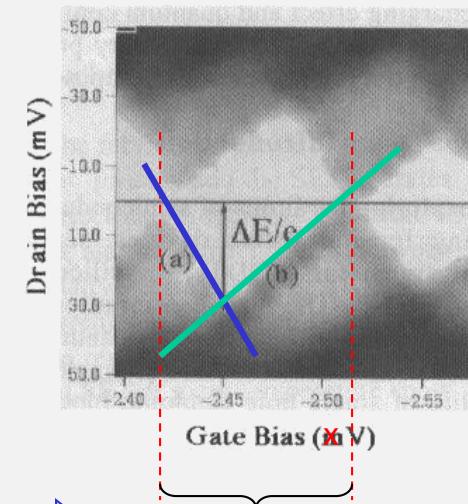
# The Single-Electron Transistor (SET)



Bias dependence



Temperature dependence



$$\text{slope } b = \frac{\Delta V_{DS}}{\Delta V_{Gate}} = \frac{C_{Gate}}{C_{Gate} + C_{Source}}$$

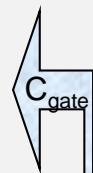
$$\text{slope } a = \frac{\Delta V_{DS}}{\Delta V_{Gate}} = \frac{C_{Gate}}{C_{Drain}}$$

Start Calculation:

$$\Delta V_{Gate} = \frac{e}{C_{Gate}}$$

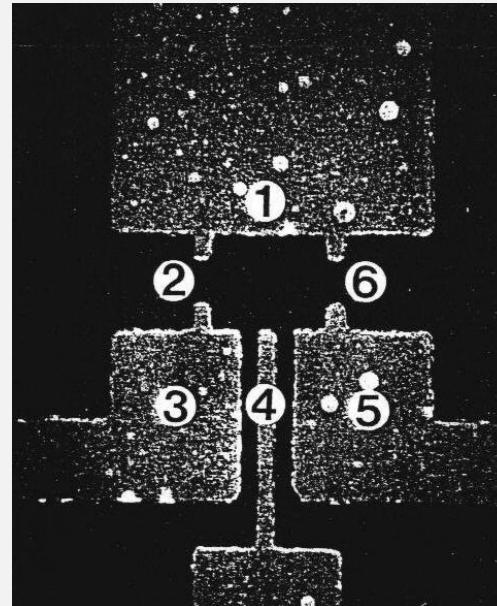
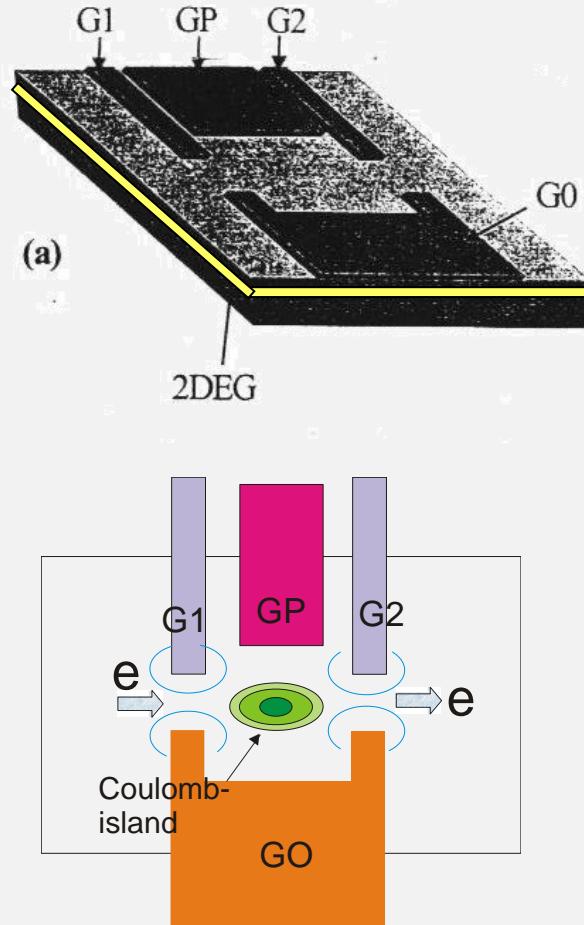
for  $n=1$

$$C_{Gate} = \frac{e}{\Delta V_{Gate}} = \frac{1.6 \cdot 10^{-19} \text{ A sec}}{0.08 \text{ V}} = 2 \text{ aF}$$



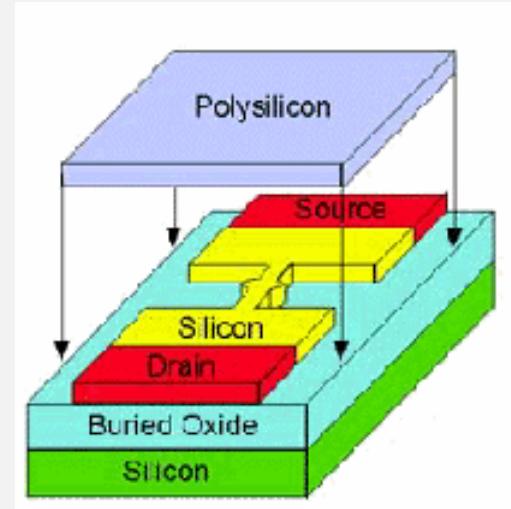
## Device Fabrication

Since the Coulomb-island must be small (0-dim), the starting structure is usually a 2-dim sheet or 1-dim wire



2-dim configurations

- by a heterostructure (e.g. AlGaAs/GaAs/AlGaAs)
- by a MOS-Gate (in Si)



SET in MOS-Technology

starting from an 1-dim wire

## Room Temperature Silicon Single-Electron MOS Memory with Nanoscale Floating Gate and Narrow Channel

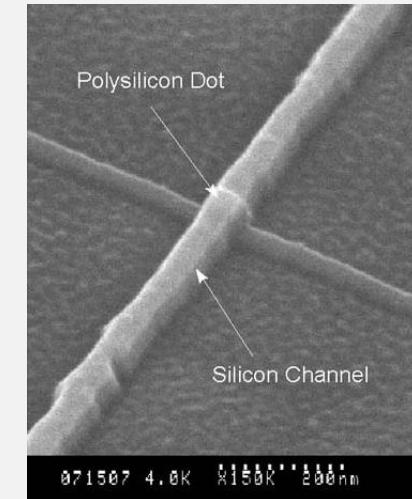
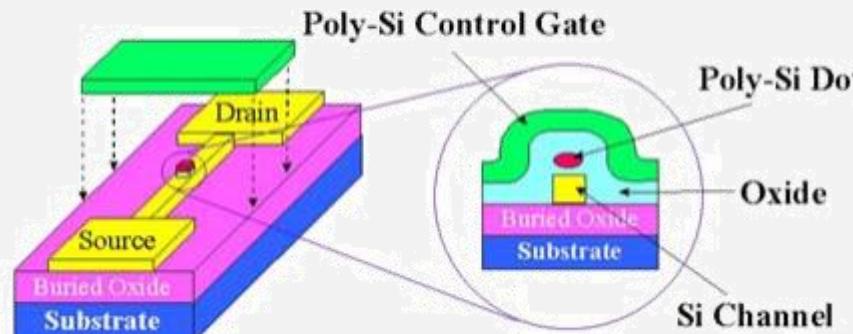
Lingjie Guo, Effendi Leobandung, and Stephen Chou  
NanoStructure Laboratory  
Department of Electrical Engineering  
University of Minnesota

\*Partially sponsored by DARPA, ONR, and ARO

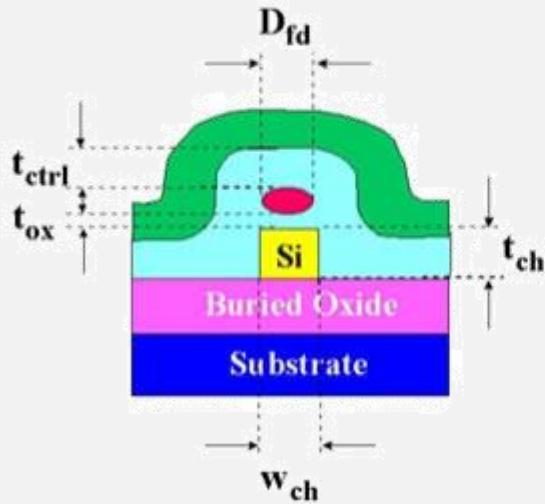
NanoStructure Lab  
UNIVERSITY OF MINNESOTA

see: SCIENCE 275 (1997) 649

## Silicon Single-Electron MOS Memory

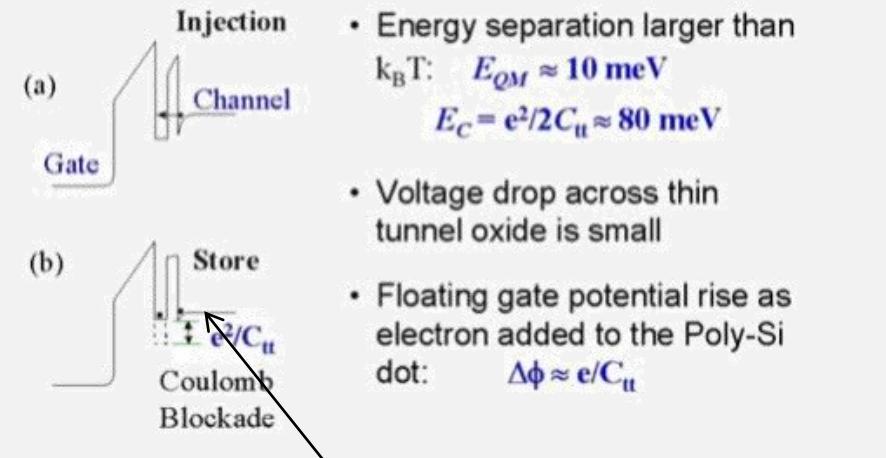


## Summary of Device Parameters

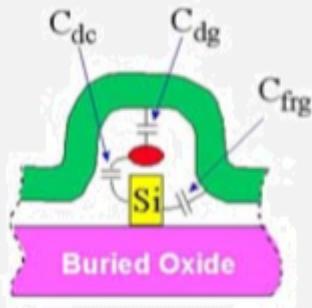


- Minimum Channel width  $w_{ch} \approx 10 \text{ nm}$
- Minimum floating gate size  $D_{fd} \approx 7 \text{ nm} \times 7 \text{ nm}$
- Final Channel thickness  $t_{ch} \approx 26 \text{ nm}$
- Control gate oxide  $t_{ctrl} = 40 \text{ nm}$
- Tunnel oxide: native oxide  $t_{ox} \approx 1 \text{ nm}$

## Self-limited Charging Process



## $V_{th}$ Shift due to Store of a Single Electron



- $\Delta V_{Ctrl-g} = e / C_{dg}$
  - $\Delta V_{th} = e / (C_{dg} + C_{frg})$
  - Size of floating gate 7nm X 7 nm
  - Debye screen length ~ 70 nm
  - Channel thickness ~ 26 nm
  - $\Rightarrow C_{dg} \approx 0.044 \text{ aF}, C_{frg} \approx 2.5 \text{ aF}$
- |              | $\Delta V_{th}$ | $\Delta V_{ctrl-g}$ |
|--------------|-----------------|---------------------|
| Theoretical  | 64 mV           | 3.6 V               |
| Experimental | 55 mV           | 4 V                 |

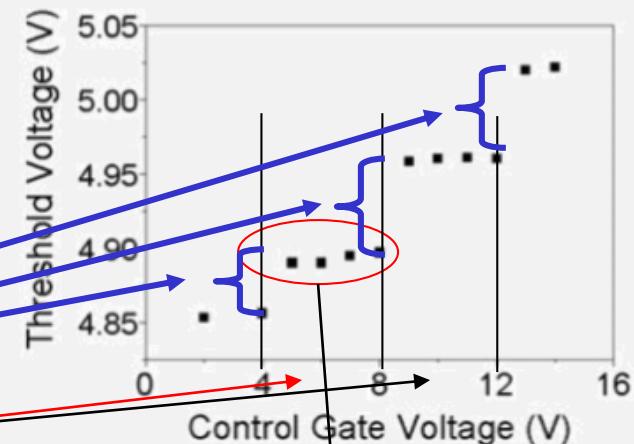
if  $V_{ctrl-g}$  is changed by  $e/C_{dot\text{-}gate} \sim 3.6\text{V}$ , an extra electron is charged in the dot.



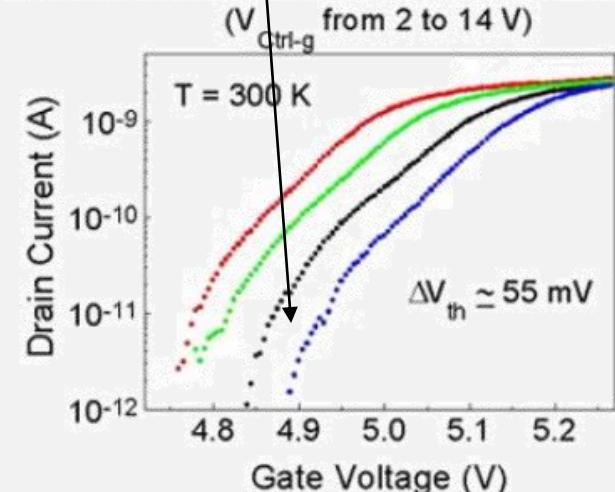
This extra electron will change in the above given geometries the threshold voltage  $V_t \sim 64\text{mV}$

The threshold voltage shift is used to detect, how many electrons are in the dot (-> multi-level memory possible)

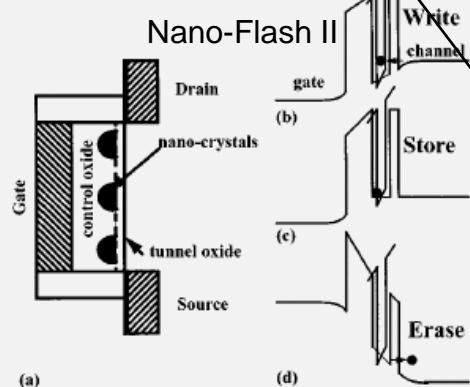
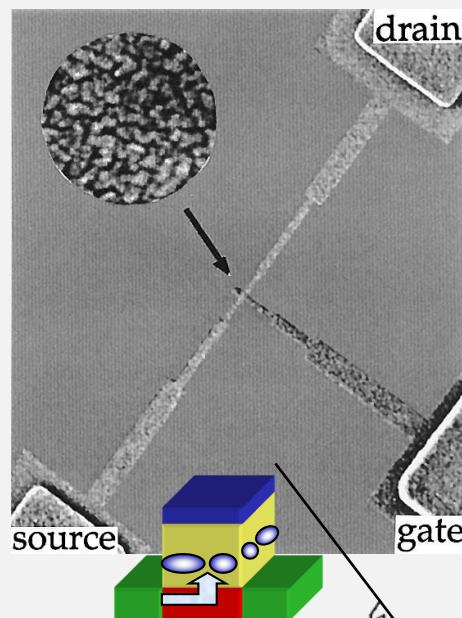
## Threshold Voltage Shift vs. Charging Voltage



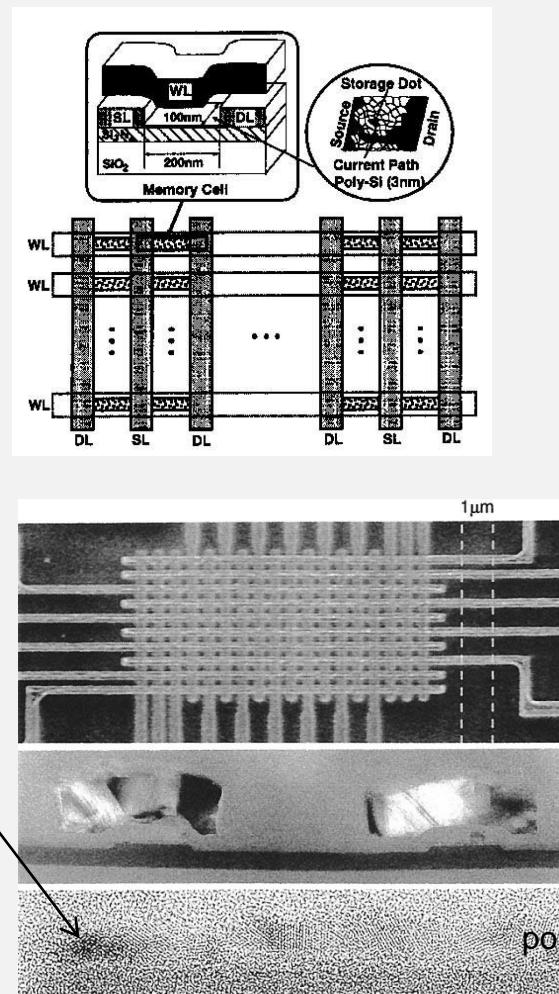
## Discrete Shift in Threshold Voltage



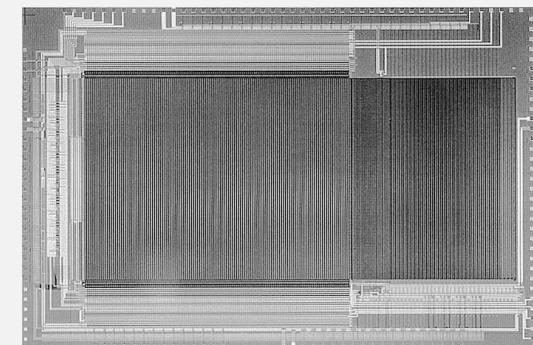
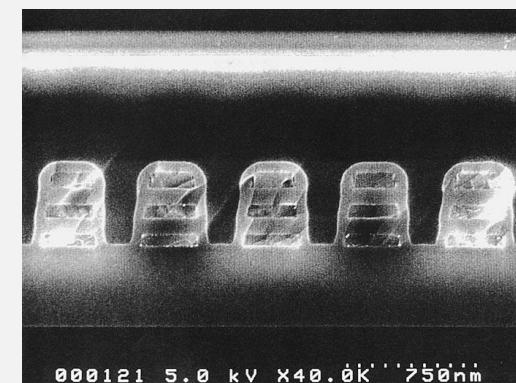
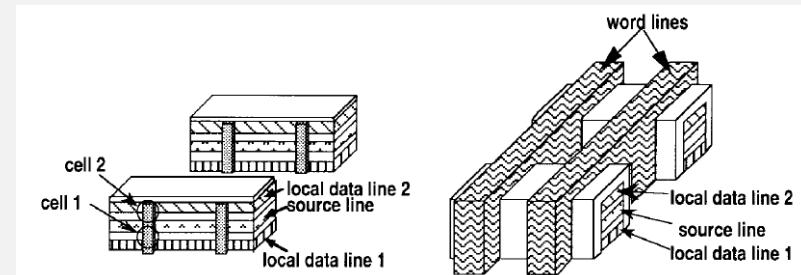
**SET**  
Room-temperature operation in 1993  
Yano, (Hitachi)



64-bit array in 1996



128 Mb in 1998



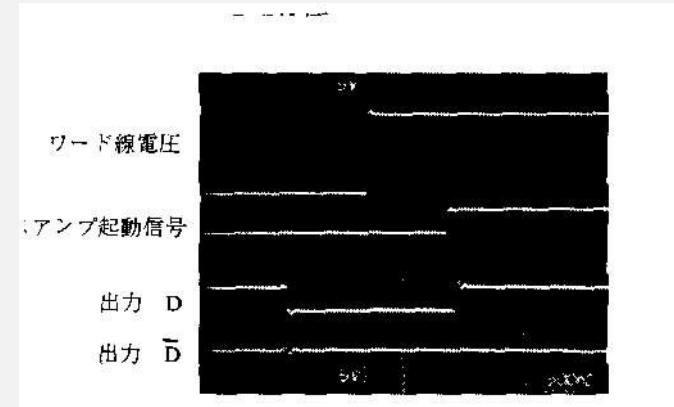
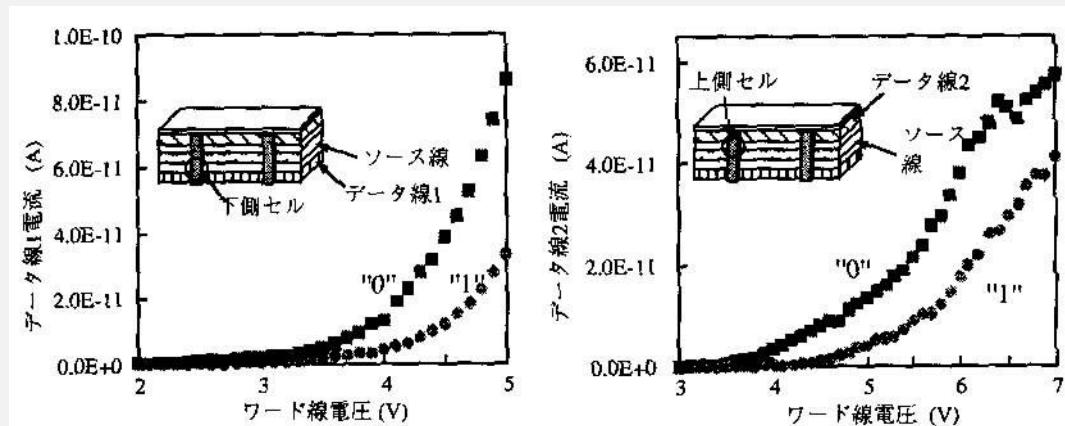


図13 読み出し波形

State of Art 2000-2012:

- ▶ Single-Electron Memories work at room-temperature
- ▶ Single-Electron Memories in 128Mb-Technology have been fabricated (although on every chip > 50% of cells failed)
- ▶ Single-Electron Memories work together with conventional CMOS peripherics
- ▶ Significant threshold variations occur from cell to cell
- ▶ The storage retention time is too short → trade-off on transparency of tunneling barrier for read/write operation and storage

Tucker (1992),  
Likharev (1996),  
showed that  
logic gatters may  
be constructed with  
SETs

### Complementary digital logic based on the "Coulomb blockade"

J. R. Tucker  
Department of Electrical and Computer Engineering and Beckman Institute, University of Illinois at Urbana-Champaign, Urbana, Illinois 61801

(Received 21 October 1991; accepted for publication 14 July 1992)

A finite charging energy,  $e^2/2C$ , is required in order to place a single electron onto a small isolated electrode lying between two tunnel junctions and having a total capacitance  $C$  to its external environment. Under suitable conditions, this elemental charging energy can effectively block all tunnel events near zero bias voltage in series arrays of ultrasmall junctions, an effect that has come to be known as the "Coulomb blockade." This article outlines a new approach to the design of digital logic circuits utilizing the Coulomb blockade in capacitively biased double-junction series arrays. A simple "on"/"off" switch is described and complementary versions of this switch are then employed to design individual logic gates in precise correspondence with standard complementary metal-oxide semiconductor architecture. A planar nanofabrication technique is also described that may eventually allow the integration of Coulomb blockade logic onto conventional semiconductor chips, thereby realizing hybrid integrated circuits having device densities and operating speeds far in excess of present technology.

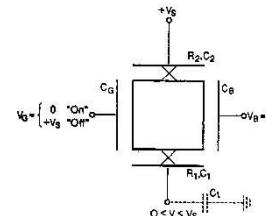


FIG. 11. Complementary double-junction "p" switch" for use in CMOS-type logic circuits. The p switch is an open circuit for high gate voltage  $V_g = V_s$  and charged the load capacitor  $C_L$  to the supply voltage when low gate voltage  $V_g = 0$  is applied.

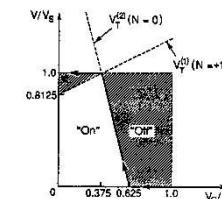


FIG. 12. Output voltage appearing on the load capacitor  $C_L$  of the p switch in Fig. 11 as the gate voltage is swept quasi-statically from off to on.  $V_g = V_s = 0$ , calculated for the example parameters in Eq. (33).

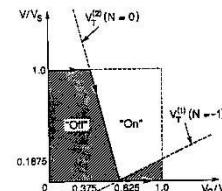


FIG. 13. Output voltage appearing on the load capacitor  $C_L$  of the x switch in Fig. 9 as the gate voltage is swept quasi-statically from off to on.  $V_g = 0 = V_s$ , calculated for the example parameters in Eq. (33).

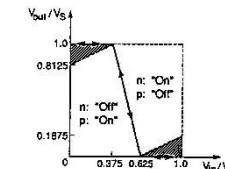


FIG. 14. Transfer characteristic of the inverter circuit in Fig. 13, calculated for the example parameters given in Eq. (33).

4410 J. Appl. Phys., Vol. 72, No. 9, 1 November 1992

### Single-electron transistor logic

A. H. Chen, A. N. Korotkov, and K. K. Likharev  
State University of New York at Stony Brook, Stony Brook, New York 11794-3800

(Received 20 November 1995; accepted for publication 29 January 1996)

We present the results of numerical simulations of a functionally complete set of complementary logic circuits based on capacitively coupled single-electron transistors (CSETs). The family includes an inverter/buffer stage, as well as two-input NOR, NAND, and XOR gates, all using similar tunnel junctions, and the same dc bias voltage and logic levels. Maximum operation temperature, switching speed, power consumption, noise tolerances, error rate, and critical parameter margins of the basic gates have been estimated. When combined with the data from a preliminary geometrical analysis, the results indicate that implementation of the CSET logic family for operation at  $T = 20$  K will require fabrication of structures with  $\sim 2$ -nm-wide islands separated by  $\sim 1$ -nm-wide tunnel gaps. © 1996 American Institute of Physics. [S0003-6951(96)02714-X]

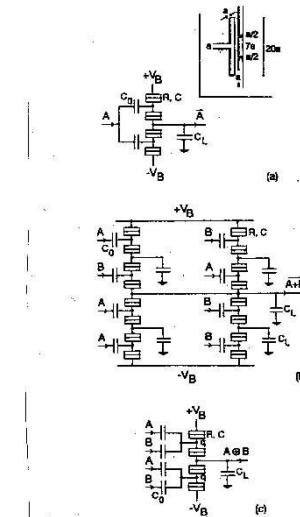
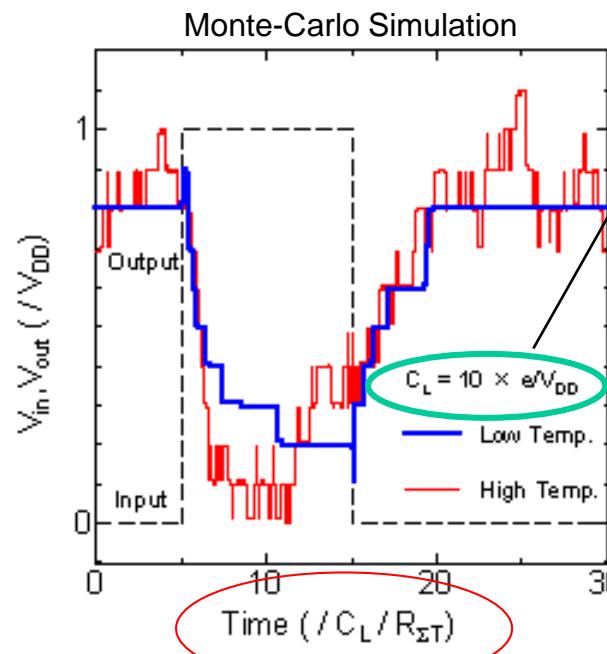
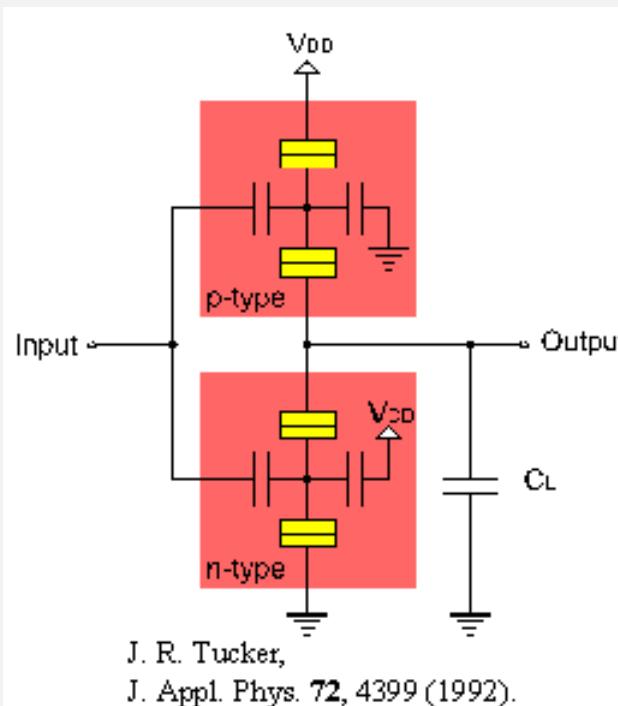


FIG. 1. Basic logic gates of the CSET family: (a) inverter/buffer; (b) NOR; (c) XOR. Vertical flipping of the NOR gate yields a NAND gate with similar performance. Inset in (a) shows the single-electron transistor structure used in our geometrical modeling.

From I-V characteristics logic gatters can be fabricated with SET

BUT ...

## Single-Electron Inverter:



simulation for load capacitance = 10 electrons

simulations for all C's = equal value

- output voltage is proportional the charge stored in the load capacitor

- output voltage  $< V_{DD}$



no voltage gain  $\rightarrow$  no stage drive

Simply expressed:  
a few electrons will always be lost to charge parasitic capacitances



BUT ...

Tucker (1992) also showed,  
that a SET- logic gatter will not  
have any FANOUT >1

because of 2 tunnel junctions with  $R \sim 25 \text{ k}\Omega$

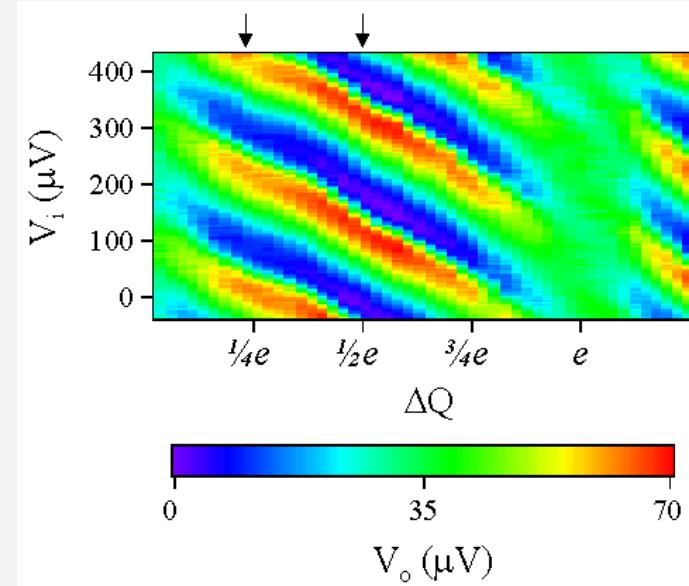
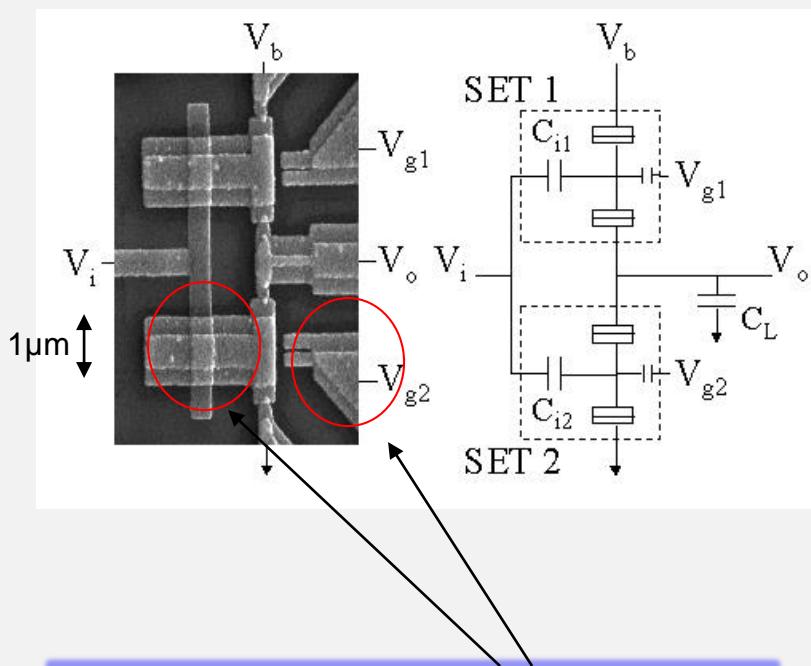
$$\text{SET: } RC \sim 10^{-18} F * 50 \text{ k}\Omega = 0.05 \text{ psec}$$

$$\text{CMOS: } RC \sim 10^{-15} F * \text{k}\Omega = 1 \text{ psec}$$



intrinsically high output impedance ( $R_{Tun} > 50 \text{ k}\Omega$ ) makes SET not much faster than CMOS

and the main problem is not the device but the interconnects with  $RC > RC_{device}$  !

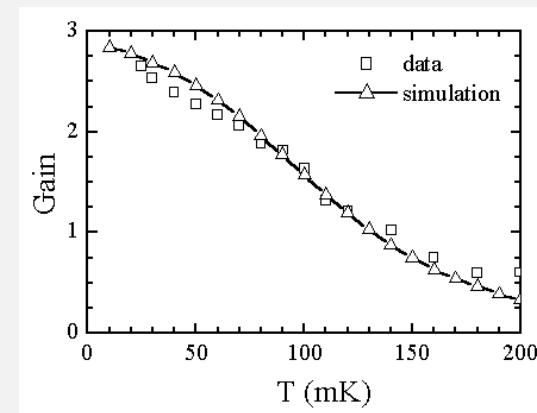
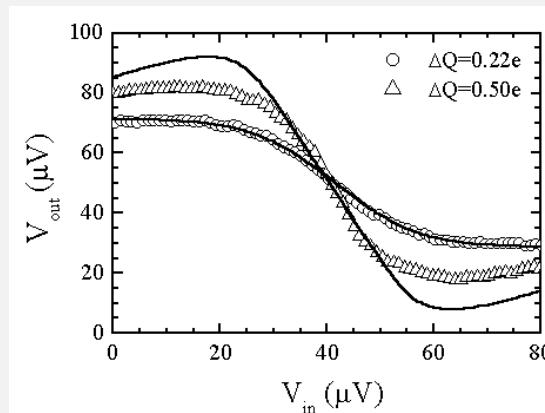


For voltage gain > 1 the gate capacitors must be larger than the tunneling capacitance.

- large overlap capacitors (3-dim stacks) are required

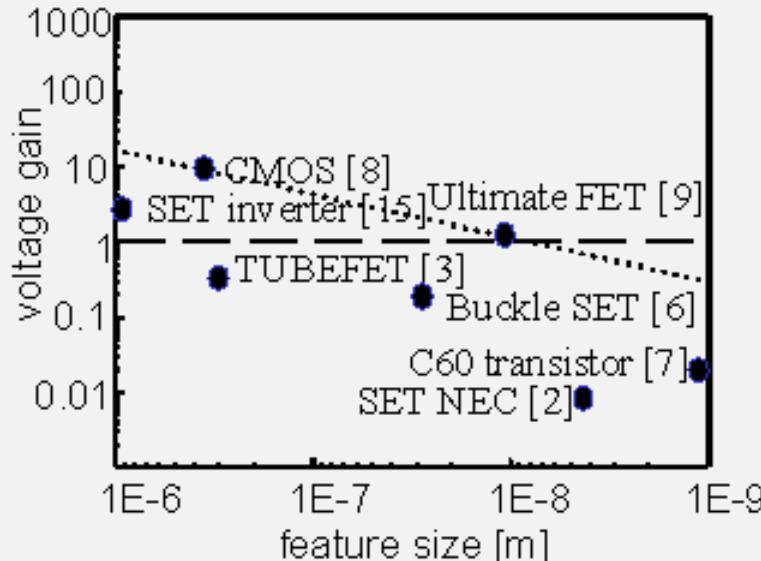


maximum gain of 2.6 at 25mK with 100μV supply



C. P. Heij, P. Hadley, J. E. Mooij, APL 78 (2001)

der Bundeswehr

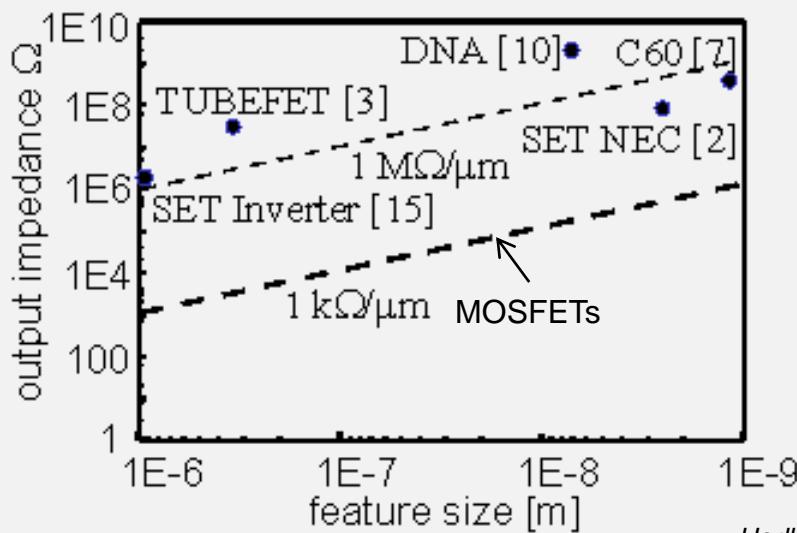


The figure shows the voltage gain of a selection of transistors as a function of feature size. The feature size is defined as the distance from the source contact to the drain contact. There is a dashed line at a voltage gain of 1. To achieve a voltage gain greater than one in a single-electron transistor, the gate capacitance must be larger than the tunnel junction capacitance.

This is most effectively achieved by making overlap gate capacitors.

Planar gates typically have too low capacitance for the voltage gain criterion. In most published reports of single-electron transistors, the voltage gain is less than one. The figure shows that **there is a general trend towards lower gain for smaller devices**. This is also true for CMOS. The dotted line is a rough indication of the gain that is achievable for CMOS transistor. Pikus et al. calculated that CMOS transistors will no longer exhibit voltage gain for a gate length less than 10nm.

Any technology that aspires to replace CMOS should have a signal gain greater than one for a feature size less than 10nm. **There are presently no nanodevices that meet this criterion.**



The speed of a circuit is related to the output impedance of devices in the circuit. To change the voltage at the output of a device, the capacitance of the output node has to be charged. This results in a RC delay where  $RC$  is the product of the output node capacitance and the output impedance of the device. The output impedance of a CMOS transistor can be adjusted by changing the width of the transistor. Typical output impedances are on the order of  $1 k\Omega$  per micron width.

The left figure shows the **output impedances of various devices as a function of feature size**. Most single-electron devices that have been reported have much higher output impedances than field-effect transistors. The output impedance of a single-electron transistor has to be greater than the quantum resistance  $\sim 25 k\Omega$ , otherwise quantum fluctuations wash out the charging effects. **Room temperature SET's tend to have much higher output impedances than  $25 k\Omega$**

Hadley et al. Department of Applied Sciences and DIMES, Delft University of Technology, Netherlands.

### Summarizing SET logic:



- + functionally small structures -> a priori for high density capable
- + working with mV or  $\mu$ V supply voltage and few electron transfer -> ultra-low power consumption
- + SET inverters behave the same as CMOS inverters -> good compatibility to CMOS



- precise nm-dimensions are needed -> very sophisticated fabrication processes needed
- for room-temperature operation even atomically resolution is needed -> very sophisticated fabrication processes needed
- very sensitive to charge distortion from surroundings -> very controlled fabrication processes
- intrinsically high output impedance ( $R_T > 100k\Omega$ ) makes SET not much faster than CMOS
- little or no voltage gain -> sophisticated gate-structures (3-dim) needed for Gain >1

### State-of Art (2013):

no SET with nm-dimensions and voltage gain > 1 at room-temperature exist up today

voltage gain of 1.3 at 30K at  $V_{DD}=20mV$  achieved,  
maximum gain of 2.6 at 25mK

State-of Art (2013):

no SET with nm-dimensions and voltage gain > 1 at room-temperature exist up today



since 10 years no one is working on SET

## Documents Related by Co-Citation

- 9 Single-Electron Logic and Memory Devices – A Korotkov - 1999
- 50 Single-electron devices and their applications – K K Likharev - 1999
- 9 K.Likharev, "Possible Performance of Capacitively Coupled Single-Electron Transistors in Digital Circuits – R Chen A Korotkov - 1995
- 22 Complementary digital logic based on the Coulomb blockade – J R Tucker - 1992
- 5 Odintsov, "Macroscopic quantum tunneling of the electric charge in small tunnel junctions," Phys – D Averin, A Odintsov - 1989
- 5 Virtual Electron Diffusion during Quantum Tunneling of the Electric Charge – D Averin, Y Nazarov - 1990
- 3 Storage capabilities of a four-junction single-electron trap with an on-chip resistor – S Lotkhov, H Zangerle, A Zorin, J Niemeyer - 1999
- 4 Coulomb blockade and cotunneling in single electron circuits with on-chip resistors – A B Zorin, S V Lotkhov, H Zangerle, J Niemeyer - 2000
- 3 Operation of a three-junction single-electron pump with on-chip resistors – S Lotkhov, S Bogoslovsky, A Zorin, J Niemeyer - 2001
- 9 Discrete Transfer of Single Electrons in Ultrasmall Tunnel Junctions – "Correlated K K Likharev - 1988
- 11 K.Murase, "Fabrication Method for IC Oriented Si Single-Electron Transistors – Y Takahashi Y Ono, M Nagase K Yamazaki, K Kurihara H Namatsu - 2000
- 22 K.K.Likharev, "Single-electron Transistor Logic – A N Korotkov R H Chen - 1996
- 6 M.Sugahara, "Complementary Digital Logic Using Resistively Coupled SingleElectron transistor – Y Jinguu N Yoshikawa, H Ishibashi - 1996
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- 6 A Linear Threshold Gate Implementation – C Lageweg, S Cotofana, S Vassiliadis - 2001
- 2 S.Vassiliadis, "Digital to Analog Conversion Performed – S Cotofana C Lageweg - 2001
- 1 and Stable Single-Electron Logic Utilizing Tunnel-Junction Load – M Fukushima H Fukui, "Simple K Hoh - 1995
- 1 D.Kim, "Performance of Single-Electron Transistor Logic Composed of Multi-Gate Single-Electron Transistors – Y Jeong M Jeong, S Hwang - 1997
- 140 Threshold logic and its applications – S Muroga - 1971



Single-Electron devices/Coulomb-Blockade devices are gaining interest to be used as quantum bit (qbit) devices

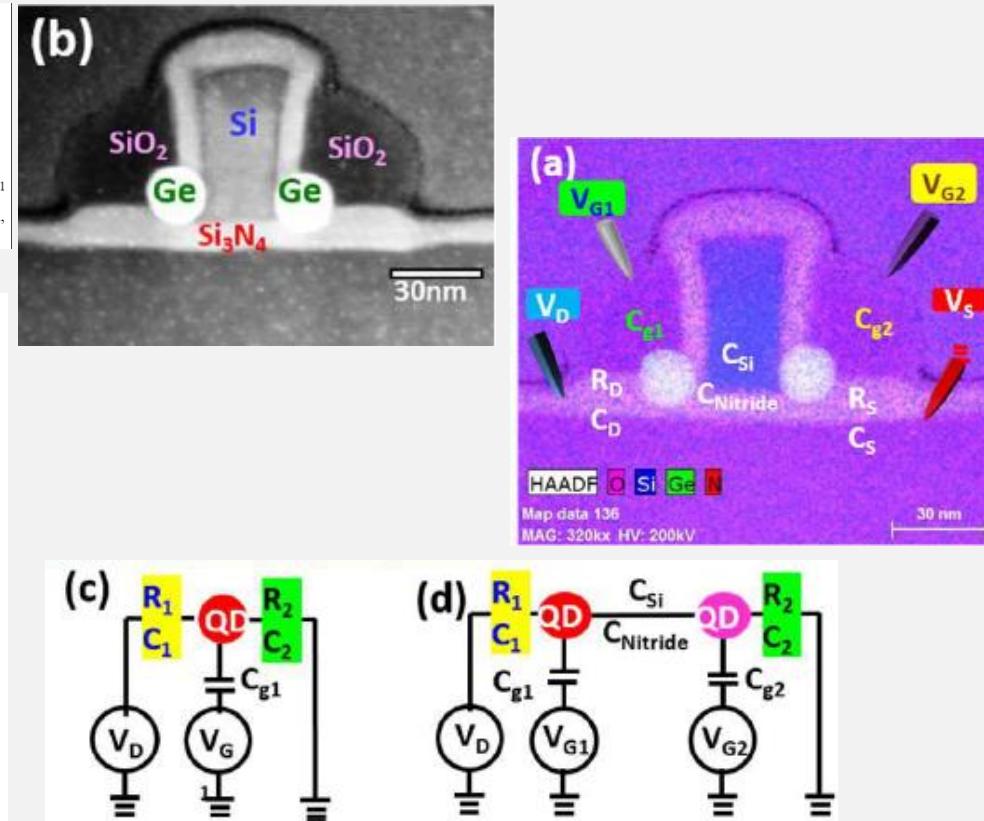
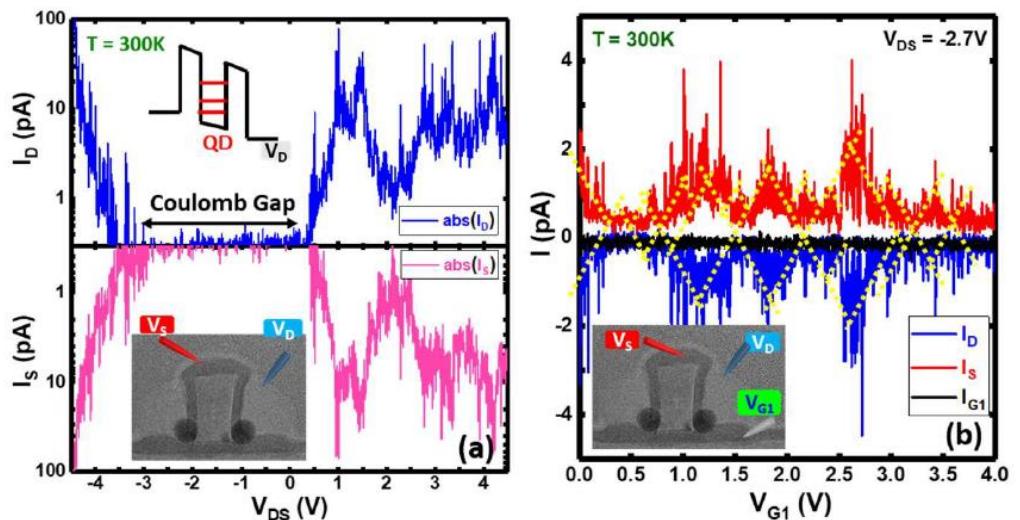
## Self-organized Pairs of Ge Double Quantum Dots with Tunable Sizes and Spacings Enable Room-Temperature Operation of Qubit and Single-Electron Devices

IEEE 2019

Kang-Ping Peng,<sup>1</sup> Ching-Lun Chen,<sup>1</sup> Ying-Tsan Tang,<sup>2</sup> David Kuo,<sup>3</sup> Thomas George,<sup>1</sup> Horng-Chih Lin<sup>1</sup> and Pei-Wen Li<sup>1</sup>

<sup>1</sup>Institute of Electronics, National Chiao Tung Univ, HsinChu, Taiwan, <sup>2</sup>Taiwan Semiconductor Research Institute, HsinChu, Taiwan,

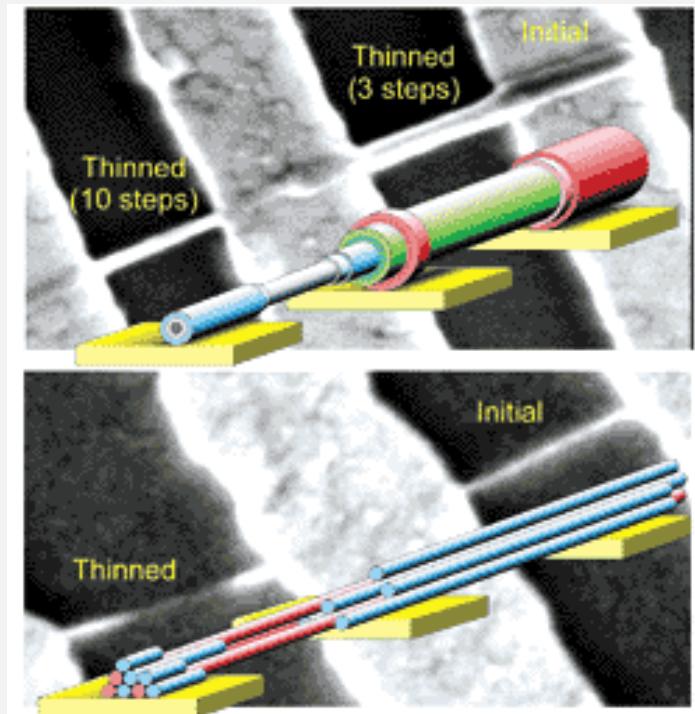
<sup>3</sup>Department of Electrical Engineering, National Central Univ, JongLi, Taiwan, email: [pwli@nctu.edu.tw](mailto:pwli@nctu.edu.tw)



Single-Electron device used for sense and read-out of the qubit

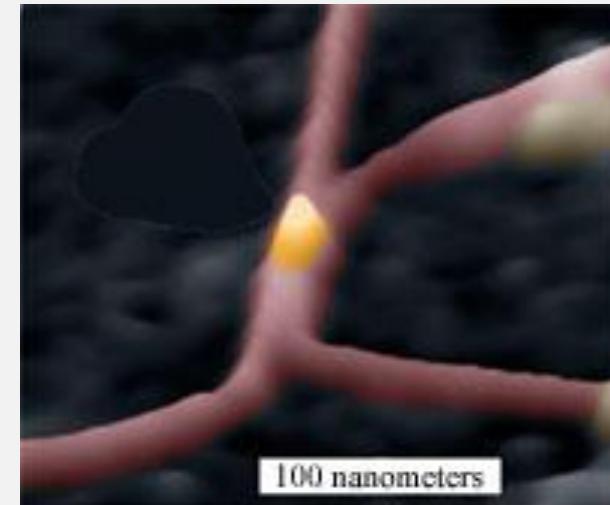


Fabricated in CMOS-technology



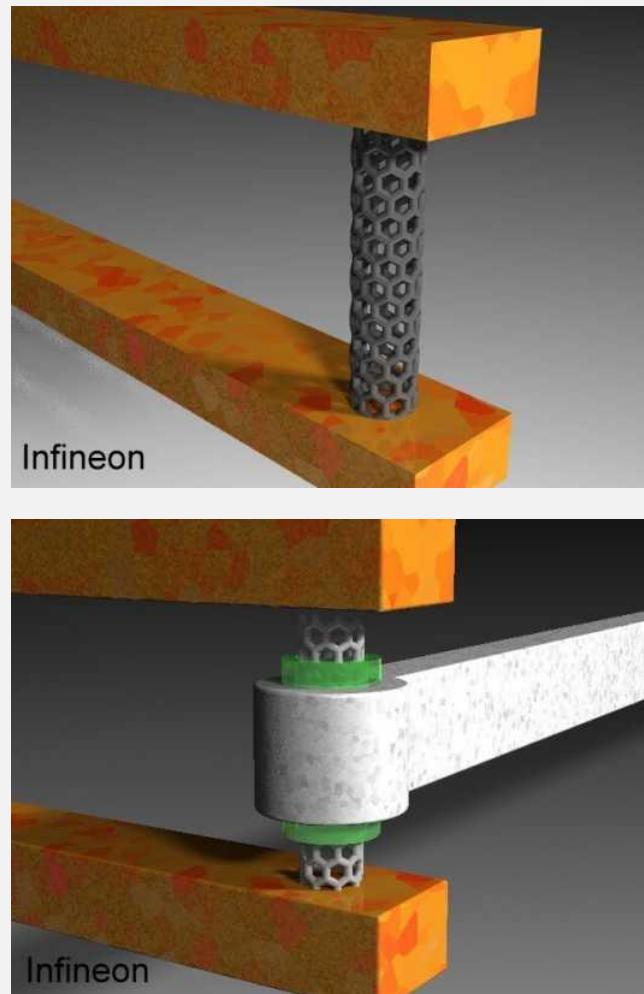
[www.research.ibm.com/resources/news/20010425\\_Carbon\\_nanotubes.shtml](http://www.research.ibm.com/resources/news/20010425_Carbon_nanotubes.shtml)

- 1 Manipulating nanotubes by AFM
2. Modify tubes

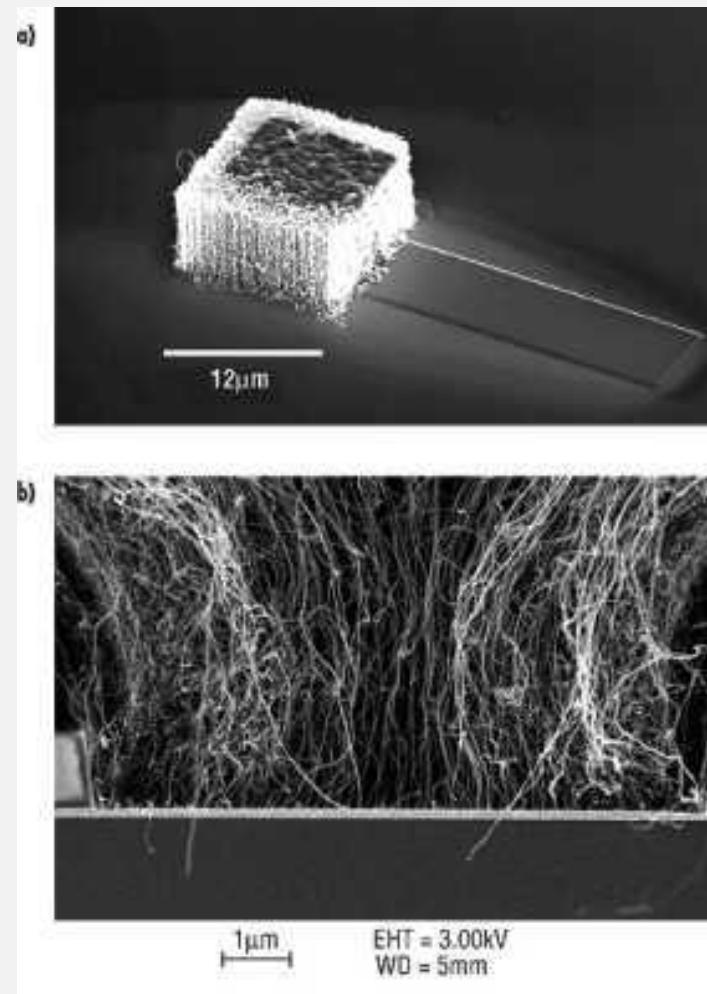


A tiny speck of gold positioned between two parallel carbon nanotubes forms a transistor that forwards one electron at a time. These single electron transistors could be used to make extremely small, low-power logic circuits.

Source: Lund University

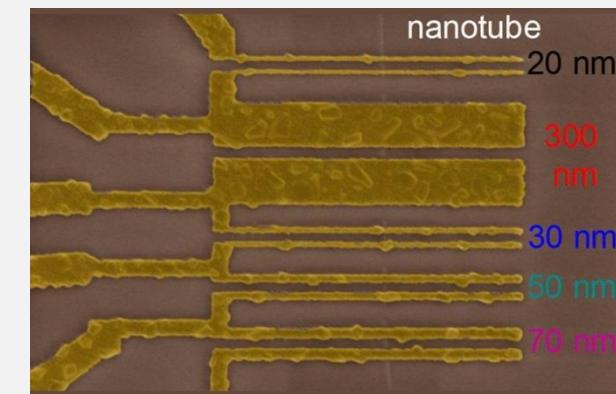


This is the dream



This is still reality

**IBM's carbon nanotube breakthrough takes processors beyond silicon 2015**



Density is still too low  
Missing information:  
- IV-characteristics  
- Reliability

## 8.1 Introduction

Overview of Tunneling Transistors

Tunneling in MOSFETs

## 8.2 The Esaki-Tunneling MOSFET

MOSFET problems need to be solved

Esaki-Tunneling and Esaki-Diode

Esaki-Tunneling MOSFET

## 8.3 Coulomb Blockade Devices

CMOS roadmap to single-electron MOSFETs

Nanotechnology

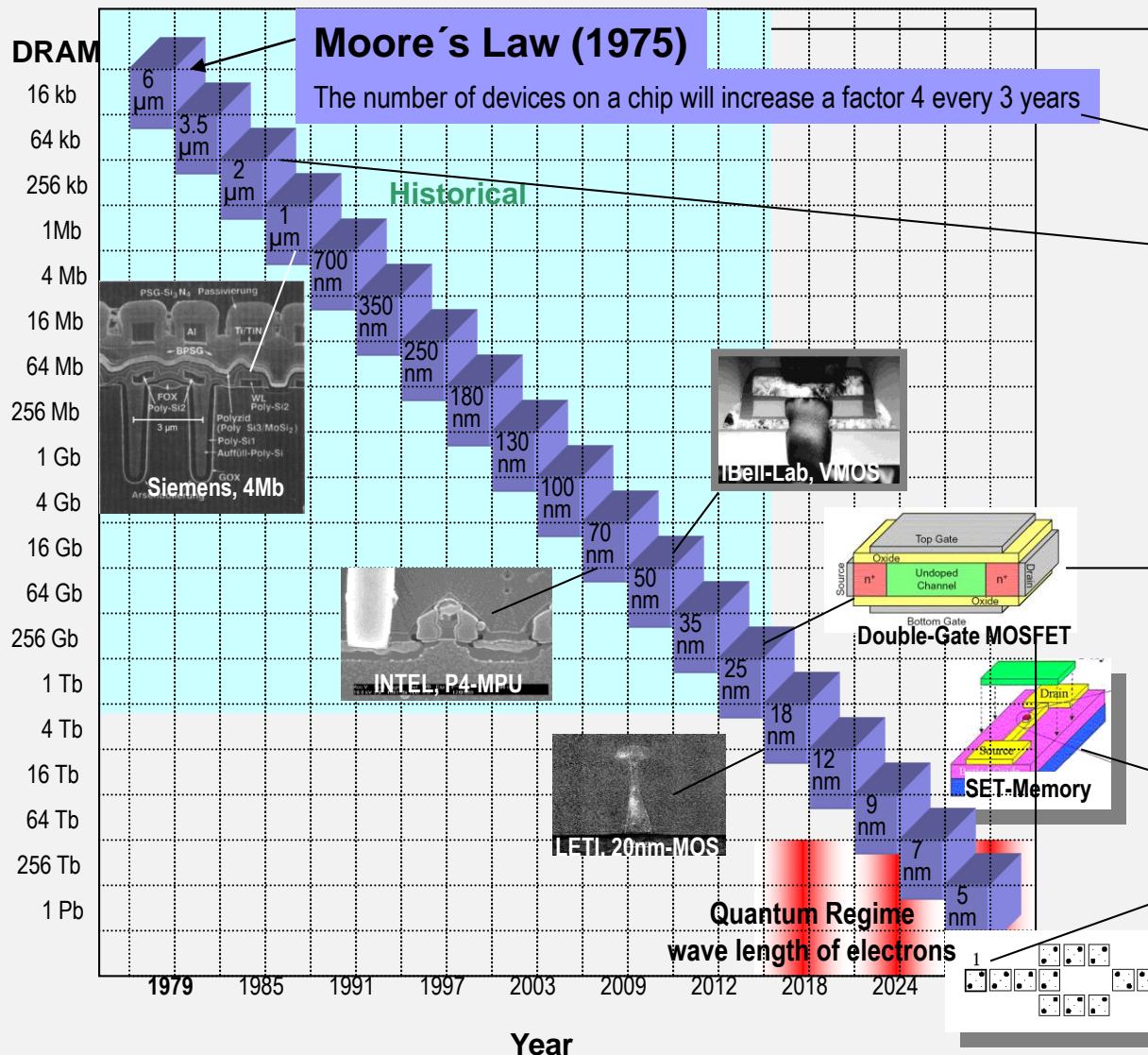
Physics of Coulomb-Blockade

Coulomb-Blockade Devices

Single-Electron Transistor

Single-Electron Memory and Single-Electron Logic

End  
of  
Chapter 8



- **1 History**  
Planar technology, Transistors, ICs
- **2 Economics**  
Future Applications, Markets, Semiconductors
- **3 Long-channel MOSFETs**  
Basic Behavior, High-Field Effects
- **4 Short-channel MOSFETs**  
Short-Channel Effects, Scaling
- **5 Carrier Transport**  
Theory, Simulation, Experiment
- **6 Advanced MOSFETs**  
SiGe, high-k, vertical MOS, Double-Gate,
- **7 Hot Electron Transistors**  
PDB-FET, IMOS, Spin-Valve-Transistor
- **8 Tunneling Transistors**  
Tunneling-FET, Single-Electron Transistor
- **9 Quantum-Coherence Transistors**  
Spin-Resonance Transistor, Quantum Computing

Good Luck and Success  
for your future

