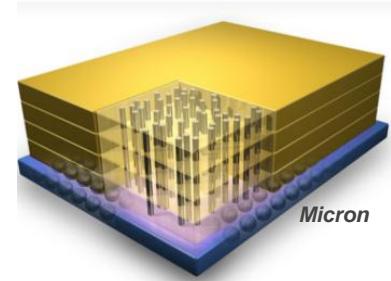
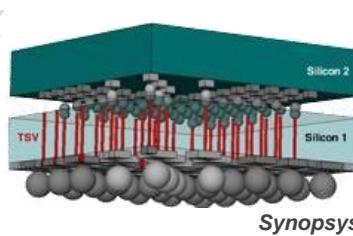
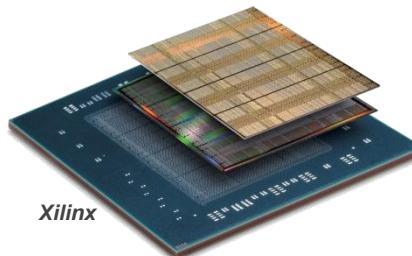
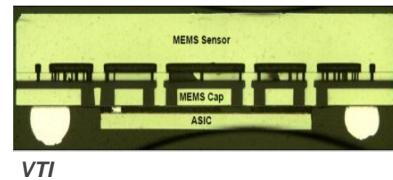
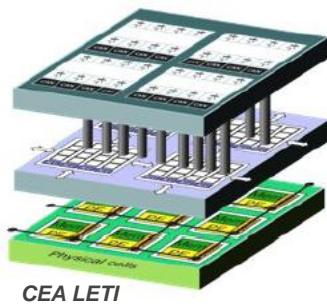


3DIC & TSV interconnects

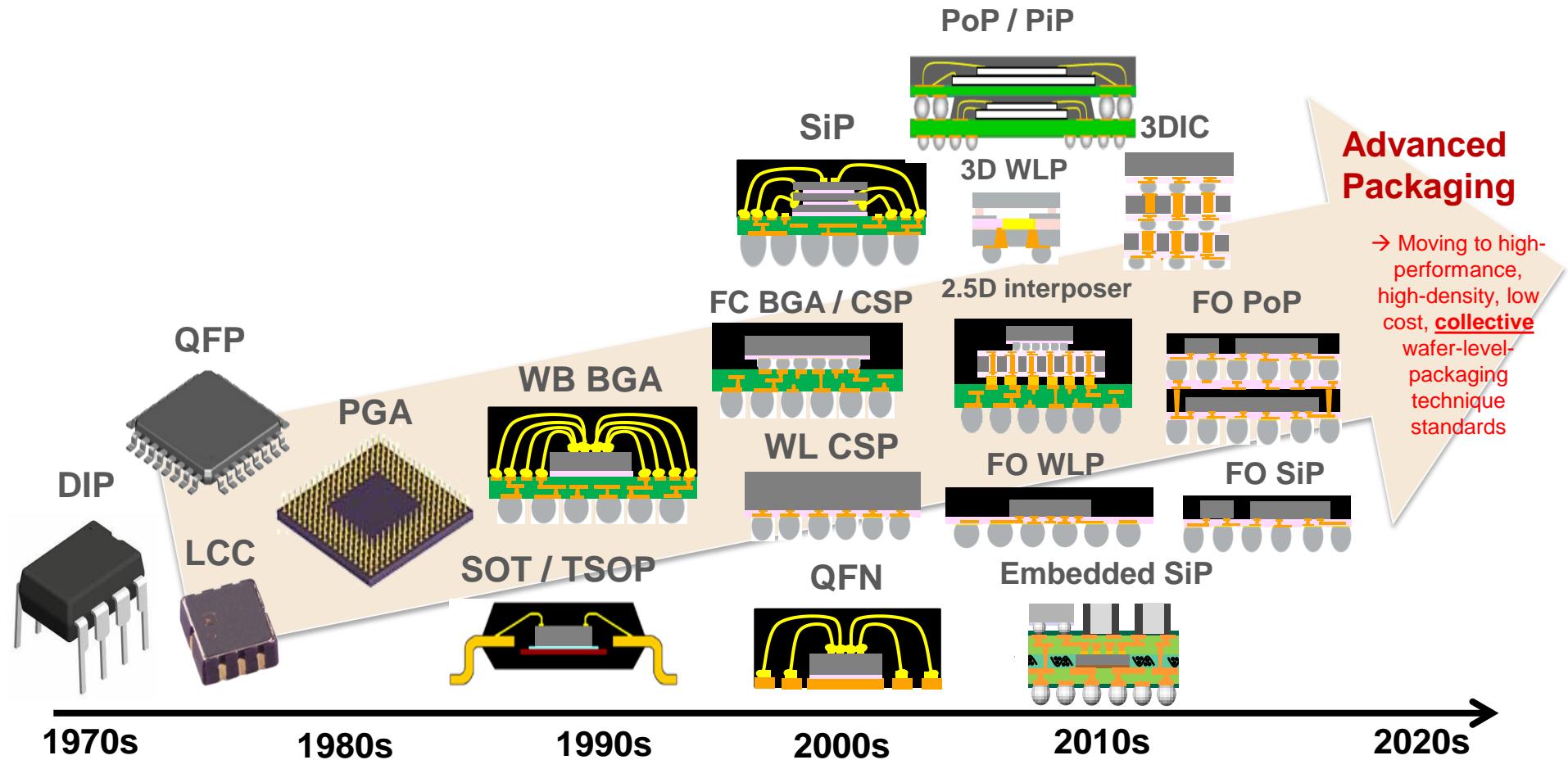
2012 Business update

Semicon Taiwan 2012 – *baron@yole.fr*

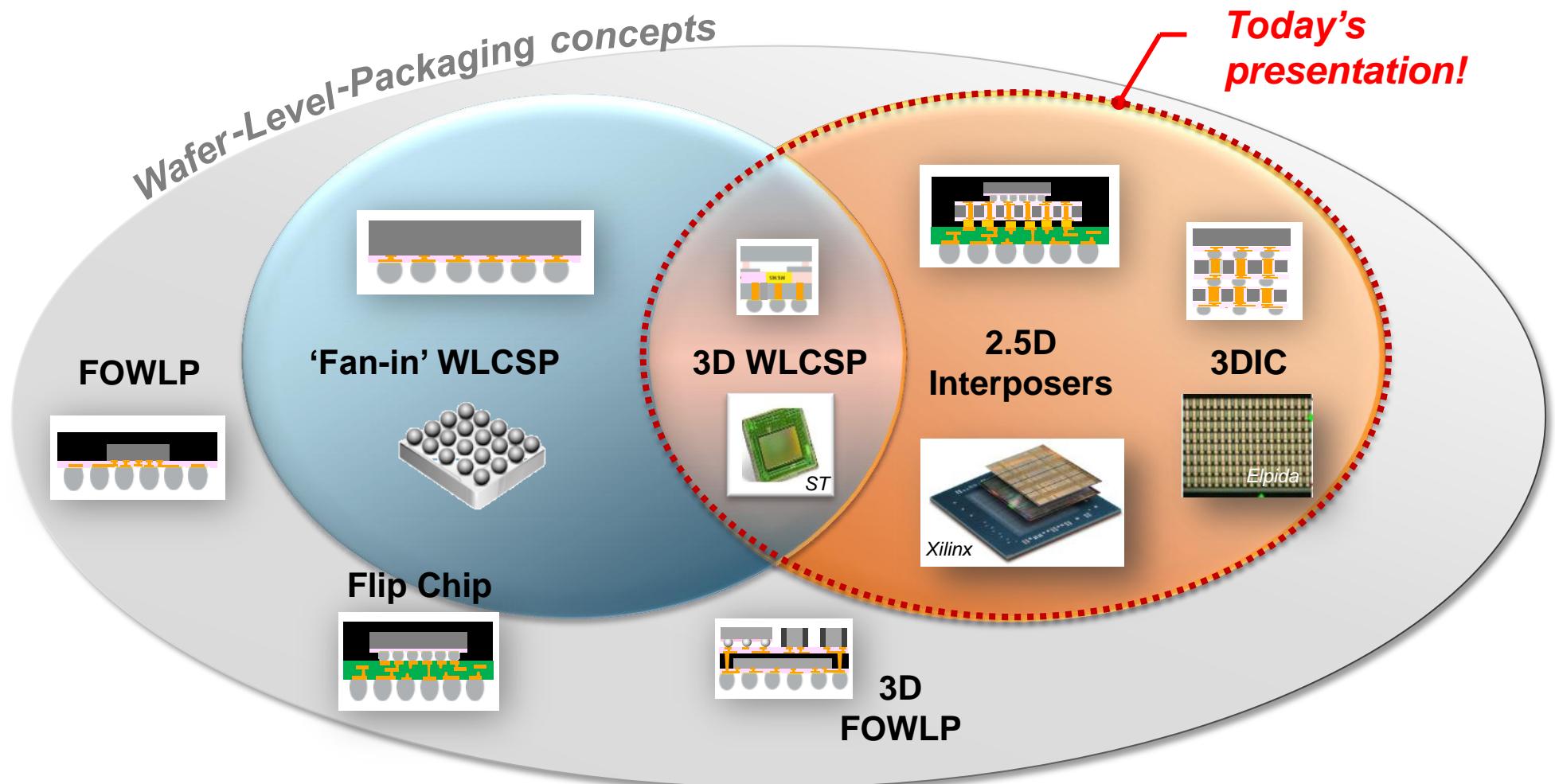


Semiconductor chip packaging market evolution

- The pace of innovation in chip packaging industry has never been faster!
 - Today driven by semiconductor company giants (Intel, Samsung, TI, STMicro, TSMC, Qualcomm...) along with “Top 5” biggest packaging subcontractors (ASE, Amkor, SPIL, STATschippac, PTI...)



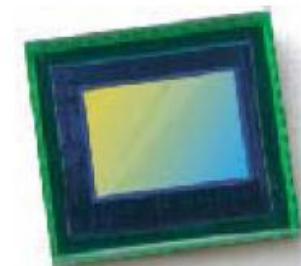
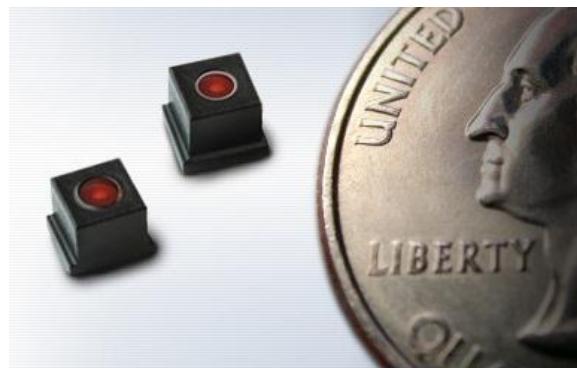
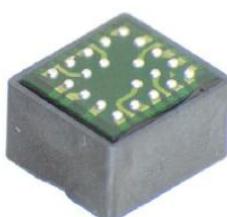
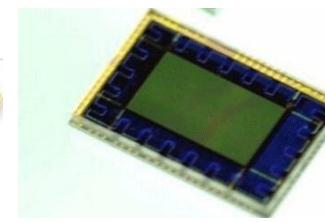
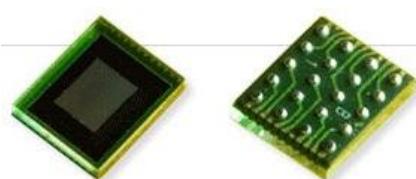
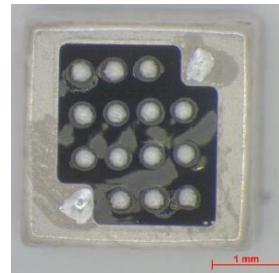
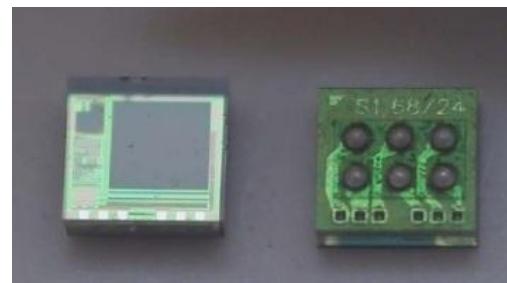
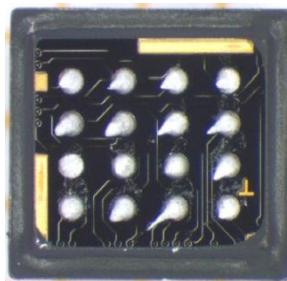
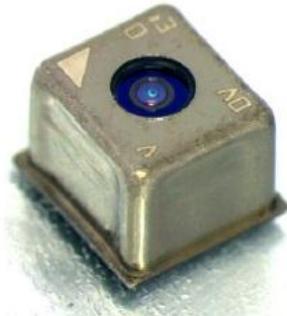
Scope of today's presentation



- This report is focused on the three middle-end technological platforms in which TSV is used as a vertical interconnect: 3D WLCSP, 2.5D Interposer and 3DIC

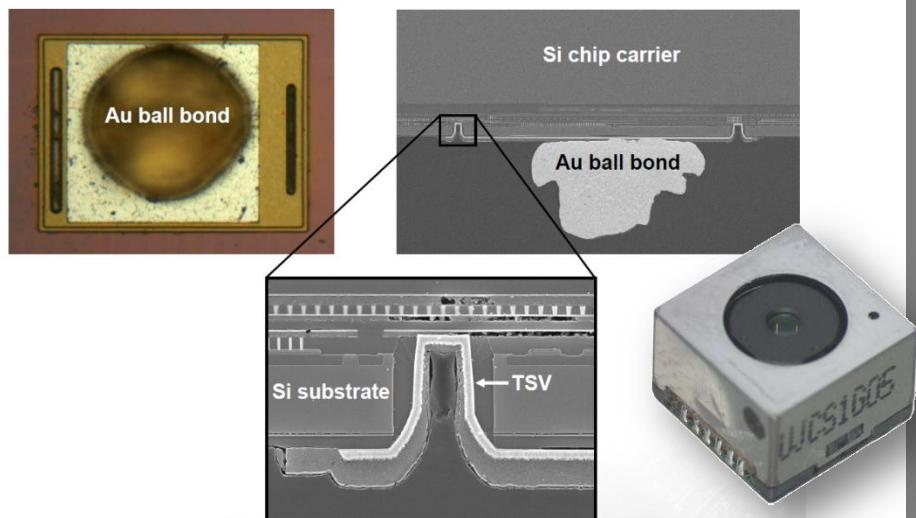
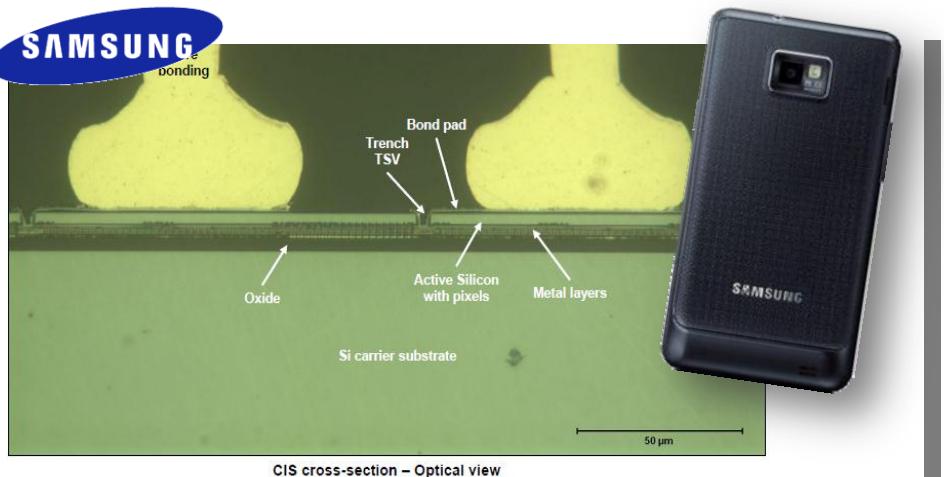
TSV / WLP Reality in Low-End, FSI CMOS Image Sensors

- Most low-end CIS (CIF, VGA to 2MPixels resolutions) are adopting 3D WLCSP packaging:

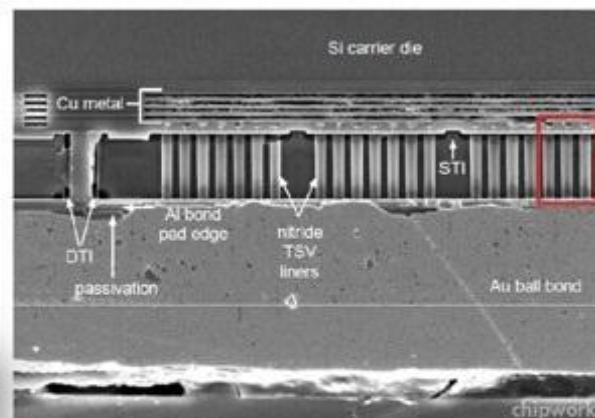


TSV / WLP Reality in High-End, BSI CMOS Image Sensors

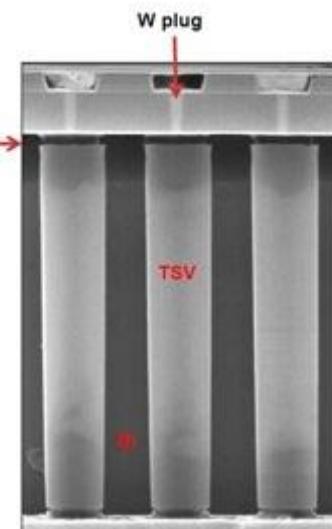
- In high-end applications (video cameras, DSC, Smart phones) with > 5-8Mpixel sensor resolutions, BSI architectures are using 'front-side' etched TSV to reach the BEOL metal layers



Samsung's TSV trench TSV in BSI image sensors found in
Galaxy SII Smart phone product
(Courtesy of System Plus Consulting, Chipworks)



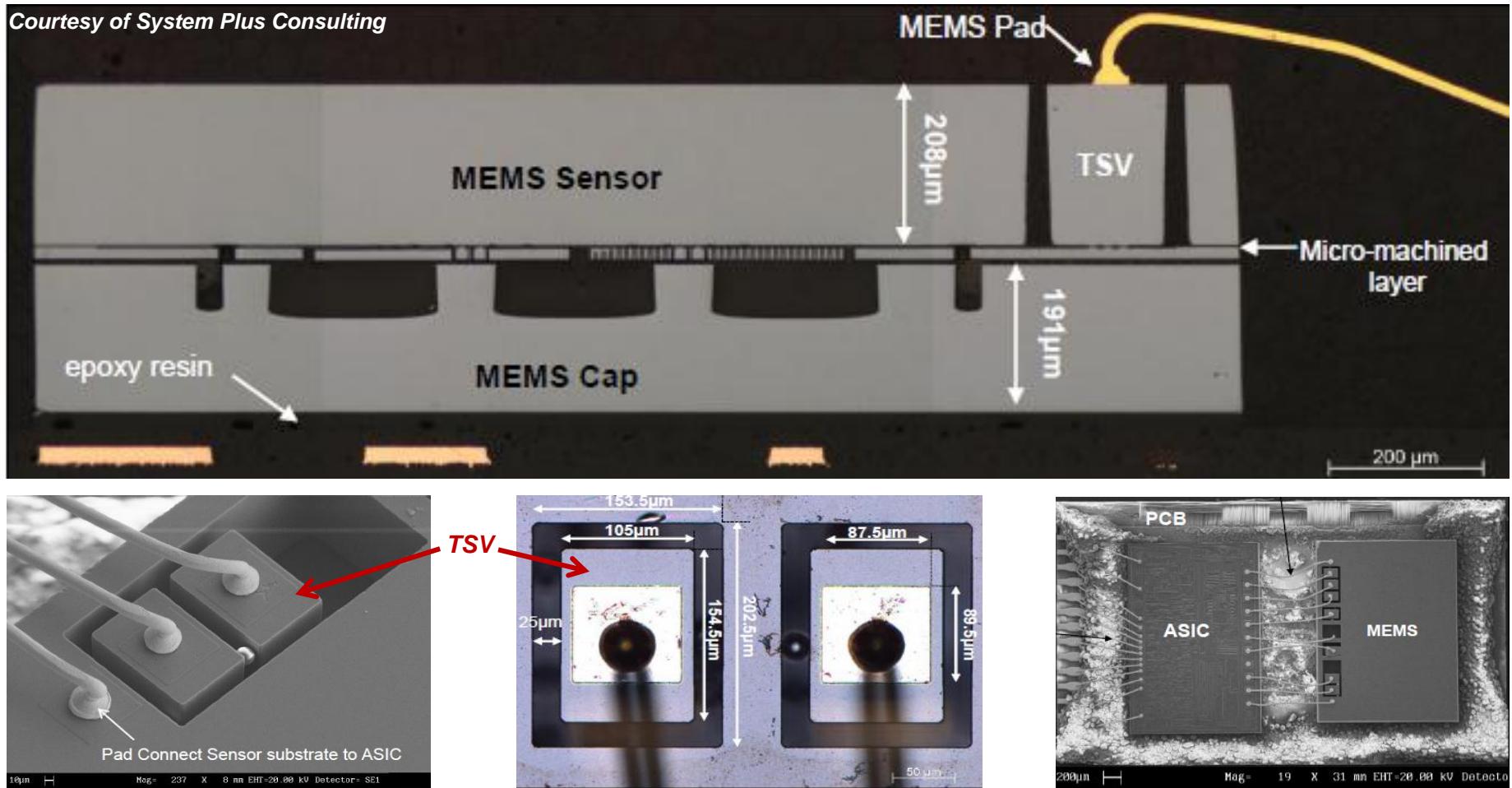
- Silicon stain used, so TSVs stand proud of Si
- TSV pitch 1.1 μm, diameter ~0.5 μm
- Bond pads are isolated by deep trench isolation (DTI)



Toshiba's redundant TSV interconnects in BSI image sensors
found in Fujifilm camera (Courtesy of Chipworks)

TSV Implementation in MEMS Accelerometer

- **STMicroelectronics Accelerometer with TSV in MEMS IC**
 - Device was introduced in 2011 and can be found in Nokia's mobile phone

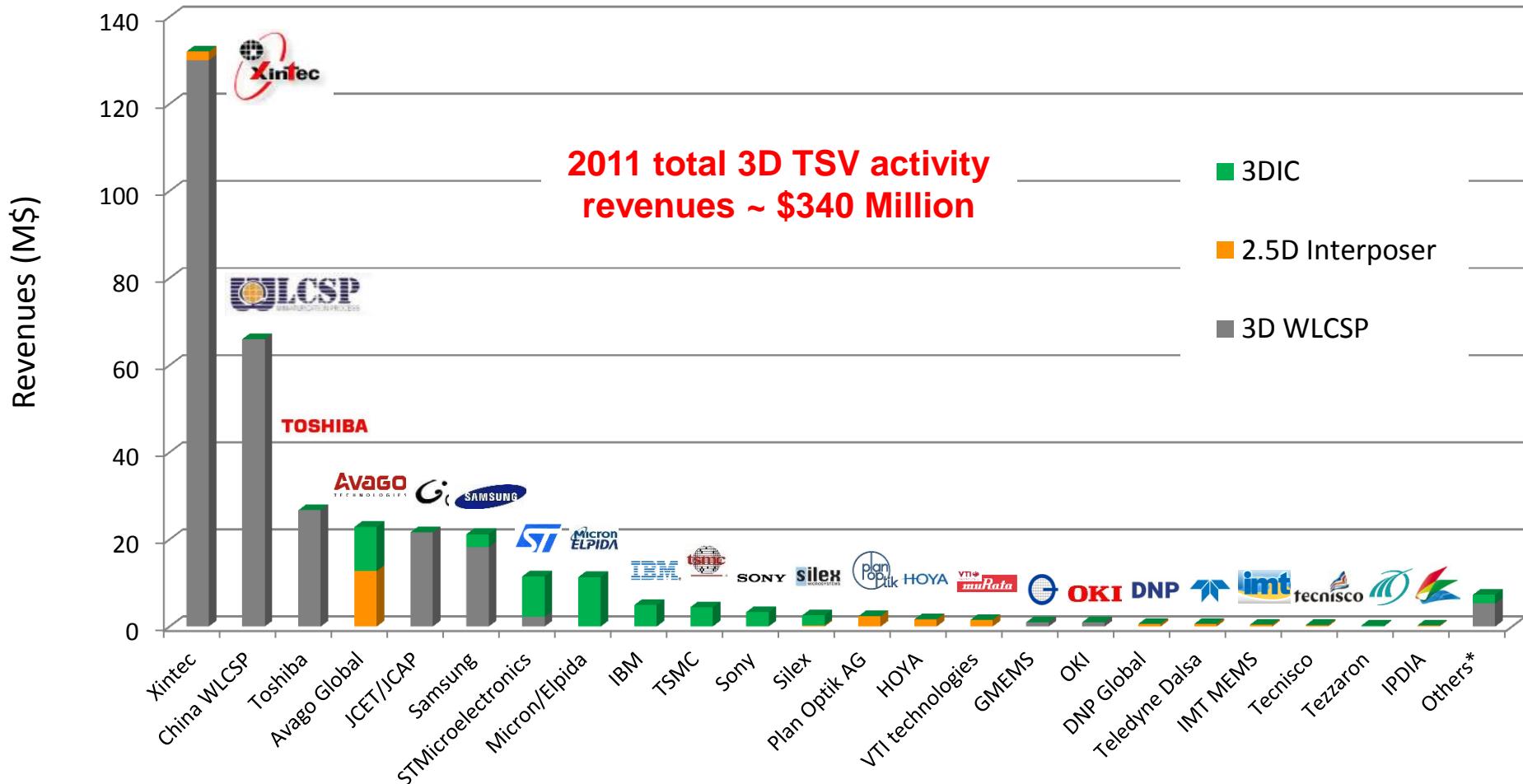


2011 Global 3D TSV activity - Breakdown by top players

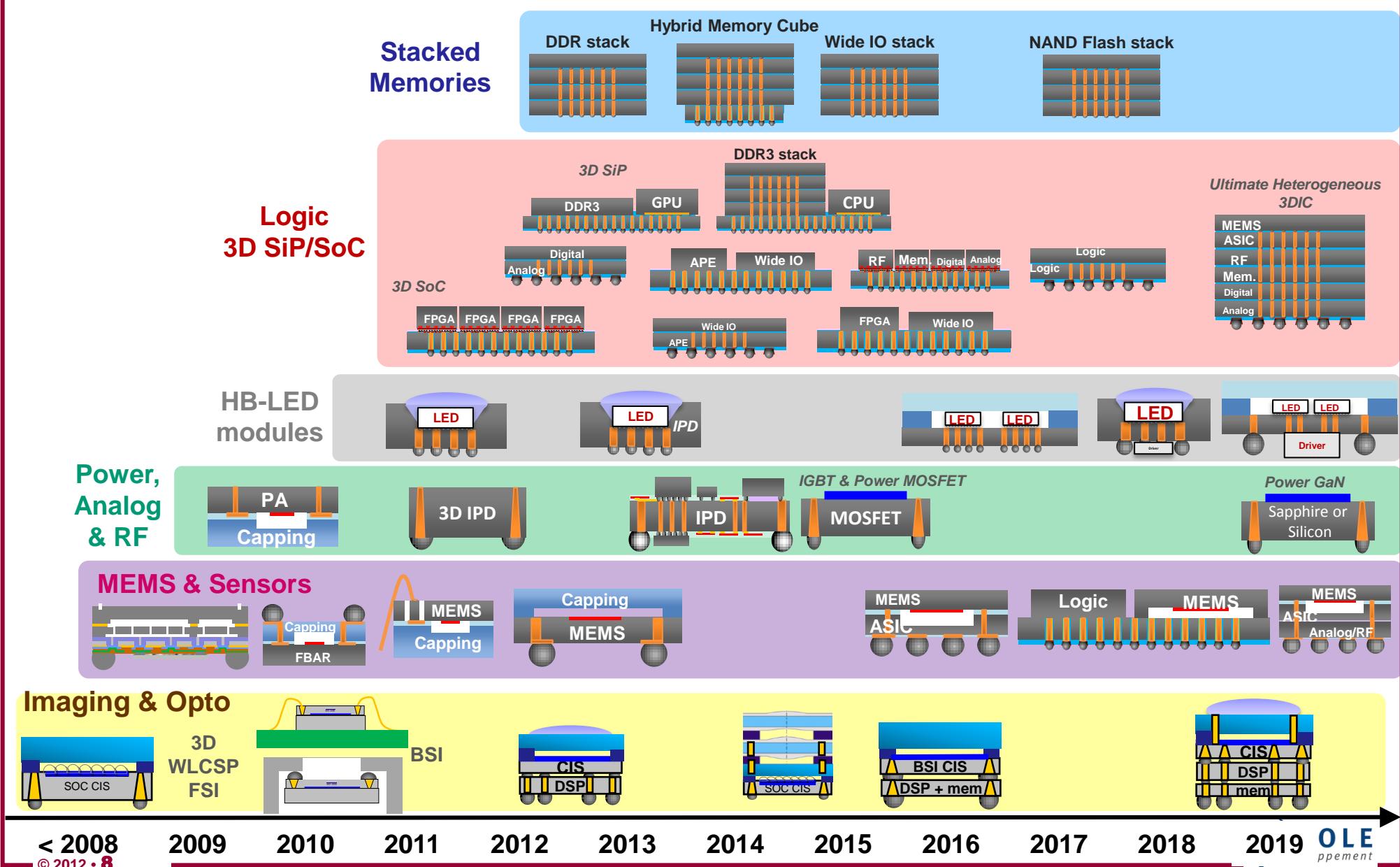
2011 global 3D TSV activity*

- Including internal production lines -

* Middle-end activity or revenues including
TSV etching, Via Filling, RDL, Bumping,
wafer test & wafer level assembly



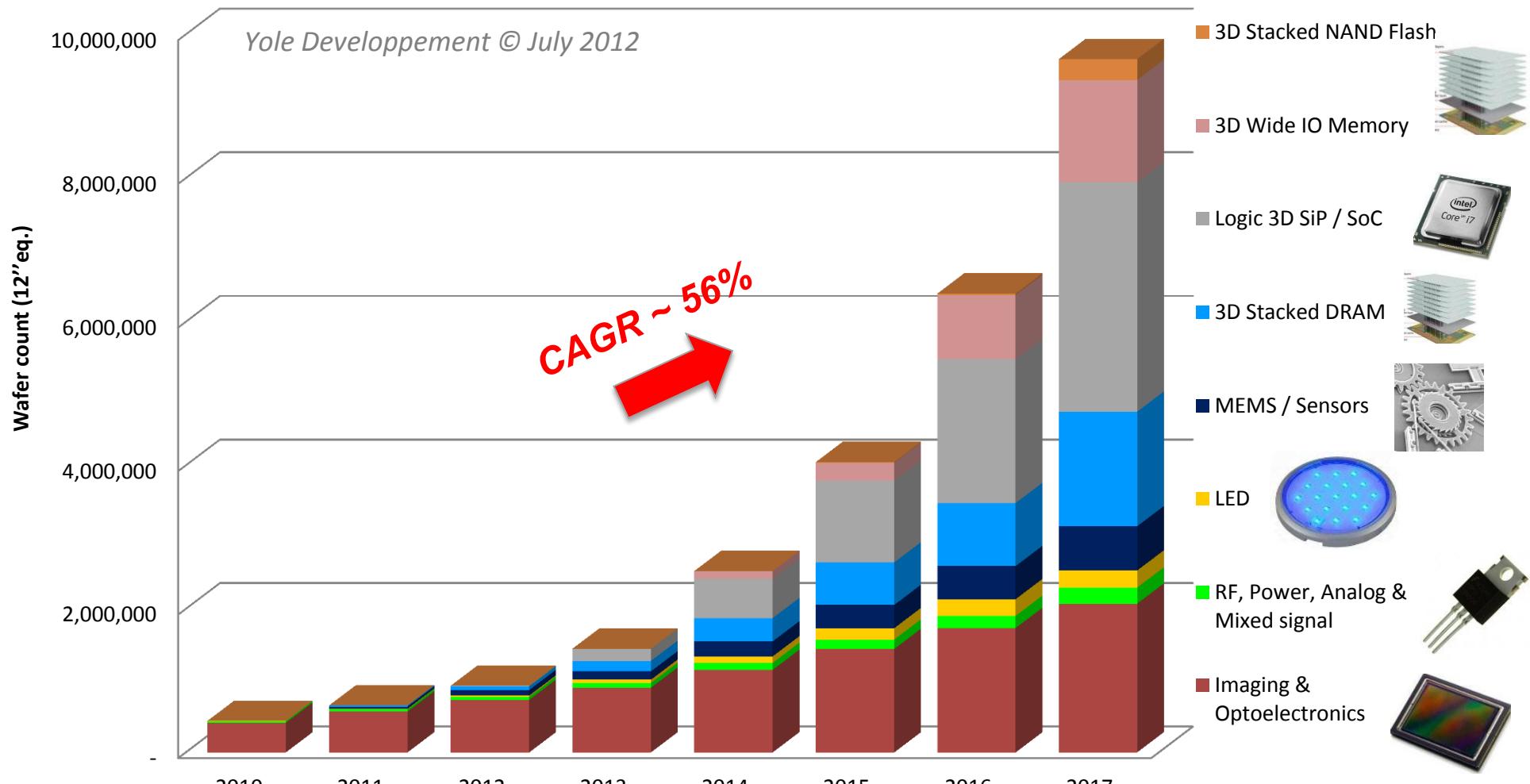
Global 3DIC & TSV interconnects roadmap



Global TSV chip wafer forecast

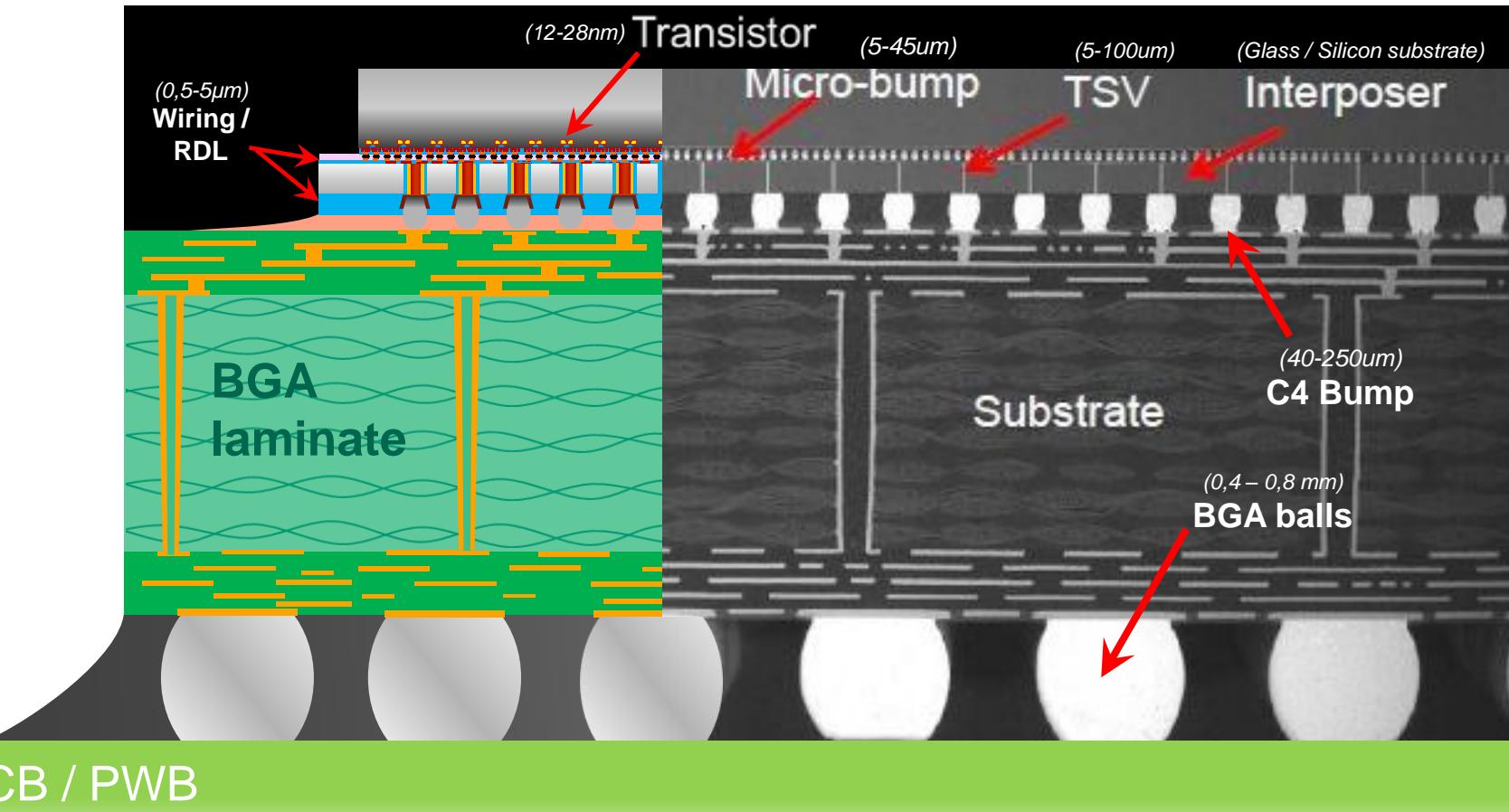
Global TSV Chip Wafer Forecast (All 3D Platforms)

Breakdown by Segment (12"eq wafers)



Why 2.5D glass / silicon interposers are needed?

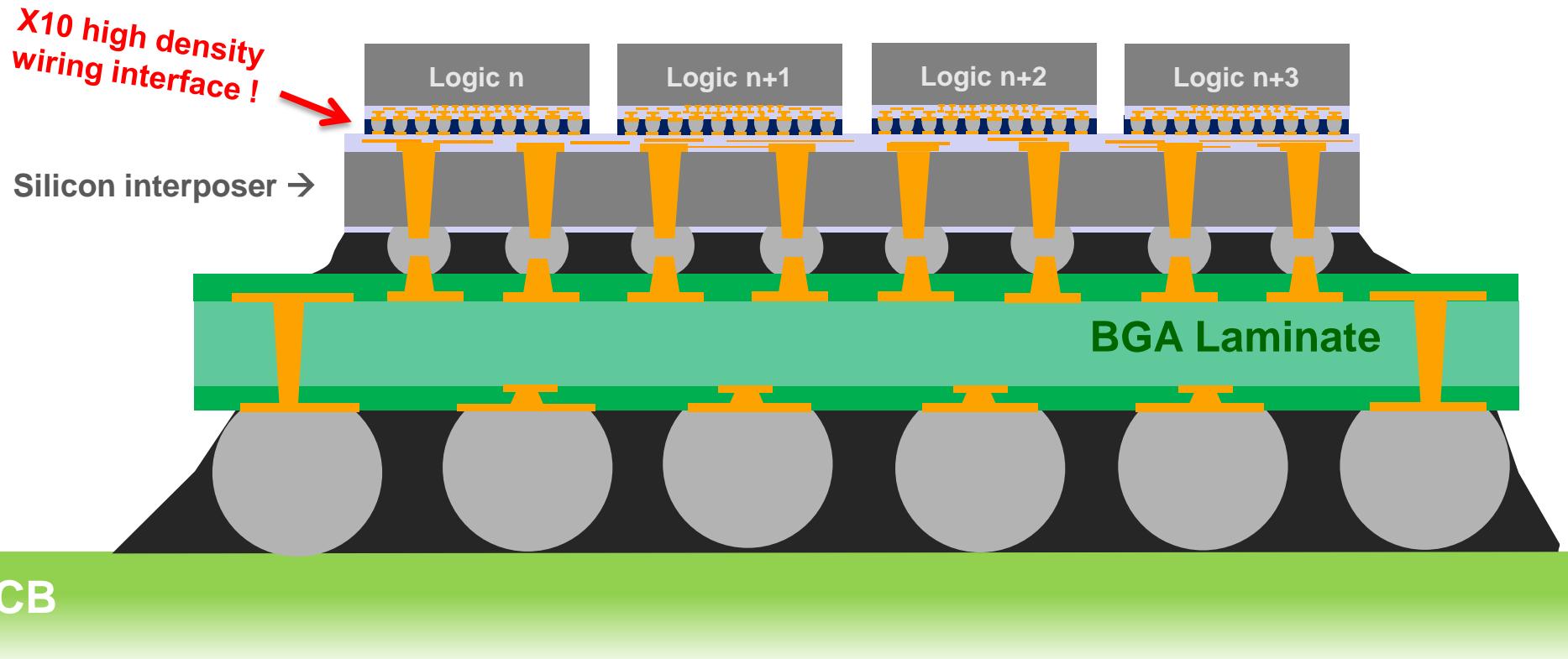
- 2.5D Glass / Silicon interposers are emerging as key substrate elements for connecting the nanometer to millimeter worlds in future semiconductor chip packaging assembly



2.5D interposer solution

for Large die Logic applications (FPGA, ASICs, DSP, etc...)

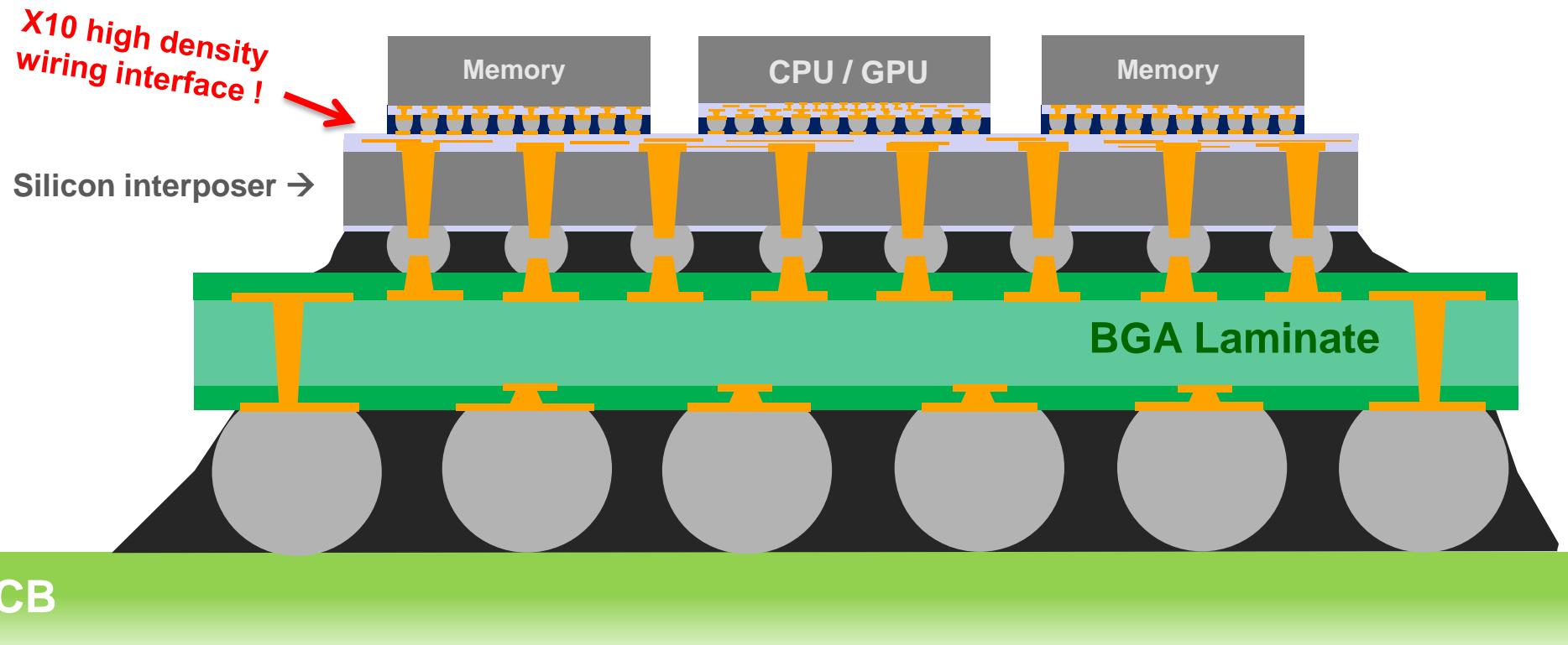
- **'4 slices' instead of one die 3D-SOC re-partitionned logic design**
 - Increase back of CMOS manufacturing yield (because of smaller die size)
 - High density wiring at the surface of the 4 layer copper damascene silicon interposer wafer
→ breakthrough in COST versus POWER CONSUMPTION versus PERFORMANCE



2.5D interposer solution

for Logic + Memory integration (*FPGA, ASICs, DSP, CPU / GPU, etc...*)

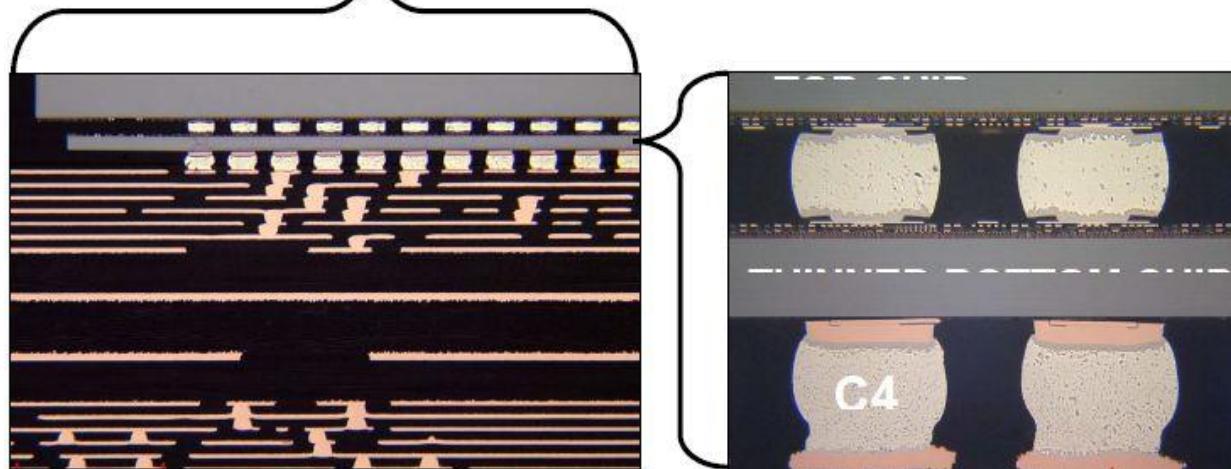
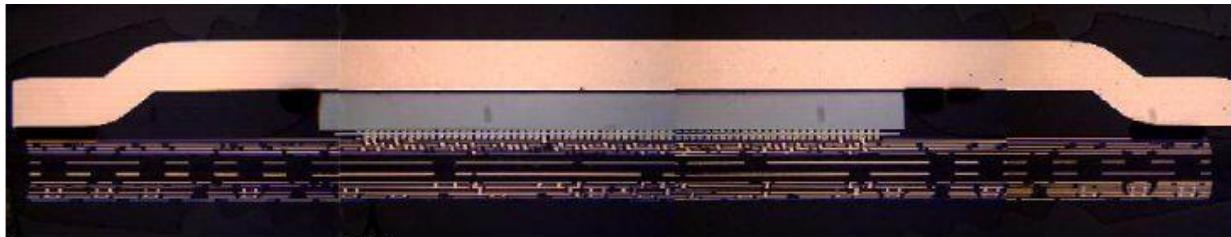
- **Breakthrough in bandwidth & performance versus power consumption**
 - Massive parallel DDR memory integration close to logic IC and interconnected through high density / high speed silicon interposer wiring layers
 - Unprecedented level of computing performance and thermal management possible (side by side)



2.5D interposers for large CPUs / GPUs



- Power 8 by IBM to be based on 2.5D Interposers
- Haswell, Intel GPU on 2.5D interposers for computing with lots of on board memory and ultra large data bus



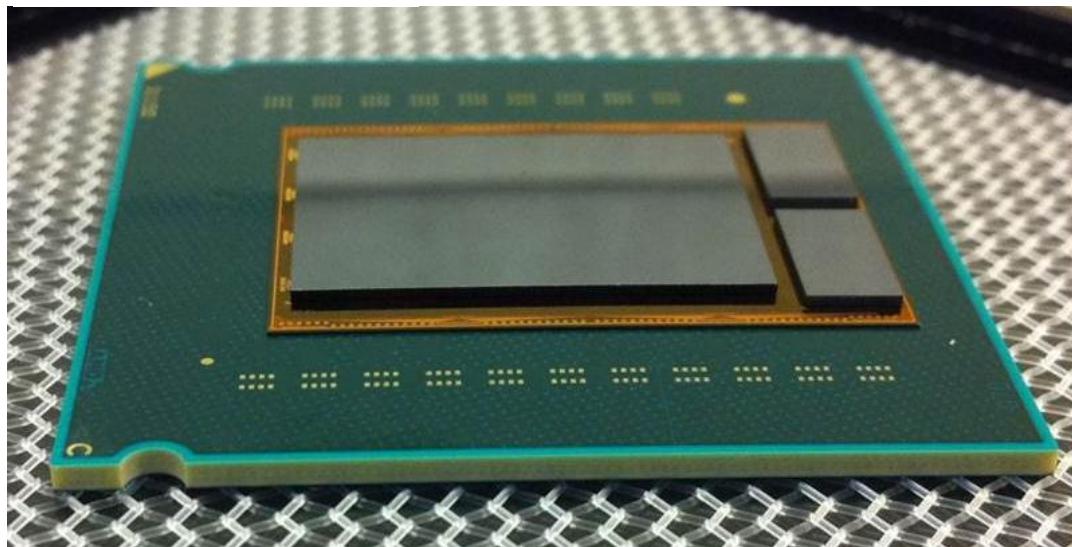
*IBM Power 7+: four 32nm CMOS multi-core CPU dies are placed side by side on a silicon interposer.
(Courtesy of SemiAccurate.com)*

*Cross section pictures of an IBM 3D stacked module demonstrator with TSVs in the thinner die
(courtesy of Chipworks)*

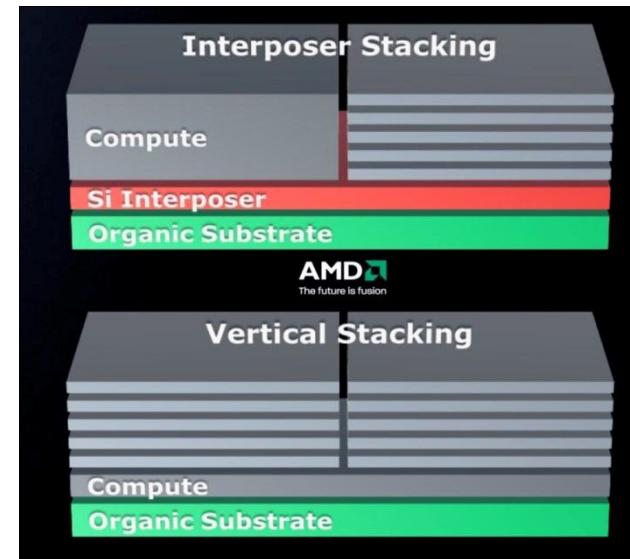
GPU in 2.5D for gaming console applications



- Sony PS4 (2013) will have a GPU on interposer with a 512-wide data bus and on interposer memory
 - Will probably be an AMD chip. Future gaming platforms will offer 3D imagery, which requires fast & high bandwidth computing power. 2.5D is unanimously praised as the solution for this purpose

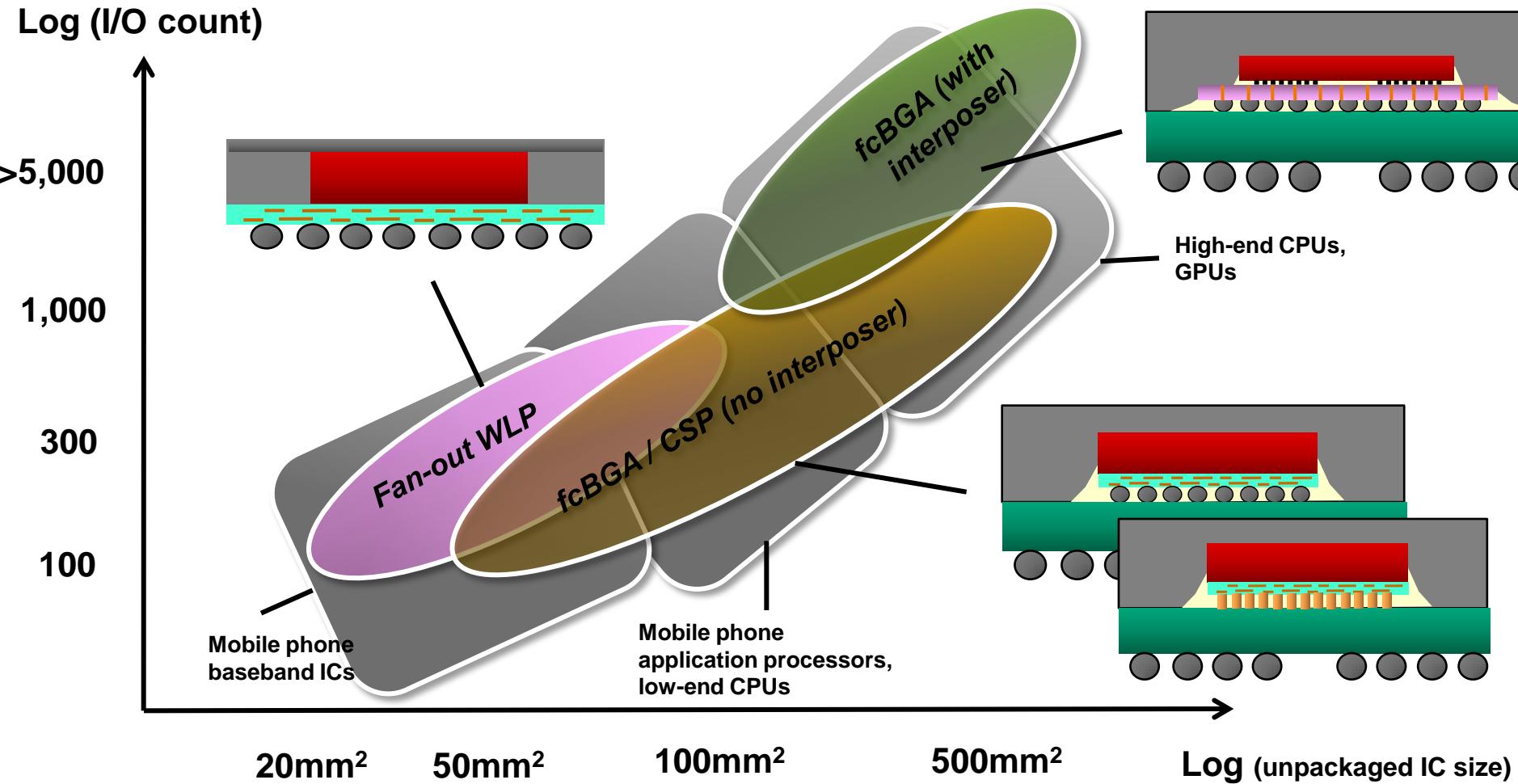


An interposer module for GPU demonstrator
Courtesy of Global Foundries, 2012



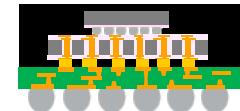
Logic-only 2.5D interposer

competing solutions for high performance / large digital single packaged ICs



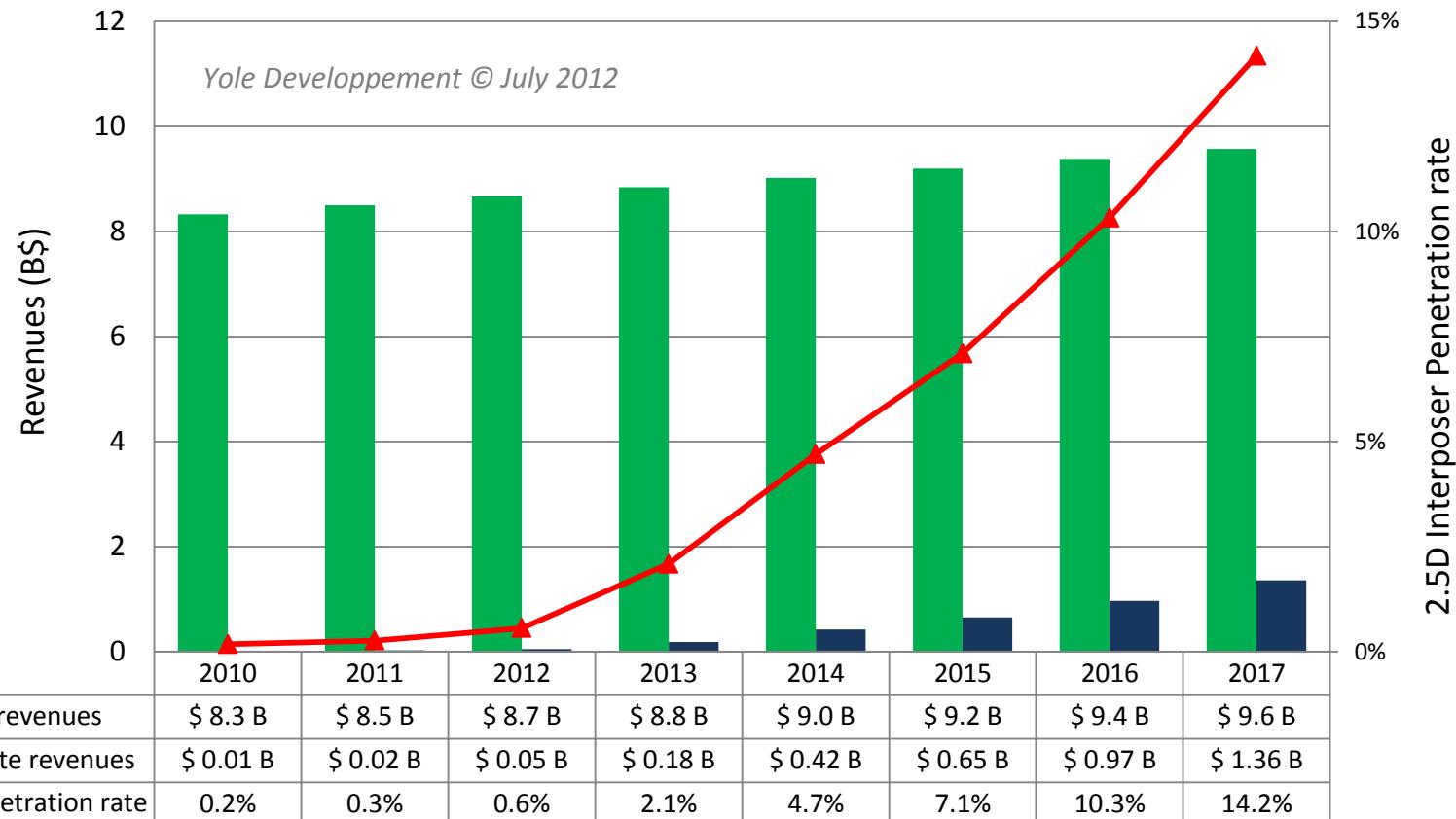
- Fan-out WLP and fcBGA with copper pillars are likely to take on most of today's fcBGA market
- Logic-only 3D interposers are only expected to develop for very high I/O density and I/O count processors

2.5D Interposer Platform Revenues



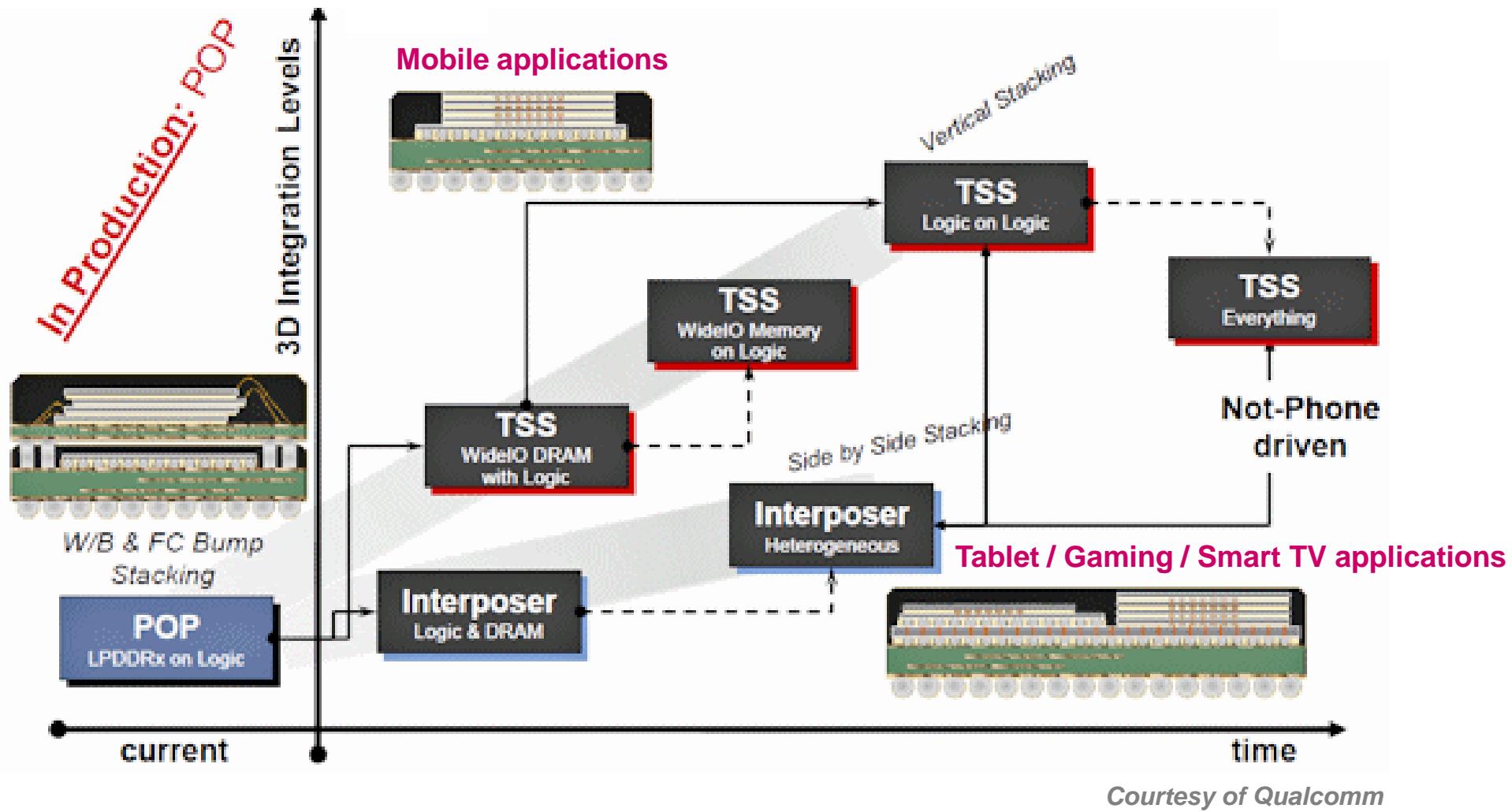
2.5D Glass & Silicon Interposer Platform Revenues

Comparison with laminate substrate industry (B\$)



- By 2017, we expect 2.5D interposer revenues to reach 14% of the packaging substrate market value

Qualcomm CPU roadmap: from PoP to 2.5D / 3DIC



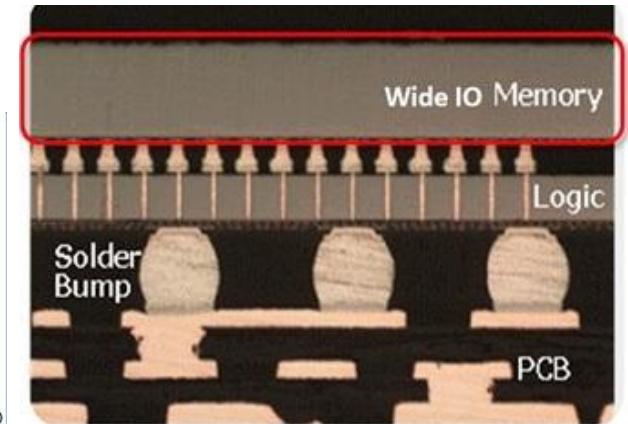
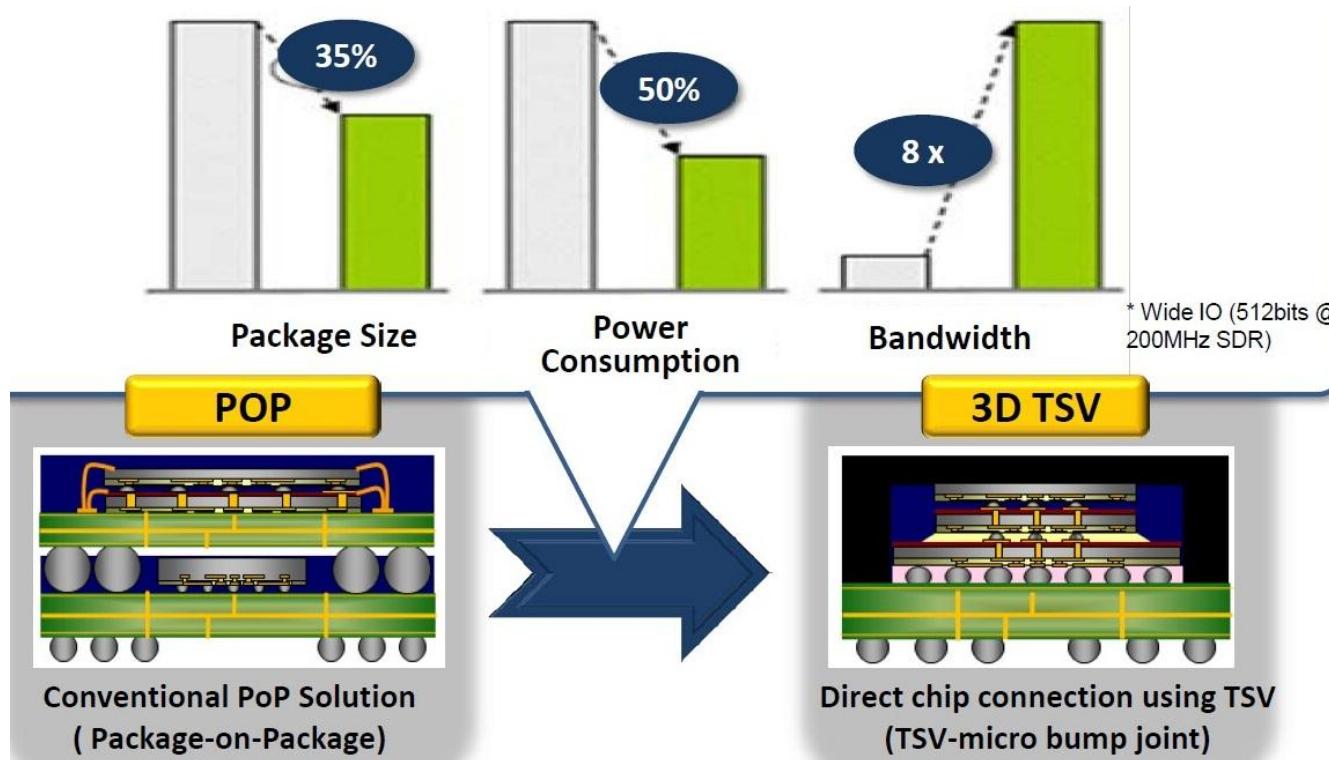
- Qualcomm is actively developing the 2.5D interposers & 3DIC architectures

Wide IO memories - Coming Soon!

Focus on Samsung's recent announcement

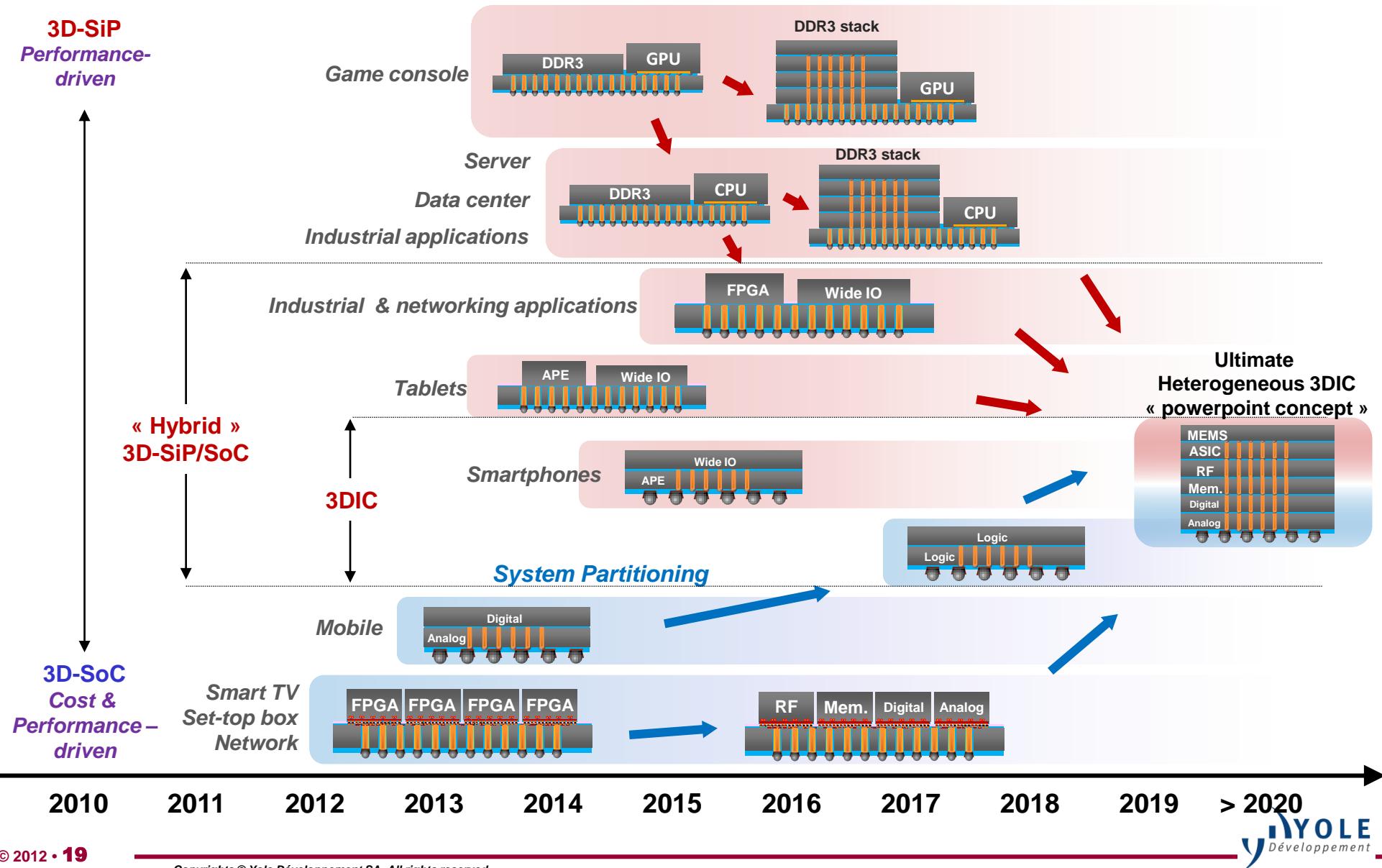


- Samsung foundry announced it will be ready next year to release 3D TSV Technology and Wide IO Memory!
 - Switching from a conventional PoP approach to 3D stack with wide IO memory will enable package size reduction by 35%, and power consumption by 50%
 - Bandwidth is expected to increase by 8



Courtesy of Samsung

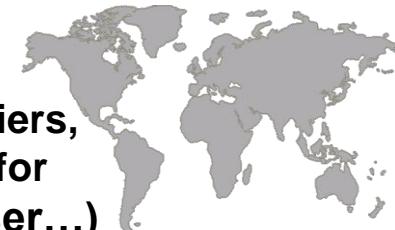
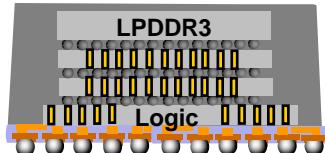
Logic 2.5D / 3D SoC verus SiP packaging roadmap



Roadblocks toward 2.5D / 3DIC commercialization in HVM

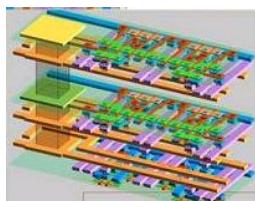
- There are 5 main challenges ahead for a wide adoption of 3DICs:

- **Infrastructure availability & supply chain:** availability of a second source 3D packaging service provider is critical before starting any production. Additionally, key strategic alliances / partnerships between memory suppliers, Logic IDMs, Foundries and Packaging subcontractors need to be in place for 3D SiP applications involving multiple-party ICs (memory, logic, interposer...)



- **I/O standardization** between interfaces such as memory / logic / interposer layers is also critical. Such specifications need to be defined in order to establish a standardized and flexible supply chain (e.g. of *JEDEC initiative for defining Wide IO memory standards for 3D TSV in consumer applications*)

- **Thermal management & interconnect reliability:** in many applications such as stacking of DRAM modules, SSD for enterprise market and memory + logic stacking applications, thermal management is certainly the biggest barrier to entry for 3D if we cannot manage to dissipate heat well through the whole package



- **Shift in the Design / Test method paradigm & system co-design:** heterogeneous functions, packaging, new CAD tools (thermal & mechanical simulation), test for KGD and new design architectures are required to get the full benefits of 3D

- **Cost:** depending on end-product, 3D TSV manufacturing cost should be reasonable and reduced in order to make it widely occurring in cost sensitive applications



TSV manufacturing tool-box

Technology Readiness Dashboard

Ready for HVM

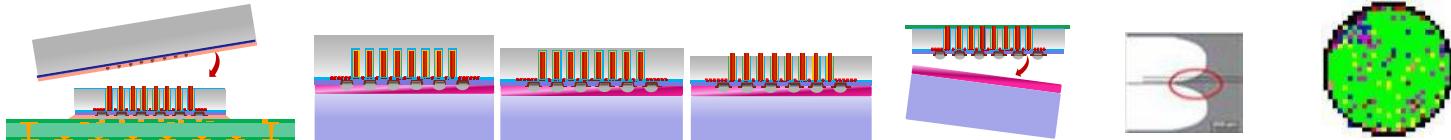
Ready for initial ramp-up

Not ready



TSV Middle Manufacturability

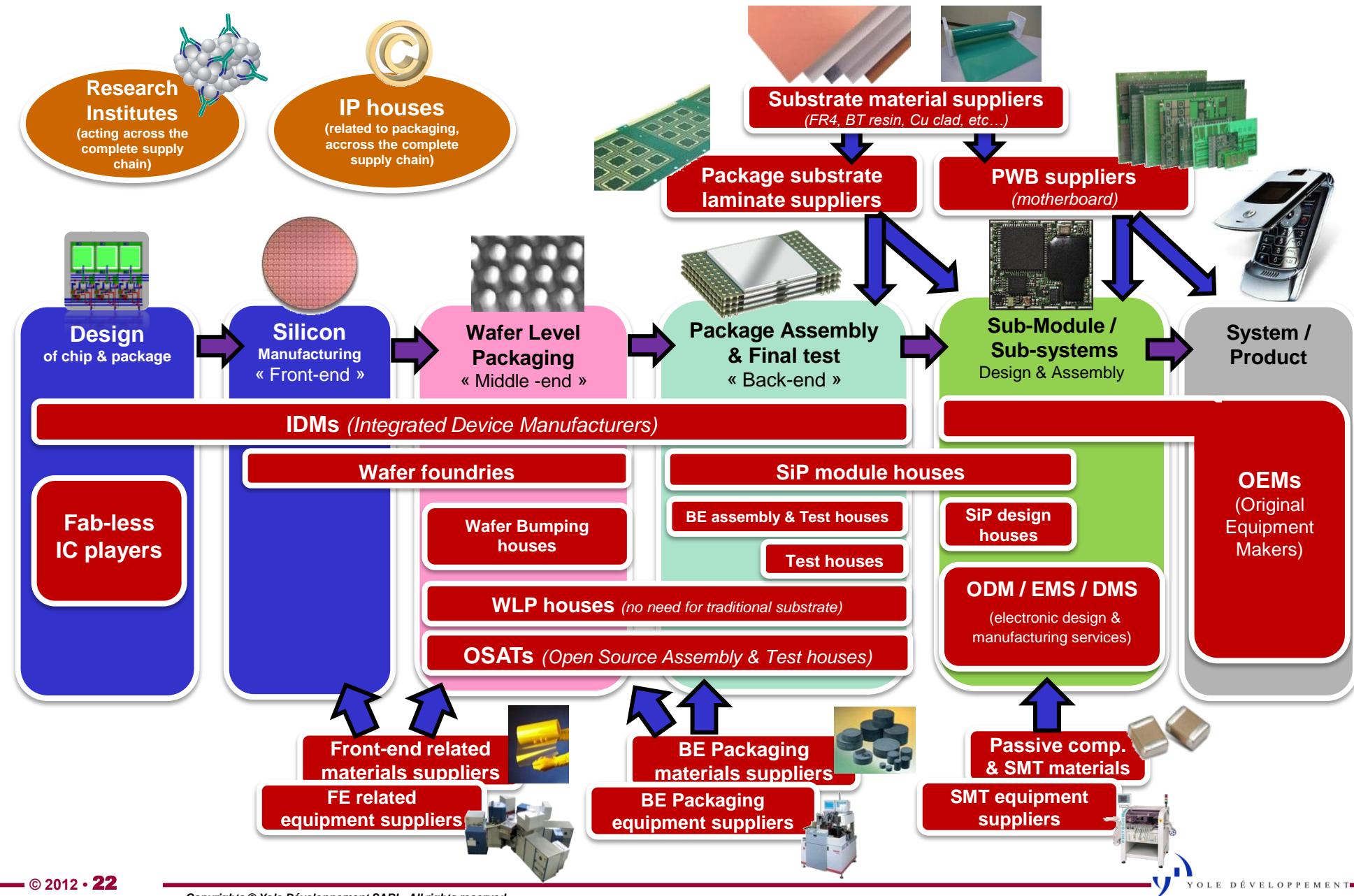
	TSV Lithography	TSV etching	TSV isolation	Barrier & Seed layer	TSV filling	CMP	Passiv./UBM & Bumping
Process performance (vs technical requirements)	Green	Green	Yellow	Yellow	Green	Green	Green
Repeatability Uniformity & process Window	Green	Green	Yellow	Yellow	Green	Green	Green
Tool availability & maturity	Green	Green	Yellow	Yellow	Green	Green	Green
Throughput & cost of Ownership	Yellow	Yellow	Yellow	Yellow	Yellow	Green	Green



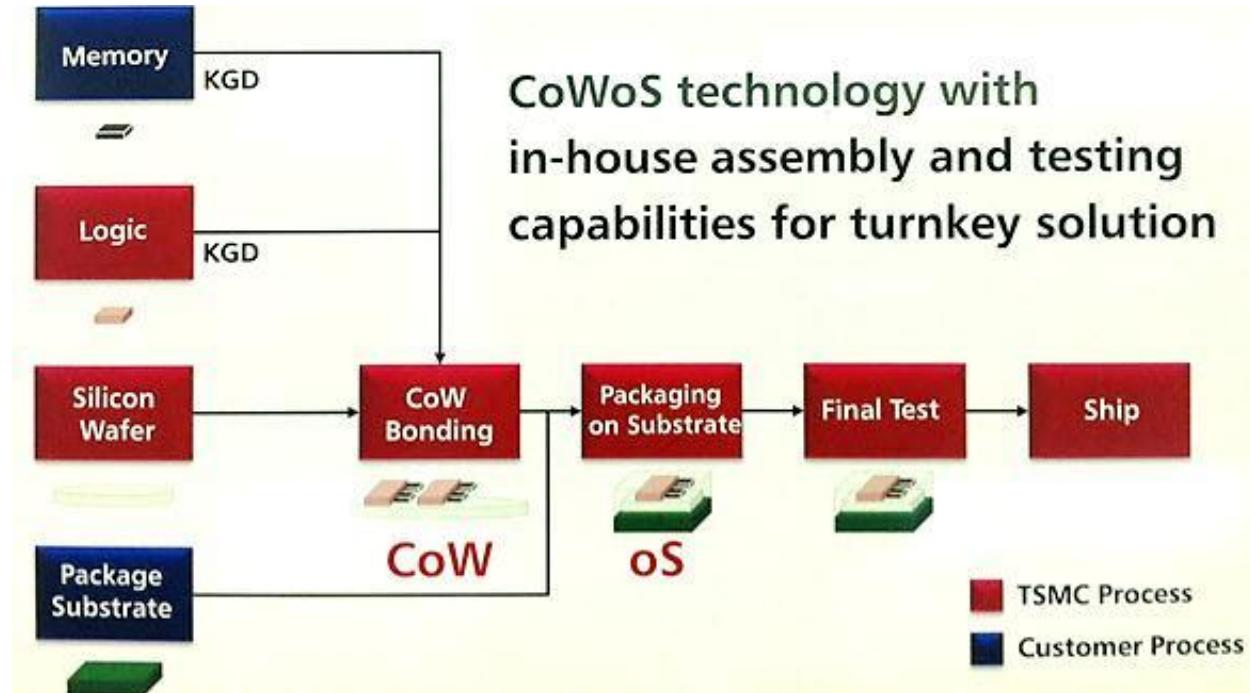
TSV Middle Manufacturability

	Stacking / Bonding			Temporary bonding to carrier	Thinning / grinding	TSV nailing	Carrier debonding	Inspection & metrology	Testing (probing & final test)
	C2C	C2W	W2W						
Process performance (vs technical requirements)	Yellow	Green	Green	Yellow	Green	Green	Yellow	Green	Yellow
Repeatability Uniformity & process Window	Yellow	Yellow	Yellow	Yellow	Yellow	Yellow	Red	Green	Yellow
Tool availability & maturity	Green	Red	Red	Red	Yellow	Yellow	Red	Yellow	Yellow
Throughput & cost of Ownership	Green	Red	Yellow	Yellow	Green	Green	Yellow	Green	Yellow

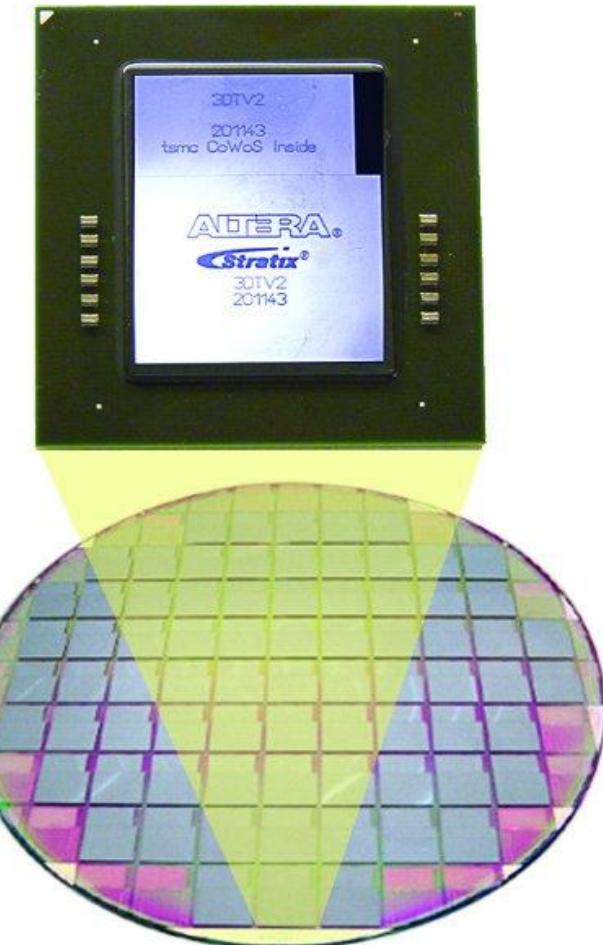
Complex IC packaging supply chain (main business models)



TSMC's Integrated Supply-Chain for efficient 2.5D Interposer integration



- TSMC's vertical integration move from wafer manufacturing to bumping, packaging, assembly & test will tackle the supply chain challenge related to the commercialization of 2.5D/3DIC modules



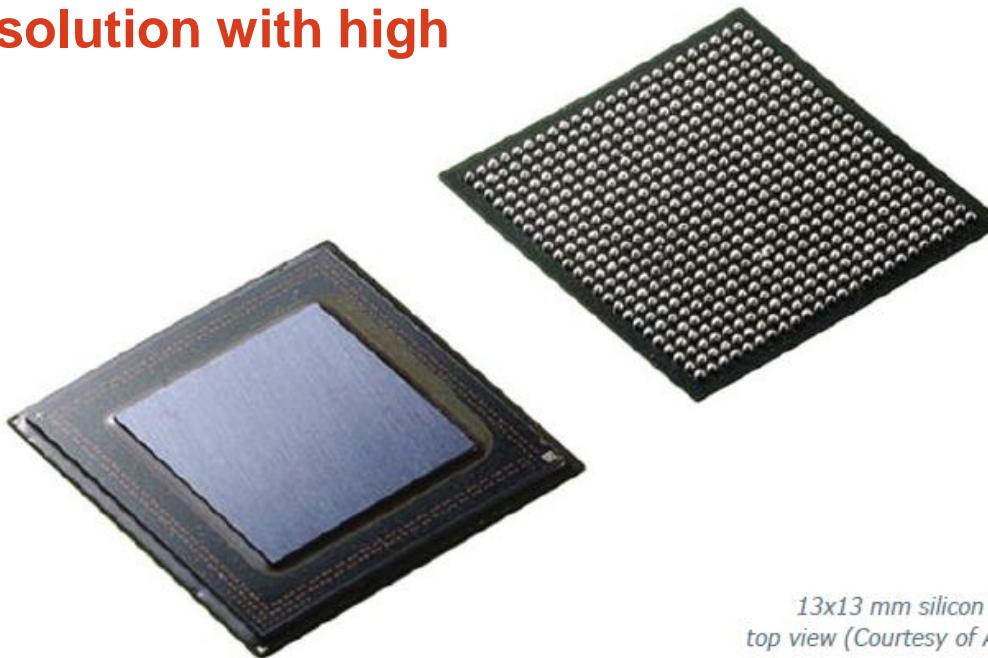
Altera's FPGA supported by
TSMC's CoWoS 2.5D interposer platform

ASE 2.5D silicon interposer platform

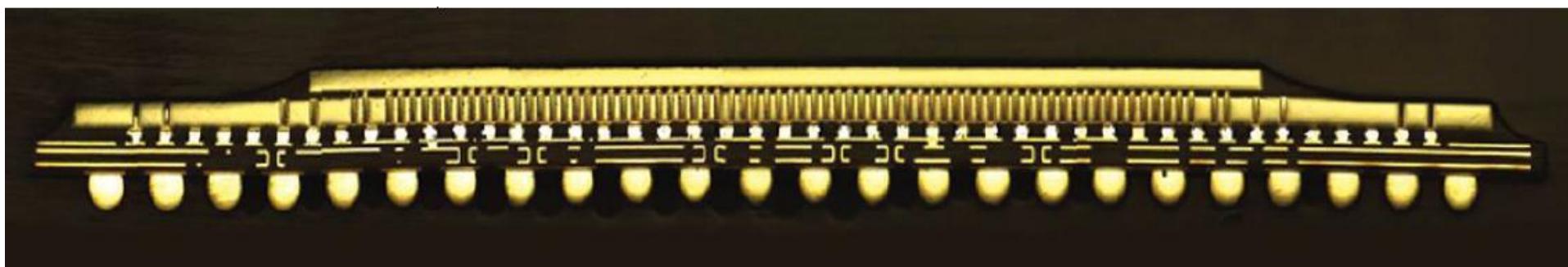


- ASE (TW) is developing 'coarse' type of 2.5D silicon interposer substrate solution with high electrical performances

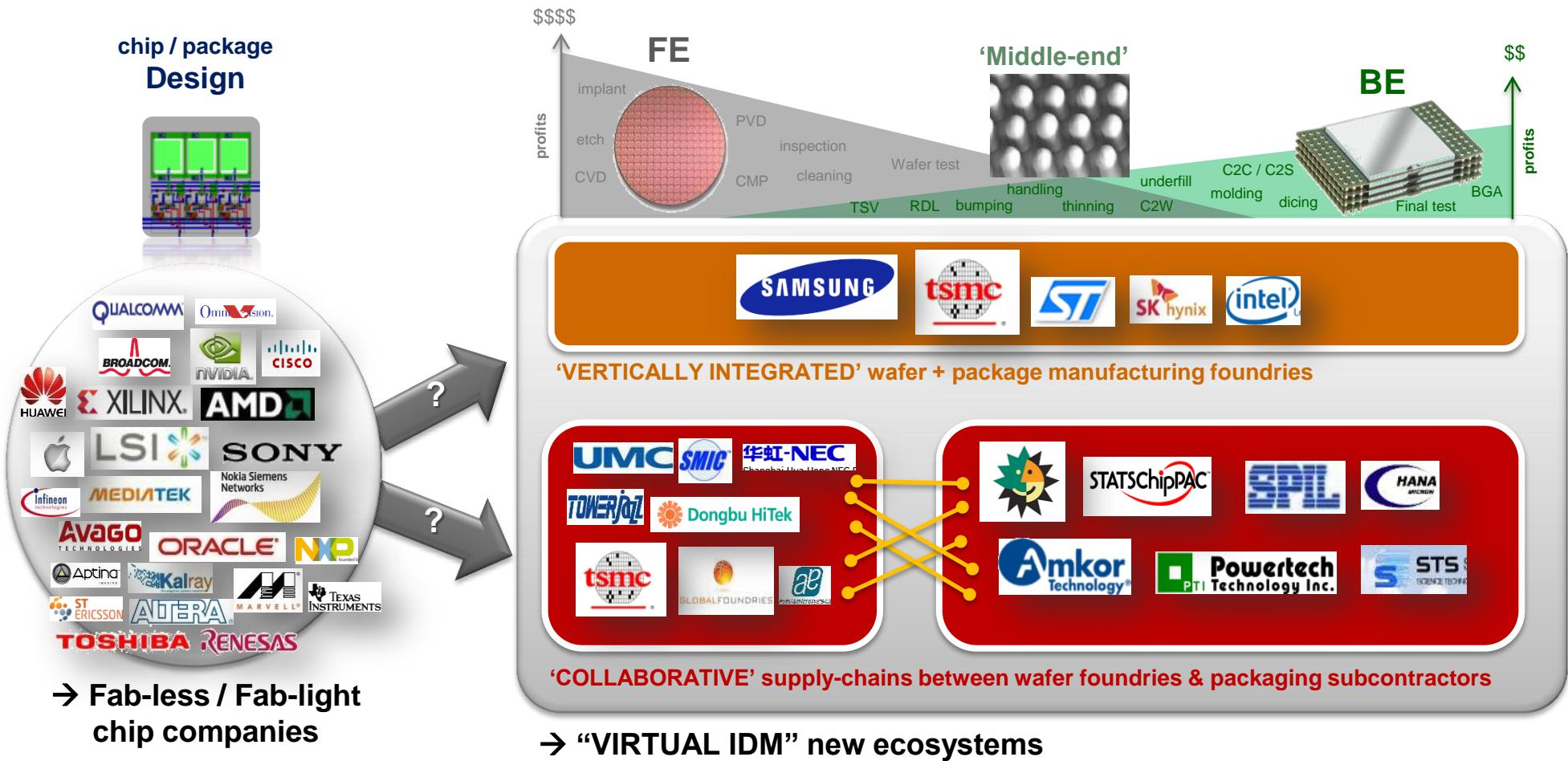
- 5/5 μ m to 10/10 μ m Line/Spaces (supported by RDL technology)
- 100-150 μ m thick silicon
- Via diameters of 30-50 μ m (DRIE or laser drilled)
- Copper via plating



13x13 mm silicon interposer,
top view (Courtesy of ASE Group)



Emerging 2.5D / 3DIC Open Ecosystems of “Virtual IDMs”



Silicon & Glass 2.5D Interposers: Who is doing what?

Coarse-pitch
Interposers
Fine-pitch
Interposers

	Wafer /panel supply	TSV/TGV making	Wiring (BEOL, RDL)	Interposer test	Bumping	Packaging & assembly	Final test
Silicon substrate makers							
Glass substrate makers	  						
IC wafer foundry							New TSMC model
MEMS wafer foundry (or IPD wafer foundry)							
OSATs							
PCB manufacturers			 				
IDMs							

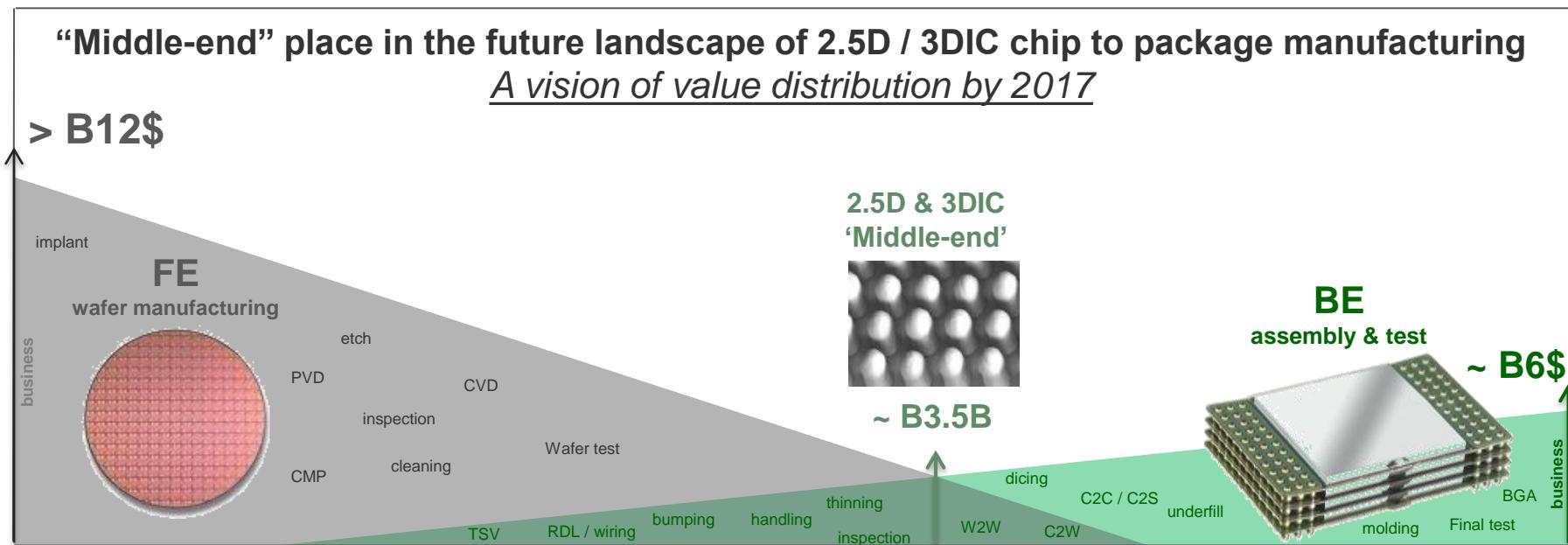
'Middle-end' versus 'Back-end' 2.5D / 3DIC opportunity

Global 3D TSV semiconductors packaging, assembly & test market value



- The “role sharing” between each party is not obvious
 - Indeed, the “middle-end” space is almost a ‘zero-margin’ business, while front-end wafer manufacturing as well as back-end assembly & test remain profitable enough areas for sustainable business. We estimate that the global 3D TSV semiconductors packaging, assembly and test markets will reach \$9B in business by 2017

“Middle-end” place in the future landscape of 2.5D / 3DIC integration



- It is clear from this picture that the OSAT suppliers have a defined role to play in the future landscape for 2.5D & 3DIC packages:
 - First in the back-end area, where their large infrastructure and expertise in advanced assembly & test will be key in the successful ramp-up of ever more complex 3D package products
 - Secondly, in the ‘middle-end’ area by establishing strategic collaborations with key IDM and wafer foundries in the IC industry, in order to partner ‘tactically’ while leveraging the high capacity of investment of these powerful semiconductor chip companies

→ Taken alone, the back-end space represents a clear opportunity for sustainable growth for major OSAT suppliers in this emerging “2.0” advanced packaging industry. However, this segment won’t be accessible without the settlement of a viable ecosystem, including putting the back-end to middle-end processing together. Expect “vertically integrated” and “collaborative” models to emerge as the most successful in this game!

Thank you very much for your attention!



NEW
Yole Développement
headquarters:
Le Quartz
75 cours Émile Zola
69100 Lyon-Villeurbanne
France
Phone: +33 472 83 01 80
Email: info@yole.fr



Yole Inc.
One DeMercurio Drive, Suite 6
Allendale, NJ 07401 - USA
Phone: +1 (650) 906 7877

Yole K. K.
Level 20 Marunouchi Trust Tower
Main - 1-8-3 Marunouchi
Chiyoda-ku 100-0005 Tokyo - Japan
Phone: +81 362 693 457

NEW
Taiwan Office
7F, 307, Dunhua N. Rd.
Taipei 10583 - Taiwan
Phone: +886 (0)9 3757 6016

NEW
Korea Office
#1510 Hanrim Tower 7-3
Hwayang-dong - Gwangin-gu,
Seoul 143-717 - Korea
Phone: +82 10 4097 5810

www.yole.fr - www.i-micronews.com

Visit us during Semicon'Taiwan 2012 @ Booth #1327