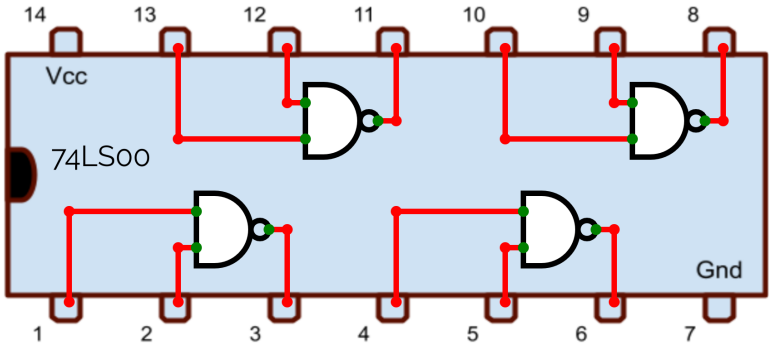
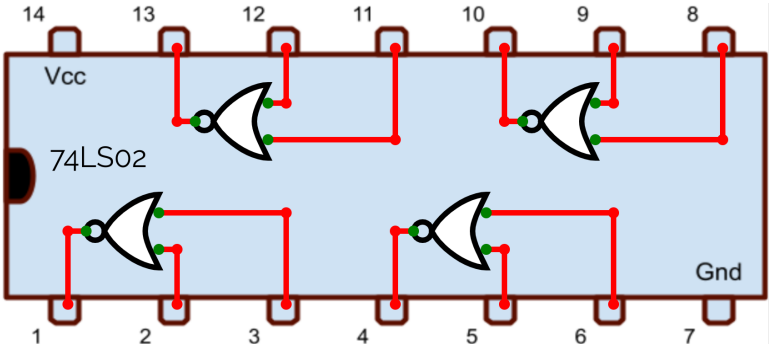
ECE 265 Lab kit IC pin-outs

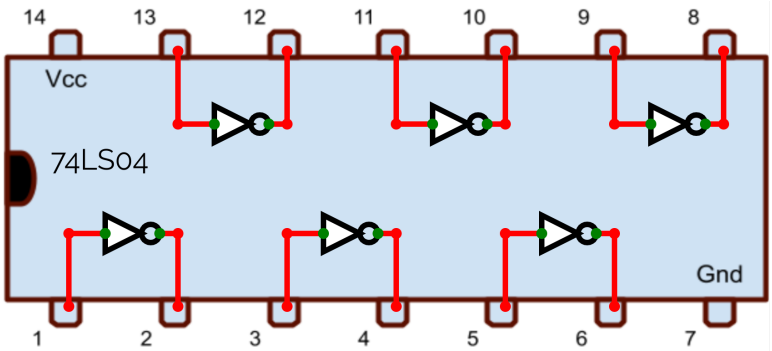
74LS00, QUAD 2-INPUT NAND GATE



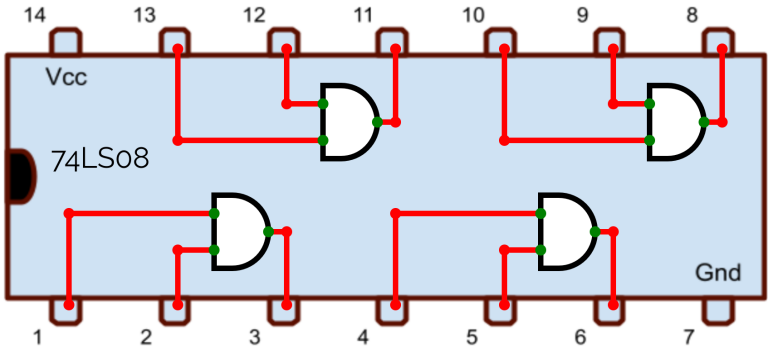
74LS02, QUAD 2-INPUT NOR GATE



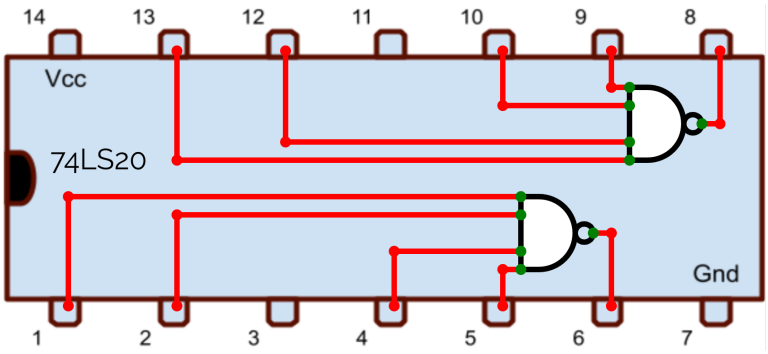
74LS04, HEX INVERTER



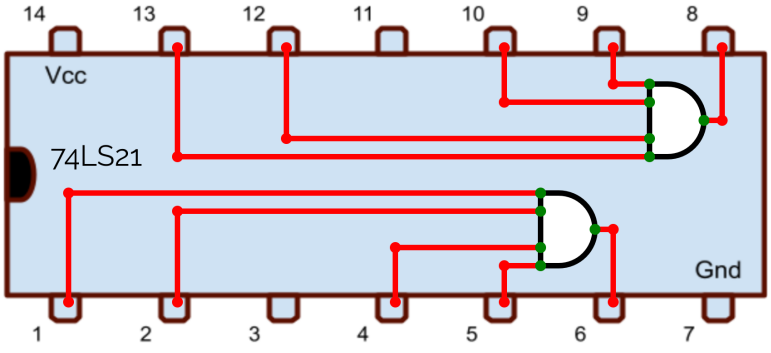
74LS08, QUAD 2-INPUT AND GATE



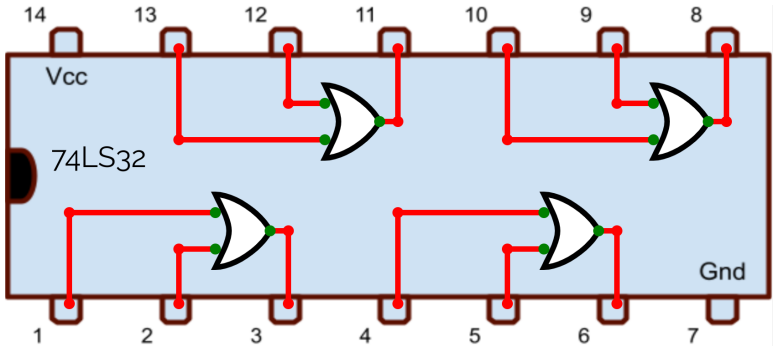
74LS20, DUAL 4-INPUT NAND GATE



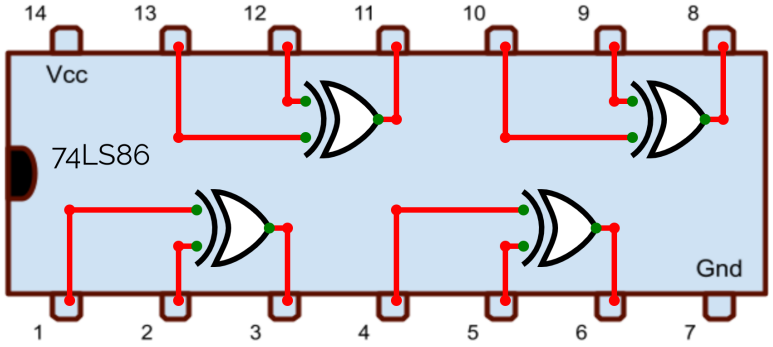
74LS21, DUAL 4-INPUT AND GATE



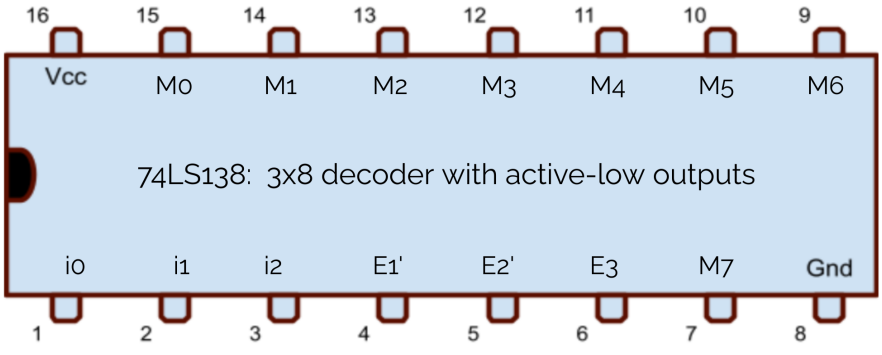
74LS32, QUAD 2-INPUT OR GATE



74LS86, QUAD 2-INPUT XOR GATE



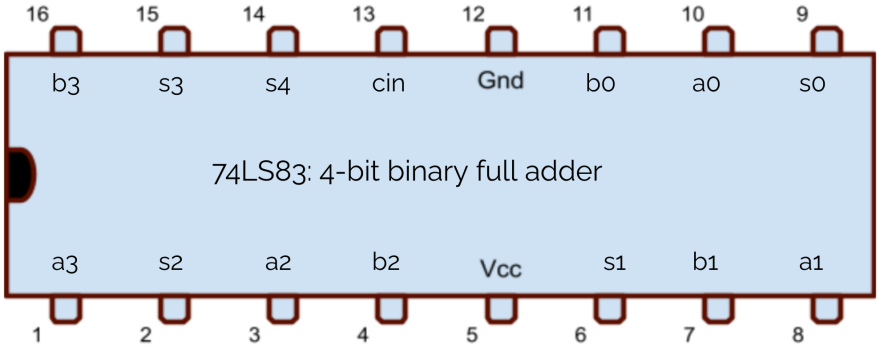
74S138, 3-to-8 DECODER



When the decoder is enabled (E1’ = E2’ = 0, E3 = 1), Maxterm functions of {i2, i1, i0} are produced at the outputs. Otherwise, all outputs are high.

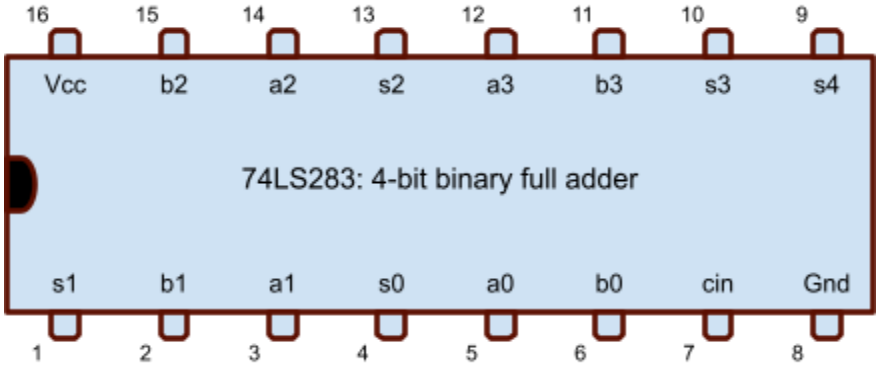
Your lab kit will include one of these two binary adder IC's. They are functionally identical, and differ only in the pin assignments:

74LS83, 4-BIT BINARY FULL ADDER



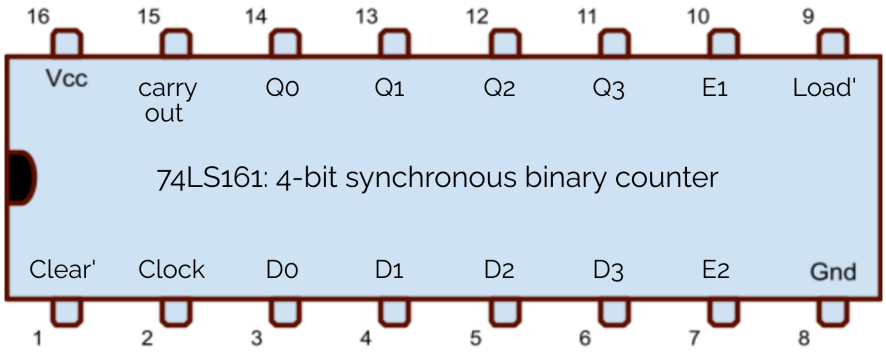
{s4 s3 s2 s1 s0} = {a3 a2 a1 a0} + {b3 b2 b1 b0} + {0 0 0 cin}

74LS283, 4-BIT BINARY FULL ADDER



{s4 s3 s2 s1 s0} = {a3 a2 a1 a0} + {b3 b2 b1 b0} + {0 0 0 cin}

74LS161, 4-BIT BINARY COUNTER



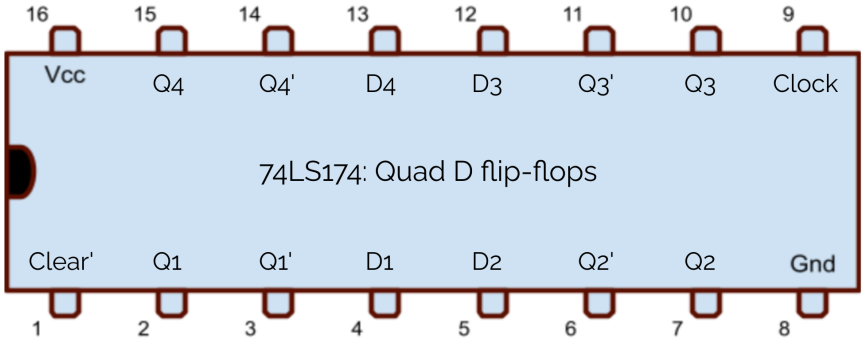
For normal counting up in binary, E1 = E2 = Load’ = Clear’ = 1 (see note below): then the output word {Q3 Q2 Q1 Q0} increments at every positive clock edge.

To initialize the count, E1 = E2 = Clear’ = 1, Load’ = 0: {Q3 Q2 Q1 Q0} are loaded with data from inputs {D3 D2 D1 D0} on the next rising clock edge.

When Clear’ = 0, the count is immediately cleared to {0 0 0 0}.

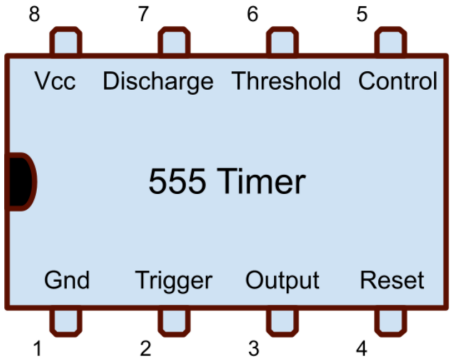
Note: in the LS TTL logic family, unconnected inputs are interpreted as = 1.

74LS175, QUAD D FLIP-FLOP



When the clock has a rising edge, all four flip-flops are updated according to their respective data inputs. Flip-flops are immediately reset to zero when Clear’ = 0.

555 TIMER


8
7
6
5
Vcc
Discharge
Threshold
Control
555 Timer
Gnd
Trigger
Output
Reset
1
2
3
4