REC Register Description

ADDRESS	BITS	FUNCTION
$DF00 57088	7-0	***Status Register*** – Read Only 7 – Interrupt Pending 1 = Interrupt waiting to be serviced 6 – End of Block 1 = Transfer complete 5 – Fault 1 = Block verify error 4 – Size 0 = Total expansion = 128K 1 = Total expansion = 512K 3-0 – Version Note: Bits 7-5 are cleared when this register is read
$DF01 57089	7-0	***Command Register*** – Read/Write 7 – *Execute!* 1 = Transfer per current config 6 – Reserved 5 – Load 1 = Enable AUTOLOAD option 4 – FF00 1 = Disable FF00 decode 3 – Reserved 2 – Reserved 1,0 – Transfer type: 00 = transfer from C64 to RAM module 01 = transfer from RAM module to C64 10 = swap between C64 and RAM module 11 = verify C64 and RAM module
$DF02 57090	7-0	C64 Base Address, LSB – Read/Write Lower 8 bits of base address
$DF03 57091	7-0	C64 Base Address, MSB – Read/Write Upper 8 bits of base address
$DF04 57092	7-0	RAM module address, LSB – Read/Write Lower 8 bits of base address
$DF05 57093	7-0	RAM module address, MSB – Read/Write Upper 8 bits of base address
$DF06 57094	2-0	RAM module bank – Read/Write RAM module bank pointer Bits 2 (MSB) to 0 (LSB) are significant
$DF07 57095	7-0	Transfer length, LSB – Read/Write Lower 8 bits of the byte counter
$DF08 57096	7-0	Transfer length, MSB – Read/Write Upper 8 bits of the byte counter
$DF09 57097	7-5	***Interrupt Mask Register*** – Read/Write 7 – Interrupt enable 1 = Interrupt enabled 6 – End of Block mask 1 = Interrupt on end of block 5 – Verify error 1 = Interrupt on verify error
$DF0A 57098	7-6	***Address Control Register*** – Read/Write 00 = Increment both addresses (default) 01 = Fix RAM module addresses 10 = Fix C64 addresses 11 = Fix both addresses