### 7.1.2. 8080-Ⅰ Series Parallel Interface

ILI9341 can be accessed via 8-/9-/16-/18-bit MCU 8080-Ⅰ series parallel interface. The chip-select CSX (active low) is used to enable or disable ILI9341 chip. The RESX (active low) is an external reset signal. WRX is the parallel data write strobe, RDX is the parallel data read strobe and D[17:0] is parallel data bus.

ILI9341 latches the input data at the rising edge of WRX signal. The D/CX is the signal of data/command selection. When D/CX='1', D [17:0] bits are display RAM data or command's parameters. When D/CX='0', D [17:0] bits are commands.

The 8080-Ⅰ series bi-directional interface can be used for communication between the MCU controller and LCD driver chip. The 8080-Ⅰ Interface selection is done when IM3 pin is low state (VSS level). Interface bus width can be selected by IM [2:0] bits.

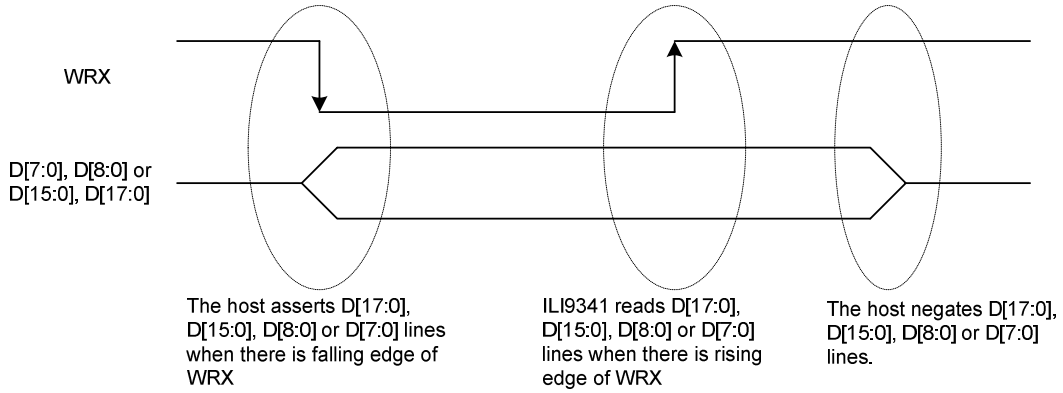
The selection of 8080-Ⅰ series parallel interface is shown as the table in the following.

| IM3 | IM2 | IM1 | IM0 | MCU-Interface Mode | CSX | WRX | RDX | D/CX | Function |
|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 8080 MCU 8-bit bus interface Ⅰ | "L" | ↑ | "H" | "L" | Write command code. |
| | | | | | "L" | "H" | ↑ | "H" | Read internal status. |
| | | | | | "L" | ↑ | "H" | "H" | Write parameter or display data. |
| | | | | | "L" | "H" | ↑ | "H" | Reads parameter or display data. |
| 0 | 0 | 0 | 1 | 8080 MCU 16-bit bus interface Ⅰ | "L" | ↑ | "H" | "L" | Write command code. |
| | | | | | "L" | "H" | ↑ | "H" | Read internal status. |
| | | | | | "L" | ↑ | "H" | "H" | Write parameter or display data. |
| | | | | | "L" | "H" | ↑ | "H" | Reads parameter or display data. |
| 0 | 0 | 1 | 0 | 8080 MCU 9-bit bus interface Ⅰ | "L" | ↑ | "H" | "L" | Write command code. |
| | | | | | "L" | "H" | ↑ | "H" | Read internal status. |
| | | | | | "L" | ↑ | "H" | "H" | Write parameter or display data. |
| | | | | | "L" | "H" | ↑ | "H" | Reads parameter or display data. |
| 0 | 0 | 1 | 1 | 8080 MCU 18-bit bus interface Ⅰ | "L" | ↑ | "H" | "L" | Write command code. |
| | | | | | "L" | "H" | ↑ | "H" | Read internal status. |
| | | | | | "L" | ↑ | "H" | "H" | Write parameter or display data. |
| | | | | | "L" | "H" | ↑ | "H" | Reads parameter or display data. |

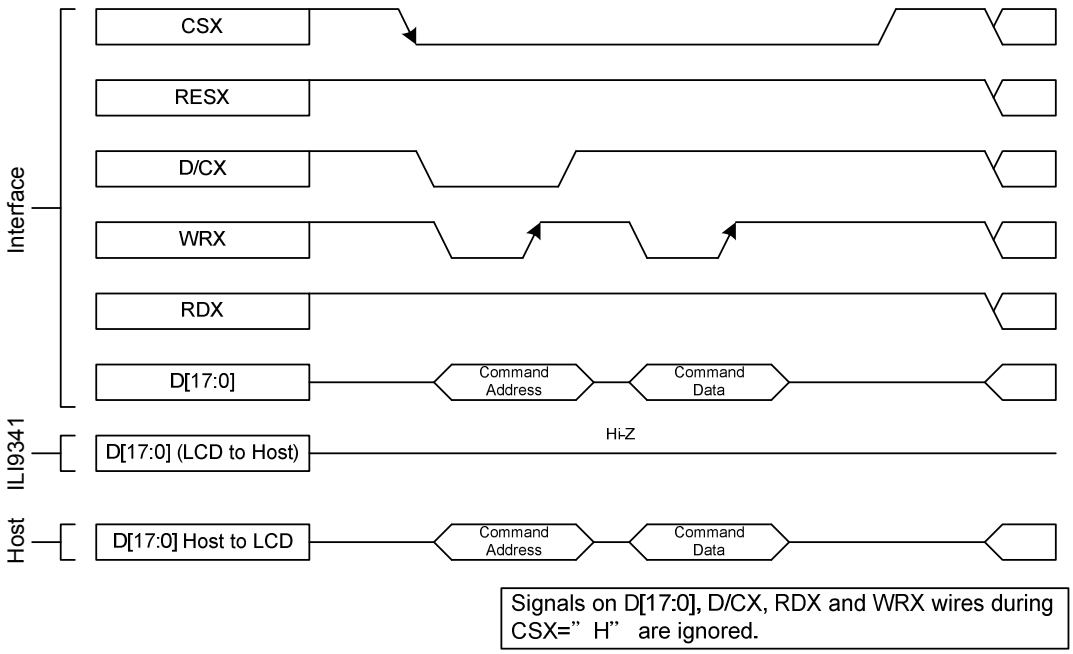
### 7.1.3. Write Cycle Sequence

The WRX signal is driven from high to low and then be pulled back to high during the write cycle. The host processor provides information during the write cycle when the display module captures the information from host processor on the rising edge of WRX. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command information. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command's parameter.

The following figure shows a write cycle for the 8080- Ⅰ MCU interface.



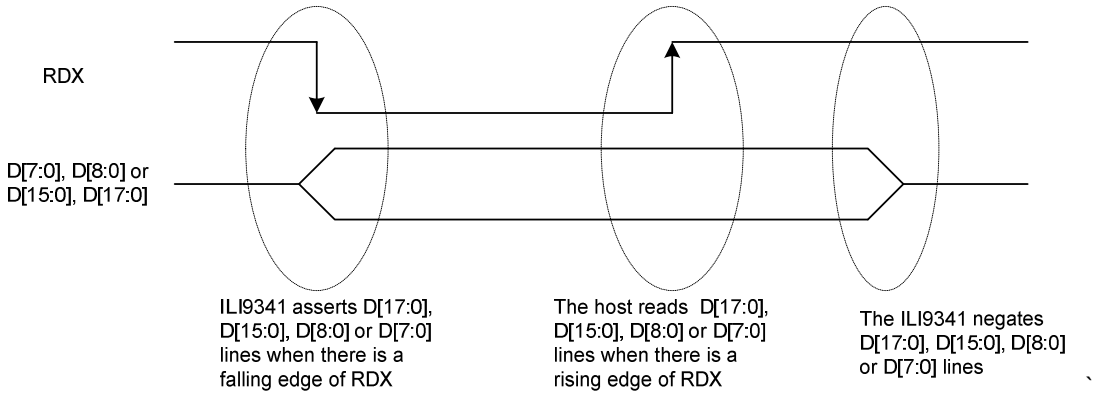

*Note: WRX is an unsynchronized signal (It can be stopped)*



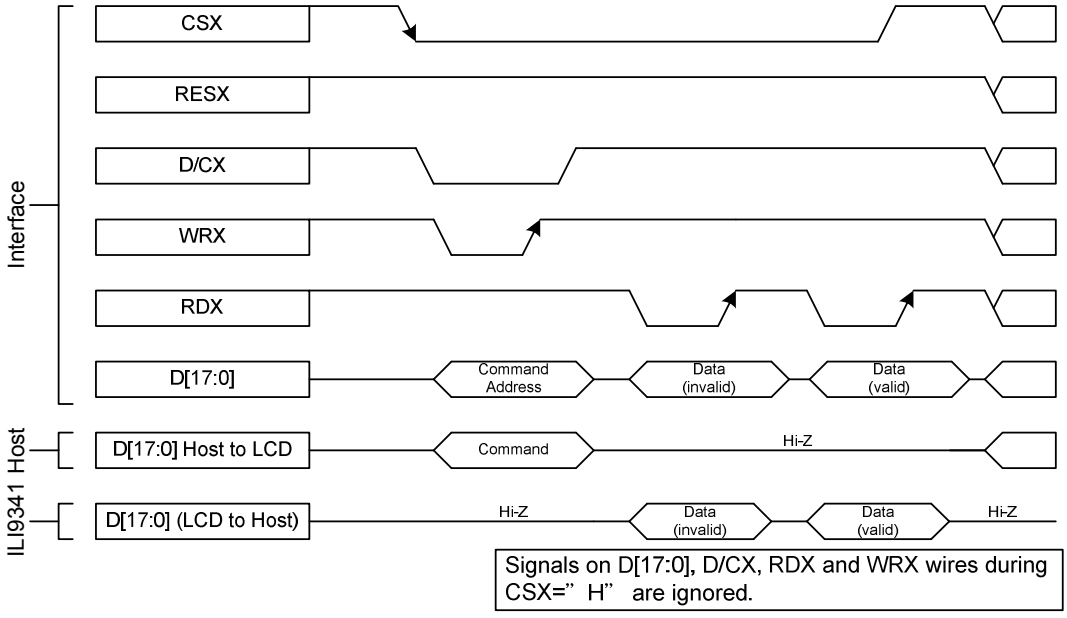
### 7.1.4. Read Cycle Sequence

The RDX signal is driven from high to low and then allowed to be pulled back to high during the read cycle. The display module provides information to the host processor during the read cycle while the host processor reads the display module information on the rising edge of RDX signal. When the D/CX signal is driven to low level, then input data on the interface is interpreted as command. The D/CX signal also can be pulled high level when the data on the interface is RAM data or command parameter.

The following figure shows the read cycle for the 8080- Ⅰ MCU interface.

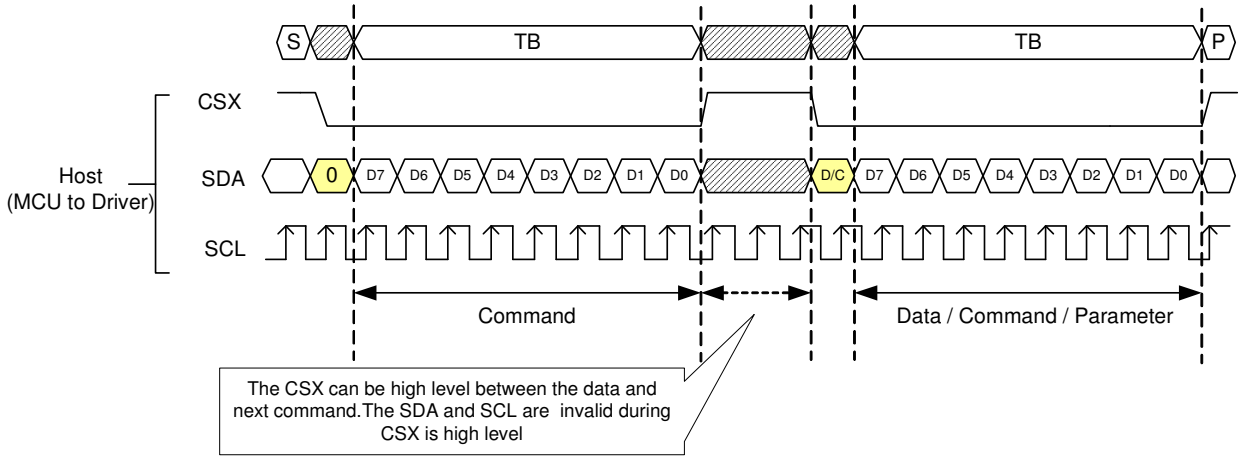



*Note: RDX is an unsynchronized signal (It can be stopped).*

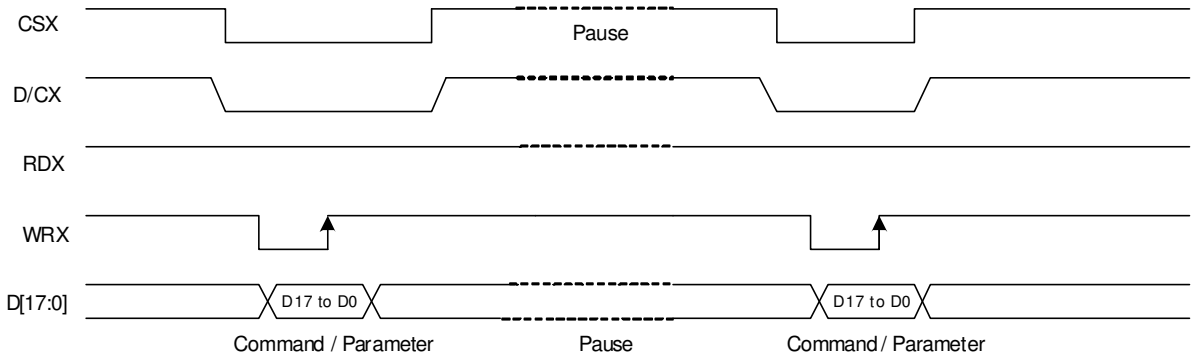



*Note: Read data is only valid when the D/CX input is pulled high. If D/CX is driven low during read then the display information outputs will be High-Z.*

### 7.1.13. Serial Interface Pause (3_wire)




### 7.1.14. Parallel Interface Pause

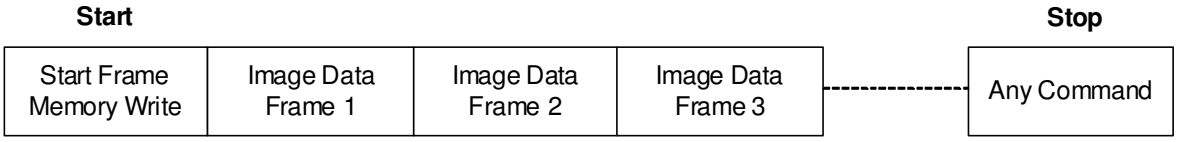


### 7.1.15. Data Transfer Mode

ILI9341 can provide two different kinds of color depth (16-bit/pixel and 18-bit/pixel) display data to the graphic RAM. The data format is described for each interface. Data can be downloaded to the frame memory by 2 methods.

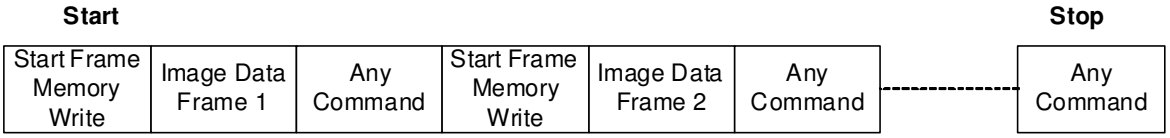
### 7.1.16. Data Transfer Method 1

The image data is sent to the frame memory in the successive frame writing, each time the frame memory is filled by image data, the frame memory pointer is reset to the start point and the next frame is written.




### 7.1.17. Data Transfer Method 2

Image data is sent and at the end of each frame memory download, a command is sent to stop frame memory writing. Then start memory write command is sent, and a new frame is downloaded.




*Note 1: These methods are applied to all data transfer color modes on both serial and parallel interfaces.*

*Note 2: The frame memory can contain both odd and even number of pixels for both methods. Only complete pixel data will be stored in the frame memory.*

## 7.5. Display Data RAM (DDRAM)

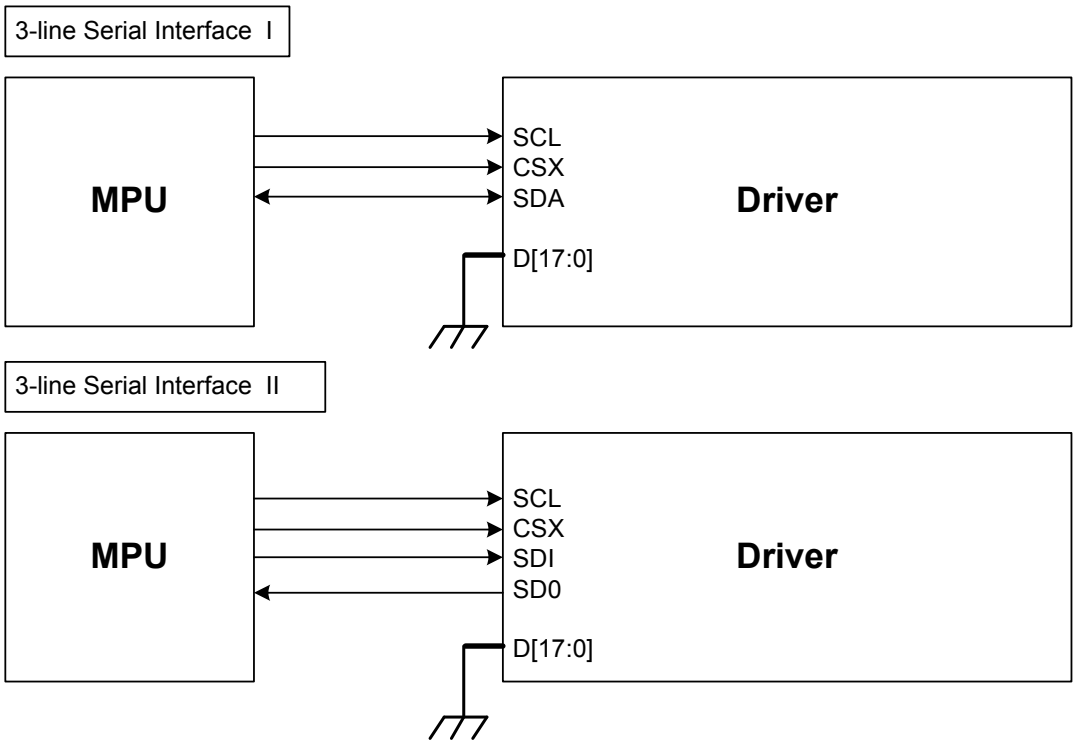
ILI9341 has an integrated 240x320x18-bit graphic type static RAM. This 172,800-byte memory allows storing a 240xRGBx320 image with an 18-bit resolution (262K-color). There is no abnormal visible effect on the display when there are simultaneous panel display read and interface read/write to the same location of the frame memory.

## 7.6. Display Data Format

ILI9341 supplies 18-/16-/9-/8-bit parallel MCU interface with 8080-Ⅰ/8080-Ⅱ series, 3-/4-line serial interface and 6-/16-18-bit parallel RGB interface. The parallel MCU interface and serial interface mode can be selected by external pins IM [3:0] and RGB interface mode can be selected by software command parameters RCM[1:0].

### 7.6.1. 3-line Serial Interface

The 3-line/9-bit serial bus interface of ILI9341 can be used by setting external pin as IM [3:0] to “0101” for serial interface I or IM [3:0] to “1101” for serial interface II. The shown figure is the example of 3-line SPI interface.



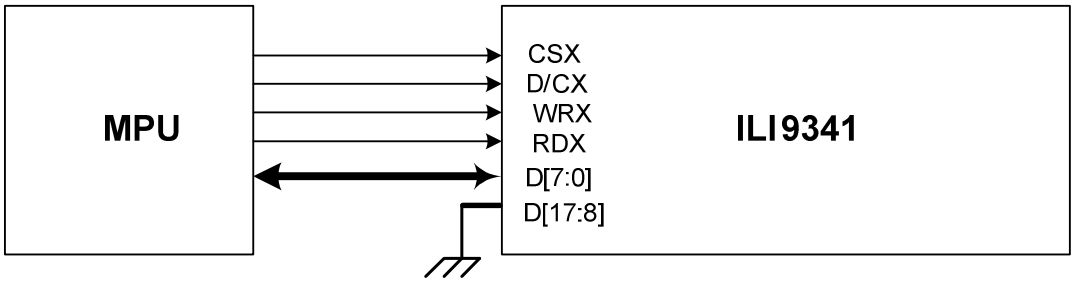

In 3-line serial interface, different display data format is available for two color depths supported by the LCM listed below.

-65k colors, RGB 5, 6, 5 -bits input

-262k colors, RGB 6, 6, 6 -bits input.

### 7.6.3. 8-bit Parallel MCU Interface

The 8080-Ⅰ system 8-bit parallel bus interface of ILI9341 can be used by setting external pin as IM [3:0] to "0000".The following shown figure is the example of interface with 8080-Ⅰ MCU system interface.




Different display data formats are available for two color depths supported by listed below.

- 65K-Colors, RGB 5, 6, 5 -bits input data.
- 262K-Colors, RGB 6, 6, 6 -bits input data.

#### 65K color: 16-bit/pixel (RGB 5-6-5 bits input)

One pixel (3 sub-pixels) display data is sent by 2 byte transfers when DBI [2:0] bits of 3Ah register are set to "101".

| Count | 0 | 1 | 2 | 3 | 4 | … | 477 | 478 | 479 | 480 |
|---|---|---|---|---|---|---|---|---|---|---|
| D/CX | 0 | 1 | 1 | 1 | 1 | … | 1 | 1 | 1 | 1 |
| D7 | C7 | 0R4 | 0G2 | 1R4 | 1G2 | … | 238R4 | 238G2 | 239R4 | 239G2 |
| D6 | C6 | 0R3 | 0G1 | 1R3 | 1G1 | … | 238R3 | 238G1 | 239R3 | 239G1 |
| D5 | C5 | 0R2 | 0G0 | 1R2 | 1G0 | … | 238R2 | 238G0 | 239R2 | 239G0 |
| D4 | C4 | 0R1 | 0B4 | 1R1 | 1B4 | … | 238R1 | 238B4 | 239R1 | 239B4 |
| D3 | C3 | 0R0 | 0B3 | 1R0 | 1B3 | … | 238R0 | 238B3 | 239R0 | 239B3 |
| D2 | C2 | 0G5 | 0B2 | 1G5 | 1B2 | … | 238G5 | 238B2 | 239G5 | 239B2 |
| D1 | C1 | 0G4 | 0B1 | 1G4 | 1B1 | … | 238G4 | 238B1 | 239G4 | 239B1 |
| D0 | C0 | 0G3 | 0B0 | 1G3 | 1B0 | … | 238G3 | 238B0 | 239G3 | 239B0 |

#### 262K color: 18-bit/pixel (RGB 6-6-6 bits input)

One pixel (3 sub-pixels) display data is sent by 3 bytes transfer when DBI [2:0] bits of 3Ah register are set to "110".

| Count | 0 | 1 | 2 | 3 | … | 718 | 719 | 720 |
|---|---|---|---|---|---|---|---|---|
| D/CX | 0 | 1 | 1 | 1 | … | 1 | 1 | 1 |
| D7 | C7 | 0R5 | 0G5 | 0B5 | … | 239R5 | 239G5 | 239B5 |
| D6 | C6 | 0R4 | 0G4 | 0B4 | … | 239R4 | 239G4 | 239B4 |
| D5 | C5 | 0R3 | 0G3 | 0B3 | … | 239R3 | 239G3 | 239B3 |
| D4 | C4 | 0R2 | 0G2 | 0B2 | … | 239R2 | 239G2 | 239B2 |
| D3 | C3 | 0R1 | 0G1 | 0B1 | … | 239R1 | 239G1 | 239B1 |
| D2 | C2 | 0R0 | 0G0 | 0B0 | … | 239R0 | 239G0 | 239B0 |
| D1 | C1 | | | | … | | | |
| D0 | C0 | | | | … | | | |

# 8. Command

## 8.1. Command List

| Regulative Command Set | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Command Function | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| No Operation | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00h |
| Software Reset | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 01h |
| Read Display Identification Information | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 04h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | ID1 [7:0] | | | | | | | | XX |
| | 1 | ↑ | 1 | XX | ID2 [7:0] | | | | | | | | XX |
| | 1 | ↑ | 1 | XX | ID3 [7:0] | | | | | | | | XX |
| Read Display Status | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 09h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | D [31:25] | | | | | | | X | 00 |
| | 1 | ↑ | 1 | XX | X | D [22:20] | | | D [19:16] | | | | 61 |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | D [10:8] | | | 00 |
| | 1 | ↑ | 1 | XX | D [7:5] | | | X | X | X | X | X | 00 |
| Read Display Power Mode | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0Ah |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | D [7:2] | | | | | | 0 | 0 | 08 |
| Read Display MADCTL | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0Bh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | D [7:2] | | | | | | 0 | 0 | 00 |
| Read Display Pixel Format | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 0Ch |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | RIM | DPI [2:0] | | | X | DBI [2:0] | | | 06 |
| Read Display Image Format | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0Dh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | D [2:0] | | | 00 |
| Read Display Signal Mode | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 0Eh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | D [7:2] | | | | | | 0 | 0 | 00 |
| Read Display Self-Diagnostic Result | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0Fh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | D [7:6] | | X | X | X | X | X | X | 00 |
| Enter Sleep Mode | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 10h |
| Sleep OUT | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | 11h |
| Partial Mode ON | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 12h |
| Normal Display Mode ON | 0 | 1 | ↑ | XX | 0 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 13h |
| Display Inversion OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 20h |
| Display Inversion ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 21h |
| Gamma Set | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 0 | 26h |
| | 1 | 1 | ↑ | XX | GC [7:0] | | | | | | | | 01 |
| Display OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 28h |
| Display ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 29h |
| Column Address Set | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 2Ah |
| | 1 | 1 | ↑ | XX | SC [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | SC [7:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EC [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EC [7:0] | | | | | | | | XX |
| Page Address Set | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 2Bh |
| | 1 | 1 | ↑ | XX | SP [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | SP [7:0] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EP [15:8] | | | | | | | | XX |
| | 1 | 1 | ↑ | XX | EP [7:0] | | | | | | | | XX |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Memory Write | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 2Ch |
| | 1 | 1 | ↑ | D [17:0] | | | | | | | | | XX |
| Color SET | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 2Dh |
| | 1 | ↑ | 1 | XX | | | R00 [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | Rnn [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | R31 [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | G00 [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | Gnn [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | G64 [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | B00 [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | Bnn [5:0] | | | | | | XX |
| | 1 | ↑ | 1 | XX | | | B31 [5:0] | | | | | | XX |
| Memory Read | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 2Eh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | D [17:0] | | | | | | | | | XX |
| Partial Area | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 30h |
| | 1 | 1 | ↑ | XX | SR [15:8] | | | | | | | | 00 |
| | 1 | 1 | ↑ | XX | SR [7:0] | | | | | | | | 00 |
| | 1 | 1 | ↑ | XX | ER [15:8] | | | | | | | | 01 |
| | 1 | 1 | ↑ | XX | ER [7:0] | | | | | | | | 3F |
| Vertical Scrolling Definition | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 33h |
| | 1 | 1 | ↑ | XX | TFA [15:8] | | | | | | | | 00 |
| | 1 | 1 | ↑ | XX | TFA [7:0] | | | | | | | | 00 |
| | 1 | 1 | ↑ | XX | VSA [15:8] | | | | | | | | 01 |
| | 1 | 1 | ↑ | XX | VSA [7:0] | | | | | | | | 40 |
| | 1 | 1 | ↑ | XX | BFA [15:8] | | | | | | | | 00 |
| | 1 | 1 | ↑ | XX | BFA [7:0] | | | | | | | | 00 |
| Tearing Effect Line OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 34h |
| Tearing Effect Line ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 35h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | M | 00 |
| Memory Access Control | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 36h |
| | 1 | 1 | ↑ | XX | MY | MX | MV | ML | BGR | MH | X | X | 00 |
| Vertical Scrolling Start Address | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 37h |
| | 1 | 1 | ↑ | XX | VSP [15:8] | | | | | | | | 00 |
| | 1 | 1 | ↑ | XX | VSP [7:0] | | | | | | | | 00 |
| Idle Mode OFF | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 38h |
| Idle Mode ON | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 39h |
| Pixel Format Set | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3Ah |
| | 1 | 1 | ↑ | XX | X | DPI [2:0] | | | X | DBI [2:0] | | | 66 |
| Write Memory Continue | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 3Ch |
| | 1 | 1 | ↑ | D [17:0] | | | | | | | | | XX |
| Read Memory Continue | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 3Eh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | D [17:0] | | | | | | | | | XX |
| Set Tear Scanline | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | STS [8] | 00 |
| | 1 | 1 | ↑ | XX | STS [7:0] | | | | | | | | 00 |
| Get Scanline | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 45h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | GTS [9:8] | | 00 |
| | 1 | ↑ | 1 | XX | GTS [7:0] | | | | | | | | 00 |
| Write Display Brightness | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 51h |
| | 1 | 1 | ↑ | XX | DBV [7:0] | | | | | | | | 00 |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read Display Brightness | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 52h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | DBV [7:0] | | | | | | | | 00 |
| Write CTRL Display | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53h |
| | 1 | 1 | ↑ | XX | X | X | BCTRL | X | DD | BL | X | X | 00 |
| Read CTRL Display | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 54h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | X | X | BCTRL | X | DD | BL | X | X | 00 |
| Write Content Adaptive Brightness Control | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 55h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | C [1:0] | | 00 |
| Read Content Adaptive Brightness Control | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 56h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | C [1:0] | | 00 |
| Write CABC Minimum Brightness | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 5Eh |
| | 1 | 1 | ↑ | XX | CMB [7:0] | | | | | | | | 00 |
| Read CABC Minimum Brightness | 0 | 1 | ↑ | XX | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 5Fh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | CMB [7:0] | | | | | | | | 00 |
| Read ID1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | DAh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | Module's Manufacture [7:0] | | | | | | | | XX |
| Read ID2 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | DBh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | LCD Module / Driver Version [7:0] | | | | | | | | XX |
| Read ID3 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | DCh |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | LCD Module / Driver ID [7:0] | | | | | | | | XX |

| **Extended Command Set** | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Command Function | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | Hex |
| RGB Interface | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | B0h |
| Signal Control | 1 | 1 | ↑ | XX | ByPass_MODE | RCM [1:0] | | X | VSPL | HSPL | DPL | EPL | 40 |
| Frame Control (In Normal Mode) | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 | B1h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | DIVA [1:0] | | 00 |
| | 1 | 1 | ↑ | XX | X | X | X | RTNA [4:0] | | | | | 1B |
| Frame Control (In Idle Mode) | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 | B2h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | DIVB [1:0] | | 00 |
| | 1 | 1 | ↑ | XX | X | X | X | RTNB [4:0] | | | | | 1B |
| Frame Control (In Partial Mode) | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | B3h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | DIVC [1:0] | | 00 |
| | 1 | 1 | ↑ | XX | X | X | X | RTNC [4:0] | | | | | 1B |
| Display Inversion Control | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | B4h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | NLA | NLB | NLC | 02 |
| Blanking Porch Control | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | B5h |
| | 1 | 1 | ↑ | XX | 0 | VFP [6:0] | | | | | | | 02 |
| | 1 | 1 | ↑ | XX | 0 | VBP [6:0] | | | | | | | 02 |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | HFP [4:0] | | | | | 0A |
| | 1 | 1 | ↑ | XX | 0 | 0 | 0 | HBP [4:0] | | | | | 14 |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Display Function Control | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | B6h |
| | 1 | 1 | ↑ | XX | X | X | X | X | PTG [1:0] | | PT [1:0] | | 0A |
| | 1 | 1 | ↑ | XX | REV | GS | SS | SM | ISC [3:0] | | | | 82 |
| | 1 | 1 | ↑ | XX | X | X | NL [5:0] | | | | | | 27 |
| | 1 | 1 | ↑ | XX | X | X | PCDIV [5:0] | | | | | | XX |
| Entry Mode Set | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | B7h |
| | 1 | 1 | ↑ | XX | X | X | X | X | 0 | GON | DTE | GAS | 07 |
| Backlight Control 1 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | B8h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | 1 | ↑ | XX | X | X | X | X | TH_UI [3:0] | | | | 04 |
| Backlight Control 2 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | B9h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | 1 | ↑ | XX | TH_MV [3:0] | | | | TH_ST [3:0] | | | | B8 |
| Backlight Control 3 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | BAh |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | 1 | ↑ | XX | X | X | X | X | DTH_UI [3:0] | | | | 04 |
| Backlight Control 4 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | BBh |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | 1 | ↑ | XX | DTH_MV [3:0] | | | | DTH_ST [3:0] | | | | C9 |
| Backlight Control 5 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | BCh |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | 1 | ↑ | XX | DIM2 [3:0] | | | | X | DIM1 [2:0] | | | 44 |
| Backlight Control 7 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | BEh |
| | 1 | 1 | ↑ | XX | PWM_DIV [7:0] | | | | | | | | 0F |
| Backlight Control 8 | 0 | 1 | ↑ | XX | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | BFh |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | LEDONR | LEDONPOL | LEDPWMOPL | 00 |
| Power Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | C0h |
| | 1 | 1 | ↑ | XX | X | X | VRH [5:0] | | | | | | 26 |
| Power Control 2 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | C1h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | BT [2:0] | | | 00 |
| VCOM Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | C5h |
| | 1 | 1 | ↑ | XX | X | VMH [6:0] | | | | | | | 31 |
| | 1 | 1 | ↑ | XX | X | VML [6:0] | | | | | | | 3C |
| VCOM Control 2 | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | C7h |
| | 1 | 1 | ↑ | XX | nVM | VMF [6:0] | | | | | | | C0 |
| NV Memory Write | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | D0h |
| | 1 | 1 | ↑ | XX | X | X | X | X | X | PGM_ADR [2:0] | | | 00 |
| | 1 | 1 | ↑ | XX | PGM_DATA [7:0] | | | | | | | | XX |
| NV Memory Protection Key | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | D1h |
| | 1 | 1 | ↑ | XX | KEY [23:16] | | | | | | | | 55 |
| | 1 | 1 | ↑ | XX | KEY [15:8] | | | | | | | | AA |
| | 1 | 1 | ↑ | XX | KEY [7:0] | | | | | | | | 66 |
| NV Memory Status Read | 0 | 1 | ↑ | XX | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | D2h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | X | ID2_CNT [2:0] | | | X | ID1_CNT [2:0] | | | XX |
| | 1 | ↑ | 1 | XX | BUSY | VMF_CNT [2:0] | | | X | ID3_CNT [2:0] | | | XX |

| | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Read ID4 | 0 | ↑ | 1 | XX | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | D3h |
| | 1 | ↑ | 1 | XX | X | X | X | X | X | X | X | X | XX |
| | 1 | ↑ | 1 | XX | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00 |
| | 1 | ↑ | 1 | XX | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | 93 |
| | 1 | ↑ | 1 | XX | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 41 |
| Positive Gamma Correction | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | E0h |
| | 1 | 1 | ↑ | XX | X | X | X | X | VP0 [3:0] | | | | 08 |
| | 1 | 1 | ↑ | XX | X | X | VP1 [5:0] | | | | | | 0E |
| | 1 | 1 | ↑ | XX | X | X | VP2 [5:0] | | | | | | 12 |
| | 1 | 1 | ↑ | XX | X | X | X | X | VP4 [3:0] | | | | 05 |
| | 1 | 1 | ↑ | XX | X | X | X | VP6 [4:0] | | | | | 03 |
| | 1 | 1 | ↑ | XX | X | X | X | X | VP13 [3:0] | | | | 09 |
| | 1 | 1 | ↑ | XX | X | VP20 [6:0] | | | | | | | 47 |
| | 1 | 1 | ↑ | XX | VP36 [3:0] | | | | VP27 [3:0] | | | | 86 |
| | 1 | 1 | ↑ | XX | X | VP43 [6:0] | | | | | | | 2B |
| | 1 | 1 | ↑ | XX | X | X | X | X | VP50 [3:0] | | | | 0B |
| | 1 | 1 | ↑ | XX | X | X | X | VP57 [4:0] | | | | | 04 |
| | 1 | 1 | ↑ | XX | X | X | X | X | VP59 [3:0] | | | | 00 |
| | 1 | 1 | ↑ | XX | X | X | VP61 [5:0] | | | | | | 00 |
| | 1 | 1 | ↑ | XX | X | X | VP62 [5:0] | | | | | | 00 |
| | 1 | 1 | ↑ | XX | X | X | X | X | VP63 [3:0] | | | | 00 |
| Negative Gamma Correction | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | E1h |
| | 1 | 1 | ↑ | XX | X | X | X | X | VN0 [3:0] | | | | 08 |
| | 1 | 1 | ↑ | XX | X | X | VN1 [5:0] | | | | | | 1A |
| | 1 | 1 | ↑ | XX | X | X | VN2 [5:0] | | | | | | 20 |
| | 1 | 1 | ↑ | XX | X | X | X | X | VN4 [3:0] | | | | 07 |
| | 1 | 1 | ↑ | XX | X | X | X | VN6 [4:0] | | | | | 0E |
| | 1 | 1 | ↑ | XX | X | X | X | X | VN13 [3:0] | | | | 05 |
| | 1 | 1 | ↑ | XX | X | VN20 [6:0] | | | | | | | 3A |
| | 1 | 1 | ↑ | XX | VN36 [3:0] | | | | VN27 [3:0] | | | | 8A |
| | 1 | 1 | ↑ | XX | X | VN43 [6:0] | | | | | | | 40 |
| | 1 | 1 | ↑ | XX | X | X | X | X | VN50 [3:0] | | | | 04 |
| | 1 | 1 | ↑ | XX | X | X | X | VN57 [4:0] | | | | | 18 |
| | 1 | 1 | ↑ | XX | X | X | X | X | VN59 [3:0] | | | | 0F |
| | 1 | 1 | ↑ | XX | X | X | VN61 [5:0] | | | | | | 3F |
| | 1 | 1 | ↑ | XX | X | X | VN62 [5:0] | | | | | | 3F |
| | 1 | 1 | ↑ | XX | X | X | X | X | VN63 [3:0] | | | | 0F |
| Digital Gamma Control 1 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | E2h |
| 1st Parameter | 1 | 1 | ↑ | XX | RCA0 [3:0] | | | | BCA0 [3:0] | | | | XX |
| : | 1 | 1 | ↑ | XX | RCAx [3:0] | | | | BCAx [3:0] | | | | XX |
| 16th Parameter | 1 | 1 | ↑ | XX | RCA15 [3:0] | | | | BCA15 [3:0] | | | | XX |
| Digital Gamma Control 2 | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | E3h |
| 1st Parameter | 1 | 1 | ↑ | XX | RFA0 [3:0] | | | | BFA0 [3:0] | | | | XX |
| : | 1 | 1 | ↑ | XX | RFAx [3:0] | | | | BFAx [3:0] | | | | XX |
| 64th Parameter | 1 | 1 | ↑ | XX | RFA63 [3:0] | | | | BFA63 [3:0] | | | | XX |
| Interface Control | 0 | 1 | ↑ | XX | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | F6h |
| | 1 | 1 | ↑ | XX | MY_EOR | MX_EOR | MV_EOR | X | BGR_EOR | X | X | WEMODE | 01 |
| | 1 | 1 | ↑ | XX | X | X | EPF [1:0] | | X | X | MDT [1:0] | | 00 |
| | 1 | 1 | ↑ | XX | X | X | ENDIAN | X | DM [1:0] | | RM | RIM | 00 |

*Note 1: Undefined commands are treated as NOP (00h) command.*

*Note 2: B0 to D9 and DE to FF are for factory use of display supplier. USER can decide if these commands are available or they are treated as NOP (00h) commands before shipping to USER. Default value is NOP*

*(00h).*

*Note 3: Commands 10h, 12h, 13h, 26h, 28h, 29h, 30h, 36h (Bit B4 only), 38h and 39h are updated during V-SYNC when ILI9341 is in Sleep OUT mode to avoid abnormal visual effects. During Sleep IN mode, these commands are updated immediately. Read status (09h), Read display power mode (0Ah), Read display MADCTL (0Bh), Read display pixel format (0Ch), Read display image mode (0Dh), Read display signal mode (0Eh) and Read display self diagnostic result (0Fh) of these commands are updated immediately both in Sleep IN mode and Sleep OUT mode.*

## 8.2.33. COLMOD: Pixel Format Set (3Ah)

| 3Ah | PIXSET (Pixel Format Set) | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | D/CX | RDX | WRX | D17-8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | HEX |
| Command | 0 | 1 | ↑ | XX | 0 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 3Ah |
| Parameter | 1 | 1 | ↑ | XX | 0 | DPI [2:0] | | | 0 | DBI [2:0] | | | 66 |

**Description**

This command sets the pixel format for the RGB image data used by the interface. DPI [2:0] is the pixel format select of RGB interface and DBI [2:0] is the pixel format of MCU interface. If a particular interface, either RGB interface or MCU interface, is not used then the corresponding bits in the parameter are ignored. The pixel format is shown in the table below.

| DPI [2:0] | | | RGB Interface Format |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | 16 bits / pixel |
| 1 | 1 | 0 | 18 bits / pixel |
| 1 | 1 | 1 | Reserved |

| DBI [2:0] | | | MCU Interface Format |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | Reserved |
| 0 | 1 | 0 | Reserved |
| 0 | 1 | 1 | Reserved |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | 16 bits / pixel |
| 1 | 1 | 0 | 18 bits / pixel |
| 1 | 1 | 1 | Reserved |

If using RGB Interface must selection serial interface.

X = Don't care

**Restriction**

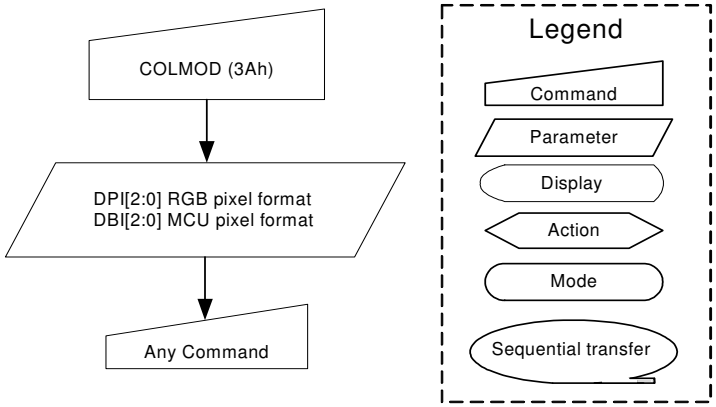
**Register Availability**

| Status | Availability |
|---|---|
| Normal Mode On, Idle Mode Off, Sleep Out | Yes |
| Normal Mode On, Idle Mode On, Sleep Out | Yes |
| Partial Mode On, Idle Mode Off, Sleep Out | Yes |
| Partial Mode On, Idle Mode On, Sleep Out | Yes |
| Sleep In | Yes |

**Default**

| Status | Default Value | |
|---|---|---|
| | DPI [2:0] | DBI [2:0] |
| Power On Sequence | 3'b110 | 3'b110 |
| SW Reset | No Change | No Change |
| HW Reset | 3'b110 | 3'b110 |

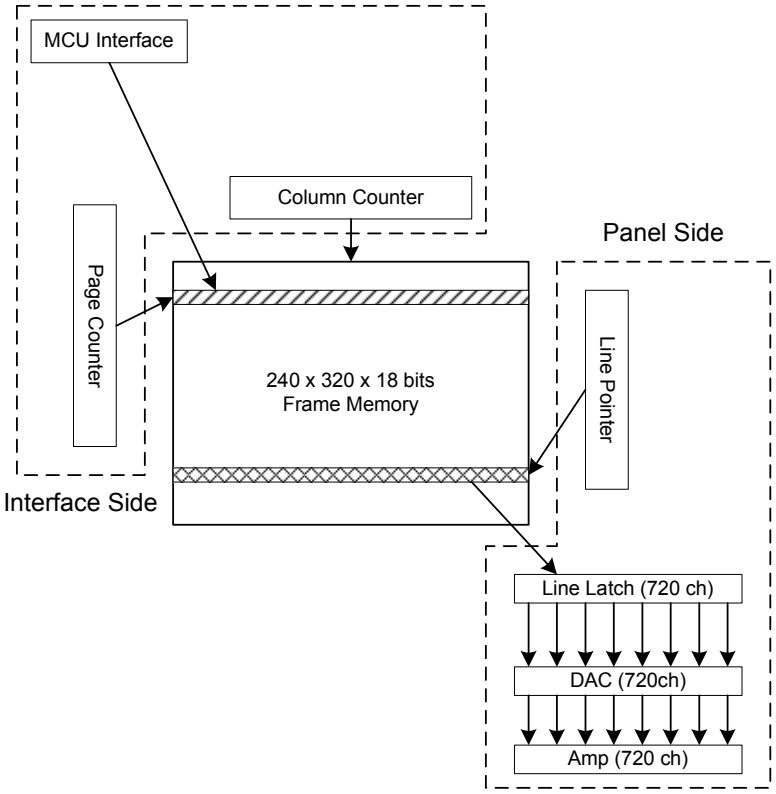
**Flow Chart**



# 9. Display Data RAM

## 9.1. Configuration

The display data RAM stores display dots and consists of 1,382,400 bits (240x18x320 bits). There is no restriction on access to the RAM even when the display data on the same address is loaded to DAC. There will be no abnormal visible effect on the display when there is a simultaneous panel read and interface read or write display data to the same location of the frame memory.

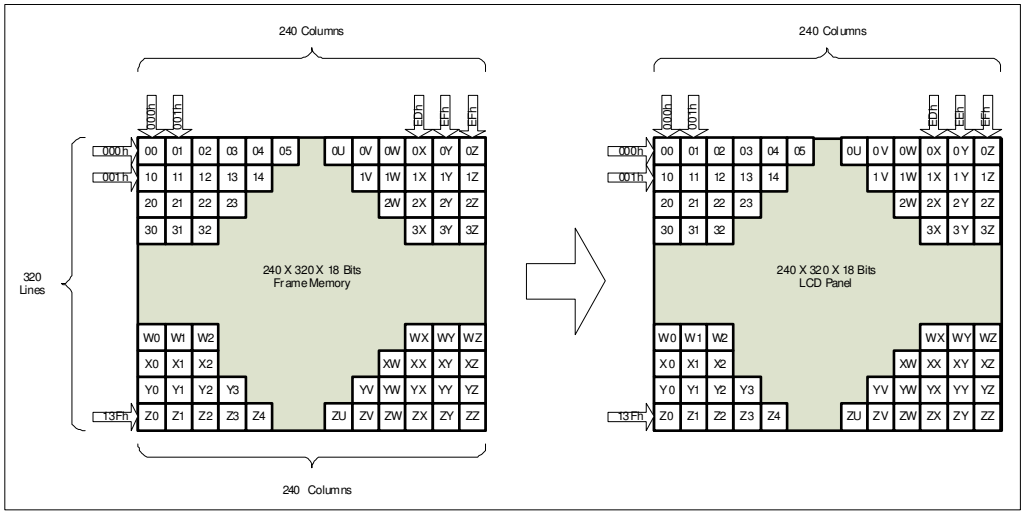


# 9.2. Memory to Display Address Mapping

## 9.2.1. Normal Display ON or Partial Mode ON, Vertical Scroll Mode OFF

In this mode, the content of frame memory within an area where column pointer is 0000h to 00EFh and page pointer is 0000h to 013Fh is displayed.

To display a dot on leftmost top corner, store the dot data at (column pointer, page pointer) = (0, 0)

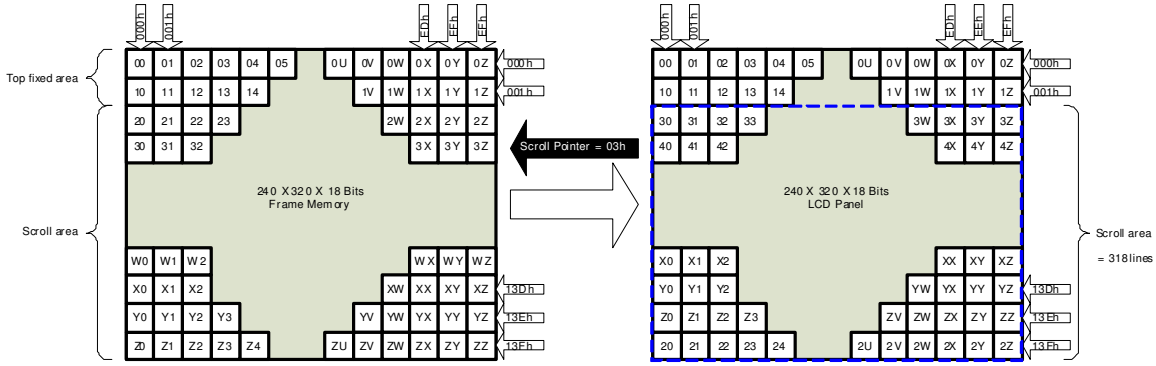


### 9.2.2. Vertical Scroll Mode

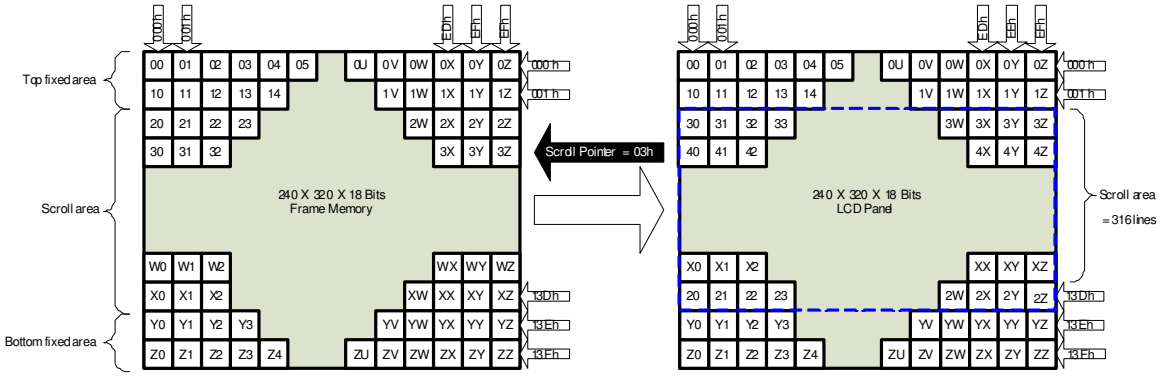
There is a vertical scrolling mode, which is determined by the commands “Vertical Scrolling Definition” (33h) and “Vertical Scrolling Start Address” (37h).

The Vertical Scroll Mode function is explained by these examples in the following.

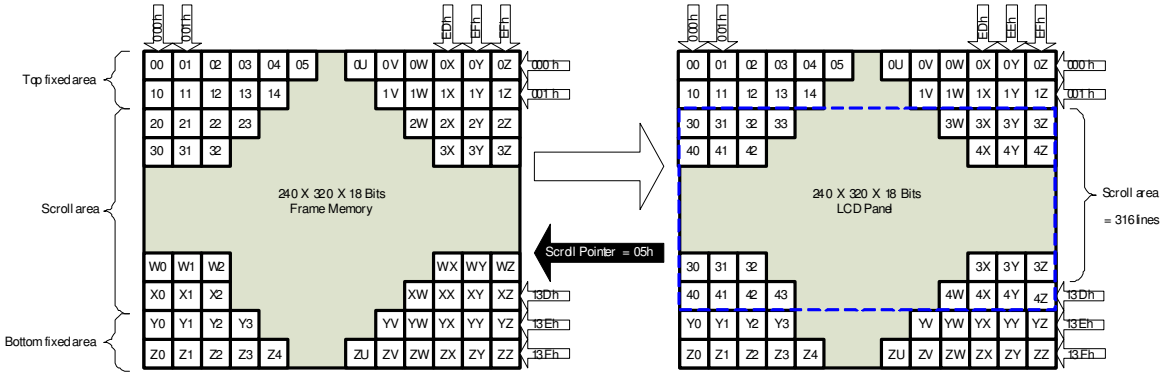
TFA=2, VSA=318, BFA=0 when MADCTL ML bit = 0




TFA=2, VSA=316, BFA=2 when MADCTL ML bit = 0




TFA=2, VSA=316, BFA=4 when MADCTL ML bit = 0




Note: When Vertical Scrolling Definition Parameters (TFA+VSA+BFA) ≠ 320, Scrolling Mode is undefined.

### 9.2.3. Vertical Scroll Example

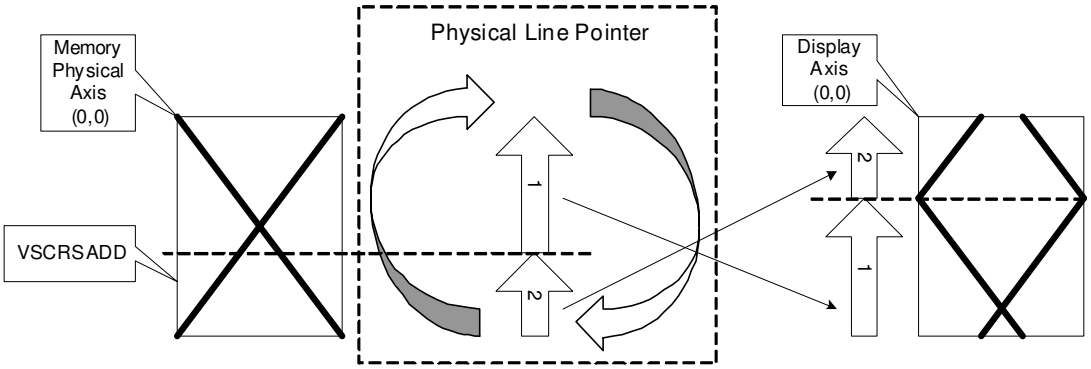
### 9.2.4. Case1: TFA+VSA+BFA < 320

This setting is prohibited, unless unexpected picture will be shown.

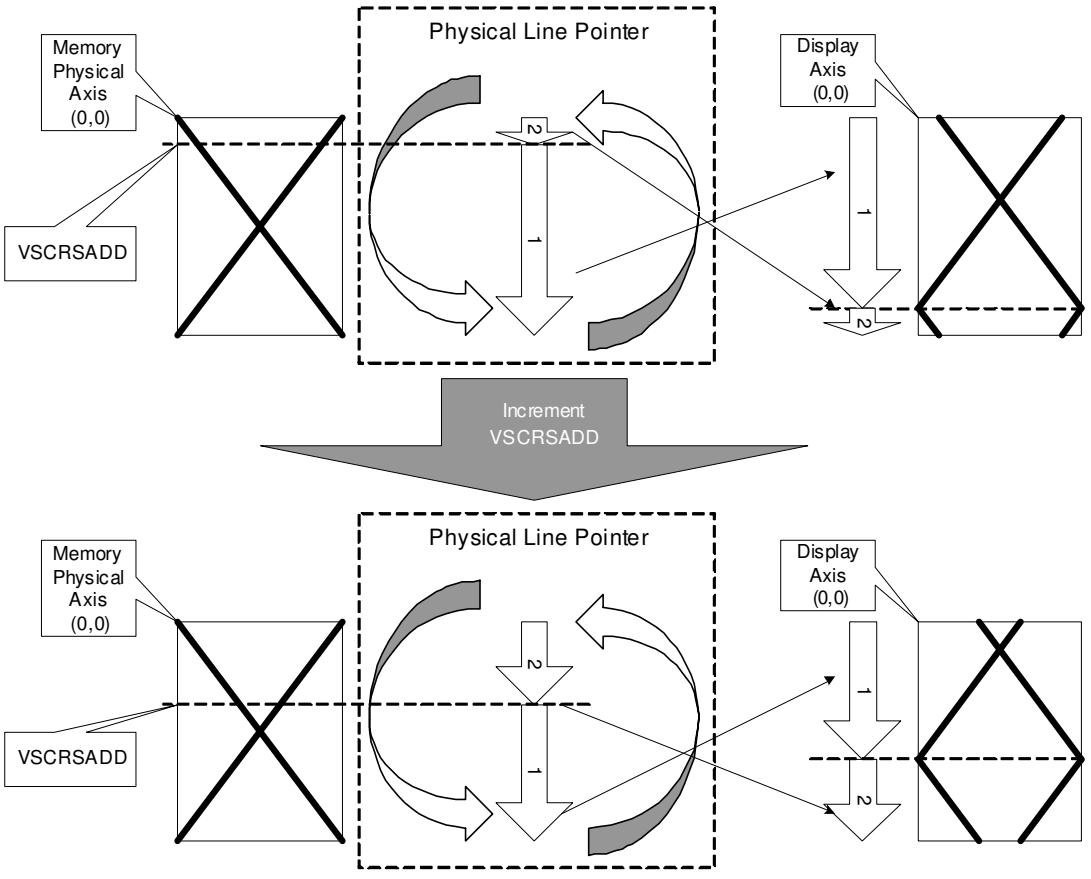
### 9.2.5. Case2: TFA+VSA+BFA = 320 (Rolling Scrolling)

The operation of Rolling Scrolling is explained by these examples in the following.

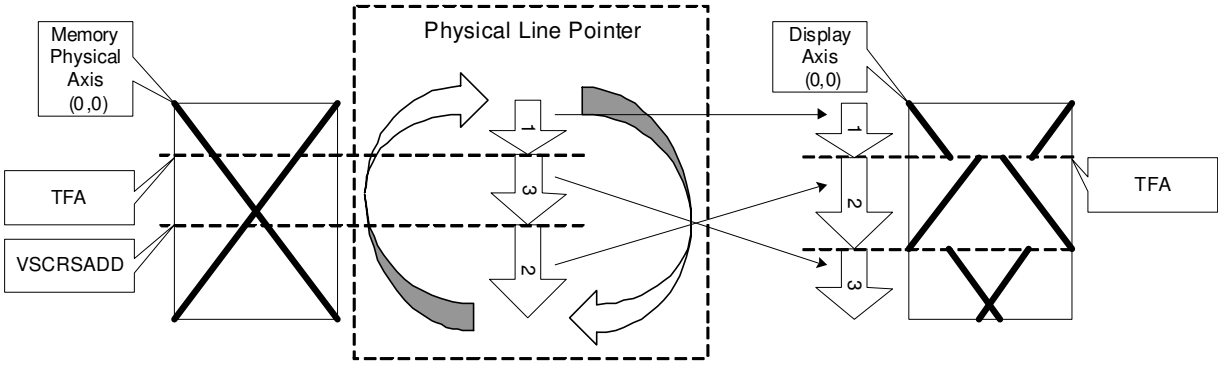
When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 1



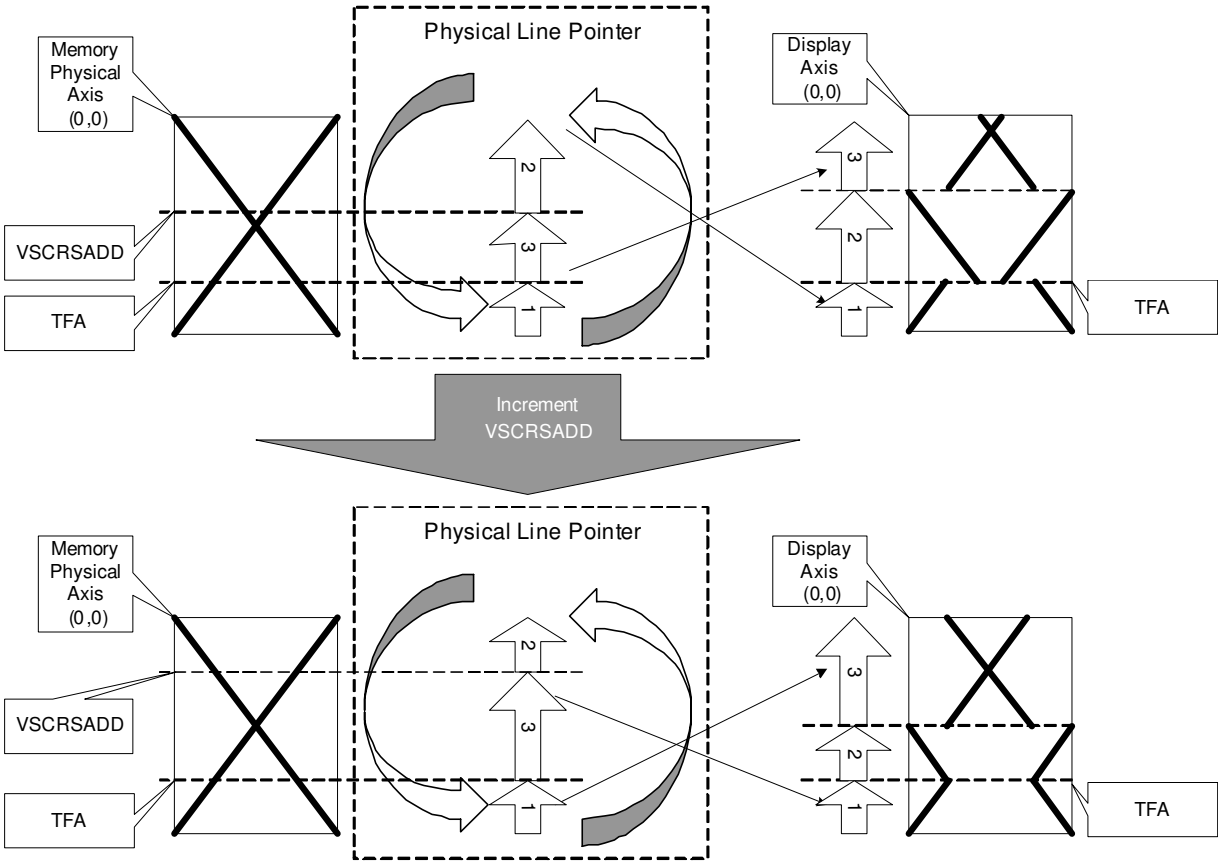

When TFA=0, VSA=320, BFA=0, VSCRSADD=40 and MADCTL ML bit = 0



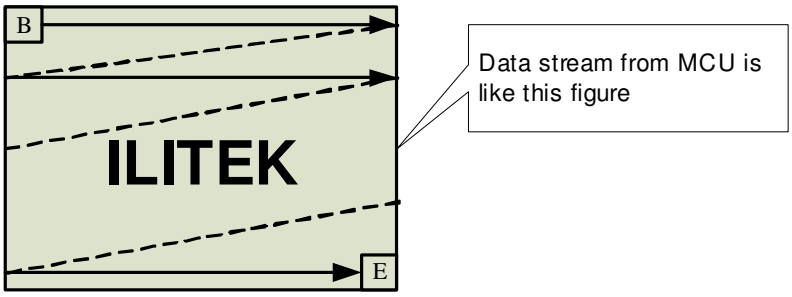
When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 0



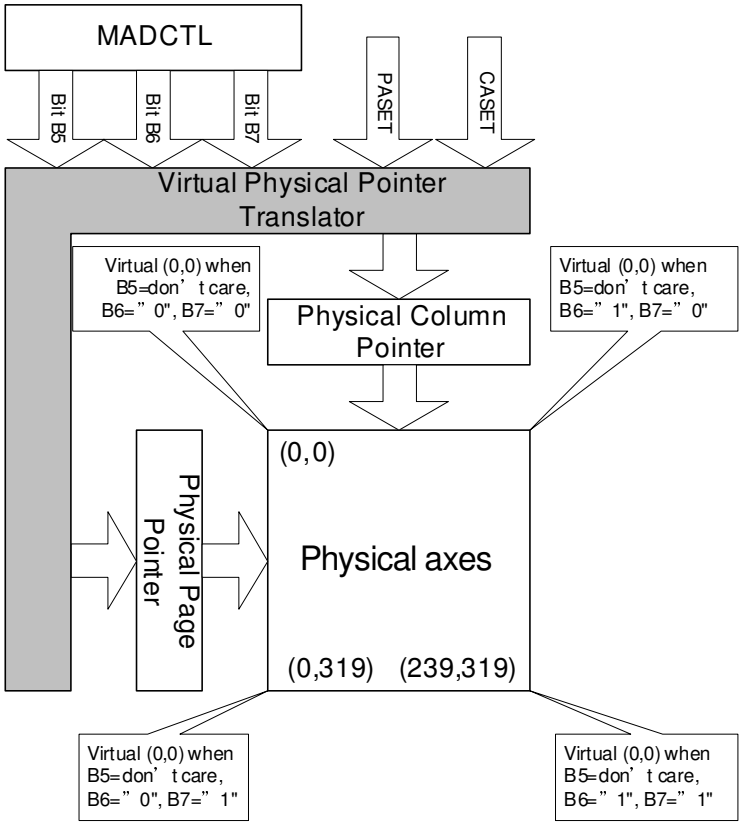

When TFA=30, VSA=290, BFA=0, VSCRSADD=80 and MADCTL ML bit = 1



## 9.3. MCU to memory write/read direction




The data is written in the order illustrated above. The Counter which dictates where in the physical memory the data is to be written is controlled by “Memory Data Access Control” Command, Bits B5, B6, and B7 as described below.




| B5 | B6 | B7 | CASET | PASET |
|---|---|---|---|---|
| 0 | 0 | 0 | Direct to Physical Column Pointer | Direct to Physical Page Pointer |
| 0 | 0 | 1 | Direct to Physical Column Pointer | Direct to (319-Physical Page Pointer) |
| 0 | 1 | 0 | Direct to (239-Physical Column Pointer) | Direct to Physical Page Pointer |
| 0 | 1 | 1 | Direct to (239-Physical Column Pointer) | Direct to (319-Physical Page Pointer) |
| 1 | 0 | 0 | Direct to Physical Page Pointer | Direct to Physical Column Pointer |
| 1 | 0 | 1 | Direct to (319-Physical Page Pointer) | Direct to Physical Column Pointer |
| 1 | 1 | 0 | Direct to Physical Page Pointer | Direct to (239-Physical Column Pointer) |
| 1 | 1 | 1 | Direct to (319-Physical Page Pointer) | Direct to (239-Physical Column Pointer) |

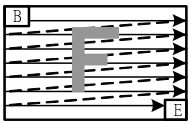
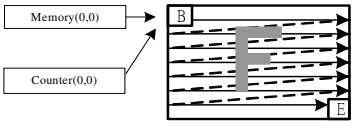
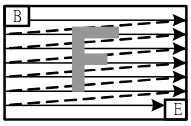
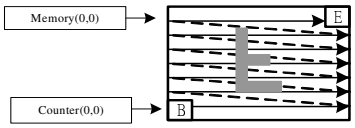
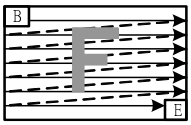
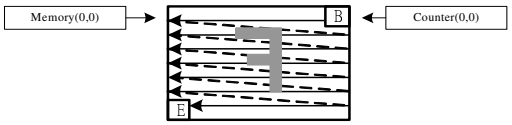
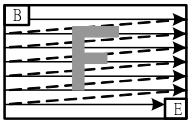
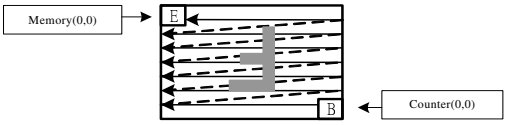
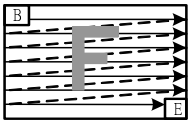
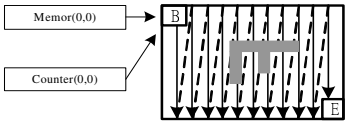
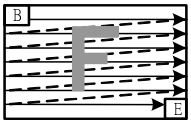
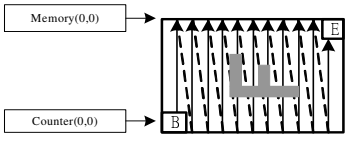
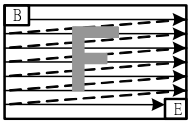
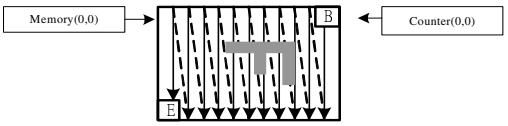
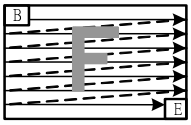
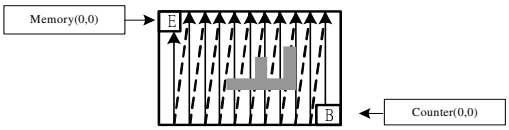
| Condition | Column Counter | Page counter |
|---|---|---|
| When RAMWR/RAMRD command is accepted | Return to “Start column” | Return to “Start Page” |
| Complete Pixel Read/Write action | Increment by 1 | No change |
| The Column values is large than “End Column” | Return to “Start column” | Increment by 1 |
| The Page counter is large than “End Page” | Return to “Start column” | Return to “Start Page” |

Note:

Data is always written to the Frame Memory in the same order, regardless of the Memory Write Direction set by MADCTL bits B7, B6 and B5. The write order for each pixel unit is

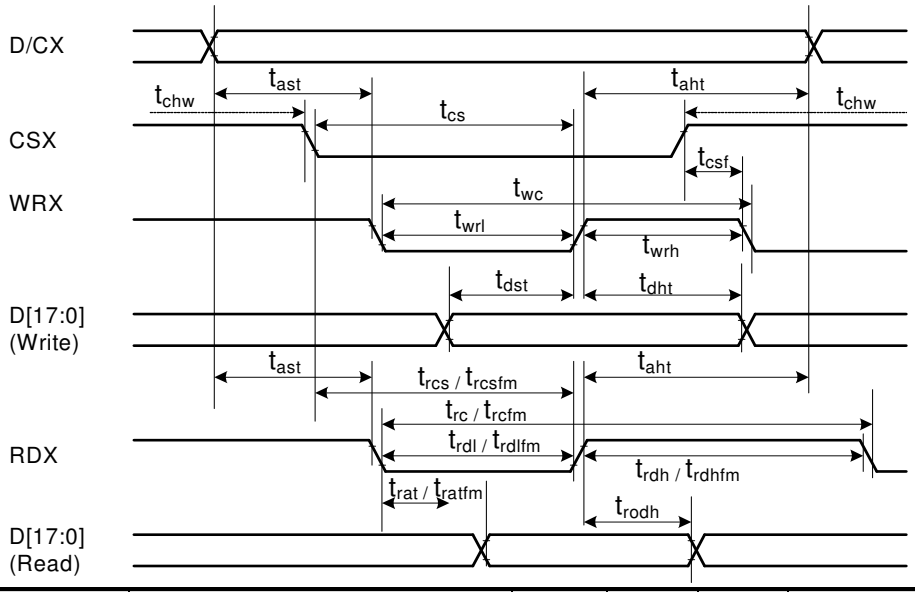
| D17 | D16 | D15 | D14 | D13 | D12 | D11 | D10 | D9 | D8 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| R5 | R4 | R3 | R2 | R1 | R0 | G5 | G4 | G3 | G2 | G1 | G0 | B5 | B4 | B3 | B2 | B1 | B0 |

One pixel unit represents 1 column and 1 page counter value on the Frame Memory.

| Display Data Direction | MADCTR Parameter | | | Image in the Memory (MPU) | Image in the Driver (Frame Memory) |
|---|---|---|---|---|---|
| | MV | MX | MY | | |
| Normal | 0 | 0 | 0 |  |  |
| Y-Mirror | 0 | 0 | 1 |  |  |
| X-Mirror | 0 | 1 | 0 |  |  |
| X-Mirror Y-Mirror | 0 | 1 | 1 |  |  |
| X-Y Exchange | 1 | 0 | 0 |  |  |
| X-Y Exchange Y-Mirror | 1 | 0 | 1 |  |  |
| XY Exchange X-Mirror | 1 | 1 | 0 |  |  |
| XY Exchange XY-Mirror | 1 | 1 | 1 |  |  |

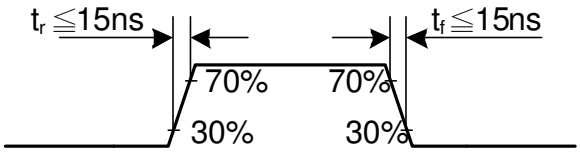
## 18.3 AC Characteristics

### 18.3.1 Display Parallel 18/16/9/8-bit Interface Timing Characteristics (8080- Ⅰ system)

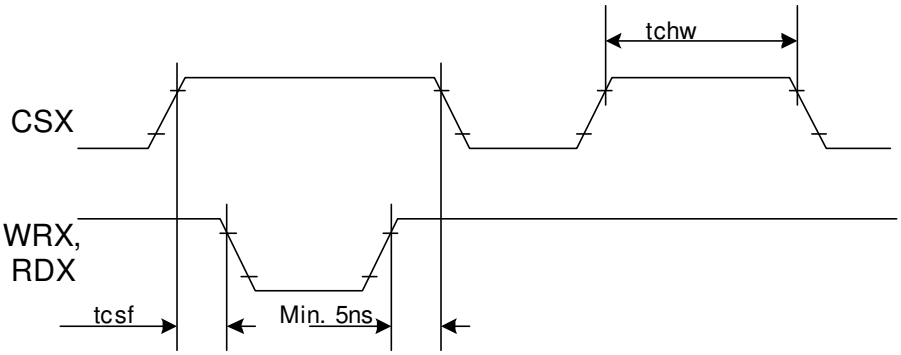



| Signal | Symbol | Parameter | min | max | Unit | Description |
|---|---|---|---|---|---|---|
| DCX | tast | Address setup time | 0 | - | ns | |
| | taht | Address hold time (Write/Read) | 0 | - | ns | |
| CSX | tchw | CSX "H" pulse width | 0 | - | ns | |
| | tcs | Chip Select setup time (Write) | 15 | - | ns | |
| | trcs | Chip Select setup time (Read ID) | 45 | - | ns | |
| | trcsfm | Chip Select setup time (Read FM) | 355 | - | ns | |
| | tcsf | Chip Select Wait time (Write/Read) | 10 | - | ns | |
| WRX | twc | Write cycle | 66 | - | ns | |
| | twrh | Write Control pulse H duration | 15 | - | ns | |
| | twrl | Write Control pulse L duration | 15 | - | ns | |
| RDX (FM) | trcfm | Read Cycle (FM) | 450 | - | ns | |
| | trdhfm | Read Control H duration (FM) | 90 | - | ns | |
| | trdlfm | Read Control L duration (FM) | 355 | - | ns | |
| RDX (ID) | trc | Read cycle (ID) | 160 | - | ns | |
| | trdh | Read Control pulse H duration | 90 | - | ns | |
| | trdl | Read Control pulse L duration | 45 | - | ns | |
| D[17:0], D[15:0], D[8:0], D[7:0] | tdst | Write data setup time | 10 | - | ns | For maximum CL=30pF<br>For minimum CL=8pF |
| | tdht | Write data hold time | 10 | - | ns | |
| | trat | Read access time | - | 40 | ns | |
| | tratfm | Read access time | - | 340 | ns | |
| | trod | Read output disable time | 20 | 80 | ns | |

*Note: Ta = -30 to 70 ℃, VDDI=1.65V to 3.3V, VCI=2.5V to 3.3V, VSS=0V*

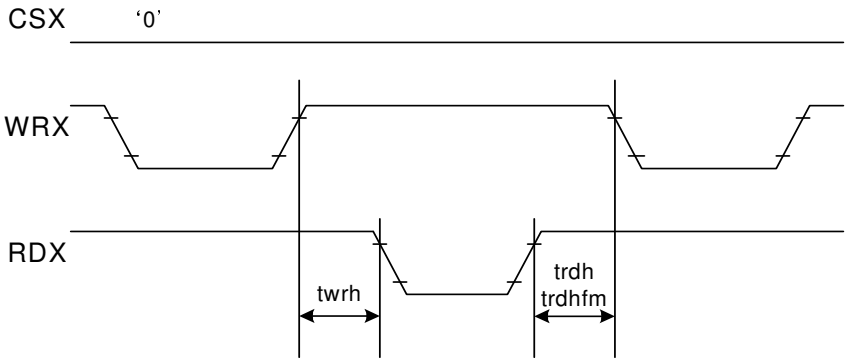


CSX timings :




*Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*

Write to read or read to write timings:




*Note: Logic high and low levels are specified as 30% and 70% of VDDI for Input signals.*