BlueSeed, RISC-V Emulator

1. RISC-V a blurry world

RISC-V is an open source hardware ISA (Instruction Set Architecture) for RISC (Reduce Instruction Set Computer).

This ISA is not much used to date but has potential to exploit.

The problem is that, there is a lot of lacks in tools used for RISC-V developpement.

Typically, GCC use some opcode undefined in the official specification (pseudo-instruction used as instruction with “arbitrary“ opcode for example).

Advanced in this world is so complicated and there are few information and precedent on the subject.

By the way, we will try for the best.

2. BlueSeed

BlueSeed is a basic emulator for RISC-V 32/64 (128 maybe later).

The idea is that the TARGET architecture to emulate is selected in compile-time to decrease the binary size.

The repository architecture is made to easily accommodate new architectures if needed (scalability).

The system calls are interfaced with the host machine, there is no self emulator interface.

BlueSeed specifity:

- Binary format : ELF

- Syscall interfaced : x86/x64 only

- IS handle: rv32i/rv64i (standard Instruction Set)

BlueSeed own a runtime debugger. Lauch the binary with the “--debug”

will open a Command Line Interface (CLI) and execute instruction one by one.

Handled command are display using the command “help” in the CLI.

As an emulator, BlueSeed is very permissive, keep that in mind.