Summary of this week

- This week, you continued to learn about balancing
- You saw some capacitor-based balancing circuits and learned that they don't work very well (slow)
- You saw some inductive/transformer-based balancing circuits and learned that they can work better, but tend to be heavy and expensive
- You learned about a shared-bus dc–dc converter design that can work very well and be cost-neutral with respect to passive balancing in some cases
- You learned how to use simulation to estimate how quickly you must balance and to investigate causes of imbalance

Where from here?

- Next week, our focus shifts to studying power-limits estimation
- We will review the premise for power-limits computation
- You will see how to use the HPPC method to estimate voltage-based limits
- You will learn how to extend method to impose SOC-based, electronics-based, and load-based limits
- You will learn how to implement power limits computations in Octave code to predict performance of a cell

Credits

Credits for photos in this lesson

- "Signs" on slide 2: Pixabay license (`https://pixabay.com/en/service/license/`), from `https://pixabay.com/en/signposts-directions-pizol-999685/`