Cortex-M Processors Overview

Agenda

Introduction

Armv6-M Cortex processors

Armv7-M Cortex processors

Armv8-M Cortex processors

Processor selection

Learning objectives - Introduction

After completing this overview, you will be able to:

- Describe the main features of Cortex-M processors
- Discuss criteria for selecting the Cortex-M processor best suited to your need

Arm Architecture Profiles

Cortex-A

Highest performance

Designed for high-level operating systems

Cortex-R

Faster responsiveness

Designed for high performance, hard real-time applications

Cortex-M

Smallest/lowest power

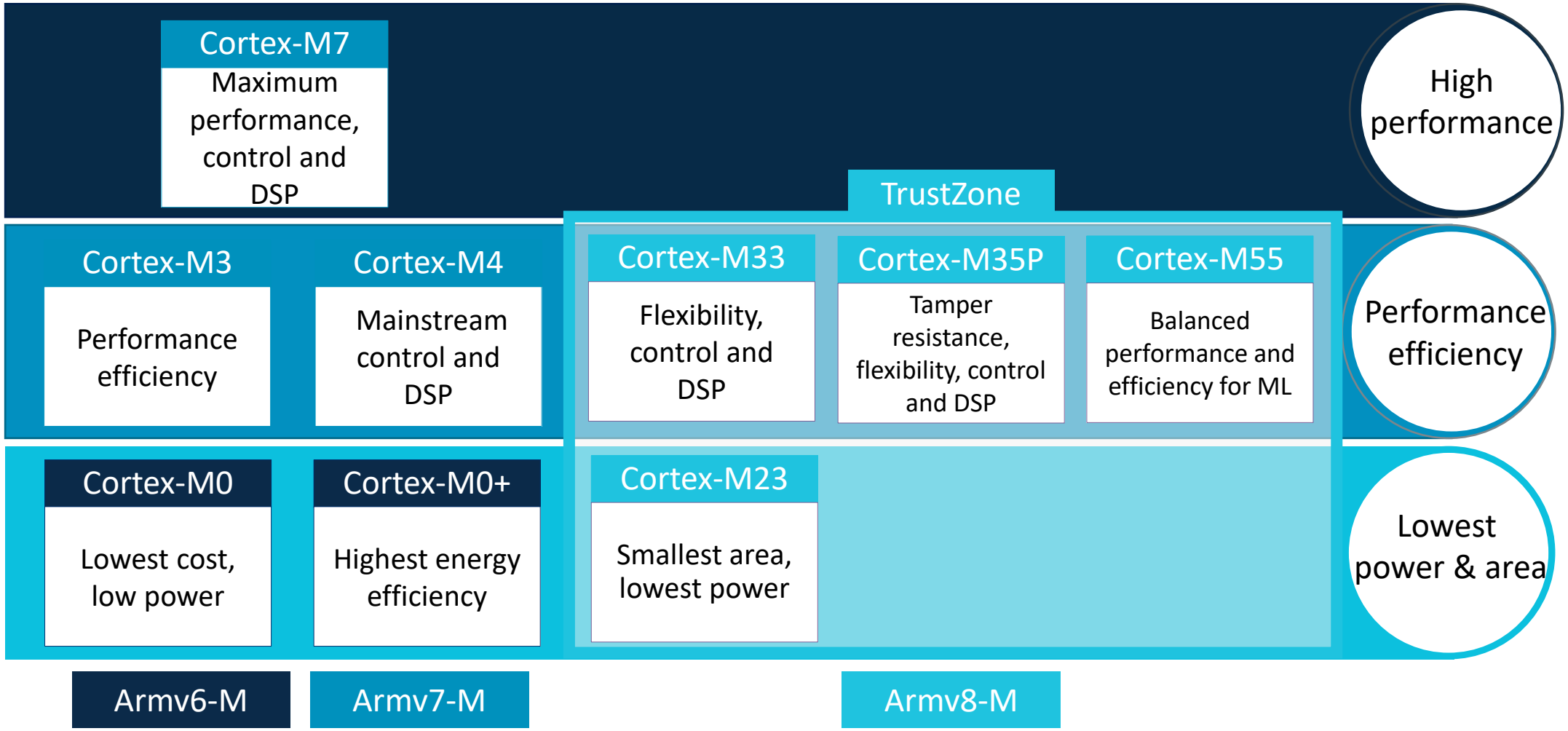
Designed for discrete processing and microcontrollers

SecurCore

Tamper resistant

Designed for physical security

Arm Cortex-M processor portfolio



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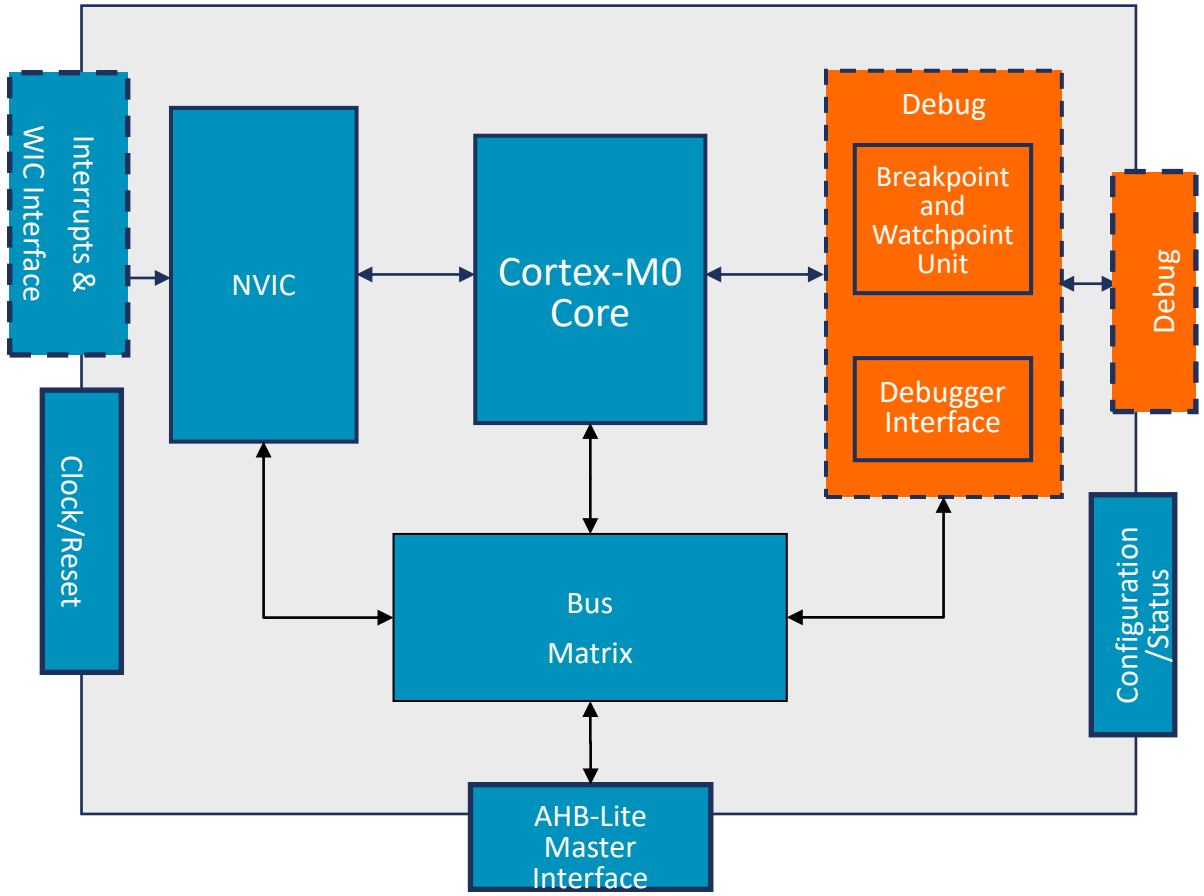
Arm Cortex-M0 processor



Armv6-M architecture

Thumb® technology

Nested Vector Interrupt Controller (NVIC)

Optional CoreSight™-compliant debug

Von-Neumann architecture

3-stage core pipeline

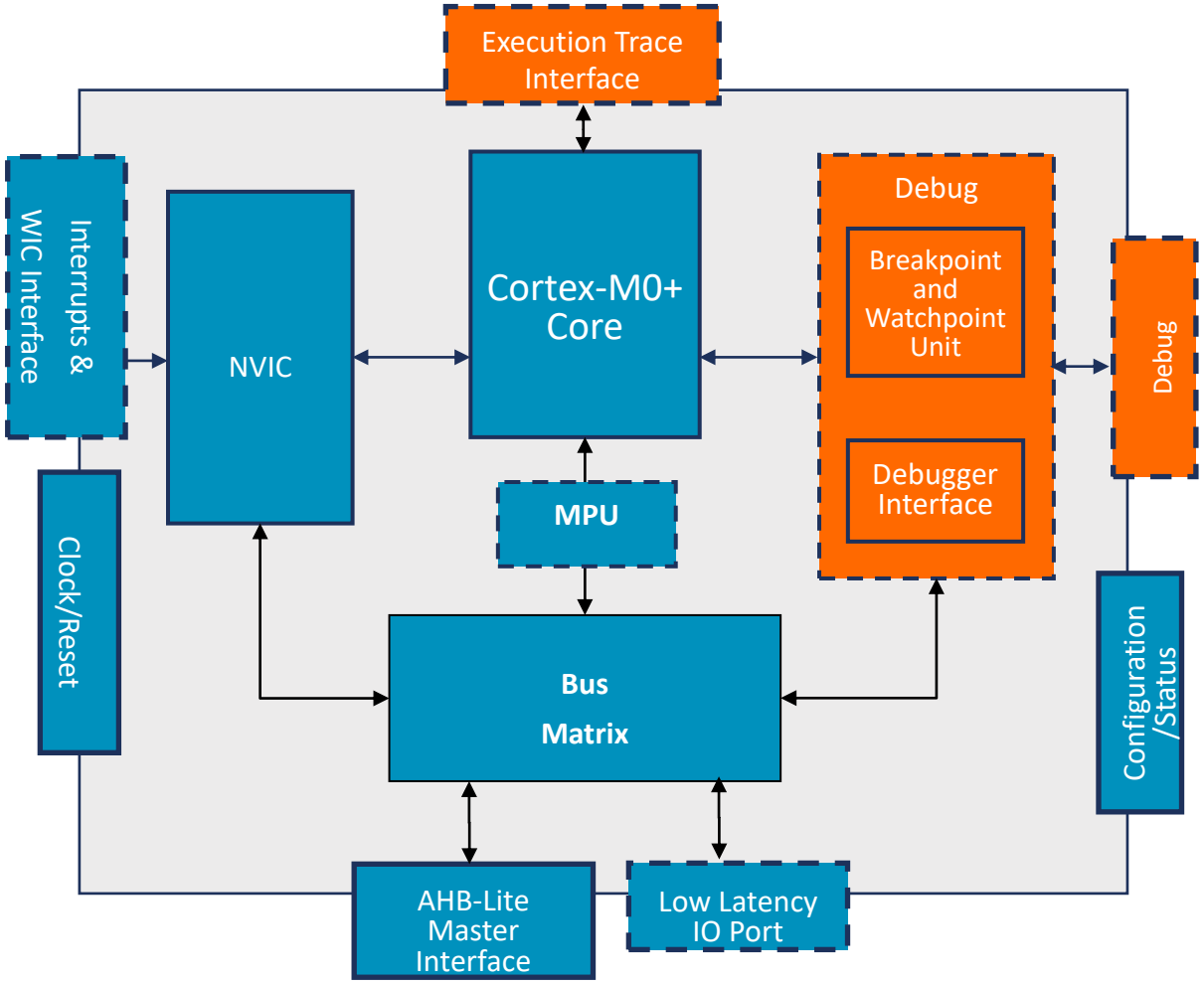
AMBA®AHB-Lite Master Interface

Ultra-low power support

Synthesizable - configurable RTL

Gate count 12 ~ 25K

Arm Cortex-M0+ processor



- Armv6-M architecture
- Thumb technology
- Nested Vector Interrupt Controller (NVIC)
- Optional CoreSight™-compliant debug
- Optional user/privileged support
- Optional MPU
- Von-Neumann architecture
- 2-stage core pipeline
- AMBA AHB-Lite master interface
- Optional Micro Trace Buffer (MTB)
- Optional single cycle IO Port
- Optional halfword instruction fetch
- Ultra-low power support
- Synthesizable - configurable RTL

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Arm Cortex-M3/M4 processor

Armv7-M Architecture

Harvard Architecture

Configurable Blocks

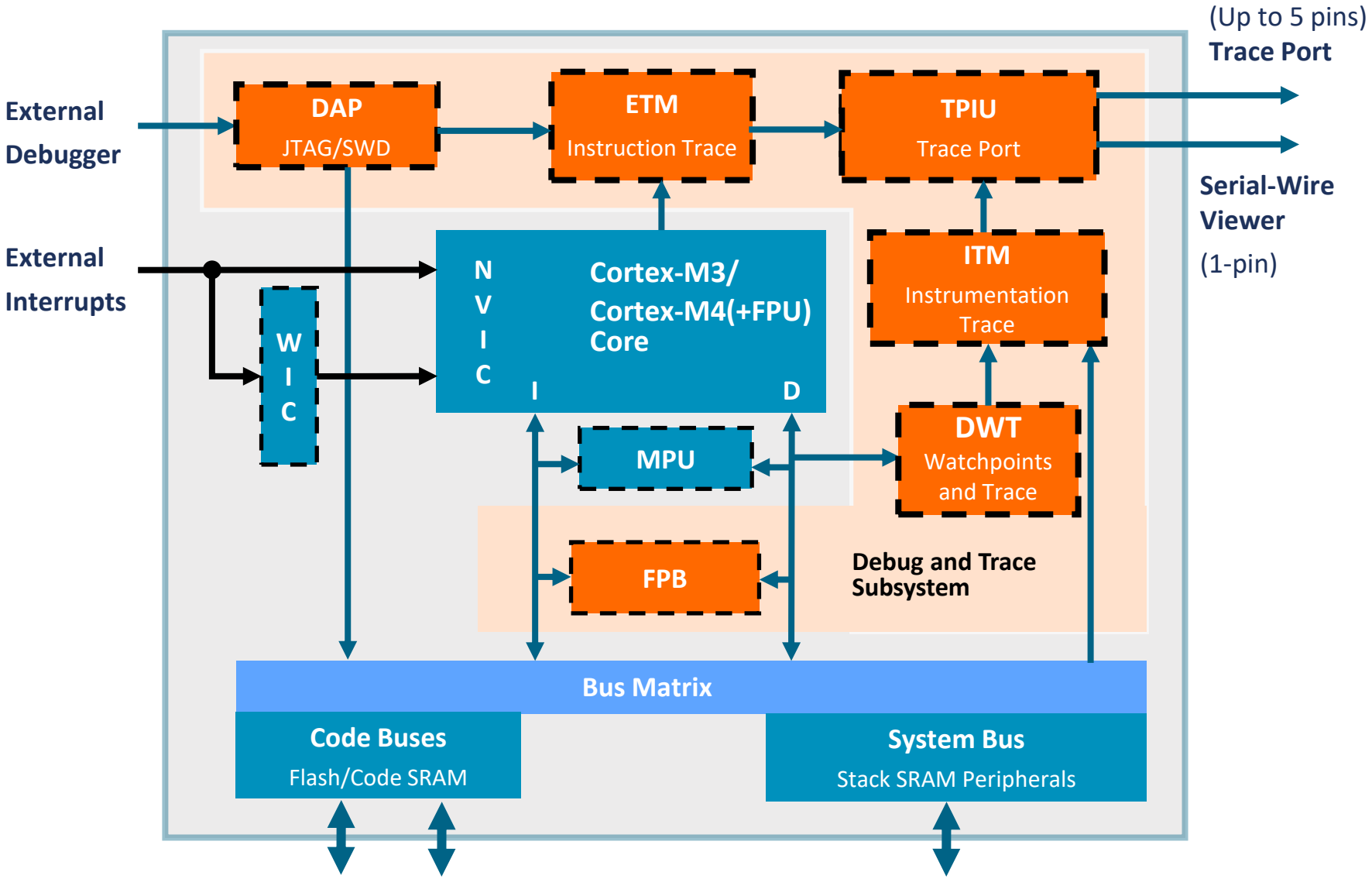
- Cortex-M3/M4 Core
  - Optional FPU on M4
- NVIC
  - Interrupts : 1 - 240
  - Priority bits : 3 – 8

Optional Blocks

- Debug and Trace Subsystem
- Wakeup Interrupt Controller
- Memory Protection Unit

Configurable Features

- Sleep modes, Endianness, Bit-Banding, and more ...



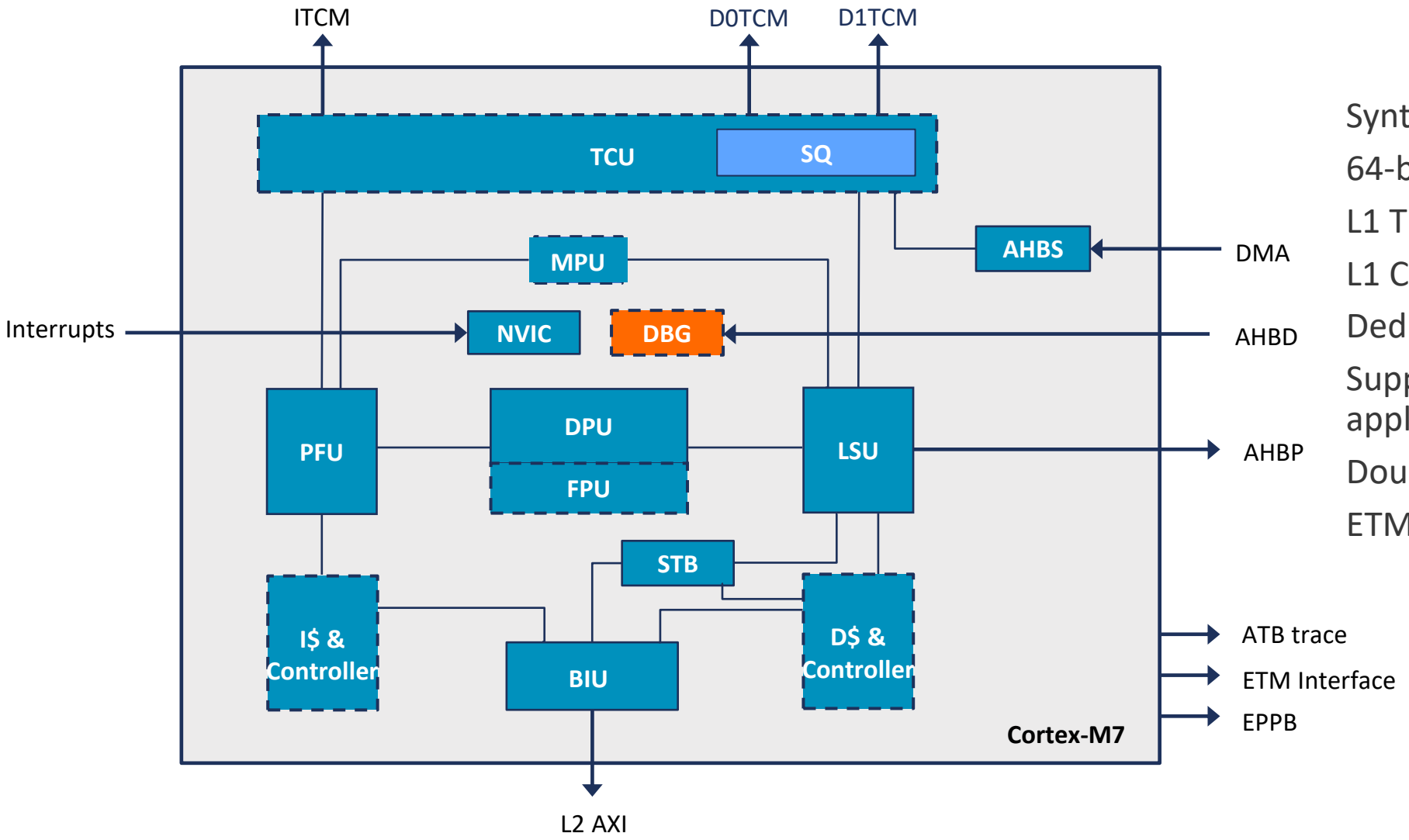
Differences between Cortex-M3 and Cortex-M4

Cortex-M3 and Cortex-M4 processors are derived from same database

Improvements and new features that make them different

Feature	Cortex-M3	Cortex-M4
Armv7-M architecture variant	**Base** *(Armv7-M)*	**Extended** *(Armv7E-M)*
SIMD & DSP instructions supported	**NO**	**YES**
Supports optional FPv4-SP extension	**NO**	**YES**
No of cycles for multiplication operation	**1-7**	**1**
Support for fault-robust interface	**Present**	**Absent**
Bundle	**Example System**	**Integration Kit**

Arm Cortex-M7 processor



- Synthesizable - configurable RTL
- 64-bit AXI bus interface
- L1 Tightly Coupled Memory (TCM)
- L1 Caches
- Dedicated peripheral and DMA ports
- Support for safety/reliability-critical applications (including ASIL-D)
- Double precision support
- ETM data trace

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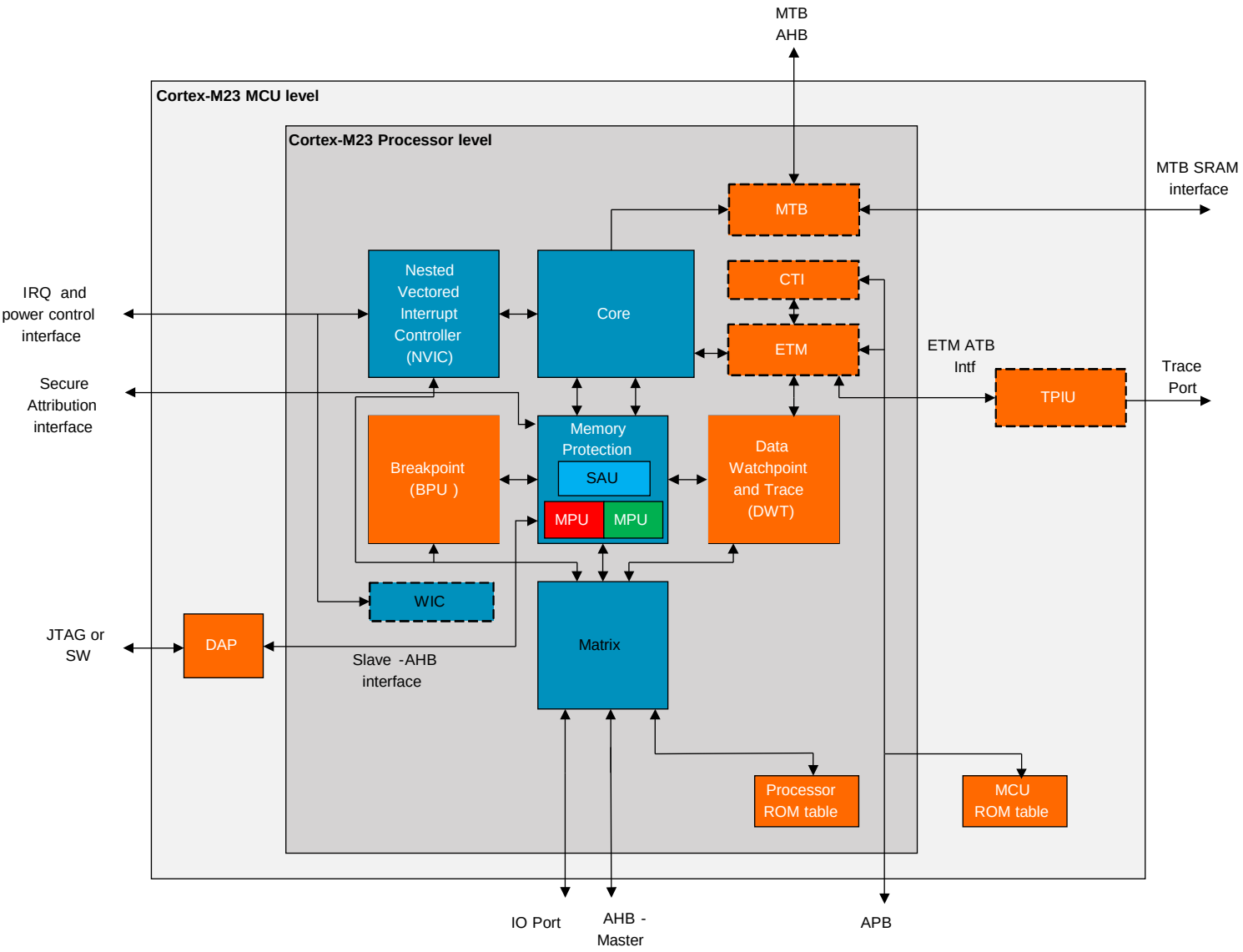
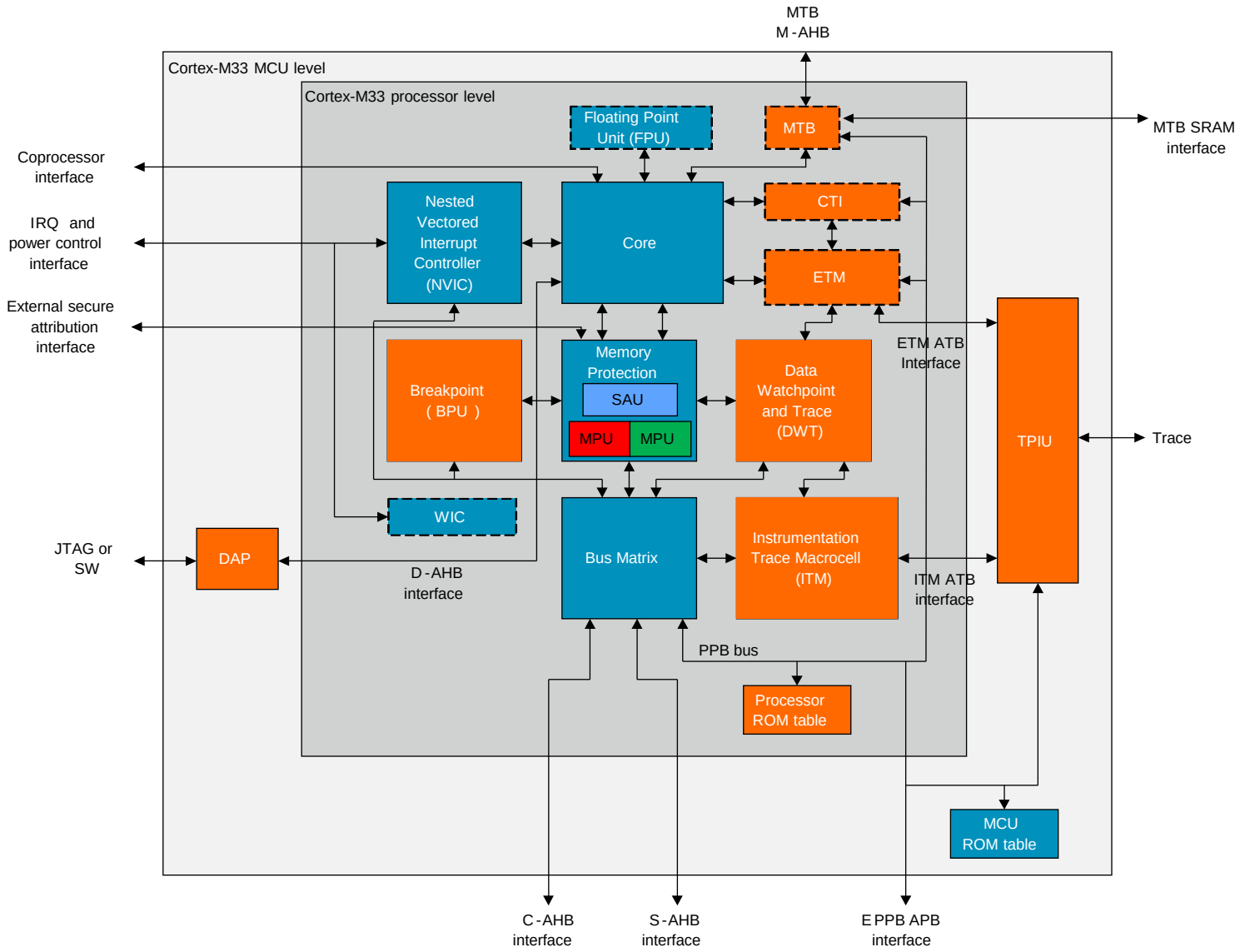
Arm Cortex-M23 Processor



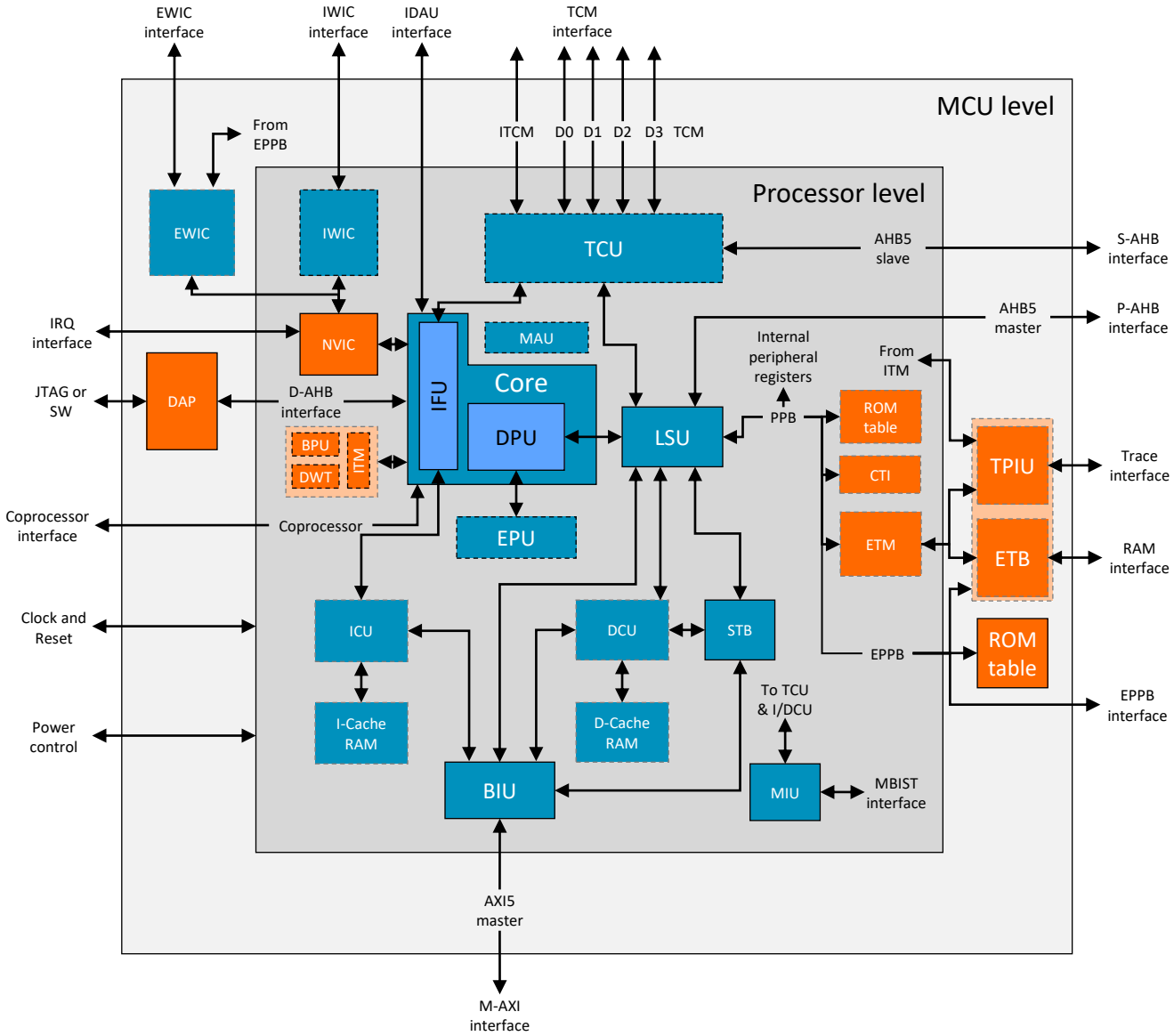
- Baseline profile of Armv8-M
- Synthesizable - configurable RTL
- In-order 2 stage pipeline
- Optional Security Extension
- PMSAv8 memory system architecture
- MPU supporting up to 16 regions
- SAU supporting up to 8 regions
- NVIC supporting up to 240 interrupts
- Hardware Multiplier (Fast/Small)
- Hardware Divider (Fast/Small)
- AMBA5 AHB Master Interface
- Optional single cycle IO Port
- Optional halfword instruction fetch
- CoreSight-compliant Debug & Trace
- Ultra-low Power Support with separate power domains

Arm Cortex-M33 Processor



- Mainline profile of Armv8-M
- Synthesizable - configurable RTL
- In-order 2/3 stage pipeline
- Optional Security Extension
- Optional Floating-point Extension (FPv5)
- Optional DSP Extension
- PMSAv8 memory system architecture
- MPU supporting up to 16 regions
- SAU supporting up to 8 regions
- NVIC supporting up to 480 interrupts
- AMBA5 AHB Master Interface
- CoreSight-compliant Debug & Trace
- Ultra-low Power Support with separate power domains
- External coprocessor support

Arm Cortex-M55 Processor



- Synthesizable - configurable RTL
- Mainline profile of Armv8.1-M with DSP Extension
- In-order 3/4 stage pipeline
- Optional Security Extension
- Optional Floating-point Extension (FPv5)
- Optional M-profile Vector Extension (MVE)
- PMSAv8 memory system architecture
- MPU supporting up to 16 regions
- SAU supporting up to 8 regions
- NVIC supporting up to 480 interrupts
- Tightly Coupled Memory (TCM)
- 64-bit AMBA AXI5 bus interface
- Separate instruction and data L1 caches
- 32-bit AMBA5 AHB Master Interface
- CoreSight-compliant Debug & Trace
- Performance Monitoring Unit (PMU)
- Ultra-low Power Support with separate power domains
- External coprocessor support

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Introduction

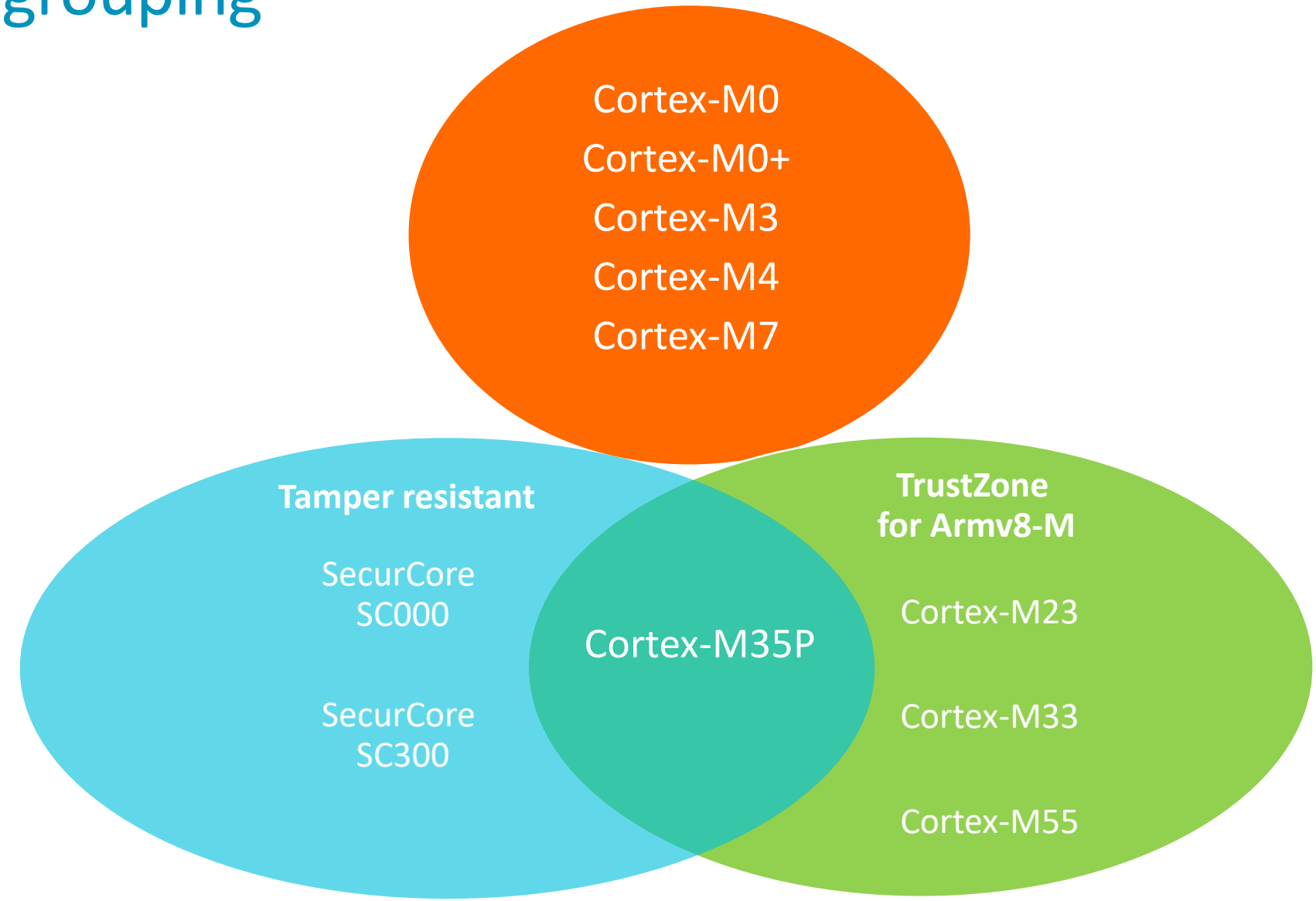
Armv6-M Cortex processors

Armv7-M Cortex processors

Armv8-M Cortex processors

Processor selection

Security grouping



Cortex-M selection considerations

- CoreMark and Dhrystone (per MHz)
  - Results depends on C compiler used
  - Might not be a good indication of the performance for your real world applications

Actual performance depends on
- System-level design
- Memory wait states
- Clock configurations, etc

Cortex-M0+ can be faster for simple I/O control tasks because of
- Shorter pipeline
- Single cycle I/O interface

Cortex-M23
- TrustZone
- HW stack protection

Cortex-M3/Cortex-M4 is high performance
- Richer instruction set
- Harvard bus architecture
- Write buffer
- Speculative fetch of branch targets

Cortex-M33
- TrustZone
- HW stack protection
- Co-processor

Cortex-M7
- 5.01 CoreMark
- TCM
- AXI
- Cache

Cortex-M35P
- Tamper resistance
- TrustZone
- HW stack protection
- Co-processor

Cortex-M55
- 4.2 CoreMark
- TCM, AXI, Cache
- Optimized for ML & signal processing

Thank You
Danke
Gracias
Grazie
谢谢
ありがとう
Asante
Merci
감사합니다
धन्यवाद
Kiitos
شكرًا
ধন্যবাদ
תודה