ARM R Series

The example application is flight control of a commercial hexapod, for this reason and given that we are using an ARM R series processor, I would consider this a hard-real time application, meaning that our main choices would be either cyclic executive or RTOS, given that this would deliver parcels in a urban environment I would feel more comfortable using a cyclic executive approach nonetheless any choice from the 2 is valid.

TABLE OF ARM R Series Processors

Cortex-R4	Cortex-R5	Cortex-R7 [†]	Cortex-R8	Cortex-R52	Cortex-R52+	Cortex-R82
Armv7-R	Armv7-R	Armv7-R	Armv7-R	Armv8-R	Armv8-R	Armv8-R
8 stage in-order, dual issue	8 stage in-order, dual issue	11 stage out-of-order, superscalar	11 stage out-of-order, superscalar	8 stage in-order, superscalar	8 stage in-order, superscalar	8 stage in-order, triple issue
32	32	32	32	32	32	40
4GB	4GB	4GB	4GB	4GB	4GB	1TB
Yes	Yes	Yes	Yes	Yes	Yes	Yes
мри	MPU	MPU	MPU	MPU	MPU	Both
12	16	16	24	24+24	24+24	32+32
1 core, No coherency	2 core, IO coherency	Up to MP2	Up to MP4	Up to UP4, No coherency	Up to MP4	Up to MP8
Optional	Optional	Optional	Optional	Optional	Optional	Optional
No	No	No	No	Optional	Optional	Optional
1.67	1.67	2.5	2.5	2.04	2.04	3.4
3.47	3.47	4.35	4.62	4.3	4.3	5.82
Up to 480	Up to 480	Up to 480	Up to 480	Up to 960	Up to 960	56K+
AXI3	AXI3	AXI3	AXI3	AXI4	AXI4	AXI5
	8 stage in-order, dual issue 32 4GB 4GB 4GB 12 1 core, No coherency Optional No 1.67 3.47 Up to 480	Armv7-R	Armv7-R Armv7-R Armv7-R Armv7-R 8 stage inn-order, dual issue 8 stage inn-order, dual issue 11 stage out-of-order, superscalar 32 32 32 32 4GB 4GB 4GB 4GB Yes Yes Yes MPU MPU MPU MPU MPU 12 16 16 16 1 core, No coherency 2 core, IO coherency Up to MP2 Optional Optional Optional No No No 1.67 2.5 3.47 3.47 4.35 Up to 480 Up to 480 Up to 480	Armv7-R Armv7-R <t< td=""><td>Armv7-R Armv7-R Armv7-R Armv7-R Armv6-R Armv6-R B stage in-order, obad issue 11 stage out-of-order, superscalar 11 stage out-of-order, superscalar Stage in-order, superscalar 32 32 32 32 32 32 32 32 32 32 32 32 32 32 32 4GB 4HPU MPU MPU MPU 4HPU</td><td>Armv7-R Armv7-R Armv7-R Armv7-R Armv7-R Armv6-R Butch of the proper to superscalar <</td></t<>	Armv7-R Armv7-R Armv7-R Armv7-R Armv6-R Armv6-R B stage in-order, obad issue 11 stage out-of-order, superscalar 11 stage out-of-order, superscalar Stage in-order, superscalar 32 32 32 32 32 32 32 32 32 32 32 32 32 32 32 4GB 4HPU MPU MPU MPU 4HPU	Armv7-R Armv7-R Armv7-R Armv7-R Armv7-R Armv6-R Butch of the proper to superscalar <

CHOOSING A CPU

Any choice from the previous table is good, this is an engineering choice, once again, it depends on budget and features that we need, I would suggest starting with the most simple and cheapest Cortex-R4 and consider if this can meet the requirements of our application. However to list a few, ECC memory, interrupts and in-order pipeline are good features to have.