RG500U Series

Hardware Design

5G Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any terminal or mobile incorporating the module. Manufacturers of the terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2022-07-13	Neeson ZHANG/ Dominic GONG/ Gale GAO	Creation of the document
1.0	2022-09-14	Neeson ZHANG/ Cavan ZHU	First official release
1.1	2023-02-28	Anthony LIU/ Cavan ZHU	1. Added RG500U-CN and the related information. 2. Added optional n5 and n71 bands for RG500U-EA. 3. Updated the requirement of reserved test points of USB interface and debugging UART; Added notes related to reserved test points of VDD_EXT and RESET_N (Table 6, Table 10 and Chapter 3.8). 4. Updated the ESR parameter requirements for bypass capacitor in power supply reference circuit (Chapter 3.5.2). 5. Added the requirement of peak current (Chapter 3.5.3). 6. Updated ADC typical resolution (Table 17). 7. Updated the data of LB operating frequencies for ANT4 and ANT5 of RG500U-EA (Table 29). 8. Updated the RF receiving sensitivity data for LTE and 5G NR bands of RG500U-EA (Table 44). 9. Updated the recommended value of ramp-to-soak slope in soak zone, and of ramp-up slope and cool-down slope in reflow zone; add a note for the measured temperature of the solder joints (Table 46). 10. Added the mounting direction of the module (Chapter 7.3.3).

1.2	2024-09-23	Kyle CHEN/ Cavan ZHU/ Achang ZHANG	1. Added applicable modules of RG500U-EB, RG500U-JO and RG500U-LA. 2. Added n66 band and deleted n79 band for RG500U-EA. 3. Added 5G SRS information; Added a note on LTE and UMTS features of RG 500U-JO; Updated the USB serial drivers (Table 7). 4. Added a note on avoiding abnormal RF functions caused by current sink on the module's pins (Chapter 3.1). 5. Added the figure of DRX run time and power consumption in sleep mode and related note (Chapter 3.4.1). 6. Updated the figure of power-up timing (Chapter 3.61.1). 7. Updated the reference circuit for RF antennas and added relevant notes (Chapter 4.1.4). 8. Updated the power consumption (Table 51 and Table 52). 9. Updated module's coplanarity standard (Chapter 6.1). 10. Updated the note for manufacturing and soldering (Chapter 7.2).

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1 Introduction

This document defines RG500U series and describes its air interface and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, an asterisk (*) after a function, feature, interface, pin name, command, argument, and so on indicates that it is under development and currently not supported; and the asterisk (*) after a model indicates that the model sample is currently unavailable.

2 Product Overview

2.1. General Description

RG500U series is a 5G NR/LTE/WCDMA wireless communication module, which provides data connectivity on 5G NR, LTE-FDD, LTE-TDD, HSDPA, HSUPA, HSPA+ and WCDMA networks.

RG500U series is an industrial-grade module for industrial and commercial applications only.

The following tables show the supported frequency bands of the module.

Table 2: RG500U-CN Frequency Bands

Mode	Frequency Band
5G NR	n1/n28/n41/n77/n78/n79
LTE-FDD	B1/B2/B3/B5/B7/B8/B20/B28
LTE-TDD	B34/B38/B39/B40/B41
WCDMA	B1/B2/B5/B8

Table 3: RG500U-EA Frequency Bands

Mode	Frequency Band
5G NR [1]	n1/n3/n5/n7/n8/n20/n28/n38/n40/n41/n66/n71*/n77/n78
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B20/B28/B66
LTE-TDD	B38/B40/B41
WCDMA	B1/B2/B5/B8

[1] n71 is optional. For more details, contact Quectel Technical Support.

Table 4: RG500U-EB Frequency Bands

Mode	Frequency Band
5G NR	n1/n3/n5/n7/n8/n20/n28/n38/n40/n41/n66/n77/n78
LTE-FDD	B1/B2/B3/B4/B5/B7/B8/B20/B28/B66
LTE-TDD	B38/B40/B41
WCDMA	B1/B2/B5/B8

Table 5: RG500U-LA Frequency Bands

Mode	Frequency Band
5G NR	n2/n5/n7/n8/n28/n38/n40/n66/n71/n78
LTE-FDD	B2/B4/B5/B7/B8/B26/B28/B66/B71
LTE-TDD	B38/B40
WCDMA	B2/B4/B5

Table 6: RG500U-JO Frequency Bands

Mode	Frequency Band
5G NR	n78

With a compact profile of 44.0 mm × 41.0 mm × 2.85 mm, RG500U series is an SMD type module which can be embedded in applications through its 392 LGA pins.

NOTE

For details about CA and EN-DC configurations, see ***document [1]***.

2.2. Key Features

Table 7: Key Features

Feature	Details
Power Supply	● Supply voltage range: 3.3–4.3 V ● Typical supply voltage: 3.8 V
Transmitting Power	**RG500U-CN:** ● WCDMA B1/B2/B5/B8: Class 3 (23 dBm ±2 dB) ● LTE B1/B2/B3/B5/B7/B8/B20/B28: Class 3 (23 dBm ±2 dB) ● LTE B34/B38/B39/B40/B41: Class 3 (23 dBm ±2 dB) ● LTE B41 HPUE: Class 2 (26 dBm ±2 dB) ● 5G NR n1: Class 3 (23 dBm ±2 dB) ● 5G NR n28: Class 3 (23 dBm +2/-2.5 dB) ● 5G NR n41/n77/n78/n79: Class 3 (23 dBm +2/-3 dB) ● 5G NR n41/n78/n79 HPUE: Class 2 (26 dBm +2/-3 dB) **RG500U-EA:** ● WCDMA B1/B2/B5/B8: Class 3 (23 dBm ±2 dB) ● LTE B1/B2/B3/B4/B5/B7/B8/B20/B28/B38/B40/B41/B66: Class 3 (23 dBm ±2 dB) ● LTE B41 HPUE: Class 2 (26 dBm ±2 dB) ● 5G NR n1/n3/n5/n7/n8/n20/n38/n40/n41/n66: Class 3 (23 dBm ±2 dB) ● 5G NR n28/n71*: Class 3 (23 dBm +2/-2.5 dB) ● 5G NR n77/n78: Class 3 (23 dBm +2/-3 dB) ● 5G NR n41/n77/n78 HPUE: Class 2 (26 dBm +2/-3 dB) **RG500U-EB:** ● WCDMA B1/B2/B5/B8: Class 3 (23 dBm ±2 dB) ● LTE B1/B2/B3/B4/B5/B7/B8/B20/B28/B38/B40/B41/B66: Class 3(23 dBm ±2 dB) ● 5G NR n1/n3/n5/n7/n8/n20/n38/n40/n41/n66: Class 3 (23 dBm ±2 dB) ● 5G NR n28: Class 3 (23 dBm +2/-2.5 dB) ● 5G NR n77/n78: Class 3 (23 dBm +2/-3 dB) ● 5G NR n41/n77/n78 HPUE: Class 2 (26 dBm +2/-3 dB) **RG500U-LA:** ● WCDMA B2/B4/B5: Class 3 (23 dBm ±2 dB) ● LTE B2/B4/B5/B7/B8/B26/B28/B38/B40/B66/B71: Class 3 (23 dBm ±2 dB) ● 5G NR n2/n5/n7/n8/n38/n40/n66: Class 3 (23 dBm ±2 dB) ● 5G NR n28/n71: Class 3 (23 dBm +2/-2.5 dB) ● 5G NR n78: Class 3 (23 dBm +2/-3 dB) ● 5G NR n78 HPUE: Class 2 (26 dBm +2/-3 dB) **RG500U-JO:** ● 5G NR n78: Class 3 (23 dBm +2/-3 dB)

	● 5G NR n78 HPUE: Class 2 (26 dBm +2/-3 dB)
5G NR Features	● 3GPP Release Standard **RG500U-CN/RG500U-EA/RG500U-EB/RG500U-LA/RG500U-JO:** Supports 3GPP Rel-15 **RG500U-CN:** 3GPP Rel-16 (Optional) ● Supported modulations: - UL: BPSK, QPSK, 16QAM, 64QAM and 256QAM - DL: QPSK, 16QAM, 64QAM and 256QAM ● Supported MIMO: - DL: 4 × 4 MIMO **RG500U-CN:** n1/n41/n77/n78/n79 **RG500U-EA:** n1/n3/n7/n38/n40/n41/n77/n78 **RG500U-EB**: n1/n3/n7/n28/n38/n40/n41/n66/n77/n78 **RG500U-LA:** n2/7/28/38/40/66/78 **RG500U-JO:** n78 - DL: 2 × 2 MIMO **RG500U-CN:** n28 **RG500U-EA:** n5/n8/n20/n28/n71* **RG500U-EB**: n5/n8/n20 **RG500U-LA:** n5/8/71 - UL: 2 × 2 MIMO **RG500U-CN:** n41/n77/n78/n79 **RG500U-EA:** n38/n40/n41/n77/n78 **RG500U-EB**: n38/n40/n41/n77/n78 **RG500U-LA:** n38/40/78 **RG500U-JO:** n78 ● Supports SCS 15 kHz and 30 kHz [2] ● Supports SA and NSA operation modes ● Supports Option 3x, 3a, 3 and Option 2 ● Max. transmission data rates [3]: **RG500U-CN:** - NSA: 2.2 Gbps (DL)/575 Mbps (UL) - SA: 2 Gbps (DL)/1 Gbps (UL) **RG500U-EA/RG500U-EB/RG500U-LA:** - NSA: 2.6 Gbps (DL)/650 Mbps (UL) - SA: 2 Gbps (DL)/1 Gbps (UL) **RG500U-JO:** - SA: 2 Gbps (DL)/1 Gbps (UL) ● SRS **RG500U-CN** - NSA: 1T2R (n41/n78/n79)

[2] 5G NR FDD bands only support 15 kHz SCS, and 5G NR TDD bands only support 30 kHz SCS.
[3] The maximum rates are theoretical and the actual values depend on the network configuration.

	- SA: 2T4R (n41/n77/n78/n79) **RG500U-EA** - NSA: 1T2R (n40) 1T4R(n38/n41/n77/n78) - SA: 2T4R (n38/n40/n41/n77/n78) **RG500U-EB** - NSA: 1T4R (n38/n40/n41/n77/n78) - SA: 2T4R (n38/n40/n41/n77/n78) **RG500U-LA** - NSA: 1T2R (n40) 1T4R(n78) - SA: 2T4R (n38/n40/n78) **RG500U-JO** - SA: 2T4R (n78)
LTE Features [4]	● Supports up to: - CA: 3CC (DL), 2CC (UL) - FDD: Cat 12 (DL), Cat 13 (UL) - TDD: Cat 12 (DL), Cat 13 (UL) ● Supports 1.4/3/5/10/15/20 MHz RF bandwidths ● Supported modulations: - UL: QPSK, 16QAM and 64QAM - DL: QPSK, 16QAM, 64QAM and 256QAM ● Supports DL 2 × 2 MIMO ● Max. transmission data rates: - 600 Mbps (DL)/150 Mbps (UL)
UMTS Features [4]	● Supports 3GPP Rel-9 DC-HSDPA, HSDPA, HSUPA, HSPA+ and WCDMA ● Supports QPSK, 16QAM and 64QAM modulations ● Max. transmission data rates: - DC-HSDPA: 42.2 Mbps (DL) - HSUPA: 11 Mbps (UL) - WCDMA: 384 kbps (DL)/384 kbps (UL)
Internet Protocol Features	● Supports TCP/UDP/PPP/NTP/NITZ/FTP/HTTP/PING/CMUX*/HTTPS/ FTPS/SSL/FILE/MQTT*/MMS*/SMTP*/SMTPS* protocols ● Supports the protocols PAP and CHAP
SMS	● Text and PDU modes ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: (U)SIM by default
(U)SIM Interfaces	Supports SIM/USIM cards: 1.8/3.0 V
USB Interface	● Compliant with USB 3.0 and 2.0 specifications, with maximum transmission rates up to 5 Gbps on USB 3.0 and 480 Mbps on USB 2.0 ● Used for AT command communication, data transmission, software debugging and firmware upgrade

[4] RG500U-JO does not support LTE and UMTS features.

	● Supports USB serial drivers for: Windows 8.1/10/11, Linux 2.6–6.7, Android 4.x–13.x
UART Interfaces	**Main UART interface:** ● Used for data transmission and AT command communication ● Baud rate: 115200 bps by default ● Not support RTS and CTS hardware flow control **Debug UART interface:** ● Used for log output ● Baud rate: 115200 bps
PCM Interface	● Supports 16-bit linear data format ● Supports short frame synchronization ● Supports master mode by default ● Can be multiplexed into I2S function
Audio Features	● Supports two digital audio interfaces: SPI and I2S ● Supports echo cancellation and noise suppression
Network Indication	NET_MODE and NET_STATUS to indicate network connectivity status
PCIe Interface	● Supports PCIe Gen 2 with backward compatibility ● Supports RC and EP modes ● Supports 1 lane, 5 Gbps/lane ● Can be used to connect to an Ethernet IC ● Supports PCIe drive for Linux 3.10–6.7
Antenna Tuner Control Interfaces	**RG500U-CN:** GRFC interfaces dedicated for the external antenna tuner **RG500U-EA/RG500U-EB/RG500U-LA/RG500U-JO:** GRFC interfaces dedicated for the external antenna tuner*
Antenna Interfaces	● Cellular antenna interfaces **RG500U-CN:** ANT0–ANT3 **RG500U-EA:** ANT0–ANT5 **RG500U-EB:** ANT0, ANT2, ANT4, ANT5 **RG500U-LA:** ANT0–ANT5 **RG500U-JO:** ANT1, ANT3, ANT4, ANT5 ● 50 Ω characteristic impedance
Rx-diversity	● RG500U-CN/EA/EB/LA 5G NR/LTE/WCDMA ● RG500U-JO 5G NR
AT Commands	● Compliant with *3GPP TS 27.007*, *27.005* ● Compliant with Quectel enhanced AT commands
Physical	● Size: (44.0 ±0.2) mm × (41.0 ±0.2) mm × (2.85 ±0.2) mm

Characteristics	● Weight: approx. 13 g
Temperature Ranges	● Operating temperature range: -30 to +75 °C [5] ● Extended temperature range: -40 to +85 °C [6] ● Storage temperature range: -40 to +90 °C
Firmware Upgrade	Via USB or DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of RG500U series and illustrates the major functional parts.

- Power management
- Baseband part
- Flash
- RF part
- Peripheral interfaces

[5] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module's indicators comply with 3GPP specification requirements.

[6] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module retains the ability to establish and maintain functions such as voice, SMS, data transmission and emergency call, without any unrecoverable malfunction. Radio spectrum and radio network remain uninfluenced, whereas the value of one or more parameters, such as Pout, may decrease and fall below the range of the 3GPP specified tolerances. When the temperature returns to the normal operating temperature range, the module's indicators will comply with 3GPP specification requirements again.

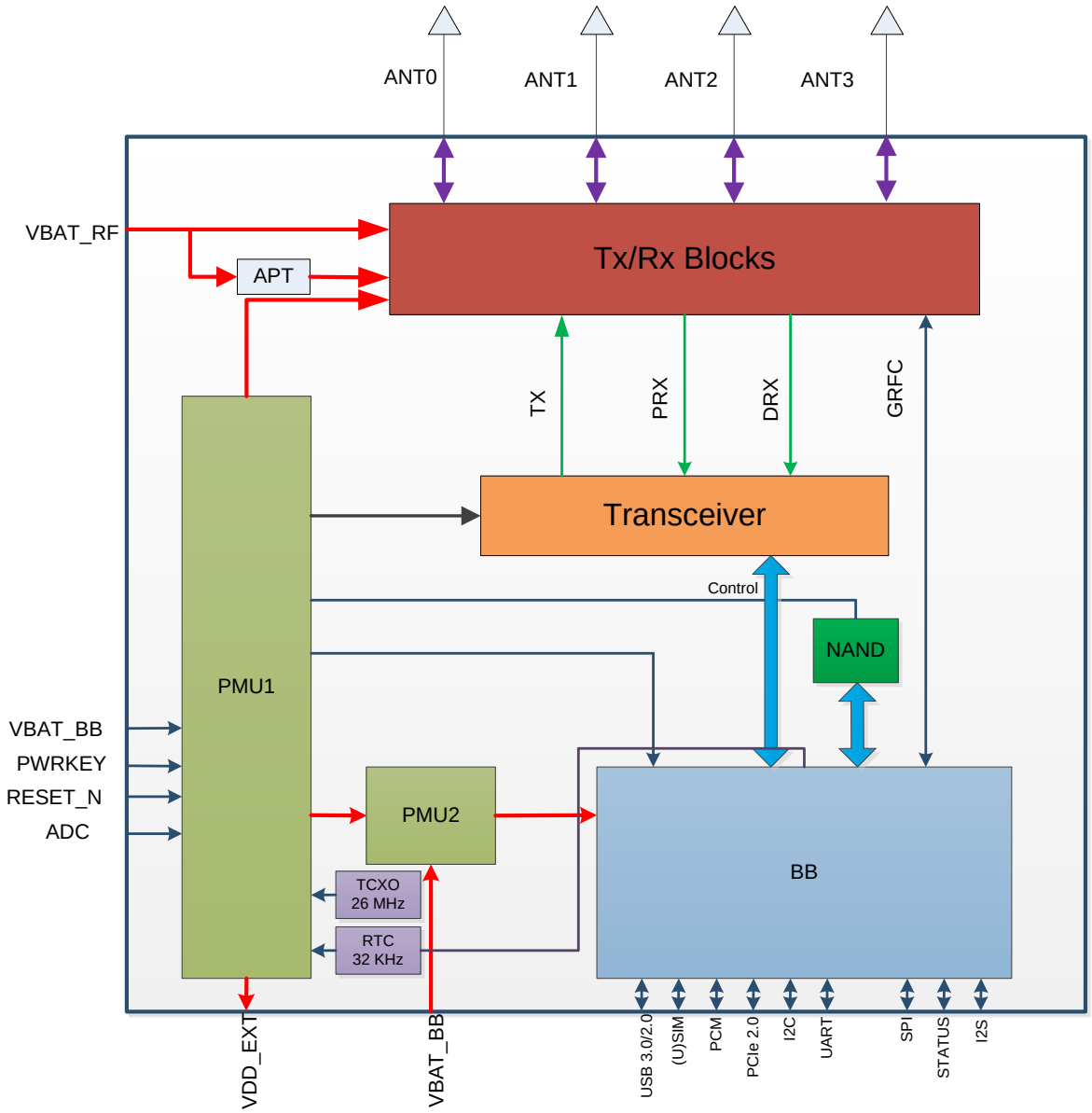


Figure 1: RG500U-CN Functional Diagram

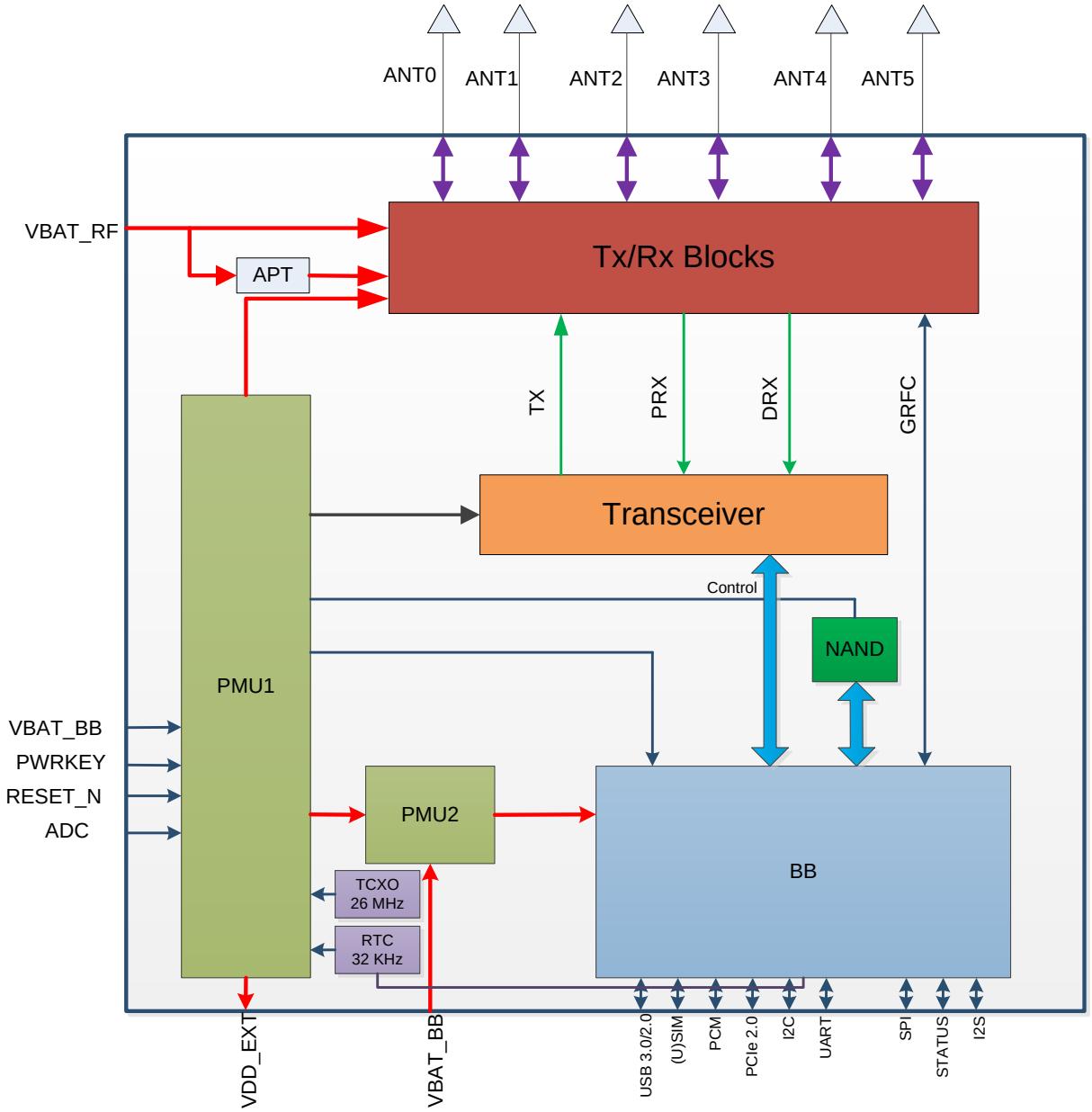


Figure 2: RG500U-EA Functional Diagram

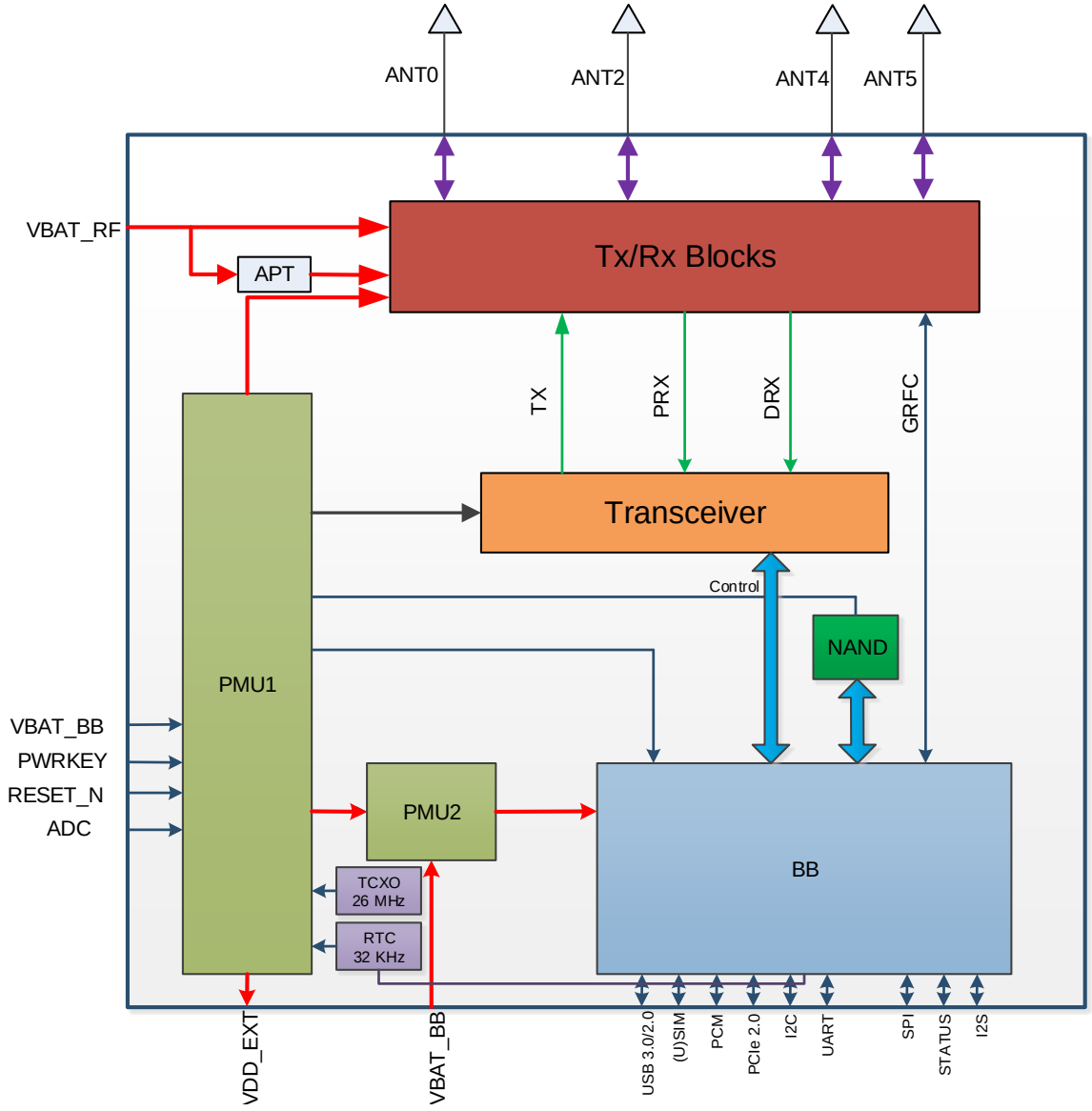


Figure 3: RG500U-EB Functional Diagram

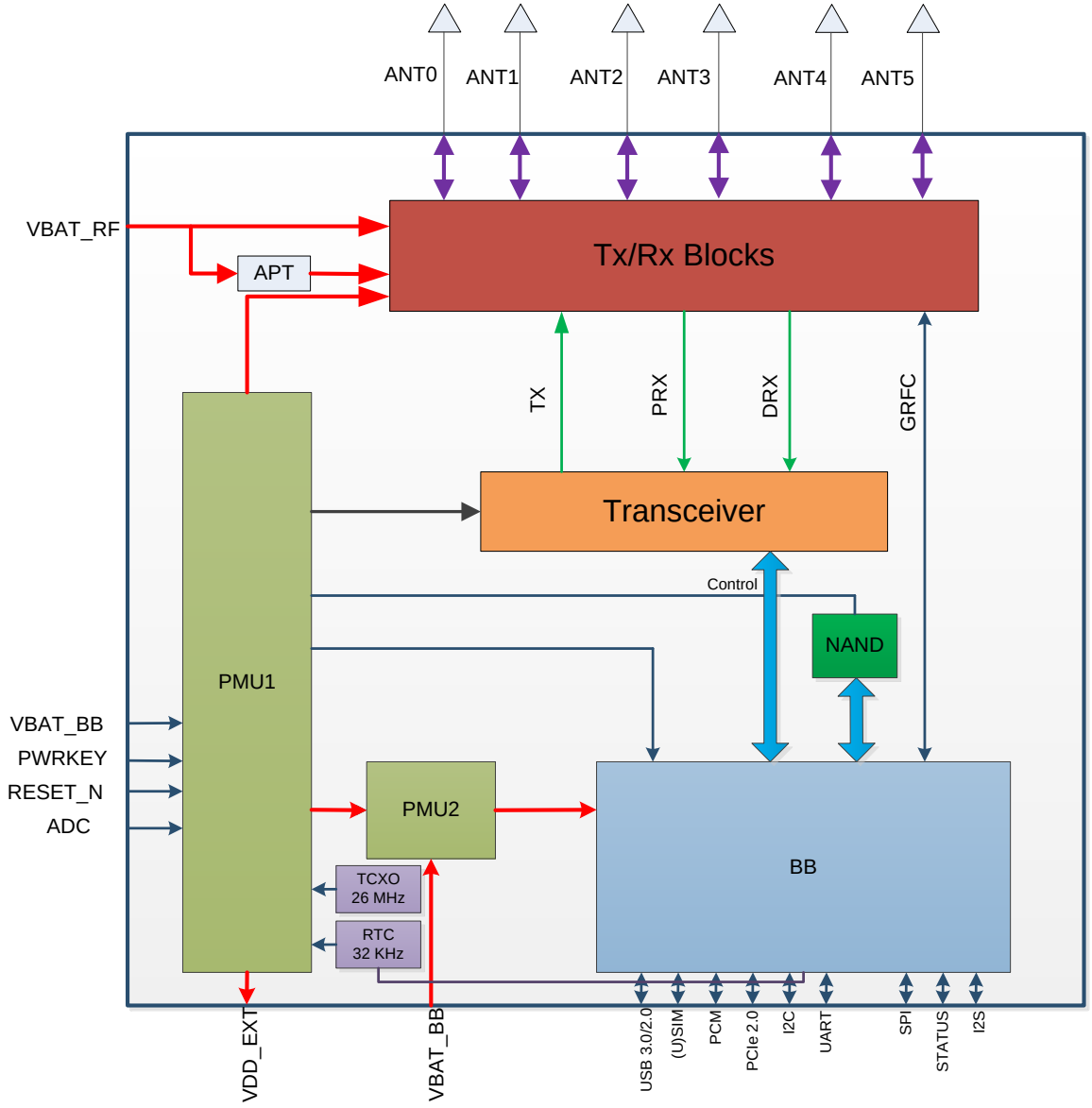


Figure 4: RG500U-LA Functional Diagram

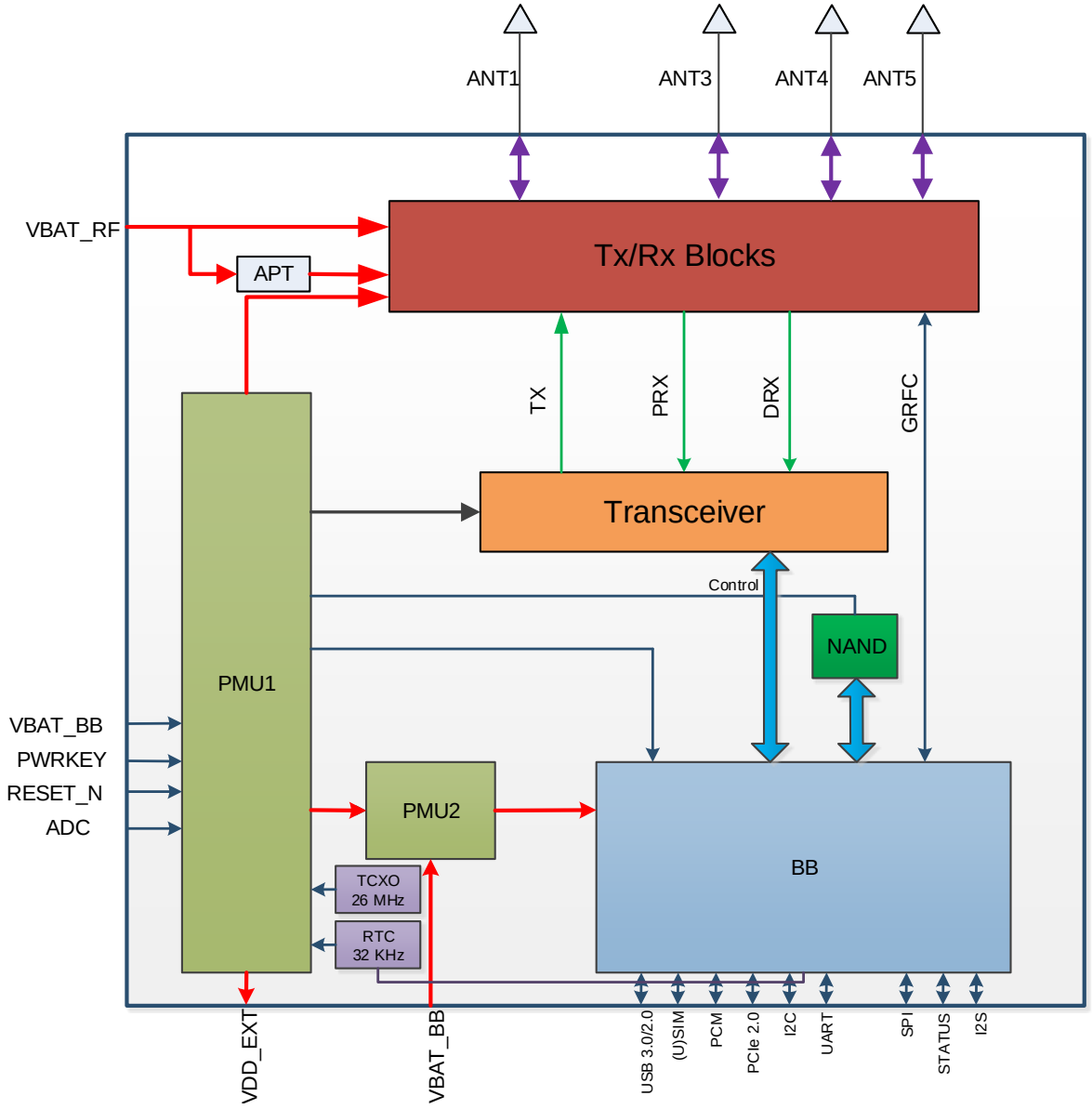


Figure 5: RG500U-JO Functional Diagram

2.4. EVB Kit

Quectel supplies an evaluation board (5G EVB) with accessories to develop and test the module. For more details, see ***document [2]***.

3 Application Interfaces

RG500U series is equipped with 392 LGA pins that can be connected to cellular application platform. The following interfaces are described in detail in subsequent chapters:

- Power supply
- (U)SIM interfaces
- USB interface
- UART interfaces
- I2S interface and SPI
- ADC interface
- Network status indication
- STATUS
- UART1_RI*
- USB_BOOT interface
- I2C interface
- PCIe interface
- Antenna tuner control interfaces

3.1. Pin Assignment

The following figure shows the pin assignment of the module.

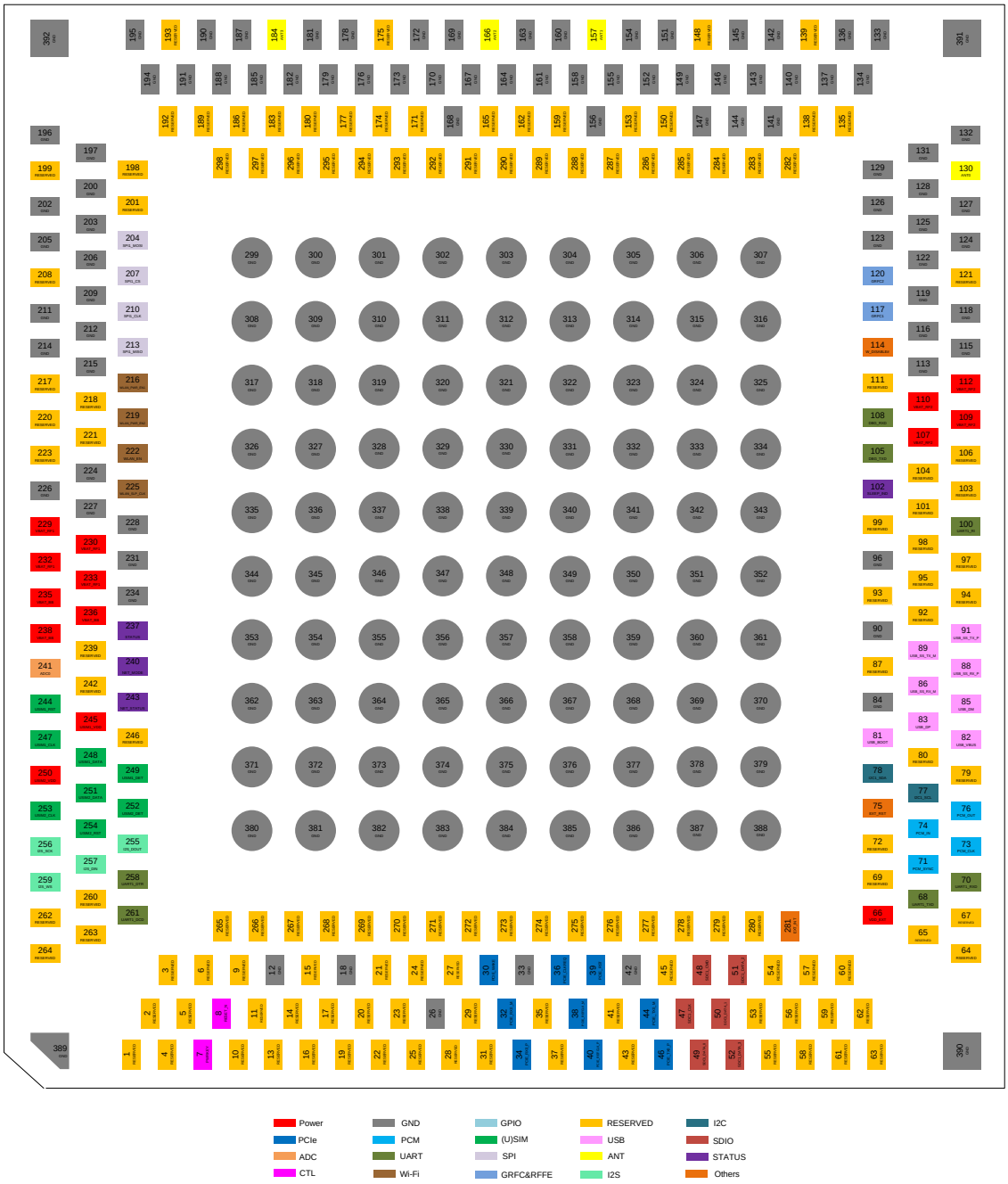


Figure 6: RG500U-CN Pin Assignment (Top View)

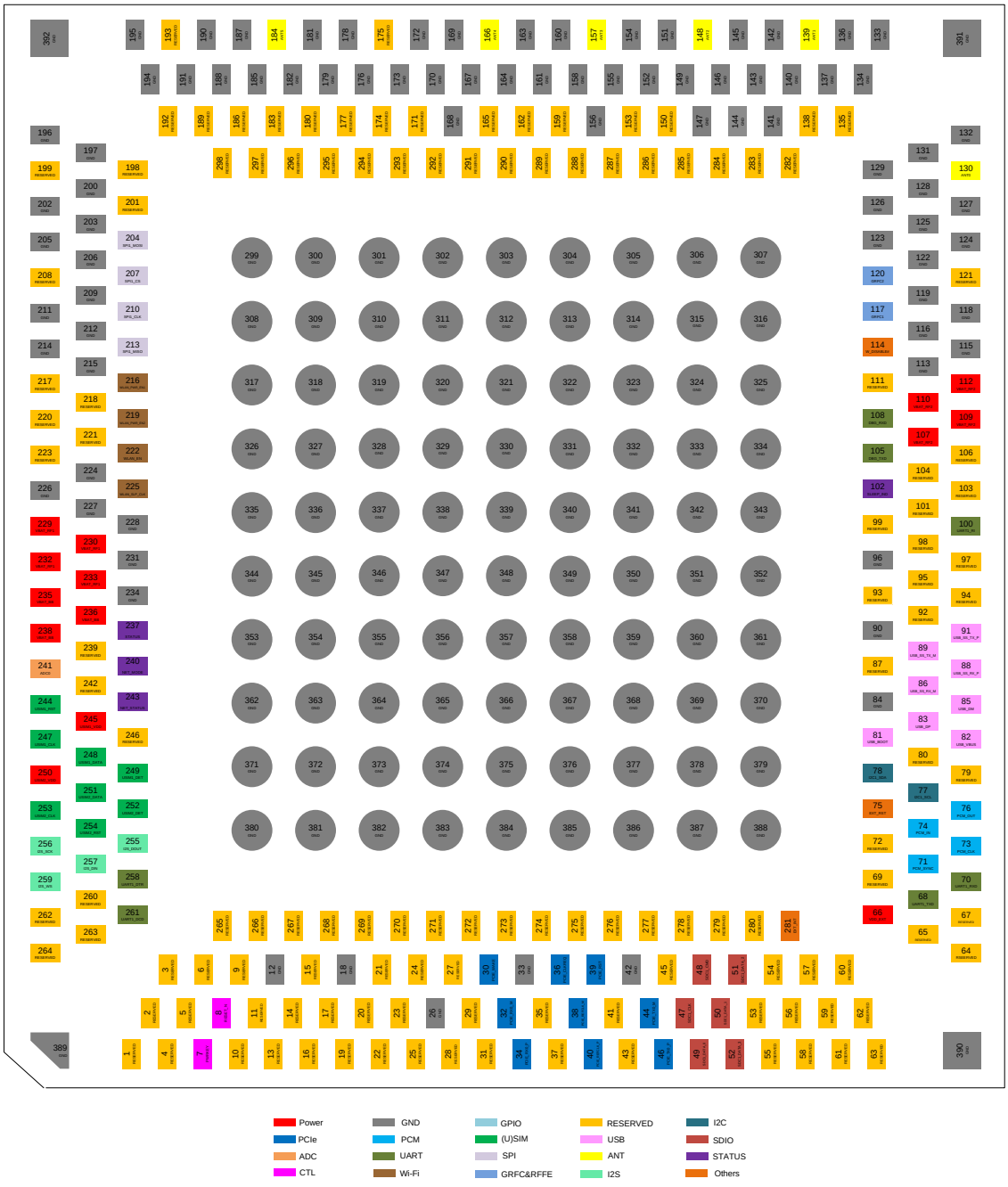


Figure 7: RG500U-EA Pin Assignment (Top View)

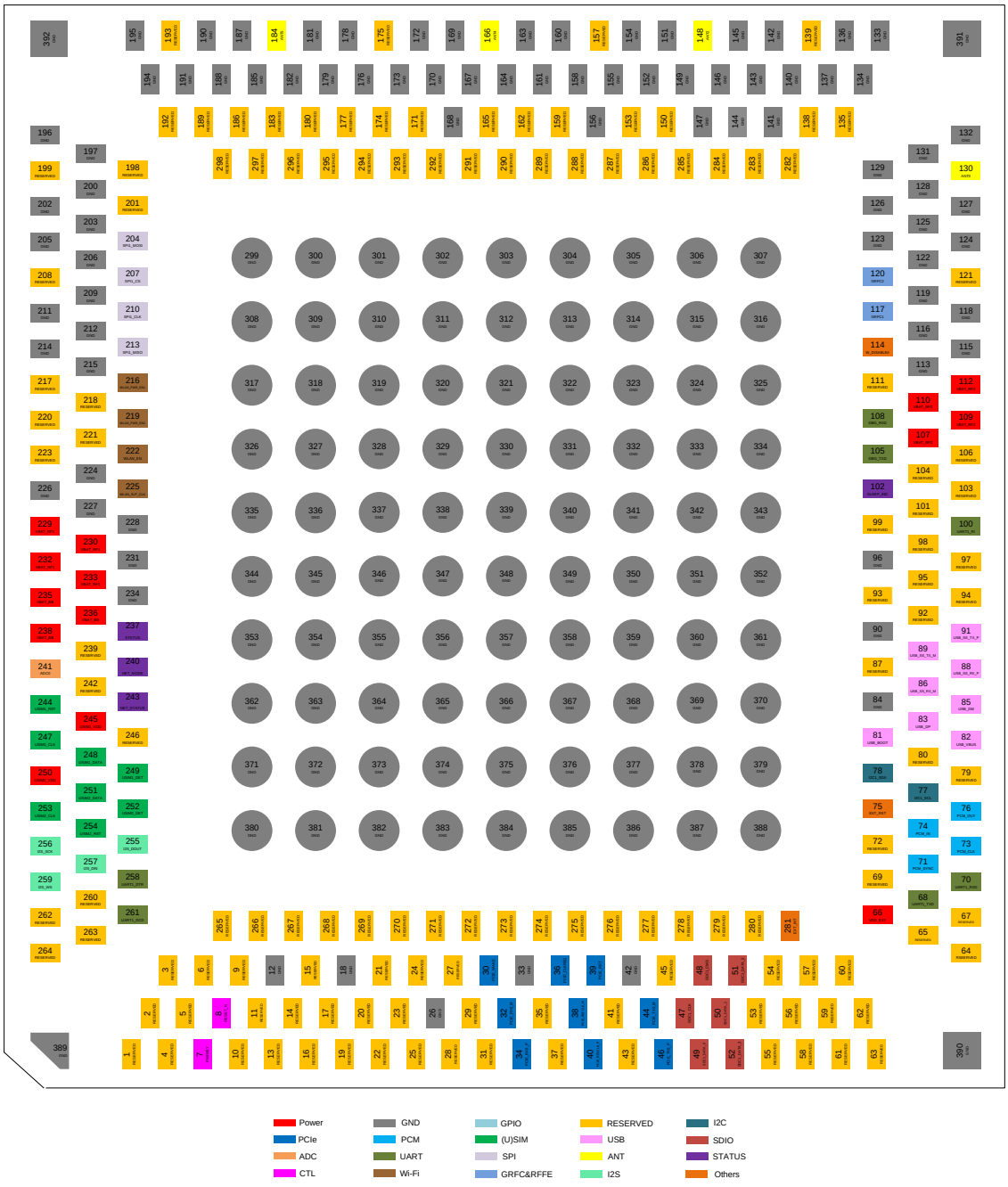


Figure 8: RG500U-EB Pin Assignment (Top View)

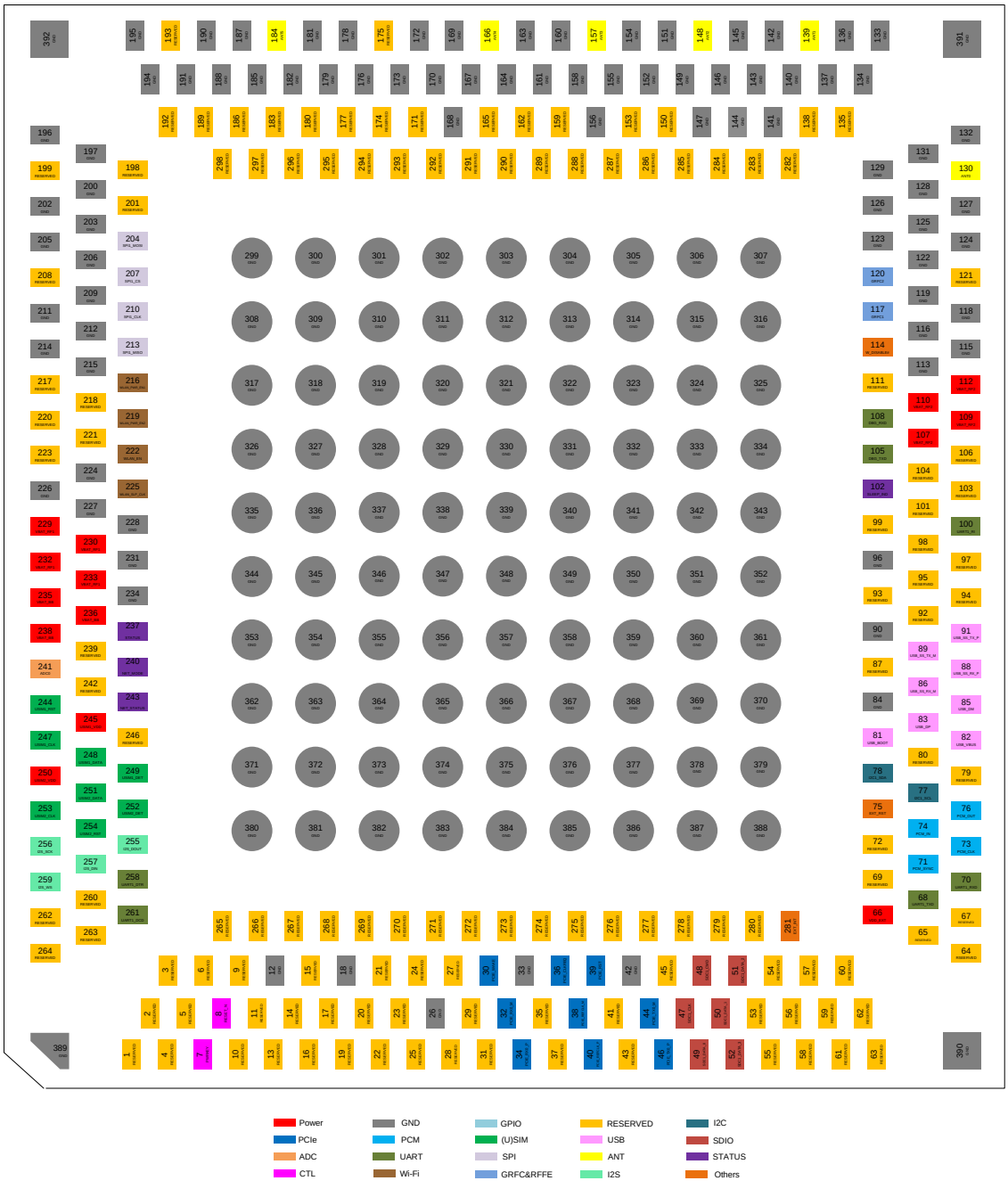


Figure 9: RG500U-LA Pin Assignment (Top View)

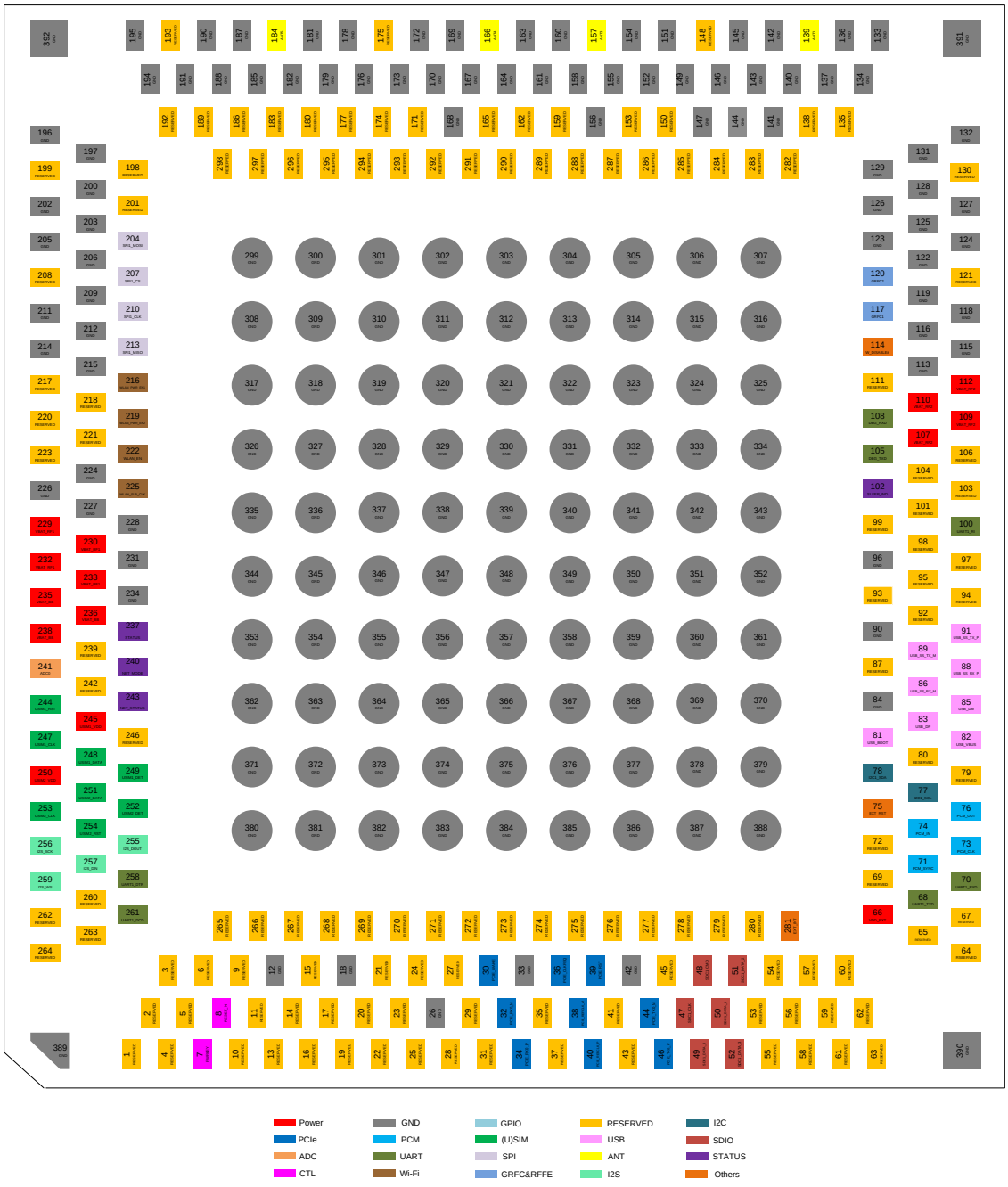


Figure 10: RG500U-JO Pin Assignment (Top View)

NOTE

1. Keep all RESERVED or unused pins unconnected.
2. All GND pins should be connected to ground.
3. Ensure that the pull-up power supply of the module's pins is VDD_EXT or controlled by VDD_EXT, and there is no current sink on the module's pins before the module turns on. For more details, contact Quectel Technical Support.

3.2. Pin Definition

The following tables show the pin definition and description of RG500U series.

Table 8: Parameter Definition

Parameter	Description
AI	Analog Input
AO	Analog Output
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

DC characteristics include power domain and rated current.

Table 9: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	235, 236, 238	PI	Power supply for the module's baseband part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF1	229, 230, 232, 233	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	
VBAT_RF2	107, 109, 110,	PI	Power supply for the module's RF part	Vmax = 4.3 V Vmin = 3.3 V Vnom = 3.8 V	VBAT_RF2 is only used to connect decoupling capacitors and there is

	112				no need to connect it to the external power supply.
VDD_EXT	66	PO	Provides 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	Used for external pull-up circuits. All external signals connected to the module that require 1.8 V pull-up must be pulled up to VDD_EXT. A test point is recommended to be reserved.
GND	12, 18, 26, 33, 42, 84, 90, 96, 113, 115, 116, 118, 119, 122–129, 131–134, 136, 137, 140–147, 149, 151, 152, 154–156, 158, 160, 161, 163, 164, 167–170, 172, 173, 176, 178, 179, 181, 182, 185, 187, 188, 190, 191, 194–197, 200, 202, 203, 205, 206, 209, 211, 212, 214, 215, 224, 226, 227, 228, 231, 234, 299–392				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	7	DI	Turns on/off the module		Active low/ Low-level pulses are active. Internally pulled up to VBAT with a 20 kΩ resistor.
RESET_N	8	DI	Resets the module		Active Low/Low-level pulses are active. Internally pulled up to VBAT with a 20 kΩ resistor. A test point is recommended to be reserved if unused.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
STATUS	237	DO	Indicates the module's operation status	1.8 V	1.8 V power domain. If unused, keep them open.
NET_MODE	240	DO	Indicates the module's network		

			registration mode		
NET_STATUS	243	DO	Indicates the module's network activity status		
SLEEP_IND	102	DO	Indicates the module's sleep mode		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	82	AI	USB connection detect	Vmax = 5.25 V Vmin = 3.4 V Vnom = 5.0 V	For USB connection detection only, not for power supply. A test point must be reserved.
USB_DP	83	AIO	USB 2.0 differential data (+)		Requires differential impedance of 90 Ω. USB 2.0 compliant. Test points must be reserved.
USB_DM	85	AIO	USB 2.0 differential data (-)		
USB_SS_TX_P	91	AO	USB 3.0 super-speed transmit (+)		Requires differential impedance of 90 Ω. If unused, keep them open. USB 3.0 compliant.
USB_SS_TX_M	89	AO	USB 3.0 super-speed transmit (-)		
USB_SS_RX_P	88	AI	USB 3.0 super-speed receive (+)		
USB_SS_RX_M	86	AI	USB 3.0 super-speed receive (-)		
(U)SIM Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM1_VDD	245	PO	(U)SIM1 card power supply	1.8/3.0 V	
USIM1_DATA	248	DIO	(U)SIM1 card data	USIM1_VDD 1.8/3.0	
USIM1_CLK	247	DO	(U)SIM1 card clock		

USIM1_RST	244	DO	(U)SIM1 card reset		
USIM1_DET	249	DI	(U)SIM1 card hot-plug detect	1.8 V	If unused, keep it open.
USIM2_VDD	250	PO	(U)SIM2 card power supply	USIM2_VDD 1.8/3.0 V	
USIM2_DATA	251	DIO	(U)SIM2 card data		
USIM2_CLK	253	DO	(U)SIM2 card clock		
USIM2_RST	254	DO	(U)SIM2 card reset		
USIM2_DET	252	DI	(U)SIM2 card hot-plug detect	1.8 V	If unused, keep it open.
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
UART1_TXD	68	DO	Main UART transmit	1.8 V	If unused, keep them open.
UART1_RXD	70	DI	Main UART receive		
UART1_DTR	258	DI	Main UART data terminal ready, sleep mode control		
UART1_RI*	100	DO	Main UART ring indication		
UART1_DCD*	261	DO	Main UART data carrier detect		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	108	DI	Debug UART receive	1.8 V	Test points must be reserved.
DBG_TXD	105	DO	Debug UART transmit		
I2C Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2C1_SCL	77	OD	I2C serial clock	1.8 V	Require an external pull-up to VDD_EXT. If unused, keep them open.
I2C1_SDA	78	OD	I2C serial data		

I2S Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
I2S_WS	259	DO	I2S word select	1.8 V	I2S supports master mode only by default. Can be multiplexed into PCM_SYNC.
I2S_SCK	256	DO	I2S clock		I2S supports master mode only by default. Can be multiplexed into PCM_CLK.
I2S_DIN	257	DI	I2S data in		I2S supports master mode only by default. Can be multiplexed into PCM_IN.
I2S_DOUT	255	DO	I2S data out		I2S supports master mode only by default. Can be multiplexed into PCM_OUT.
PCM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCM_SYNC	71	DO	PCM data frame sync	1.8 V	Can be multiplexed into I2S_WS.
PCM_CLK	73	DO	PCM clock		Can be multiplexed into I2S_SCK.
PCM_IN	74	DI	PCM data input		Can be multiplexed into I2S_DIN.
PCM_OUT	76	DO	PCM data output		Can be multiplexed into I2S_DOUT.
PCIe Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)		Requires differential impedance of 100 Ω. *PCI Express Base Specification Revision 2.1* compliant. Supports PCIe Gen 2. In RC mode, it is an output signal.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)		

					In EP mode, it is an input signal.
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)		Requires differential impedance of 100 Ω. *PCI Express Base Specification Revision 2.1* compliant. Supports PCIe Gen 2.
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)		
PCIE_RX0_M	32	AI	PCIe receive 0 (-)		
PCIE_RX0_P	34	AI	PCIe receive 0 (+)		
PCIE_CLKREQ	36	DI, OD	PCIe clock request	1.8 V	In RC mode, it is an input signal. In EP mode, it is an output signal.
PCIE_RST	39	DIO	PCIe reset		In RC mode, it is an output signal. In EP mode, it is an input signal.
PCIE_WAKE	30	DI, OD	PCIe wake up		In RC mode, it is an input signal. In EP mode, it is an output signal.
WLAN Application Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
WLAN_PWR_EN1	216	DO	Controls WLAN PA power	1.8 V	
WLAN_PWR_EN2	219	DO	Controls WLAN other power		
WLAN_EN	222	DO	WLAN enable		
WLAN_SLP_CLK	225	AO	32.768 kHz sleep clock output		
SDIO Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SDC1_CLK	47	DO	SDIO clock	1.8 V	
SDC1_CMD	48	DIO	SDIO command		
SDC1_DATA_0	49	DIO	SDIO data bit 0		
SDC1_DATA_	50	DIO	SDIO data bit 1		

1			
SDC1_DATA_2	51	DIO	SDIO data bit 2
SDC1_DATA_3	52	DIO	SDIO data bit 3

RG500U-CN Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX - LTE: LMHB TRX - 5G NR: n1/n28 TRX & n41 TRX1 & n77/n78/n79 DRX1 - Reframing: n1/n28 TRX	50 Ω characteristic impedance.
ANT1	157	AIO	**Antenna 1 interface:** - WCDMA: LMB DRX - LTE: LMHB DRX - 5G NR: n1 DRX0 & n28 DRX & n77/n78/n79 TRX1 & n41 DRX1 - Reframing: n1 DRX0 & n28 DRX	
ANT2	166	AIO	**Antenna 2 interface:** - 5G NR: n41/n77/n78/n79 DRX0 & n1 DRX1	
ANT3	184	AIO	**Antenna 3 interface:** - 5G NR: n41/n77/n78/n79 TRX0 & n1 PRX1	

RG500U-EA Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX - LTE: LMB & B40 TRX - 5G NR: n1/n3/n66 PRX1 & n5/n8/n20/n28 TRX & n40 TRX1 - Reframing: n1/n3/n66 PRX1 & n5/n8/n20/n28 TRX & n40 TRX1	50 Ω characteristic impedance.
ANT1	139	AIO	**Antenna 1 interface:** - LTE: B7/B38/B41 TRX - 5G NR: n7 PRX1 & n38/n41 TRX1 & n77/n78 DRX0 - Reframing: n38 TRX1 & n7 PRX1	

ANT2	148	AIO	**Antenna 2 interface:** - WCDMA: LMB DRX - LTE: LMB & B40 DRX - 5G NR: n1/n3/n40/n66 DRX1 & n5/n8/n20/n28 DRX - Refarming: n1/n3/n40/n66 DRX1 & n5/n8/n20/n28 DRX	
ANT3	157	AIO	**Antenna 3 interface:** - LTE: B7/B38/B41 DRX - 5G NR: n7/n38/n41 DRX1 & n77/n78 TX1 & PRX1 - Refarming: n7/n38 DRX1	
ANT4	166	AIO	**Antenna 4 interface:** - 5G NR: LMHB DRX0 & n77/n78 DRX1	
ANT5	184	AIO	**Antenna 5 interface:** - 5G NR: LMHB & n77/n78 TRX0	

RG500U-EB Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX - LTE: LMHB TRX - 5G NR: n1/n3/n7/n28/n66 PRX1 & n5/n8 TRX & n38/n40/n41 TRX1 & n77/n78 DRX0 - Refarming: n1/n3/n7/n28/n66 PRX1 & n5/n8 TRX & n38/n40 TRX1	50 Ω characteristic impedance.
ANT2	148	AIO	**Antenna 2 interface:** - WCDMA: LMB DRX - LTE: LMHB DRX - 5G NR: n1/n3/n7/n28/n38/n40/n41/n66 DRX1 & n5/n8/n20 DRX & n77/n78 TX1 & PRX1 − Refarming: n1/n3/n7/n28/n38/n40/n66 DRX1 & n5/n8/n20 DRX	50 Ω characteristic impedance.
ANT4	166	AIO	**Antenna 4 interface:** - 5G NR: LMHB DRX0 & n77/n78 DRX1	50 Ω characteristic impedance.
ANT5	184	AIO	**Antenna 5 interface:** - 5G NR: LMHB & n77/n78 TRX0	50 Ω characteristic impedance.

RG500U-LA Antenna Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX LTE: LMB & B40 TRX - 5G NR: n2/n28/n66 PRX1 & n8/n71 TRX & n40 TRX1 - Refarming: n2/n28/n66 PRX1 & n8/n71 TRX & n40 TRX1	50 Ω characteristic impedance.
ANT1	139	AIO	**Antenna 1 interface:** - LTE: B7/B38 TRX - 5G NR: n7 PRX1 & n38 TRX1 & n78 DRX0 - Refarming: n38 TRX1 & n7 PRX1	
ANT2	148	AIO	**Antenna 2 interface:** - WCDMA: LMB DRX - LTE: LMB & B40 DRX - 5G NR: n2/n28/n66/n40 DRX1 & n5/n8 DRX - Refarming: n2/n28/n66/n40 DRX1 & n5/n8 DRX	
ANT3	157	AIO	**Antenna 3 interface:** - LTE: B7/B38 DRX - 5G NR: n7/n38 DRX1 & n78 TX1 & PRX1 - Refarming: n7/n38 DRX1	
ANT4	166	AIO	**Antenna 4 interface:** - 5G NR: LMHB DRX0 & n78 DRX1	
ANT5	184	AIO	**Antenna 5 interface:** - 5G NR: LMHB & n78 TRX0	

RG500U-JO Antenna Interfaces				
Pin Name	**Pin No.**	**I/O**	**Description**	**Comment**
ANT0	130	AIO	Reserved	
ANT1	139	AIO	**Antenna 1 interface:** - 5G NR: n78 DRX0	50 Ω characteristic impedance.
ANT2	148	AIO	Reserved	
ANT3	157	AIO	**Antenna 3 interface:** - 5G NR: n78 TX1 & PRX1	50 Ω characteristic impedance.

ANT4	166	AIO	**Antenna 4 interface:** - 5G NR: n78 DRX1	50 Ω characteristic impedance.
ANT5	184	AIO	**Antenna 5 interface:** - 5G NR: n78 TRX0	50 Ω characteristic impedance.

RG500U-CN Antenna Tuner Control Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	117	DO	Generic RF Controller	1.8 V	
GRFC2	120	DO	Generic RF Controller		

RG500U-EA/EB/LA/JO Antenna Tuner Control Interfaces*					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	117	DO	Generic RF Controller	1.8 V	
GRFC2	120	DO	Generic RF Controller		

SPI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
SPI1_CLK	210	DO	SPI clock	1.8 V	Only master mode is supported by default.
SPI1_CS	207	DO	SPI chip select		
SPI1_MISO	213	DI	SPI master-in slave-out		
SPI1_MOSI	204	DO	SPI master-out slave-in		

ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	241	AI	General-purpose ADC interface	0–VBAT	

Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_BOOT	81	DI	Forces the module into download mode	1.8 V	Test points are recommended to be reserved.

W_DISABLE#	114	DI	Airplane mode control
EXT_RST	75	DO	External audio reset
EXT_INT	281	DI	External audio interrupt

RG500U-CN RESERVED Pins	
Pin Name	**Pin No.**
RESERVED	1–6, 9–11, 13–17, 19–25, 27–29, 31, 35, 37, 41, 43, 45, 53–65, 67, 69, 72, 79, 80, 87, 92–95, 97–99, 101, 103, 104, 106, 111, 121, 135, 138, 139, 148, 150, 153, 159, 162, 165, 171, 174, 175, 177, 180, 183, 186, 189, 192, 193, 198, 199, 201, 208, 217, 218, 220, 221, 223, 239, 242, 246, 260, 262–280, 282–298

RG500U-EA/LA RESERVED Pins	
Pin Name	**Pin No.**
RESERVED	1–6, 9–11, 13–17, 19–25, 27–29, 31, 35, 37, 41, 43, 45, 53–65, 67, 69, 72, 79, 80, 87, 92–95, 97–99, 101, 103, 104, 106, 111, 121, 135, 138, 150, 153, 159, 162, 165, 171, 174, 175, 177, 180, 183, 186, 189, 192, 193, 198, 199, 201, 208, 217, 218, 220, 221, 223, 239, 242, 246, 260, 262–280, 282–298

RG500U-EB RESERVED Pins	
Pin Name	**Pin No.**
RESERVED	1–6, 9–11, 13–17, 19–25, 27–29, 31, 35, 37, 41, 43, 45, 53–65, 67, 69, 72, 79, 80, 87, 92–95, 97–99, 101, 103, 104, 106, 111, 121, 135, 138, 139, 150, 153, 157, 159, 162, 165, 171, 174, 175, 177, 180, 183, 186, 189, 192, 193, 198, 199, 201, 208, 217, 218, 220, 221, 223, 239, 242, 246, 260, 262–280, 282–298

RG500U-JO RESERVED Pins	
Pin Name	**Pin No.**
RESERVED	1–6, 9–11, 13–17, 19–25, 27–29, 31, 35, 37, 41, 43, 45, 53–65, 67, 69, 72, 79, 80, 87, 92–95, 97–99, 101, 103, 104, 106, 111, 121, 130, 135, 138, 148, 150, 153, 159, 162, 165, 171, 174, 175, 177, 180, 183, 186, 189, 192, 193, 198, 199, 201, 208, 217, 218, 220, 221, 223, 239, 242, 246, 260, 262–280, 282–298

3.3. Operating Modes

Table 10: Overview of Operating Modes

Mode	Details	
Full Functionality Mode	Idle	Software is active. The module has registered on the network, and it is ready to send and receive data.
	Voice/Data	Network connection is ongoing. In this mode, the power consumption is decided by network setting and data transfer rate.
Minimum Functionality Mode	**AT+CFUN=0** can set the module to a minimum functionality mode without removing the power supply. In this case, both RF function and (U)SIM card are invalid.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode. In this case, RF function is invalid.	
Sleep Mode	In this mode, the power consumption of the module is reduced to the minimal level. During this mode, the module can still receive paging message, SMS, voice call and TCP/UDP data from the network normally.	
Power Down Mode	In this mode, the power management unit shuts down the power supply. Software is not active. The serial interfaces are not accessible. Operating voltage (connected to VBAT_RF and VBAT_BB) remains applied.	

3.4. Power Saving

3.4.1. Sleep Mode

The module is able to reduce the power consumption to an ultra-low level during sleep mode. The following section describes power saving procedures.

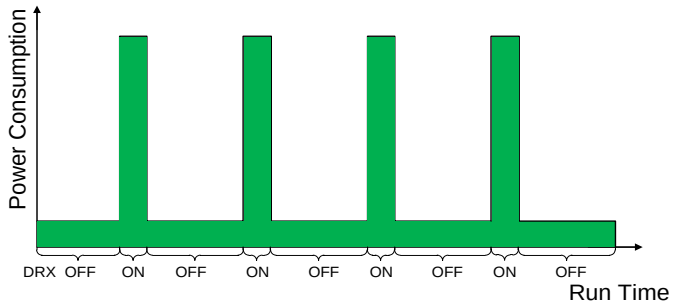


Figure 11: DRX Run Time and Power Consumption in Sleep Mode

NOTE

DRX cycle values are transmitted over the wireless network.

3.4.1.1.UART Application

If the MCU communicates with the module via main UART interface, the following preconditions can make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Drive UART1_DTR high.

The following figure shows the connection between the module and the MCU.

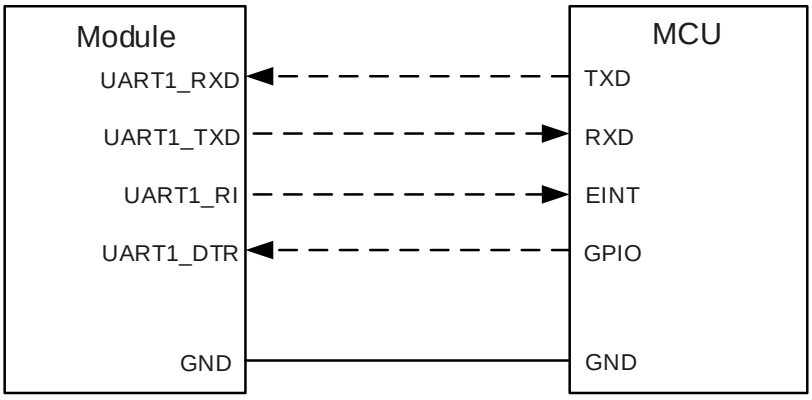


Figure 12: Sleep Mode Application via UART

You can wake up the module by driving UART1_DTR low.

NOTE

1. Pay attention to the level match shown in dotted line between the module and the MCU.
2. When the module has a URC to report, UART1_RI signal wakes up the MCU. See ***Chapter 3.14*** for details about UART1_RI behaviors.

3.4.1.2.USB Application without USB Suspend Function

The module does not support USB suspend function. Please disconnect USB_VBUS with an external control circuit to make the module enter sleep mode.

- Execute **AT+QSCLK=1** to enable sleep mode.
- Ensure UART1_DTR is held at high level or keep it open.
- Disconnect USB_VBUS.

The following figure shows the connection between the module and the host.

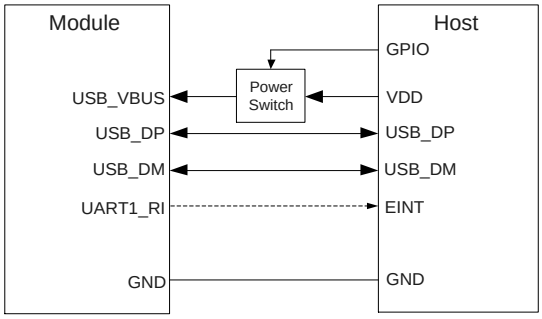


Figure 13: Sleep Mode Application without Suspend Function

You can wake up the module by switching on the power switch to supply power to USB_VBUS.

NOTE

Pay attention to the level match shown in dotted line between the module and the host.

3.4.2. Airplane Mode

When the module enters airplane mode, the RF function does not work and all AT commands related to the RF function are inaccessible. You can set this mode via the following ways.

Hardware:

The W_DISABLE# pin is pulled up by default. Driving it low makes the module enter airplane mode.

Software:

AT+CFUN=<fun> provides the choice of functionality level by setting **<fun>** into 0, 1 or 4.

- **AT+CFUN=0**: Minimum functionality mode. Both (U)SIM and RF functions are disabled.
- **AT+CFUN=1**: Full functionality mode (by default).

- **AT+CFUN=4**: Airplane mode. RF function is disabled.

3.5. Power Supply

3.5.1. Power Supply Pins

RG500U series provides 7 VBAT pins dedicated for connection with the external power supply. There are two separate voltage domains for VBAT.

- Four VBAT_RF1 pins for module's RF part.
- Three VBAT_BB pins for module's baseband part.

Table 11: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_RF1	229, 230, 232, 233	Power supply for the module's RF part	3.3	3.8	4.3	V
VBAT_BB	235, 236, 238	Power supply for the module's baseband part	3.3	3.8	4.3	V
GND	12, 18, 26, 33, 42, 84, 90, 96, 113, 115, 116, 118, 119, 122–129, 131–134, 136, 137, 140–147, 149, 151, 152, 154–156, 158, 160, 161, 163, 164, 167–170, 172, 173, 176, 178, 179, 181, 182, 185, 187, 188, 190, 191, 194–197, 200, 202, 203, 205, 206, 209, 211, 212, 214, 215, 224, 226–228, 231, 234, 299–392					

3.5.2. Voltage Stability Requirements

The power supply range of the module is from 3.3 V to 4.3 V. Make sure the input voltage never drops below 3.3 V. The following figure shows the voltage drop during burst transmission.

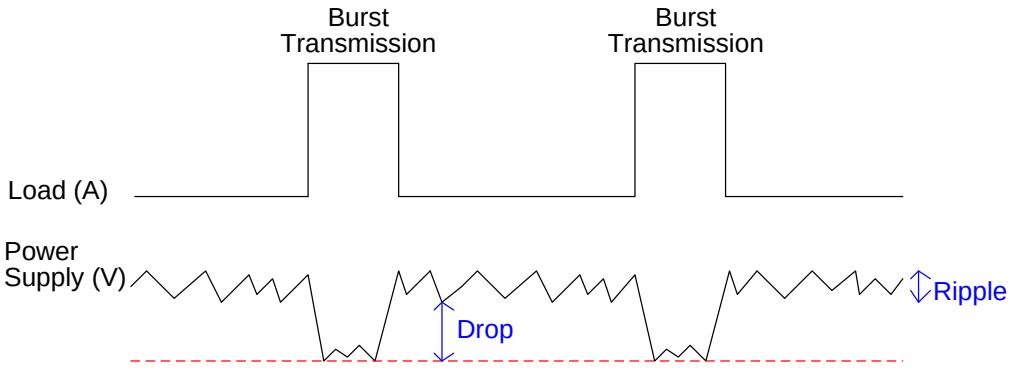


Figure 14: Power Supply Limits during Burst Transmission

To decrease the voltage drop, use a bypass capacitor of about 220 μF with low ESR (ESR ≤ 0.7 Ω). Meanwhile, it is recommended to reserve a multi-layer ceramic chip (MLCC) capacitor array composed of three ceramic capacitors (100 nF, 33 pF, 10 pF) for VBAT_BB and VBAT_RF respectively, and place these capacitors close to VBAT pins. The main power supply from an external application has to be a single voltage source and can be expanded to two sub paths with star structure. The width of VBAT_BB trace should be not less than 2.0 mm, and the width of VBAT_RF1 and VBAT_RF2 trace should be not less than 2.5 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to avoid the surge, use a TVS diode of which the reverse working voltage should be 5.1 V. The following figure shows the star structure of the power supply.

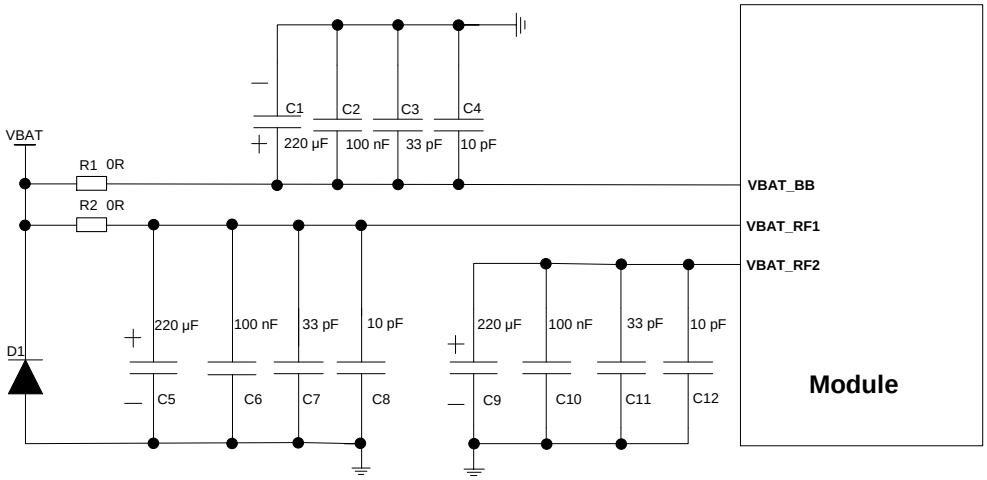


Figure 15: Reference Circuit of Power Supply

3.5.3. Reference Design for Power Supply

The power source is critical to the module's performance. The continuous current of the power supply should be 3 A at least and the peak current should be 4 A at least.

The following figure shows a reference design for +5 V input power source.

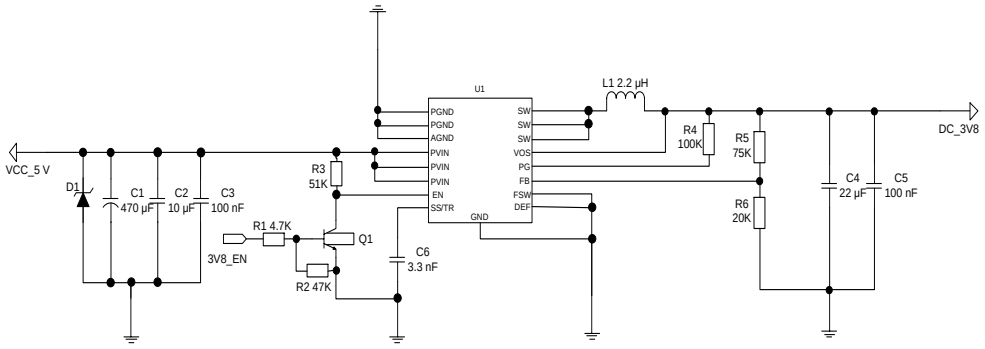


Figure 16: Reference Circuit of Power Supply

NOTE

To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after shutting down the module with PWRKEY or AT command can you cut off the power supply.

3.6. Turn On/Turn Off/Reset

3.6.1. Turn On with PWRKEY

Table 12: Pin Description of PWRKEY

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	7	DI	Turns on/off the module	Active low/Low-level pulses are active. Internally pulled up to VBAT with a 20 kΩ resistor.

The module can be turned on by driving the PWRKEY pin low for at least 1.2 s. It is recommended to use an open drain/collector driver to control the PWRKEY.

A simple reference circuit is illustrated in the following figure.

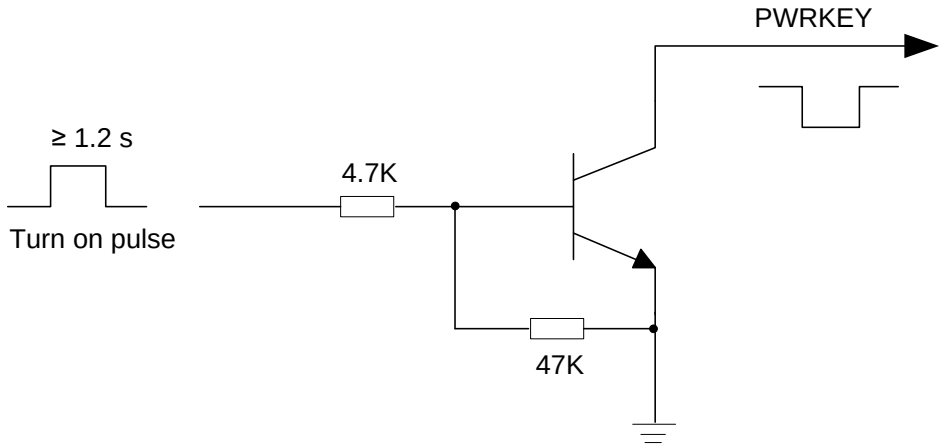


Figure 17: Turning on the Module Using Driving Circuit

Another way to control the PWRKEY is using a button directly. When you are pressing the key, electrostatic strike may be generated from finger. Therefore, you must place a TVS component nearby the button for ESD protection. A reference circuit is shown in the following figure.

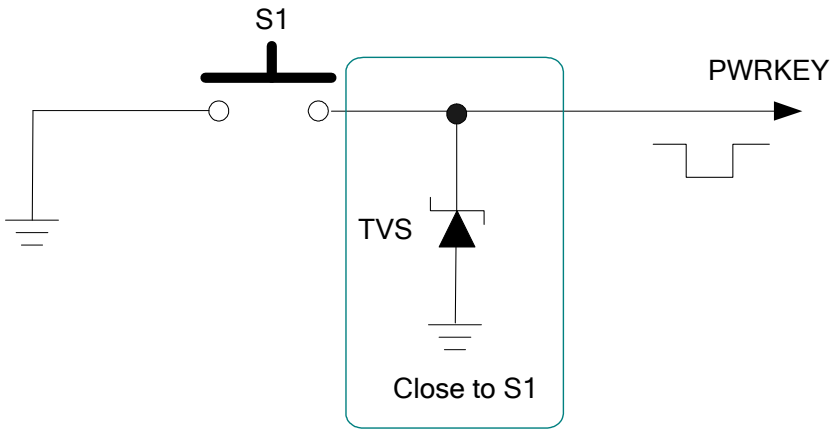


Figure 18: Turning on the Module Using a Button

The turn-on timing is illustrated in the following figure.

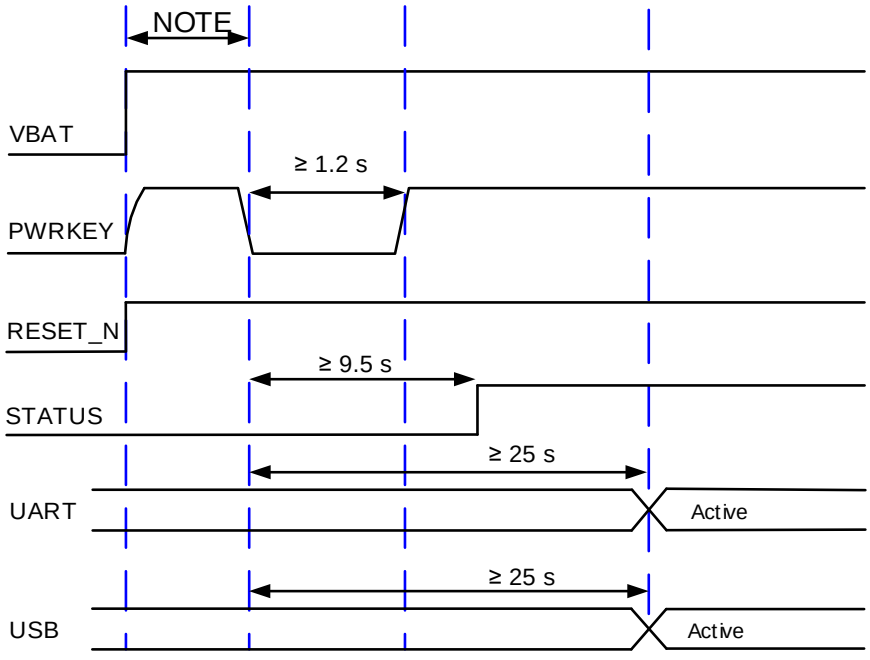


Figure 19: Power-up Timing

NOTE

1. Make sure that VBAT is stable before pulling down PWRKEY pin. It is recommended that the time difference between powering up VBAT and pulling down PWRKEY pin should not be less than 30 ms.
2. A 20K resistor is integrated internally in PWRKEY and is pulled up to VBAT_BB.
3. If the module needs to turn on automatically but does not require turn-off function, PWRKEY can be

driven low directly to ground with a 1K resistor.

3.6.2. Turn Off

The module can be turned off by following ways:

- Use the PWRKEY pin.
- Use **AT+QPOWD**.

3.6.2.1.Turn Off with PWRKEY

Drive the PWRKEY pin low for at least 800 ms and then release PWRKEY. After this, the module executes power-down procedure.

The turn-off timing is illustrated in the following figure.

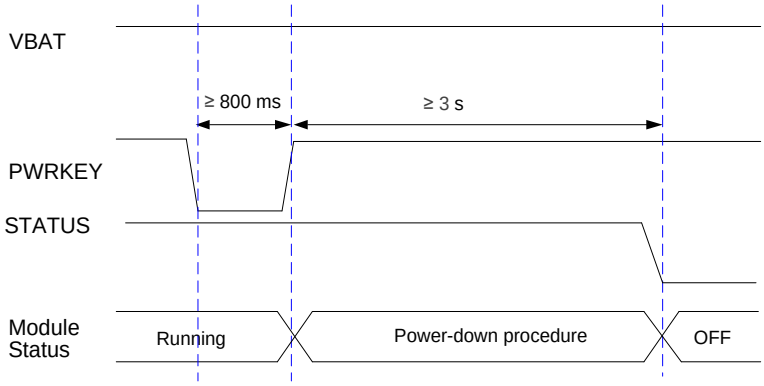


Figure 20: Power-down Timing

3.6.2.2.Turn Off with AT Command

It is also a safe way to use **AT+QPOWD** to turn off the module, which is similar to turning off the module via the PWRKEY pin.

See ***document [3]*** for details about **AT+QPOWD**.

NOTE

1. To avoid corrupting the data in the internal flash, do not switch off the power supply when the module works normally. Only after turning off the module with PWRKEY or AT command can you cut off the power supply.
2. When turning off module with the AT command, keep PWRKEY at high level after execution of the command. Otherwise, the module will be turned on again after successful turn-off.

3.6.3. Reset

You can reset the module by driving RESET_N low for 40–600 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 13: Pin Description of RESET_N

Pin Name	Pin No.	I/O	Description	Comment
RESET_N	8	DI	Resets the module	Active Low/Low-level pulses are active. Internally pulled up to VBAT with a 20 kΩ resistor. A test point is recommended to be reserved if unused.

The recommended circuit is similar to the PWRKEY control circuit. You can use an open drain/collector driver or button to control RESET_N.

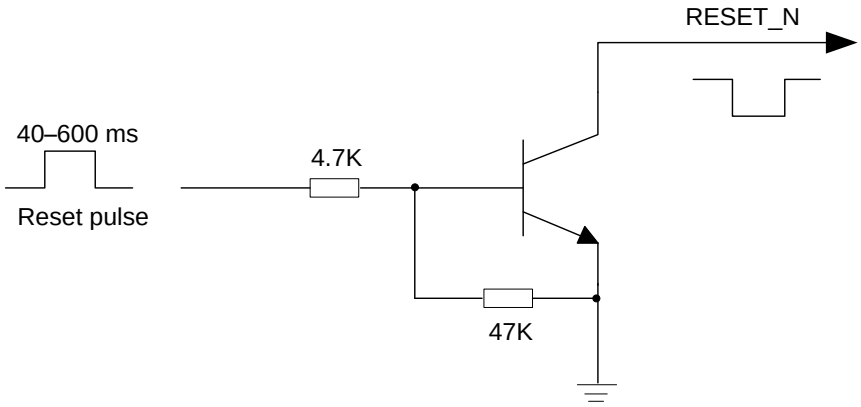


Figure 21: Reference Circuit of RESET_N by Using Driving Circuit

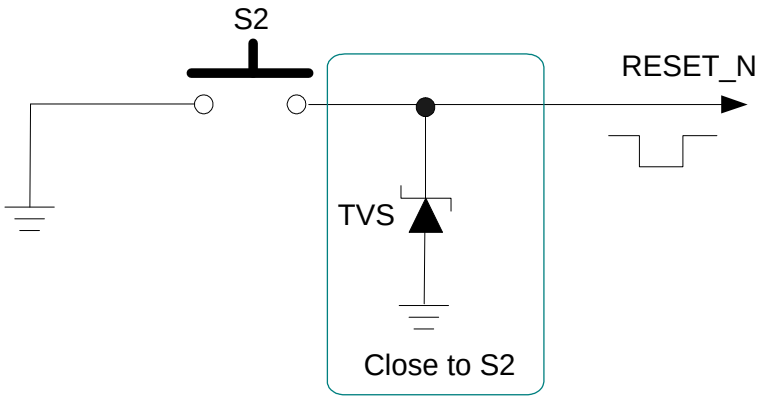


Figure 22: Reference Circuit of RESET_N with a Button

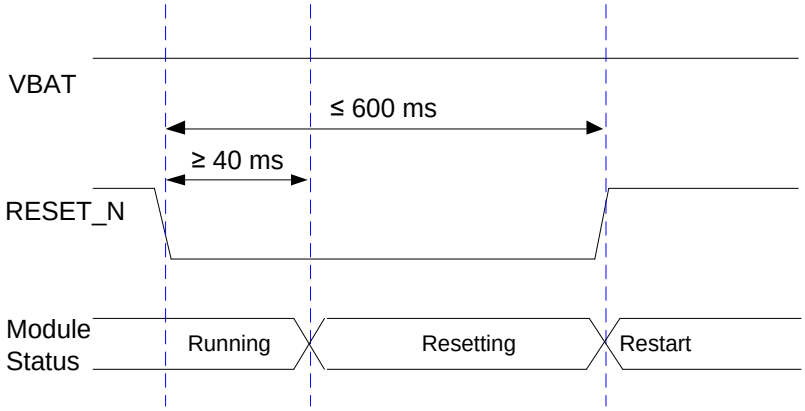


Figure 23: Timing of Resetting the Module

NOTE

1. Use RESET_N only when you fail to turn off the module with the **AT+QPOWD** and PWRKEY.
2. RESET_N is internally pulled up with a 20 kΩ resistor.
3. Ensure that there is no large capacitance on PWRKEY and RESET_N.

3.7. (U)SIM Interfaces

The (U)SIM interfaces circuitry meets ETSI and IMT-2000 requirements. Either 1.8 V or 3.0 V (U)SIM card is supported.

Table 14: Pin Description of (U)SIM Interfaces

Pin Name	Pin No.	I/O	Description	Comment
USIM1_VDD	245	PO	(U)SIM1 card power supply	
USIM1_DATA	248	DIO	(U)SIM1 card data	
USIM1_CLK	247	DO	(U)SIM1 card clock	
USIM1_RST	244	DO	(U)SIM1 card reset	
USIM1_DET	249	DI	(U)SIM1 card hot-plug detect	1.8 V power domain. If unused, keep it open.
USIM2_VDD	250	PO	(U)SIM2 card power supply	
USIM2_DATA	251	DIO	(U)SIM2 card data	
USIM2_CLK	253	DO	(U)SIM2 card clock	
USIM2_RST	254	DO	(U)SIM2 card reset	
USIM2_DET	252	DI	(U)SIM2 card hot-plug detect	1.8 V power domain. If unused, keep it open.

The module supports (U)SIM card hot-plug via the USIM1_DET and USIM2_DET, and both high and low level detections are supported. The function is disabled by default and you can configure it via **AT+QSIMDET**. See ***document [3]*** for more details about the command.

The following figure shows a reference design for (U)SIM interface with an 8-pin (U)SIM card connector.

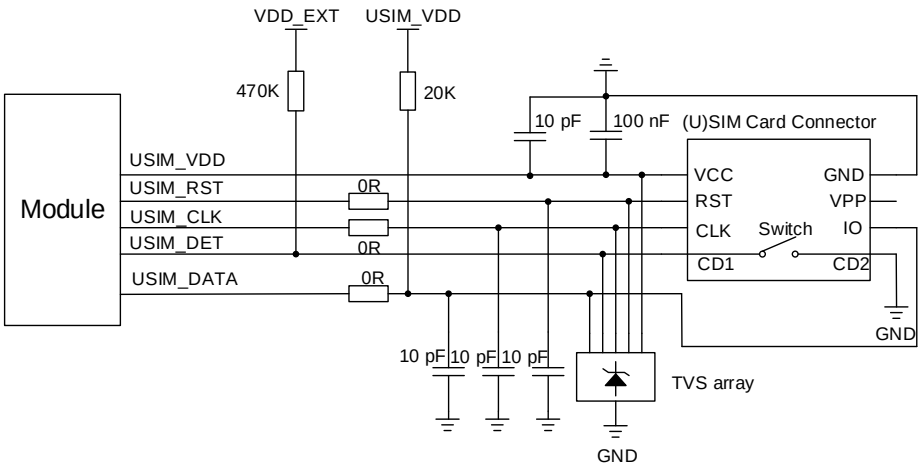


Figure 24: Reference Circuit of (U)SIM Interface with an 8-pin (U)SIM Card Connector

If the function of (U)SIM card hot-plug is not needed, keep USIM1_DET and USIM2_DET disconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

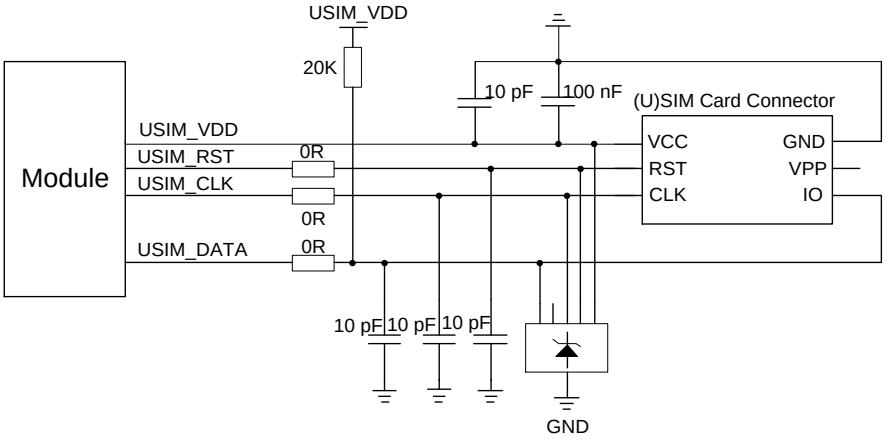


Figure 25: Reference Circuit of (U)SIM Interface with a 6-pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Place the (U)SIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.
- Make sure the ground between the module and the (U)SIM card connector is short and wide. Keep the trace width of ground and USIM_VDD not less than 0.5 mm to maintain the same electric potential.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them with surrounded ground.
- To offer good ESD protection, add a TVS array of which the junction capacitance should be less than 26 pF. Add 0 Ω resistors in series between the module and the (U)SIM card to facilitate debugging. Additionally, keep the (U)SIM peripheral circuit close to the (U)SIM card connector.
- For USIM_DATA, a 20 kΩ pull-up resistor must be added near the (U)SIM card connector.

3.8. USB Interface

RG500U series provides one integrated Universal Serial Bus (USB) interface which complies with the USB 3.0/2.0 specifications and supports SuperSpeed, high-speed, full-speed and low-speed modes. The USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade.

Table 15: Pin Description of USB Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	82	AI	USB connection detect	For USB connection detection only, not for power supply. A test point must be reserved.
USB_DP	83	AIO	USB differential data (+)	USB 2.0 compliant. Requires differential impedance of 90 Ω. Test points must be reserved.
USB_DM	85	AIO	USB differential data (-)	
USB_SS_TX_P	91	AO	USB 3.0 super-speed transmit (+)	USB 3.0 compliant. Requires differential impedance of 90 Ω.
USB_SS_TX_M	89	AO	USB 3.0 super-speed transmit (-)	
USB_SS_RX_P	88	AI	USB 3.0 super-speed receive (+)	
USB_SS_RX_M	86	AI	USB 3.0 super-speed receive (-)	

For more details about the USB 2.0/3.0 specifications, visit http://www.usb.org/home.

Test points must be reserved for USB 2.0 interface for debugging and firmware upgrading in your design. The following figure shows a reference circuit of USB interface.

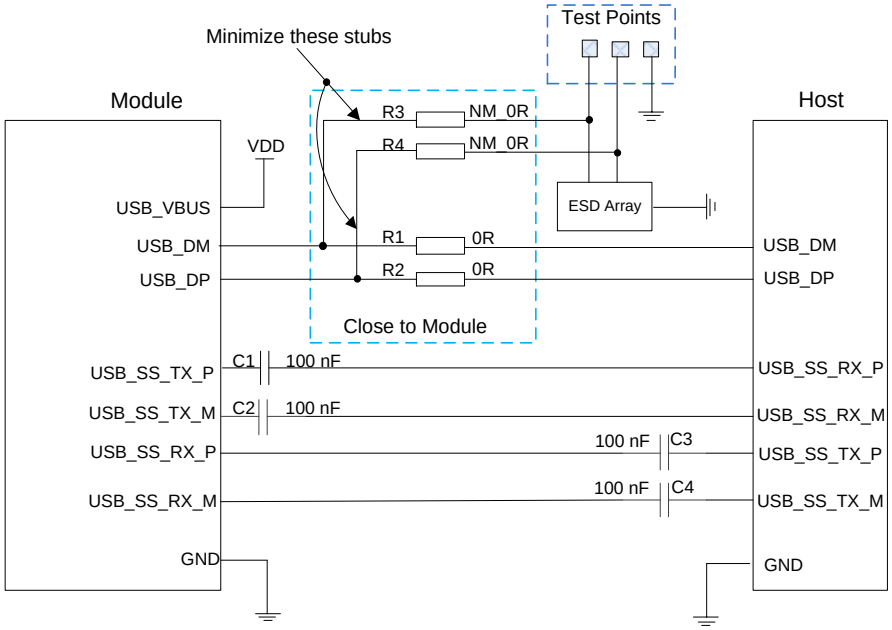


Figure 26: Reference Circuit of USB Application

To ensure the signal integrity of USB data lines, place R1, R2, R3, R4, C1 and C2 close to the module, C3 and C4 close to the host, and keep the resistors close to each other.

When designing the USB interface, you should follow the following principles to meet USB 2.0 & USB 3.0 specifications.

- Route the USB signal traces as differential pairs with ground surrounded. The impedance of USB differential trace is 90 Ω.
- For USB 2.0 signal traces, the trace length should be less than 250 mm, and the differential data pair matching should be less than 2 mm. For USB 3.0 signal traces, length matching of each differential data pair (Tx/Rx) should be less than 0.15 mm.
- Do not route signal traces under crystals, oscillators, magnetic devices, PCIe and RF signal traces. Route the USB differential traces at inner-layer of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection components might cause influences on USB data lines, so you should pay attention to the selection of the components. Typically, the stray capacitance should be less than 1.0 pF for USB 2.0, and less than 0.4 pF for USB 3.0.
- Keep the ESD protection components as close to the USB connector as possible.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM lines respectively.

3.9. UART Interfaces

The module provides two UART interfaces: one main UART interface and one debug UART interface.

- Main UART interface supports 115200 bps baud rate by default. This interface is used for data transmission and AT command communication.
- Debug UART interface supports 115200 bps baud rate. It is used for log output.

Table 16: Pin Description of Main UART Interface

Pin Name	Pin No.	I/O	Description	Comment
UART1_TXD	68	DO	Main UART transmit	1.8 V power domain. If unused, keep them open.
UART1_RXD	70	DI	Main UART receive	
UART1_DTR	258	DI	Main UART data terminal ready, sleep mode control	
UART1_RI	100	DO	Main UART ring indication	
UART1_DCD	261	DO	Main UART data carrier detection	

Table 17: Pin Description of Debug UART Interface

Pin Name	Pin No.	I/O	Description	Comment
DBG_RXD	108	DI	Debug UART receive	1.8 V power domain. Test points must be reserved.
DBG_TXD	105	DO	Debug UART transmit	

The module provides 1.8 V UART interfaces. Use a voltage-level translator if the application is equipped with a 3.3 V UART interface. A voltage-level translator TXS0108EPWR provided by Texas Instruments is recommended.

The following figure shows a reference design.

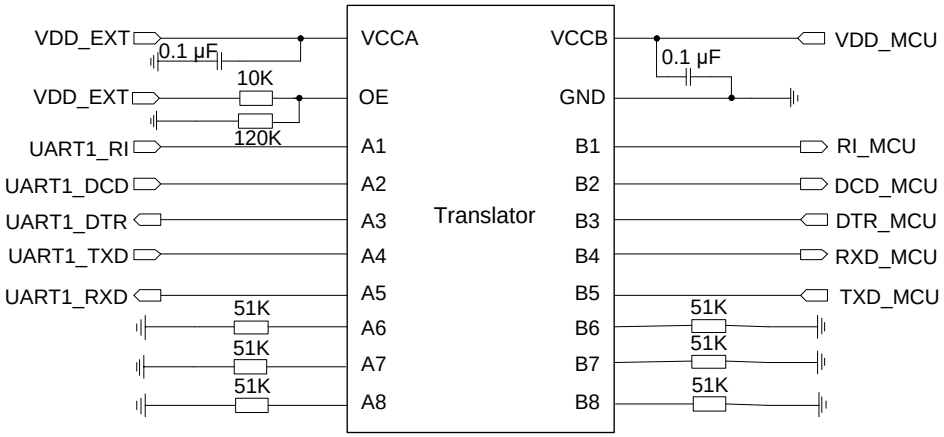


Figure 27: Reference Circuit with Voltage-level Translator Chip (Main UART)

Visit http://www.ti.com for more information.

Another example with transistor circuit is shown as below. For the design of circuits shown in dotted lines, see that shown in solid lines, but pay attention to the direction of connection.

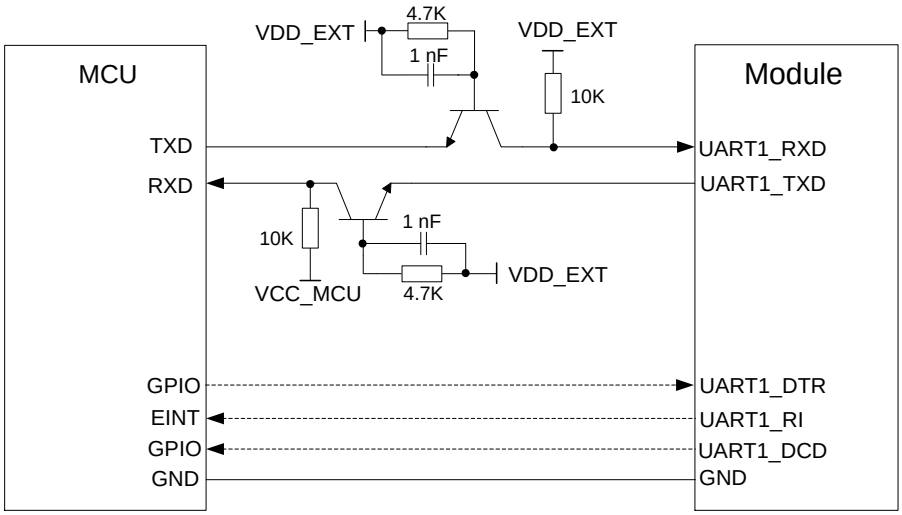


Figure 28: Reference Circuit with Transistor Circuit (Main UART)

NOTE

1. For all signals connected to the module with level-shift circuit required, the power supply for their reference voltage is required to be controlled by VDD_EXT, that is, be turned on later than VDD_EXT.
2. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
3. The level-shifting circuits (***Figure 27*** and ***Figure 28***) take the main UART as an example. The circuits of the debug UART is connected in the same way as the main UART.

3.10. I2S Interface and SPI

RG500U series supports audio communication via one I2S digital interface and one SPI. And the I2S interface can be multiplexed into PCM function.

Table 18: Pin Description of I2S Interface and SPI

Pin Name	Pin No.	I/O	Description	Comment
I2S_WS	259	DO	I2S word select	1.8 V power domain. I2S and SPI support master mode only by default.
I2S_SCK	256	DO	I2S clock	
I2S_DIN	257	DI	I2S data in	
I2S_DOUT	255	DO	I2S data out	
SPI1_CLK	210	DO	SPI clock	

SPI1_CS	207	DO	SPI chip select
SPI1_MISO	213	DI	SPI master-in slave-out
SPI1_MOSI	204	DO	SPI master-out slave-in
EXT_RST	75	DO	External audio reset
EXT_INT	281	DI	External audio interrupt

The following figure shows a reference design of SLIC application.

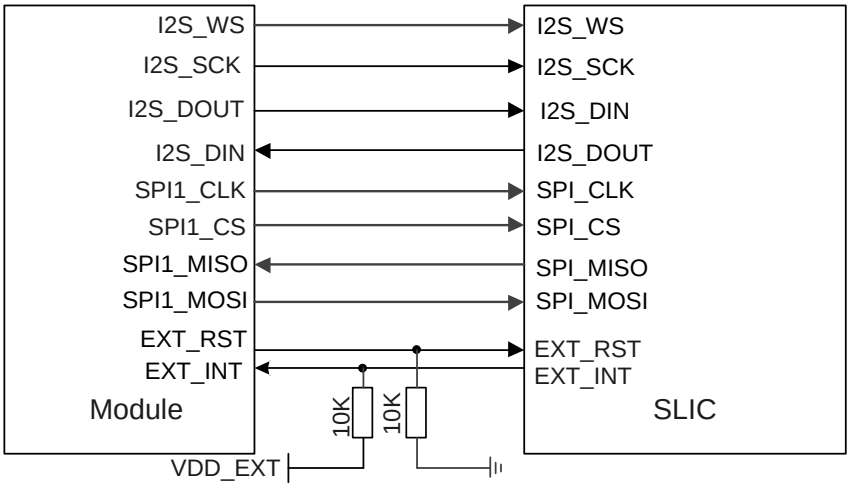


Figure 29: Reference Circuit of I2S Application with SPI

3.11. ADC Interface

The module provides one Analog-to-Digital Converter (ADC) interface. To improve the accuracy of ADC, surround the trace of ADC with ground.

Table 19: Pin Description of ADC Interface

Pin Name	Pin No.	Description
ADC0	241	General-purpose ADC interface

Table 20: Characteristics of ADC Interface

Parameter	Min.	Typ.	Max.	Unit

ADC0 Input Voltage Range	0	-	VBAT	V
ADC0 Resolution	-	11	-	bits

NOTE

1. The input voltage of ADC should not exceed VBAT.
2. It is prohibited to supply any voltage to ADC pin when VBAT is removed.

3.12. Network Status Indication

The network indication pins NET_MODE and NET_STATUS can drive the network status indication LEDs. The following tables describe the pin description and logic level changes in different network status.

Table 21: Pin Description of Network Connection Status/Activity Indication

Pin Name	Pin No.	I/O	Description	Comment
NET_MODE	240	DO	Indicates the module's network registration mode	1.8 V power domain. If unused, keep them open.
NET_STATUS	243	DO	Indicates the module's network activity status	

Table 22: Working State of the Network Connection Status/Activity Indication

Pin Name	Status	Description
NET_MODE	Always High	Registered on 5G network
	Always Low	Others
NET_STATUS	Blink slowly (200 ms High/1800 ms Low)	Network searching
	Blink slowly (1800 ms High/200 ms Low)	Idle
	Blink quickly (125 ms High/125 ms Low)	Data transmission is ongoing
	Always High	Voice calling

A reference circuit is shown in the following figure.

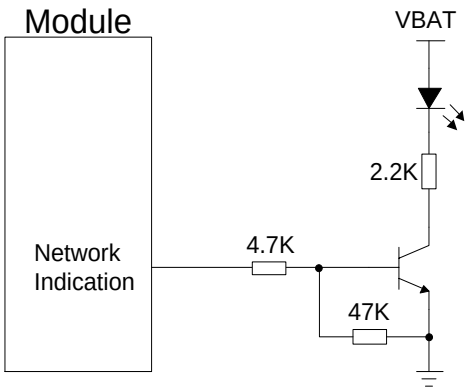


Figure 30: Reference Circuit of the Network Indication

3.13. STATUS

The STATUS pin indicates the module's operation status. It outputs high level when the module is powered on successfully

Table 23: Pin Description of STATUS

Pin Name	Pin No.	I/O	Description	Comment
STATUS	237	DO	Indicates the module's operation status	1.8 V power domain.

A reference circuit is shown as below.

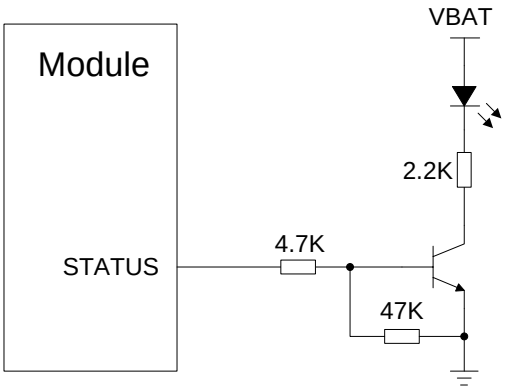


Figure 31: Reference Circuit of STATUS

NOTE

STATUS can't be used as the turn-off status indication when the module' VBAT is not turned on.

3.14. UART1_RI*

You can configure UART1_RI behaviors flexibly. The default behavior of the UART1_RI is shown as below.

Table 24: Behaviors of the UART1_RI

State	Response
Idle	UART1_RI keeps at a high level.
URC	UART1_RI outputs 120 ms low pulse when a new URC returns.

3.15. USB_BOOT Interface

RG500U series provides a USB_BOOT pin. You can make the module enter download mode after being turned on by pulling up USB_BOOT to VDD_EXT before turning on the module. In this mode, the module supports firmware upgrade over USB 2.0 interface.

Table 25: Pin Description of USB_BOOT Interface

Pin Name	Pin No.	I/O	Description	Comment
USB_BOOT	81	DI	Forces the module into download mode	1.8 V power domain. Test points are recommended to be reserved.

The following figure shows a reference circuit of USB_BOOT interface.

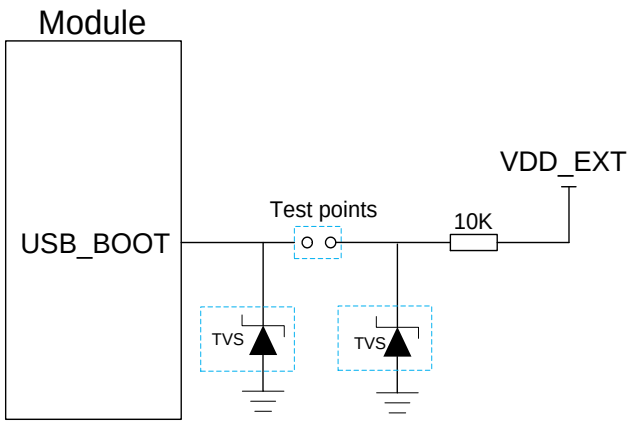


Figure 32: Reference Circuit of USB_BOOT Interface

3.16. I2C Interface

The module provides one I2C interface, and the speed rate can be up to 3.4 Mbps.

Table 26: Pin Description of I2C Interface

Pin Name	Pin No.	I/O	Description	Comment
I2C1_SCL	77	OD	I2C serial clock	Require an external pull-up to VDD_EXT. If unused, keep them open.
I2C1_SDA	78	OD	I2C serial data	

3.17. PCIe Interface

RG500U series includes one PCIe interface which is in compliance with *PCI Express Base Specification Revision 2.1*. The key features of the PCIe interface are as below:

- Supports PCIe Gen 2 with backward compatibility
- Data rate at 5 Gbps/lane
- Can be used to connect to an Ethernet IC
- Supports RC and EP mode

Table 27: Pin Description of PCIe Interface

Pin Name	Pin No.	I/O	Description	Comment
PCIE_REFCLK_P	40	AIO	PCIe reference clock (+)	*PCI Express Base Specification Revision 2.1* compliant. Supports PCIe Gen 2. Requires differential impedance of 100 Ω. In RC mode, it is an output signal. In EP mode, it is an input signal.
PCIE_REFCLK_M	38	AIO	PCIe reference clock (-)	
PCIE_TX0_M	44	AO	PCIe transmit 0 (-)	*PCI Express Base Specification Revision 2.1* compliant. Supports PCIe Gen 2. Requires differential impedance of 100 Ω.
PCIE_TX0_P	46	AO	PCIe transmit 0 (+)	
PCIE_RX0_M	32	AI	PCIe receive 0 (-)	
PCIE_RX0_P	34	AI	PCIe receive 0 (+)	
PCIE_CLKREQ	36	DI, OD	PCIe clock request	1.8 V power domain. In RC mode, it is an input signal. In EP mode, it is an output signal.
PCIE_RST	39	DIO	PCIe reset	1.8 V power domain. In RC mode, it is an output signal. In EP mode, it is an input signal.
PCIE_WAKE	30	DI, OD	PCIe wake up	1.8 V power domain. In RC mode, it is an input signal. In EP mode, it is an output signal.

The following figure shows the reference design of PCIe interface.

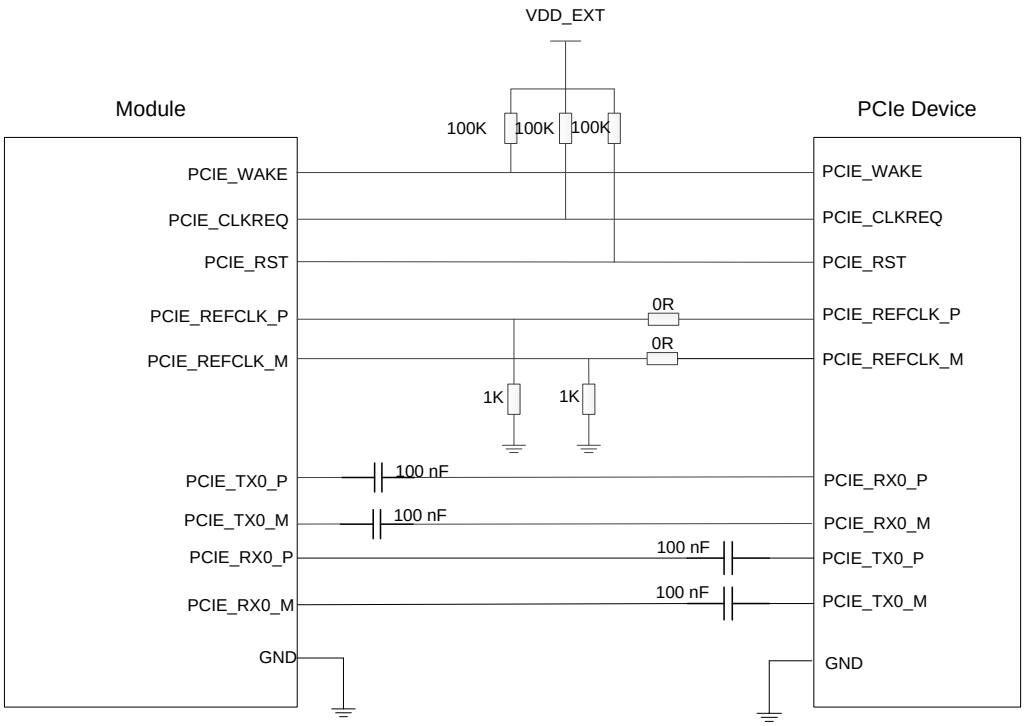


Figure 33: PCIe Interface Reference Circuit (RC Mode)

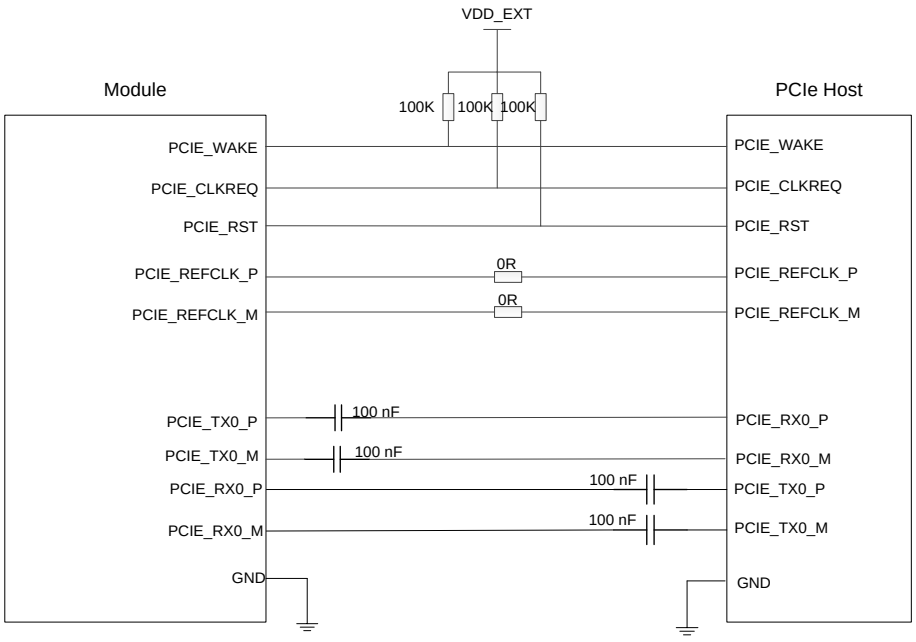


Figure 34: PCIe Interface Reference Circuit (EP Mode)

To enhance the reliability and availability in applications, follow the criteria below in the PCIe interface circuit design:

- Keep trace of the PCIe data and control signals away from sensitive circuits and signals, such as RF, audio, and clock signals.

- Add a capacitor in series on Tx/Rx traces to prevent any DC bias.
- Keep the maximum trace length less than 300 mm.
- Keep the length matching of each differential data pair (Tx/Rx/REFCLK) less than 0.15 mm for PCIe routing traces.
- Keep the differential impedance of PCIe data trace as 100 Ω ±10 %.
- You must not route PCIe data traces under components or cross them with other traces.

NOTE

When connecting PCIe interface to host or PC with 3.3 V power domain, you need to use a voltage-level translator chip to maintain level matching.

3.18. Antenna Tuner Control Interfaces

The module controls the external antenna tuner through GRFC signals. The following table shows the pin description of the interfaces.

Table 28: Pin Description of Antenna Tuner Control Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	117	DO	Generic RF Controller	If unused, keep them open.
GRFC2	120	DO	Generic RF Controller	

NOTE

For RG500U-EA/RG500U-EB/RG500U-LA/RG500U-JO, antenna tuner control interfaces are under development.

4 Antenna Interfaces

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

The module includes four or six cellular antenna interfaces. The impedance of antenna port is 50 Ω.

4.1. Cellular Antenna Interfaces

4.1.1. Pin Definition

Table 29: RG500U-CN Pin of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX - LTE: LMHB TRX - 5G NR: n1/n28 TRX & n41 TRX1 & n77/n78/n79 DRX1 - Refarming: n1/n28 TRX	50 Ω characteristic impedance.
ANT1	157	AIO	**Antenna 1 interface:** - WCDMA: LMB DRX - LTE: LMHB DRX - 5G NR: n1 DRX0 & n28 DRX & n77/n78/n79 TRX1 & n41 DRX1 - Refarming: n1 DRX0 & n28 DRX	
ANT2	166	AIO	**Antenna 2 interface:** - 5G NR: n41/n77/n78/n79 DRX0 & n1 DRX1	
ANT3	184	AIO	**Antenna 3 interface:** - 5G NR: n41/n77/n78/n79 TRX0 & n1 PRX1	

Table 30: RG500U-EA Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX LTE: LMB & B40 TRX - 5G NR: n1/n3/n66 PRX1 & n5/n8/n20/n28 TRX & n40 TRX1 - Refarming: n1/n3/n66 PRX1 & n5/n8/n20/n28 TRX & n40 TRX1	50 Ω characteristic impedance.
ANT1	139	AIO	**Antenna 1 interface:** - LTE: B7/B38/B41 TRX - 5G NR: n7 PRX1 & n38/n41 TRX1 & n77/n78 DRX0 - Refarming: n38 TRX1 & n7 PRX1	
ANT2	148	AIO	**Antenna 2 interface:** - WCDMA: LMB DRX - LTE: LMB & B40 DRX - 5G NR: n1/n3/n40/n66 DRX1 & n5/n8/n20/n28 DRX - Refarming: n1/n3/n40/n66 DRX1 & n5/n8/n20/n28 DRX	
ANT3	157	AIO	**Antenna 3 interface:** - LTE: B7/B38/B41 DRX - 5G NR: n7/n38/n41 DRX1 & n77/n78 TX1 & PRX1 - Refarming: n7/n38 DRX1	
ANT4	166	AIO	**Antenna 4 interface:** - 5G NR: LMHB DRX0 & n77/n78 DRX1	
ANT5	184	AIO	**Antenna 5 interface:** - 5G NR: LMHB & n77/n78 TRX0	

Table 31: RG500U-EB Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX - LTE: LMHB TRX - 5G NR: n1/n3/n7/n28/n66 PRX1 & n5/n8 TRX & n38/n40/n41 TRX1 & n77/n78 DRX0 - Refarming: n1/n3/n7/n28/n66 PRX1 & n5/n8 TRX & n38/n40 TRX1	50 Ω characteristic impedance.

ANT2	148	AIO	**Antenna 2 interface:** - WCDMA: LMB DRX - LTE: LMHB DRX - 5G NR: n1/n3/n7/n28/n38/n40/n41/n66 DRX1 & n5/n8/n20 DRX & n77/n78 TX1 & PRX1 - Reframing: n1/n3/n7/n28/n38/n40/n66 DRX1 & n5/n8/n20 DRX	
ANT4	166	AIO	**Antenna 4 interface:** - 5G NR: LMHB DRX0 & n77/n78 DRX1	
ANT5	184	AIO	**Antenna 5 interface:** - 5G NR: LMHB & n77/n78 TRX0	

Table 32: RG500U-LA Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	**Antenna 0 interface:** - WCDMA: LMB TRX LTE: LMB & B40 TRX - 5G NR: n2/n28/n66 PRX1 & n8/n71 TRX & n40 TRX1 - Reframing: n2/n28/n66 PRX1 & n8/n71 TRX & n40 TRX1	50 Ω characteristic impedance.
ANT1	139	AIO	**Antenna 1 interface:** - LTE: B7/B38 TRX - 5G NR: n7 PRX1 & n38 TRX1 & n78 DRX0 - Reframing: n38 TRX1 & n7 PRX1	
ANT2	148	AIO	**Antenna 2 interface:** - WCDMA: LMB DRX - LTE: LMB & B40 DRX - 5G NR: n2/n28/n66/n40 DRX1 & n5/n8 DRX - Reframing: n2/n28/n66/n40 DRX1 & n5/n8 DRX	
ANT3	157	AIO	**Antenna 3 interface:** - LTE: B7/B38 DRX - 5G NR: n7/n38 DRX1 & n78 TX1 & PRX1 - Reframing: n7/n38 DRX1	
ANT4	166	AIO	**Antenna 4 interface:** - 5G NR: LMHB DRX0 & n78 DRX1	
ANT5	184	AIO	**Antenna 5 interface:** - 5G NR: LMHB & n78 TRX0	

Table 33: RG500U-JO Pin Definition of Cellular Antenna Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ANT0	130	AIO	- Reserved	50 Ω characteristic impedance.
ANT1	139	AIO	**Antenna 1 interface:** - n78 DRX0	
ANT2	148	AIO	- Reserved	
ANT3	157	AIO	**Antenna 3 interface:** - n78 TX1 & PRX1	
ANT4	166	AIO	**Antenna 3 interface:** - 5G NR: n78 DRX1	
ANT5	184	AIO	**Antenna 4 interface:** - 5G NR: n78 TRX0	

4.1.2. Cellular Antenna Mapping

Table 34: RG500U-CN Cellular Antenna Mapping

Antenna	Pin No.	WCDMA	LTE	5G NR				LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)
				Reframing	n1	n41	n77/n78/n79				
ANT0	130	LMB TRX	LMHB TRX	n1/n28 TRX	-	TRX1	DRX1	699–960	1710–2690	3300–4200	4400–5000
ANT1	157	LMB DRX	LMHB DRX	n1 DRX0 & n28 DRX	-	DRX1	TRX1	758–960	1805–2690	3300–4200	4400–5000
ANT2	166	-	-	-	DRX1	DRX0	DRX0	-	2110–2690	3300–4200	4400–5000
ANT3	184	-	-	-	PRX1	TRX0	TRX0	-	2110–2690	3300–4200	4400–5000

Table 35: RG500U-EA Cellular Antenna Mapping

Antenna	Pin No.	WCDMA	LTE	5G NR				LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)
				Reframing	LMHB	n41	n77/n78				
ANT0	130	LMB TRX	LMB & B40 TRX	n1/n3/n66 PRX1 & n40 TRX1 & n5/n8/n20/n28 TRX	-	-	-	703–960	1710–2400	-	-
ANT1	139	-	B7/B38/B41 TRX	n38 TRX1 & n7 PRX1	-	TRX1	DRX0	-	2496–2690	3300–4200	-

ANT2	148	LMB DRX	LMB & B40 DRX	n1/n3/n40/n66 DRX1 & n5/n8/n20/n28 DRX	-	-	-	758–960	1805–2400	-	-
ANT3	157	-	B7/B38/B41 DRX	n7/n38 DRX1	-	DRX1	TX1 & PRX1	-	2496–2690	3300–4200	-
ANT4	166	-	-	-	DRX0	DRX0	DRX1	617–894	1805–2690	3300–4200	-
ANT5	184	-	-	-	TRX0	TRX0	TRX0	617–894	1710–2690	3300–4200	-

Table 36: RG500U-EB Cellular Antenna Mapping

Antenna	Pin No.	WCDMA	LTE	5G NR				LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)
				Refarming	LMHB	n41	n77/n78				
ANT0	130	LMB TRX	LMHB TRX	n1/n3/n7/ n28/n66 PRX1 & n5/n8 TRX & n38/n40 TRX1	-	TRX1	DRX0	703–960	1710–2690	3300–4200	-
ANT1	139	-		-	-	-	-	-	-	-	-
ANT2	148	LMB DRX	LMHB DRX	n1/n3/n7/n28/ n38/n40/n66 DRX1 & n5/n8/n20 DRX	-	DRX1	TX1 & PRX1	758–960	1805–2690	3300–4200	-
ANT3	157	-	-	-	-	-	-	-	-	-	-

ANT4	166	-	-	-	DRX0	DRX0	DRX1	617–894	1805–2690	3300–4200	-
ANT5	184	-	-	-	TRX0	TRX0	TRX0	617–894	1710–2690	3300–4200	-

Table 37: RG500U-LA Cellular Antenna Mapping

Antenna	Pin No.	WCDMA	LTE	5G NR				LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)
				Refarming	LMHB	n41	n78				
ANT0	130	LMB TRX	LMB & B40 TRX	n2/n28/n66 PRX1 & n40 TRX1 & n8/n71 TRX	-	-	-	617–960	1710–2400	-	-
ANT1	139	-	B7/B38 TRX	n38 TRX1 & n7 PRX1	-	-	DRX0	-	2496–2670	3300–3800	-
ANT2	148	LMB DRX	LMB & B40 DRX	n2/n28/n66/n40 DRX1 & n5/n8 DRX	-	-	-	617–960	1805–2400	-	-
ANT3	157	-	B7/B38 DRX	n7/n38 DRX1	-	-	TX1 & PRX1	-	2496–2670	3300–3800	-
ANT4	166	-	-	-	DRX0	-	DRX1	617–960	1805–2690	3300–3800	-
ANT5	184	-	-	-	TRX0	-	TRX0	617–960	1710–2690	3300–3800	-

Table 38: RG500U-JO Cellular Antenna Mapping

Antenna	Pin No.	WCDMA	LTE	5G NR				LB (MHz)	MHB (MHz)	n77/n78 (MHz)	n79 (MHz)
				Reframing	LMHB	n41	n78				
ANT0	130	-	-	-	-	-	-	-	-	-	-
ANT1	139	-	-	-	-	-	DRX0	-	-	3300–3800	-
ANT2	148	-	-	-	-	-	-	-	-	-	-
ANT3	157	-	-	-	-	-	TX1 & PRX1	-	-	3300–3800	-
ANT4	166	-	-	-	-	-	DRX1	-	-	3300–3800	-
ANT5	184	-	-	-	-	-	TRX0	-	-	3300–3800	-

NOTE

1. DRX1 = DRX MIMO
2. TRX1 = TX1 + PRX MIMO
3. PRX1 = PRX MIMO

4.1.3. Operating Frequency

Table 39: RG500U-CN Operating Frequencies

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	B1	-	B1	n1
B2	1850–1910	1930–1990	B2	-	B2	-
DCS (1800)	1710–1785	1805–1880	B3	-	-	-
Cell (850)	824–849	869–894	B5	-	B5	-
IMT-E (2600)	2500–2570	2620–2690	B7	-	-	-
EGSM (950)	880–915	925–960	B8	-	B8	-
EU800	832–862	791–821	B20	-	-	-
700 APAC	703–748	758–803	B28	-	-	n28
B34	2010–2025	2010–2025	-	B34	-	-
B38	2570–2620	2570–2620	-	B38	-	-
B39	1880–1920	1880–1920	-	B39	-	-
B40	2300–2400	2300–2400	-	B40	-	-
B41/B41-XGP	2496–2690	2496–2690	-	B41	-	n41
n77	3300–4200	3300–4200	-	-	-	n77
n78	3300–3800	3300–3800	-	-	-	n78
n79	4400–5000	4400–5000	-	-	-	n79

Table 40: RG500U-EA Operating Frequencies

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	B1	-	B1	n1
B2	1850–1910	1930–1990	B2	-	B2	-
DCS (1800)	1710–1785	1805–1880	B3	-	-	n3
B4	1710–1755	2110–2155	B4	-	-	-
Cell (850)	824–849	869–894	B5	-	B5	n5
IMT-E (2600)	2500–2570	2620–2690	B7	-	-	n7
EGSM (950)	880–915	925–960	B8	-	B8	n8
EU800	832–862	791–821	B20	-	-	n20
700 APAC	703–748	758–803	B28	-	-	n28
B38	2570–2620	2570–2620	-	B38	-	n38
B40	2300–2400	2300–2400	-	B40	-	n40
B41/B41-XGP	2496–2690	2496–2690	-	B41	-	n41
B66	1710–1780	2110–2180	B66	-	-	n66
n71	663–698	617–652				n71*
n77	3300–4200	3300–4200	-	-	-	n77
n78	3300–3800	3300–3800	-	-	-	n78

Table 41: RG500U-EB Operating Frequencies

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
IMT (2100)	1920–1980	2110–2170	B1	-	B1	n1
B2	1850–1910	1930–1990	B2	-	B2	-
DCS (1800)	1710–1785	1805–1880	B3	-	-	n3
B4	1710–1755	2110–2155	B4	-	-	-

Cell (850)	824–849	869–894	B5	-	B5	n5
IMT-E (2600)	2500–2570	2620–2690	B7	-	-	n7
EGSM (950)	880–915	925–960	B8	-	B8	n8
EU800	832–862	791–821	B20	-	-	n20
700 APAC	703–748	758–803	B28	-	-	n28
B38	2570–2620	2570–2620	-	B38	-	n38
B40	2300–2400	2300–2400	-	B40	-	n40
B41/B41-XGP	2496–2690	2496–2690	-	B41	-	n41
B66	1710–1780	2110–2180	B66	-	-	n66
n77	3300–4200	3300–4200	-	-	-	n77
n78	3300–3800	3300–3800	-	-	-	n78

Table 42: RG500U-LA Operating Frequencies

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
B2	1850–1910	1930–1990	B2	-	B2	n2
B4	1710–1755	2110–2155	B4	-	B4	-
Cell (850)	824–849	869–894	B5	-	B5	n5
IMT-E (2600)	2500–2570	2620–2690	B7	-	-	n7
EGSM (950)	880–915	925–960	B8	-	-	n8
B26	814–849	859–894	B26	-	-	-
700 APAC	703–748	758–803	B28	-	-	n28
B38	2570–2620	2570–2620	-	B38	-	n38
B40	2300–2400	2300–2400	-	B40	-	n40
B66	1710–1780	2110–2180	B66	-	-	n66
B71	663–698	617–652	B71	-	-	n71

n78	3300–3800	3300–3800	-	-	-	n78

Table 43: RG500U-JO Operating Frequencies

Band Name	Transmit (MHz)	Receive (MHz)	LTE-FDD	LTE-TDD	UMTS	5G NR
n78	3300–3800	3300–3800	-	-	-	n78

4.1.4. Reference Design of Cellular Antenna Interface

A reference design of cellular antenna interface is shown as below. Reserve a dual L-type circuit for better antenna performance. The capacitors in parallel with ground are not mounted by default.

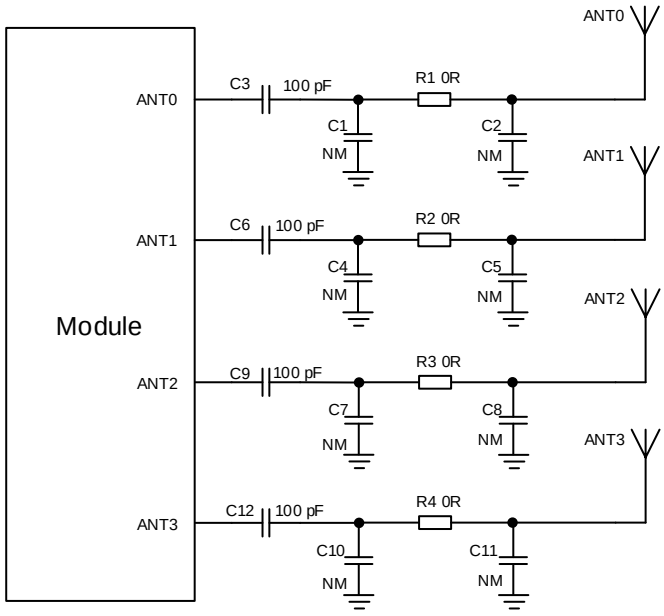


Figure 35: RG500U-CN Reference Circuit of RF Antennas

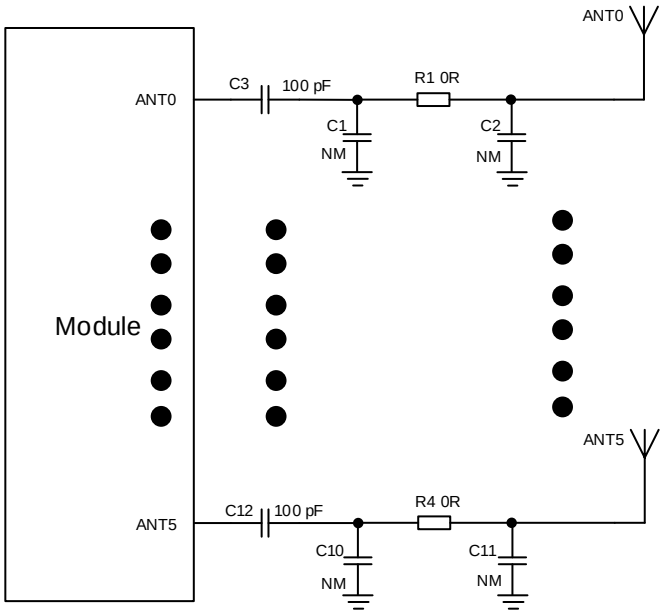


Figure 36: RG500U-EA Reference Circuit of RF Antennas

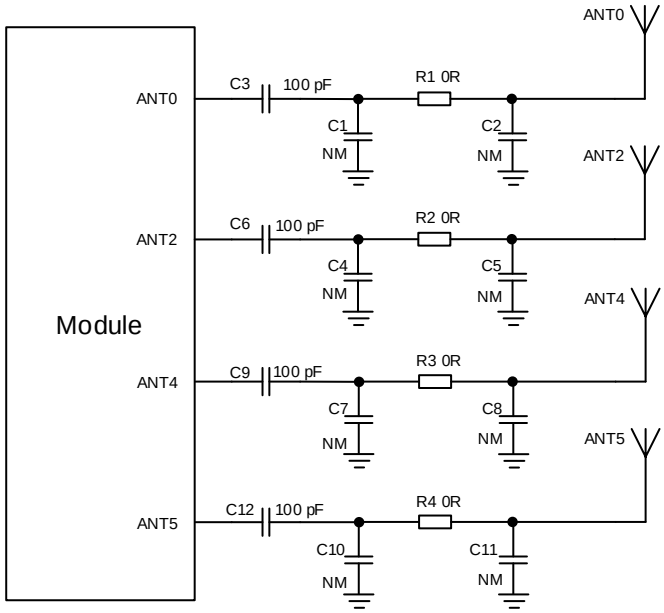


Figure 37: RG500U-EB Reference Circuit of RF Antennas

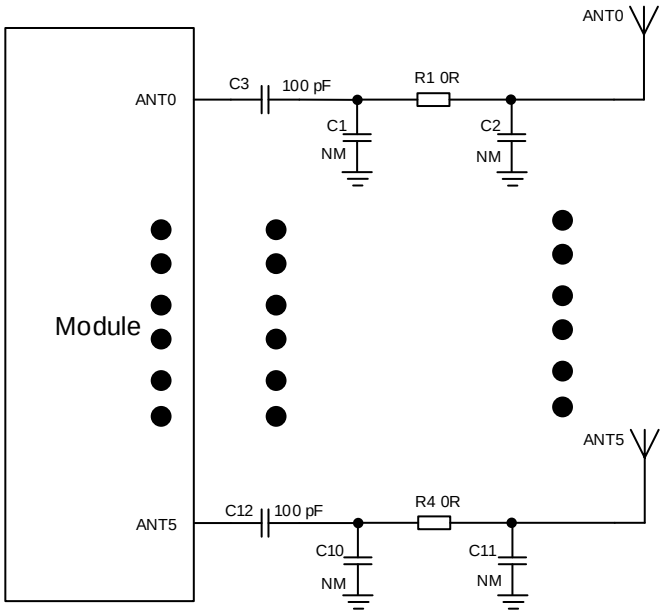


Figure 38: RG500U-LA Reference Circuit of RF Antennas

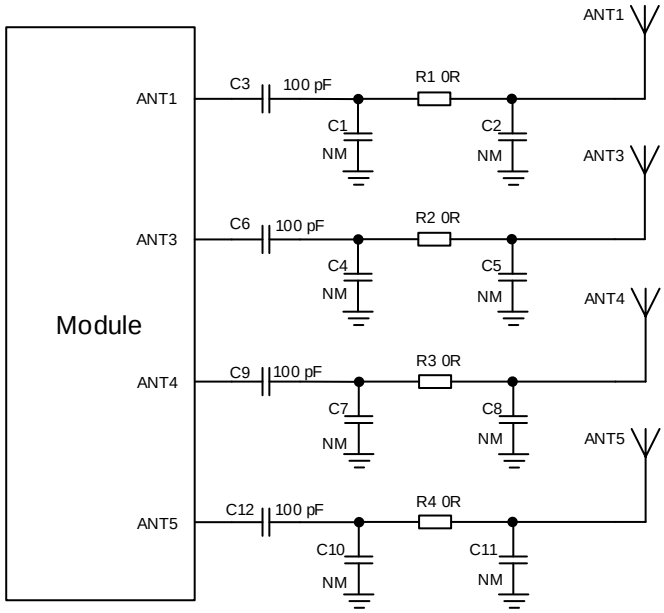


Figure 39: RG500U-JO Reference Circuit of RF Antennas

NOTE

1. Use a dual L-type circuit for antenna interfaces for better RF performances and for the ease of future debugging, and place as close to the antenna as possible.
2. Keep the impedance of the cellular antennas (ANT0–ANT5) traces as 50 Ω when routing.

3. Keep at least 15 dB isolation between RF antennas to improve the receiving sensitivity, and at least 20 dB isolation between 5G NR UL MIMO antennas.
4. The isolation between each antenna trace on PCB is recommended to be more than 75 dB.
5. Keep digital circuits such as switch mode power supply, (U)SIM card, USB interface, camera module, display connector and SD card away from the antenna traces.
6. It is recommended that the straight-line distance between the antenna and the module be greater than 15 mm to achieve better wireless performance of the whole device.
7. If there is DC power at the antenna ports, C3, C6, C9 and C12 must be used for DC-blocking to prevent short circuit to ground. The capacitance value is recommended to be 100 pF, which can be adjusted according to actual requirements. If there is no DC power in the peripheral design, C3, C6, C9 and C12 should not be reserved.

4.2. RF Routing Guidelines

For the PCB, control the characteristic impedance of all RF traces to 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the spacing between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguide with different PCB structures.

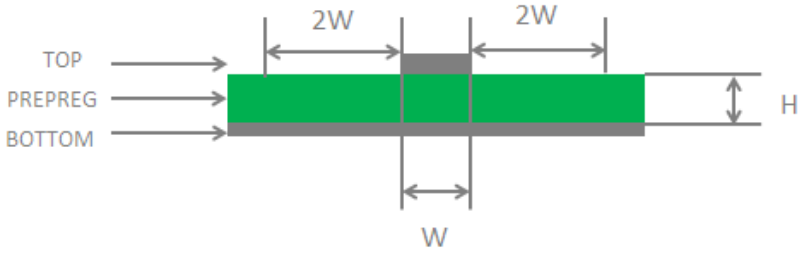


Figure 40: Microstrip Line Design on a 2-layer PCB

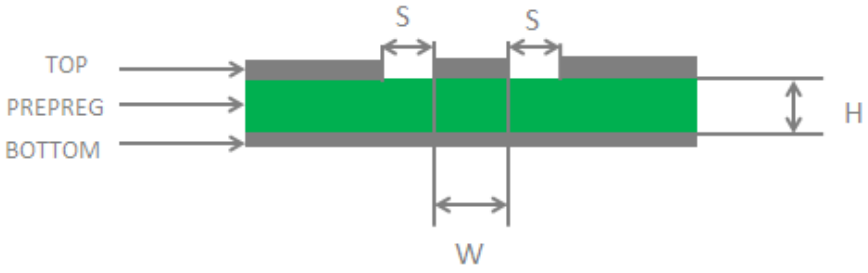


Figure 41: Coplanar Waveguide Line Design on a 2-layer PCB

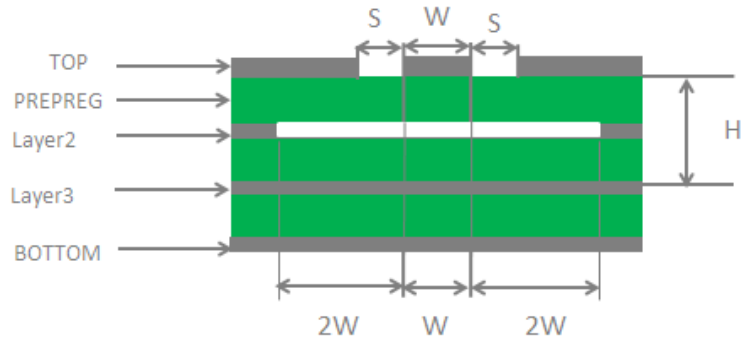


Figure 42: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 3 as Reference Ground)

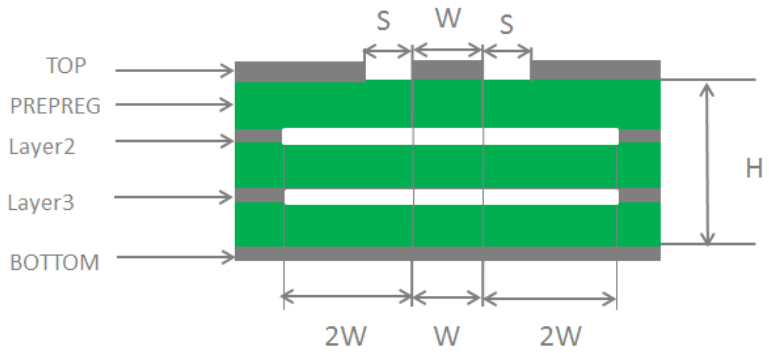


Figure 43: Coplanar Waveguide Line Design on a 4-layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- Reserve clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least twice of the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources (such as DC-DC, (U)SIM/USB/SDIO high frequency digital signals, display signals, and clock signals), and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [4]***.

4.3. Antenna Installation

4.3.1. Antenna Design Requirement

Table 44: Antenna Requirements

Type	Requirements
Cellular	● VSWR: ≤ 2 ● Efficiency: > 30 % ● Input Impedance: 50 Ω ● Cable insertion loss: < 1 dB: LB (< 1 GHz) < 1.5 dB: MB (1–2.3 GHz) < 2 dB: HB (> 2.3 GHz)

4.3.2. RF Connector Recommendation

The receptacle dimensions are illustrated as below.

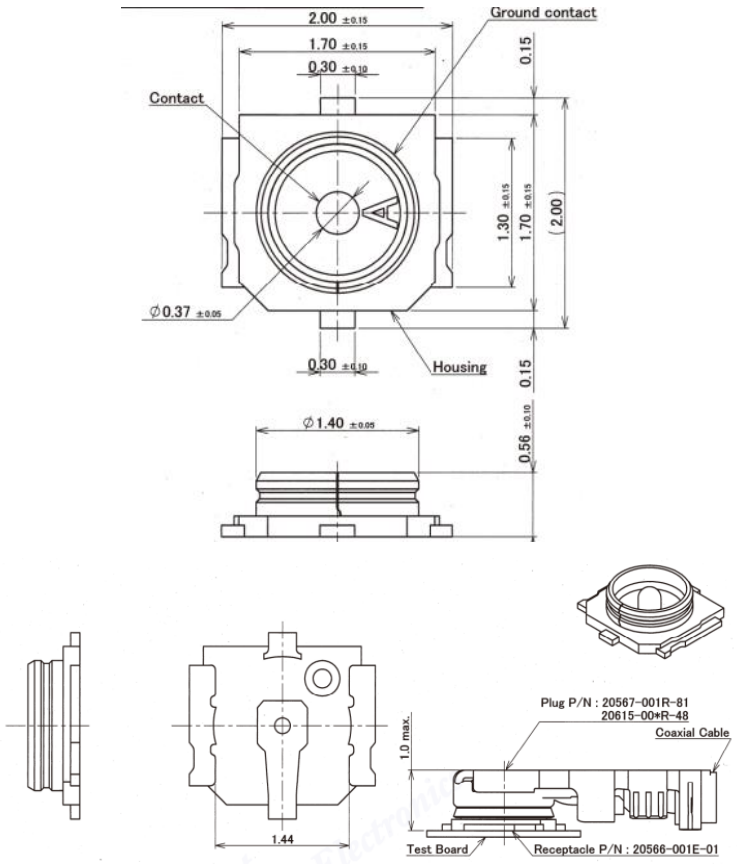


Figure 44: Dimensions of the Receptacles (Unit: mm)

The following figure shows the specifications of mated plugs using Ø0.81 mm coaxial cables.

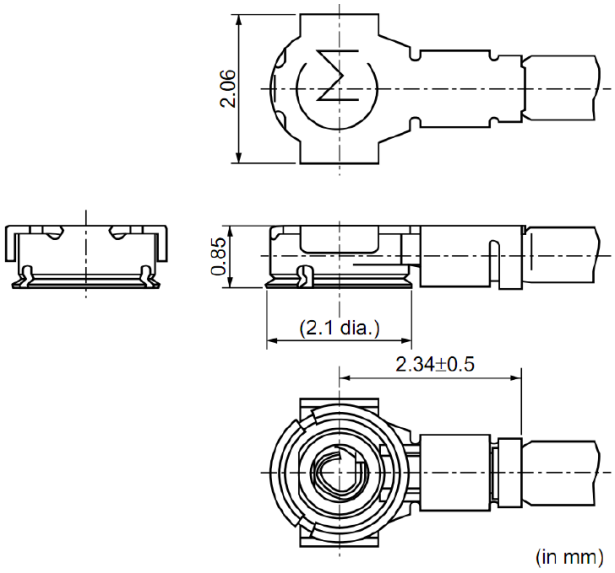


Figure 45: Specifications of Mated Plugs Using Ø0.81 mm Coaxial Cables (Unit: mm)

4.3.3. Recommended RF Connector for Installation

4.3.3.1. Assemble Coaxial Cable Plug Manually

The illustration for plugging in a coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

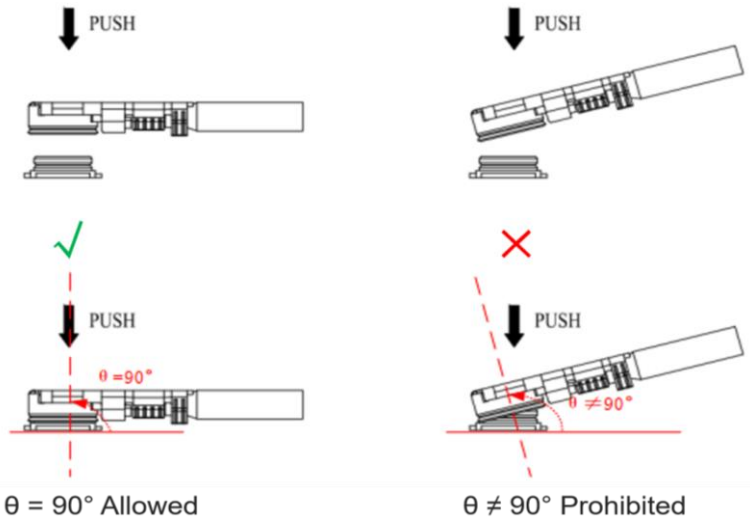


Figure 46: Plug in a Coaxial Cable Plug

The illustration of pulling out the coaxial cable plug is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

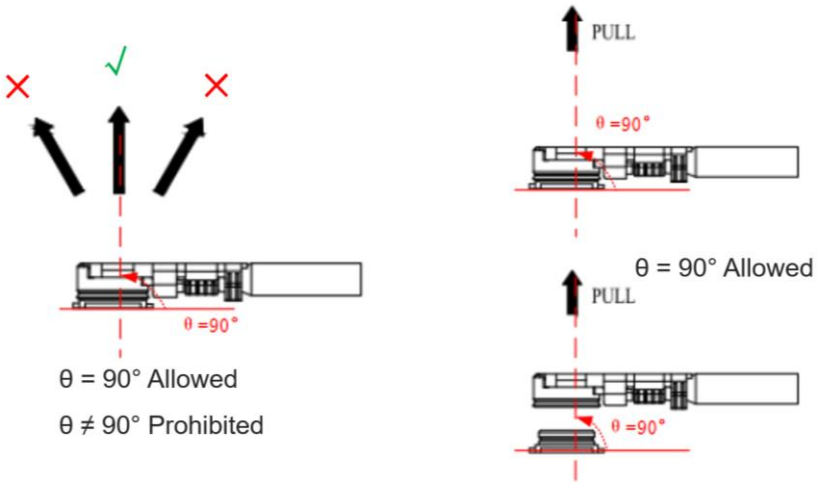


Figure 47: Pull out a Coaxial Cable Plug

4.3.3.2. Assemble Coaxial Cable Plug with Fixture

The pictures of installing the coaxial cable plug with a fixture is shown below, θ = 90° is acceptable, while θ ≠ 90° is not.

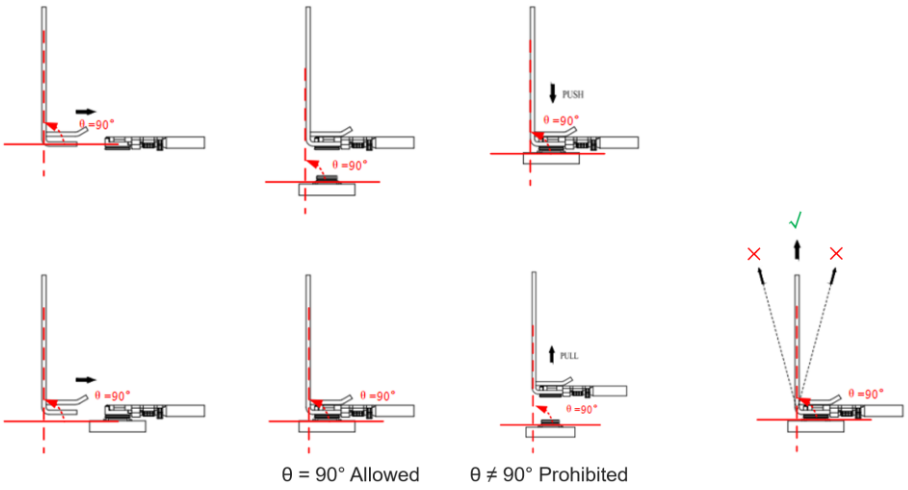


Figure 48: Install the Coaxial Cable Plug with Fixture

4.3.4. Recommended Manufacturers of RF Connector and Cable

For more details, visit https://www.i-pex.com.

5 Reliability, Radio and Electrical Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 45: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.3	6.0	V
USB_VBUS	-0.3	5.5	V
Peak Current of VBAT_BB	-	1.5	A
Peak Current of VBAT_RF	-	2.5	A
Voltage at Digital Pins	-0.3	1.98	V

5.2. Power Supply Ratings

Table 46: Module Power Supply Ratings

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
VBAT	VBAT_BB and VBAT_RF1	The actual input voltages must be kept between the minimum and maximum values.	3.3	3.8	4.3	V

5.3. Digital I/O Characteristics

Table 47: 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	High-level input voltage	0.7 × VDD_EXT	VDD_EXT	V
V_{IL}	Low-level input voltage	-0.3	0.3 × VDD_EXT	V
V_{OH}	High-level output voltage	0.9 × VDD_EXT	VDD_EXT	V
V_{OL}	Low-level output voltage	0	0.1 × VDD_EXT	V

NOTE

VDD_EXT is module's I/O voltage domain.

Table 48: (U)SIM 1.8 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.62	1.98	V
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Low-level input voltage	-0.3	0.3 × USIM_VDD	V
V_{OH}	High-level output voltage	0.9 × USIM_VDD	1.98	V
V_{OL}	Low-level output voltage	0	0.1 × USIM_VDD	V

Table 49: (U)SIM 3.0 V I/O Requirements

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	2.7	3.3	V
V_{IH}	High-level input voltage	0.7 × USIM_VDD	USIM_VDD	V
V_{IL}	Low-level input voltage	-0.3	0.3 × USIM_VDD	V
V_{OH}	High-level output voltage	0.9 × USIM_VDD	3.3	V
V_{OL}	Low-level output voltage	0	0.1 × USIM_VDD	V

5.4. Operating and Storage Temperatures

Table 50: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [7]	-30	-	+75	°C
Extended Temperature Range [8]	-40	-	+85	°C
Storage Temperature Range	-40	-	+90	°C

5.5. Power Consumption

Table 51: RG500U-CN Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	70	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	3.85	mA
	AT+CFUN=4 (USB disconnected)	3.95	mA
	WCDMA PF = 64 (USB disconnected)	6.55	mA
	LTE-FDD PF = 64 (USB disconnected)	5.95	mA
	LTE-TDD PF = 64 (USB disconnected)	5.95	mA
	5G NR-FDD PF = 64 (USB disconnected)	17.15	mA
	5G NR-TDD PF = 64 (USB disconnected)	17.15	mA
Idle state	WCDMA PF = 64 (USB disconnected)	31.5	mA

[7] To meet the normal operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module can meet 3GPP specifications.

[8] To meet the extended operating temperature range requirements, it is necessary to ensure effective thermal dissipation, e.g., by adding passive or active heatsinks, heat pipes, vapor chambers. Within this range, the module remains the ability to establish and maintain functions such as voice, SMS, data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may undergo a reduction in value, exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature level, the module will meet 3GPP specifications again.

	WCDMA PF = 64 (USB connected)	58.5	mA
	LTE-FDD PF = 64 (USB disconnected)	31.5	mA
	LTE-FDD PF = 64 (USB connected)	58.5	mA
	LTE-TDD PF = 64 (USB disconnected)	31.5	mA
	LTE-TDD PF = 64 (USB connected)	58.5	mA
	5G NR-FDD PF = 64 (USB disconnected)	43.5	mA
	5G NR-FDD PF = 64 (USB connected)	69.5	mA
	5G NR-TDD PF = 64 (USB disconnected)	43.5	mA
	5G NR-TDD PF = 64 (USB connected)	69.5	mA
WCDMA	WCDMA B1 HSDPA CH10700 @ 22.9 dBm	705	mA
	WCDMA B1 HSUPA CH10700 @ 20.4 dBm	635	mA
	WCDMA B2 HSDPA CH9800 @ 22.8 dBm	595	mA
	WCDMA B2 HSUPA CH9800 @ 20.7 dBm	515	mA
	WCDMA B5 HSDPA CH4408 @ 22.7 dBm	595	mA
	WCDMA B5 HSUPA CH4408 @ 20.7 dBm	515	mA
	WCDMA B8 HSDPA CH3012 @ 22.5 dBm	625	mA
	WCDMA B8 HSUPA CH3012 @ 20.5 dBm	540	mA
LTE	LTE-FDD B1 CH300 @ 22.8 dBm	725	mA
	LTE-FDD B2 CH900 @ 23.3 dBm	780	mA
	LTE-FDD B3 CH1575 @ 23.0 dBm	750	mA
	LTE-FDD B5 CH2525 @ 23.1 dBm	750	mA
	LTE-FDD B7 CH3100 @ 23.0 dBm	850	mA
	LTE-FDD B8 CH3625 @ 23.1 dBm	700	mA
	LTE-FDD B20 CH6300 @ 23.0dBm	650	mA
	LTE-FDD B28 CH9460 @ 23.0 dBm	700	mA
	LTE-TDD B34 CH36275 @ 23.5 dBm	370	mA

	LTE-TDD B38 CH38000 @ 23.3 dBm	415	mA
	LTE-TDD B39 CH38450 @ 23.4 dBm	315	mA
	LTE-TDD B40 CH39150 @ 23.4 dBm	425	mA
	LTE-TDD B41 CH40620 @ 23.2 dBm	405	mA
5G NR	5G NR-FDD n1 CH424000 @ 22.9 dBm	975	mA
	5G NR-FDD n1 CH428000 @ 22.2 dBm	1100	mA
	5G NR-FDD n1 CH432000 @ 22.5 dBm	1080	mA
	5G NR-FDD n28 CH153600 @ 22.9 dBm	980	mA
	5G NR-FDD n28 CH156600 @ 22.9 dBm	1010	mA
	5G NR-FDD n28 CH158600 @ 22.9 dBm	980	mA
	5G NR-TDD n41 CH501204 @ 26.5 dBm	665	mA
	5G NR-TDD n41 CH518598 @ 26.6 dBm	695	mA
	5G NR-TDD n41 CH535998 @ 26.0 dBm	670	mA
	5G NR-TDD n77 CH623334 @ 24.1 dBm	610	mA
	5G NR-TDD n77 CH650000 @ 24.3 dBm	625	mA
	5G NR-TDD n77 CH676666 @ 24.3 dBm	630	mA
	5G NR-TDD n78 CH620668 @ 26.4 dBm	635	mA
	5G NR-TDD n78 CH636666 @ 26.7 dBm	640	mA
	5G NR-TDD n78 CH652666 @ 26.4 dBm	660	mA
	5G NR-TDD n79 CH695090 @ 25.7 dBm	605	mA
	5G NR-TDD n79 CH713522 @ 25.6 dBm	640	mA
	5G NR-TDD n79 CH731976 @ 25.6 dBm	660	mA
WCDMA voice call	WCDMA B1 CH10700 @ 22.9 dBm	740	mA
	WCDMA B2 CH9800 @ 22.9 dBm	610	mA
	WCDMA B5 CH4408 @ 22.5 dBm	600	mA
	WCDMA B8 CH3012 @ 22.6 dBm	630	mA

Table 52: RG500U-EA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	81	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	4.67	mA
	AT+CFUN=4 (USB disconnected)	4.8	mA
	WCDMA PF = 64 (USB disconnected)	6.59	mA
	LTE-FDD PF = 64 (USB disconnected)	6.79	mA
	LTE-TDD PF = 64 (USB disconnected)	6.85	mA
	5G NR-FDD PF = 64 (USB disconnected)	18.17	mA
	5G NR-TDD PF = 64 (USB disconnected)	16.05	mA
Idle state	WCDMA PF = 64 (USB disconnected)	31.36	mA
	WCDMA PF = 64 (USB connected)	58.77	mA
	LTE-FDD PF = 64 (USB disconnected)	32.12	mA
	LTE-FDD PF = 64 (USB connected)	60.88	mA
	LTE-TDD PF = 64 (USB disconnected)	31.67	mA
	LTE-TDD PF = 64 (USB connected)	58.78	mA
	5G NR-FDD PF = 64 (USB disconnected)	45.15	mA
	5G NR-FDD PF = 64 (USB connected)	73.78	mA
	5G NR-TDD PF = 64 (USB disconnected)	44.82	mA
	5G NR-TDD PF = 64 (USB connected)	71.79	mA
WCDMA	WCDMA B1 HSDPA CH10700 @ 22.1 dBm	593	mA
	WCDMA B1 HSUPA CH10700 @ 20.1 dBm	517	mA
	WCDMA B2 HSDPA CH9800 @ 22.1 dBm	598	mA
	WCDMA B2 HSUPA CH9800 @ 20.3 dBm	527	mA
	WCDMA B5 HSDPA CH4400 @ 23.2 dBm	610	mA
	WCDMA B5 HSUPA CH4400 @ 20.9 dBm	522	mA

	WCDMA B8 HSDPA CH3013 @ 23.0 dBm	572	mA
	WCDMA B8 HSUPA CH3013 @ 20.8 dBm	491	mA
LTE	LTE-FDD B1 CH300 @ 22.8 dBm	749	mA
	LTE-FDD B2 CH900 @ 22.7 dBm	680	mA
	LTE-FDD B3 CH1575 @ 23.0 dBm	672	mA
	LTE-FDD B4 CH2175 @ 23.0 dBm	700	mA
	LTE-FDD B5 CH2525 @ 23.4 dBm	671	mA
	LTE-FDD B7 CH3100 @ 23.0 dBm	932	mA
	LTE-FDD B8 CH3625 @ 23.4 dBm	638	mA
	LTE-FDD B20 CH6300 @ 23.4 dBm	675	mA
	LTE-FDD B28 CH9460 @ 23.0 dBm	670	mA
	LTE-FDD B66 CH38000 @ 23.0 dBm	670	mA
	LTE-TDD B38 CH38000 @ 23.1 dBm	420	mA
	LTE-TDD B40 CH39150 @ 23.4 dBm	540	mA
	LTE-TDD B41 CH40620 @ 26.2 dBm	620	mA
5G NR	5G NR-FDD n1 CH427000 @ 22.9 dBm	1143	mA
	5G NR-FDD n1 CH428000 @ 22.7 dBm	1149	mA
	5G NR-FDD n1 CH429000 @ 22.9 dBm	1149	mA
	5G NR-FDD n3 CH364000 @ 22.5 dBm	1003	mA
	5G NR-FDD n3 CH368500 @ 22.4 dBm	1055	mA
	5G NR-FDD n3 CH373000 @ 22.5 dBm	1061	mA
	5G NR FDD n5 CH175800 @ 22.7 dBm	913	mA
	5G NR FDD n5 CH176300 @ 22.8 dBm	909	mA
	5G NR FDD n5 CH176800 @ 22.8 dBm	886	mA
	5G NR-FDD n7 CH526000 @ 23.4 dBm	1310	mA
	5G NR-FDD n7 CH531000 @ 23.2 dBm	1189	mA

	5G NR-FDD n7 CH536000 @ 23.3 dBm	1311	mA
	5G NR-FDD n8 CH187000 @ 23.0 dBm	893	mA
	5G NR-FDD n8 CH188500 @ 22.7 dBm	903	mA
	5G NR-FDD n8 CH190000 @ 22.9 dBm	942	mA
	5G NR-FDD n20 CH160200 @ 23.6 dBm	948	mA
	5G NR-FDD n20 CH161200 @ 23.4 dBm	914	mA
	5G NR-FDD n20 CH162200 @ 23.2 dBm	950	mA
	5G NR-FDD n28 CH154600 @ 23.2 dBm	971	mA
	5G NR-FDD n28 CH157600 @ 23.0 dBm	982	mA
	5G NR-FDD n28 CH158600 @ 23.0 dBm	982	mA
	5G NR-TDD n38 CH518000 @ 24.6 dBm	610	mA
	5G NR-TDD n38 CH519000 @ 24.6 dBm	607	mA
	5G NR-TDD n38 CH520000 @ 24.6 dBm	606	mA
	5G NR-TDD n40 CH468000 @ 24.2 dBm	642	mA
	5G NR-TDD n40 CH470000 @ 24.2 dBm	637	mA
	5G NR-TDD n40 CH472000 @ 24.4 dBm	630	mA
	5G NR-TDD n41 CH509202 @ 26.7 dBm	751	mA
	5G NR-TDD n41 CH518598 @ 26.4 dBm	749	mA
	5G NR-TDD n41 CH528000 @ 26.6 dBm	750	mA
	5G NR-FDD n66 CH426000 @ 24.2 dBm	1175	mA
	5G NR-FDD n66 CH429000 @ 23.9 dBm	1185	mA
	5G NR-FDD n66 CH434000 @ 24.4 dBm	1195	mA
	5G NR-TDD n77 CH623334 @ 26.2 dBm	715	mA
	5G NR-TDD n77 CH650000 @ 26.9 dBm	692	mA
	5G NR-TDD n77 CH676666 @ 26.5 dBm	689	mA
	5G NR-TDD n78 CH623334 @ 26.3 dBm	717	mA

	5G NR-TDD n78 CH636666 @ 26.7 dBm	719	mA
	5G NR-TDD n78 CH650000 @ 26.7 dBm	685	mA
WCDMA voice call	WCDMA B1 CH10700 @ 22.9 dBm	617	mA
	WCDMA B2 CH9800 @ 23.0 dBm	613	mA
	WCDMA B5 CH4400 @ 23.6 dBm	635	mA
	WCDMA B8 CH3013 @ 23.6 dBm	594	mA

Table 53: RG500U-EB Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	85	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	4.72	mA
	AT+CFUN=4 (USB disconnected)	4.79	mA
	WCDMA PF = 64 (USB disconnected)	6.72	mA
	LTE-FDD PF = 64 (USB disconnected)	6.91	mA
	LTE-TDD PF = 64 (USB disconnected)	7	mA
	5G NR-FDD PF = 64 (USB disconnected)	17.28	mA
	5G NR-TDD PF = 64 (USB disconnected)	15.58	mA
Idle state	WCDMA PF = 64 (USB disconnected)	31.93	mA
	WCDMA PF = 64 (USB connected)	59.76	mA
	LTE-FDD PF = 64 (USB disconnected)	32.05	mA
	LTE-FDD PF = 64 (USB connected)	59.78	mA
	LTE-TDD PF = 64 (USB disconnected)	32.14	mA
	LTE-TDD PF = 64 (USB connected)	60.18	mA
	5G NR-FDD PF = 64 (USB disconnected)	43.17	mA
	5G NR-FDD PF = 64 (USB connected)	71.55	mA
	5G NR-TDD PF = 64 (USB disconnected)	41.15	mA

	5G NR-TDD PF = 64 (USB connected)	69.41	mA
WCDMA	WCDMA B1 HSDPA CH10700 @ 22.7 dBm	592	mA
	WCDMA B1 HSUPA CH10700 @ 20.7 dBm	507	mA
	WCDMA B2 HSDPA CH9800 @ 22.4 dBm	548	mA
	WCDMA B2 HSUPA CH9800 @ 20.2 dBm	471	mA
	WCDMA B5 HSDPA CH4400 @ 22.6 dBm	602	mA
	WCDMA B5 HSUPA CH4400 @ 20.0 dBm	494	mA
	WCDMA B8 HSDPA CH3013 @ 22.4 dBm	530	mA
	WCDMA B8 HSUPA CH3013 @ 20.9 dBm	481	mA
LTE	LTE-FDD B1 CH300 @ 23.0 dBm	681	mA
	LTE-FDD B2 CH900 @ 22.8 dBm	649	mA
	LTE-FDD B3 CH1575 @ 22.8 dBm	670	mA
	LTE-FDD B4 CH2175 @ 22.9 dBm	687	mA
	LTE-FDD B5 CH2525 @ 23.6 dBm	706	mA
	LTE-FDD B7 CH3100 @ 23.3 dBm	1116	mA
	LTE-FDD B8 CH3625 @ 23.3 dBm	626	mA
	LTE-FDD B20 CH6300 @ 23.6dBm	670	mA
	LTE-FDD B28 CH9460 @ 23.7 dBm	668	mA
	LTE-FDD B66 CH38000 @ 22.8 dBm	636	mA
	LTE-TDD B38 CH38000 @ 23.1 dBm	388	mA
	LTE-TDD B40 CH39150 @ 23.4 dBm	551	mA
	LTE-TDD B41 CH40620 @ 23.0 dBm	388	mA
5G NR	5G NR-FDD n1 CH427000 @ 22.9 dBm	1084	mA
	5G NR-FDD n1 CH428000 @ 22.7 dBm	1086	mA
	5G NR-FDD n1 CH429000 @ 22.9 dBm	1098	mA
	5G NR-FDD n3 CH364000 @ 22.6 dBm	976.	mA

	5G NR-FDD n3 CH368500 @ 22.5 dBm	1001	mA
	5G NR-FDD n3 CH373000 @ 22.8 dBm	1033	mA
	5G NR FDD n5 CH175800 @ 22.7 dBm	899	mA
	5G NR FDD n5 CH176300 @ 22.5 dBm	916	mA
	5G NR FDD n5 CH176800 @ 22.6 dBm	924	mA
	5G NR-FDD n7 CH526000 @ 23.3 dBm	1178	mA
	5G NR-FDD n7 CH531000 @ 23.2 dBm	1138	mA
	5G NR-FDD n7 CH536000 @ 23.1 dBm	1226	mA
	5G NR-FDD n8 CH187000 @ 22.4 dBm	909	mA
	5G NR-FDD n8 CH188500 @ 22.0 dBm	954	mA
	5G NR-FDD n8 CH190000 @ 22.9 dBm	868	mA
	5G NR-FDD n20 CH160200 @ 23.0 dBm	922	mA
	5G NR-FDD n20 CH161200 @ 23.3 dBm	922	mA
	5G NR-FDD n20 CH162200 @ 23.2 dBm	913	mA
	5G NR-FDD n28 CH154600 @ 23.1 dBm	976	mA
	5G NR-FDD n28 CH157600 @ 23.3 dBm	992	mA
	5G NR-FDD n28 CH157600 @ 23.3 dBm	992	mA
	5G NR-TDD n38 CH518000 @ 24.3 dBm	577	mA
	5G NR-TDD n38 CH519000 @ 24.3 dBm	574	mA
	5G NR-TDD n38 CH520000 @ 24.3 dBm	576	mA
	5G NR-TDD n40 CH468000 @ 23.9 dBm	609	mA
	5G NR-TDD n40 CH470000 @ 23.9 dBm	604	mA
	5G NR-TDD n40 CH472000 @ 24.1 dBm	602	mA
	5G NR-TDD n41 CH509202 @ 26.7 dBm	736.	mA
	5G NR-TDD n41 CH518598 @ 26.8 dBm	706	mA
	5G NR-TDD n41 CH528000 @ 26.6 dBm	739	mA

	5G NR-FDD n66 CH426000 @ 24.3 dBm	1129	mA
	5G NR-FDD n66 CH429000 @ 24.2 dBm	1153	mA
	5G NR-FDD n66 CH434000 @ 24.4 dBm	1146	mA
	5G NR-TDD n77 CH623334 @ 26.6 dBm	663	mA
	5G NR-TDD n77 CH650000 @ 26.6 dBm	659	mA
	5G NR-TDD n77 CH676666 @ 26.5 dBm	662	mA
	5G NR-TDD n78 CH623334 @ 26.7 dBm	663	mA
	5G NR-TDD n78 CH636666 @ 27.1 dBm	663	mA
	5G NR-TDD n78 CH650000 @ 27.1 dBm	656	mA
WCDMA voice call	WCDMA B1 CH10700 @ 23.3 dBm	619.	mA
	WCDMA B2 CH9800 @ 23.3 dBm	583	mA
	WCDMA B5 CH4400 @ 23.5 dBm	660	mA
	WCDMA B8 CH3013 @ 23.7 dBm	589.	mA

Table 54: RG500U-LA Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	85	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	4.46	mA
	AT+CFUN=4 (USB disconnected)	4.59	mA
	WCDMA PF = 64 (USB disconnected)	6.2	mA
	LTE-FDD PF = 64 (USB disconnected)	6.73	mA
	LTE-TDD PF = 64 (USB disconnected)	6.81	mA
	5G NR-FDD PF = 64 (USB disconnected)	16.82	mA
	5G NR-TDD PF = 64 (USB disconnected)	15.75	mA
Idle state	WCDMA PF = 64 (USB disconnected)	32.16	mA
	WCDMA PF = 64 (USB connected)	59.94	mA

	LTE-FDD PF = 64 (USB disconnected)	32.18	mA
	LTE-FDD PF = 64 (USB connected)	60.15	mA
	LTE-TDD PF = 64 (USB disconnected)	32.38	mA
	LTE-TDD PF = 64 (USB connected)	60.53	mA
	5G NR-FDD PF = 64 (USB disconnected)	43.21	mA
	5G NR-FDD PF = 64 (USB connected)	71.31	mA
	5G NR-TDD PF = 64 (USB disconnected)	41.94	mA
	5G NR-TDD PF = 64 (USB connected)	69.58	mA
WCDMA	WCDMA B2 HSDPA CH9800 @ 21.9 dBm	554	mA
	WCDMA B2 HSUPA CH9800 @ 19.8 dBm	481	mA
	WCDMA B4 HSDPA CH1675 @ 22.3 dBm	630	mA
	WCDMA B4 HSUPA CH1675 @ 21.6 dBm	605	mA
	WCDMA B5 HSDPA CH4400 @ 21.9 dBm	529	mA
	WCDMA B5 HSUPA CH4400 @ 19.6 dBm	452	mA
LTE	LTE-FDD B2 CH900 @ 23.3 dBm	687	mA
	LTE-FDD B4 CH2175 @ 23.8 dBm	659	mA
	LTE-FDD B5 CH2525 @ 23.5 dBm	640	mA
	LTE-FDD B7 CH3100 @ 23.0 dBm	671	mA
	LTE-FDD B8 CH3625 @ 23.5 dBm	670	mA
	LTE-FDD B26 CH8865 @ 23.5 dBm	671	mA
	LTE-FDD B28 CH9460 @ 23.3 dBm	689	mA
	LTE-FDD B66 CH66886 @ 23.6 dBm	651	mA
	LTE-TDD B38 CH38000 @ 23.3 dBm	401	mA
	LTE-TDD B40 CH39150 @ 23.4 dBm	434	mA
	LTE-FDD B71 CH68786 @ 22.9 dBm	610	mA
5G NR	5G NR-FDD n2 CH388000 @ 23.4 dBm	972	mA

	5G NR-FDD n2 CH392000 @ 23.2 dBm	1010	mA
	5G NR-FDD n2 CH396000 @ 23.5 dBm	1025	mA
	5G NR FDD n5 CH175800 @ 22.8 dBm	871	mA
	5G NR FDD n5 CH176300 @ 23.6 dBm	864	mA
	5G NR FDD n5 CH176800 @ 23.6 dBm	871	mA
	5G NR-FDD n7 CH526000 @ 22.3 dBm	1105	mA
	5G NR-FDD n7 CH531000 @ 22.2 dBm	1147	mA
	5G NR-FDD n7 CH536000 @ 22.2 dBm	1137	mA
	5G NR-FDD n8 CH187000 @ 22.9 dBm	842	mA
	5G NR-FDD n8 CH188500 @ 22.8 dBm	857	mA
	5G NR-FDD n8 CH190000 @ 22.6 dBm	887	mA
	5G NR-FDD n28 CH153600 @ 23.3 dBm	920	mA
	5G NR-FDD n28 CH156600 @ 22.5 dBm	914	mA
	5G NR-FDD n28 CH158600 @ 22.9 dBm	970	mA
	5G NR-TDD n38 CH516000 @ 24.0 dBm	575	mA
	5G NR-TDD n38 CH519000 @ 23.9 dBm	570	mA
	5G NR-TDD n38 CH522000 @ 23.8 dBm	570	mA
	5G NR-TDD n40 CH462000 @ 23.1 dBm	600	mA
	5G NR-TDD n40 CH470000 @ 23.2 dBm	595	mA
	5G NR-TDD n40 CH478000 @ 23.2 dBm	590	mA
	5G NR-FDD n66 CH424000 @ 23.4 dBm	1028	mA
	5G NR-FDD n66 CH429000 @ 23.5 dBm	1033	mA
	5G NR-FDD n66 CH434000 @ 23.4 dBm	1046	mA
	5G NR-FDD n71 CH125400 @ 23.2 dBm	818	mA
	5G NR-FDD n71 CH126900 @ 23.1 dBm	826	mA
	5G NR-FDD n71 CH128400 @ 23.4 dBm	799	mA

	5G NR-TDD n78 CH620668 @ 25.3 dBm	674	mA
	5G NR-TDD n78 CH636666 @ 25.5 dBm	657	mA
	5G NR-TDD n78 CH652666 @ 25.5 dBm	654	mA
WCDMA voice call	WCDMA B2 CH9800 @ 23.3 dBm	616	mA
	WCDMA B4 CH1675 @ 22.3 dBm	625	mA
	WCDMA B5 CH4400 @ 23.2 dBm	584	mA

Table 55: RG500U-JO Power Consumption

Description	Condition	Typ.	Unit
OFF state	Power down	89.8	μA
Sleep state	**AT+CFUN=0** (USB disconnected)	4.75	mA
	AT+CFUN=4 (USB disconnected)	4.88	mA
	5G NR-TDD PF = 64 (USB disconnected)	15.26	mA
	5G NR-TDD PF = 64 (USB connected)	NA	mA
Idle state	5G NR-TDD PF = 64 (USB disconnected)	43.7	mA
	5G NR-TDD PF = 64 (USB connected)	69	mA
5G NR	5G NR-TDD n78 CH623334 @ 26.7 dBm	663	mA
	5G NR-TDD n78 CH636666 @ 27.1 dBm	663	mA
	5G NR-TDD n78 CH650000 @ 27.1 dBm	656	mA

5.6. Tx Power

Table 56: RG500U-CN RF Output Power

Mode	Frequency Band	Max. RF Output Power	Min. RF Output Power
WCDMA	B1/B2/B5/B8	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	B1/B2/B3/B5/B7/B8/B20/B28/ B34/B38/B39/B40/B41	23 dBm ±2 dB (Class 3)	< -40 dBm
	B41 HPUE	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	n1	23 dBm ±2 dB (Class 3)	< -40 dBm [9]
	n28	23 dBm +2/-2.5 dB (Class 3)	< -40 dBm [9]
	n41/n77/n78/n79	23 dBm +2/-3 dB (Class 3)	< -40 dBm [9]
	n41/n78/n79 HPUE	26 dBm +2/-3 dB (Class 2)	< -40 dBm [9]

Table 57: RG500U-EA RF Output Power

Mode	Frequency Band	Max. RF Output Power	Min. RF Output Power
WCDMA	B1/B2/B5/B8	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	B1/B2/B3/B4/B5/B7/B8/B20/28/ B38/B40/B41/B66	23 dBm ±2 dB (Class 3)	< -40 dBm
	B41 HPUE	26 dBm ±2 dB (Class 2)	< -40 dBm
5G NR	n1/n3/n5/n7/n8/n20/n38/n40/ n41/n66	23 dBm ±2 dB (Class 3)	< -40 dBm [9]
	n28	23 dBm +2/-2.5 dB (Class 3)	< -40 dBm [9]
	n77/n78	23 dBm +2/-3 dB (Class 3)	< -40 dBm [9]
	n41/n77/n78 HPUE	26 dBm +2/-3 dB (Class 2)	< -40 dBm [9]

[9] For 5G NR bands, different channel bandwidth has different minimum power standard. For details, see ***Clause 6.3.1*** in *TS 38.101-1 [2].*

Table 58: RG500U-EB RF Output Power

Mode	Frequency Band	Max. RF Output Power	Min. RF Output Power
WCDMA	B1/B2/B5/B8	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	B1/B2/B3/B4/B5/B7/B8/B20/28/B38/B40/B41/B66	23 dBm ±2 dB (Class 3)	< -40 dBm
5G NR	n1/n3/n5/n7/n8/n20/n38/n40/n41/n66	23 dBm ±2 dB (Class 3)	< -40 dBm [9]
	n28	23 dBm +2/-2.5 dB (Class 3)	< -40 dBm [9]
	n77/n78	23 dBm +2/-3 dB (Class 3)	< -40 dBm [9]
	n41/n77/n78 HPUE	26 dBm +2/-3 dB (Class 2)	< -40 dBm [9]

Table 59: RG500U-LA RF Output Power

Mode	Frequency Band	Max. RF Output Power	Min. RF Output Power
WCDMA	B2/B4/B5	23 dBm ±2 dB (Class 3)	< -50 dBm
LTE	B2/B4/B5/B7/B8/B26/28/B38/B40/B66/B71	23 dBm ±2 dB (Class 3)	< -40 dBm
5G NR	n2/n5/n7/n8/n38/n40/n66	23 dBm ±2 dB (Class 3)	< -40 dBm [9]
	n28/n71	23 dBm +2/-2.5 dB (Class 3)	< -40 dBm [9]
	n78	23 dBm +2/-3 dB (Class 3)	< -40 dBm [9]
	n78 HPUE	26 dBm +2/-3 dB (Class 2)	< -40 dBm [9]

Table 60: RG500U-JO RF Output Power

Mode	Frequency Band	Max. RF Output Power	Min. RF Output Power
5G NR	n78	23 dBm +2/-3 dB (Class 3)	< -40 dBm [9]
	n78 HPUE	26 dBm +2/-3 dB (Class 2)	< -40 dBm [9]

5.7. Rx Sensitivity

Table 61: RG500U-CN Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Band	RF Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO [10]	
WCDMA B1	-109.0	-110.0	-112	-106.7
WCDMA B2	-108.0	-108.5	-111	-104.7
WCDMA B5	-108.5	-111.0	-112.5	-104.7
WCDMA B8	-108.5	-109.5-	-112	-103.7
LTE-FDD B1 (10 MHz)	-98.0	-98.0	-101.5	-96.3
LTE-FDD B2 (10 MHz)	-97.5	-97.0	-101.0	-94.3
LTE-FDD B3 (10 MHz)	-97.0	-97.5	-101.0	-93.3
LTE-FDD B5 (10 MHz)	-97.5	-99.5	-102.0	-94.3
LTE-FDD B7 (10 MHz)	-95.5	-97.0	-100.0	-94.3
LTE-FDD B8 (10 MHz)	-97.5	-99.0	-101.5	-93.3
LTE-FDD B20 (10 MHz)	-98.0	-97.5	-101.0	-93.3
LTE-FDD B28 (10 MHz)	-97.5	-98.5	101.0	-94.8
LTE-TDD B34 (10 MHz)	-97.5	-96.5	-100.5	-96.3
LTE-TDD B38 (10 MHz)	-96.5	-97.5	-100.5	-96.3
LTE-TDD B39 (10 MHz)	-98.5	-97.5	-101.5	-96.3
LTE-TDD B40 (10 MHz)	-97.0	-96.0	-100.0	-96.3
LTE-TDD B41 (10 MHz)	-96.5	-96.5	-100.0	-94.3
5G NR FDD n1 (5 MHz)	-99.5	-100.0	-107	-102
5G NR FDD n28 (5 MHz)	-96.5	-97.3	-100.0	-97.8

[10] For the SIMO receiving sensitivity, WCDMA, LTE and 5G n28 bands are tested with 2 Rx antennas, and 5G n1/n41/n77/n78/n79 bands are tested with 4 Rx antennas.

5G NR TDD n41 (100 MHz)	-87.0	-88.1	-92.5	-86.7
5G NR TDD n77 (100 MHz)	-86.5	-87.0	-93.5	-86.3
5G NR TDD n78 (100 MHz)	-86.5	-88.2	-92.5	-86.8
5G NR TDD n79 (100 MHz)	-87.5	-88.6	-94.5	-86.8

Table 62: RG500U-EA Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Band	RF Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO [11]	
WCDMA B1	-109.2	-109.4	-112.1	-106.7
WCDMA B2	-108.6	-108.3	-111.3	-104.7
WCDMA B5	-109.7	-109.5	-112.6	-104.7
WCDMA B8	-108.8	-109.9	-112.5	-103.7
LTE-FDD B1 (10 MHz)	-97.3	-97.1	-100.2	-96.3
LTE-FDD B2 (10 MHz)	-97.2	-97.1	-.100.1	-94.3
LTE-FDD B3 (10 MHz)	-98.0	-98.5	-101.2	-93.3
LTE-FDD B4 (10 MHz)	-96.9	-95.5	-99.3	-96.3
LTE-FDD B5 (10 MHz)	-97.7	-97.7	-100.6	-94.3
LTE-FDD B7 (10 MHz)	-96.2	-97.8	-100.1	-94.3
LTE-FDD B8 (10 MHz)	-96.9	-98.0	-100.4	-93.3
LTE-FDD B20 (10 MHz)	-98.2	-97.5	-100.9	-93.3
LTE-FDD B28 (10 MHz)	-97.6	-97.9	-100.7	-94.8
LTE-FDD B66 (10 MHz)	-96.7	-95.6	-99.2	-95.8
LTE-TDD B38 (10 MHz)	-96.7	-96.5	-99.5	-96.3
LTE-TDD B40 (10 MHz)	-97.2	-97.5	-100.3	-96.3

[11] For the SIMO receiving sensitivity, WCDMA, LTE and 5G n5/n8/n20/n28/n71 bands are tested with 2 Rx antennas, and 5G n1/n3/n7/n38/n40/n41/n66/n77/n78/n79 bands are tested with 4 Rx antennas.

LTE-TDD B41 (10 MHz)	-96.4	-96.3	-99.3	-94.3
5G NR FDD n1 (20 MHz)	-94.0	-95.7	-99.6	-95.8
5G NR FDD n3 (20 MHz)	-94.9	-96.0	-99.1	-92.8
5G NR FDD n5 (20MHz)	-94.4	-93.3	-96.6	-90.1
5G NR FDD n7 (20 MHz)	-92.7	-94.4	-99.3	-93.8
5G NR FDD n8 (20 MHz)	-95.0	-93.6	-96.9	-89.3
5G NR FDD n20 (20 MHz)	-94.0	-94.9	-97.0	-89.1
5G NR FDD n28 (20 MHz)	-95.4	-95.3	-97.7	-90.1
5G NR TDD n38 (40 MHz)	-90.5	-92.1	-96.6	-92.7
5G NR TDD n40 (80 MHz)	-88.4	-89.0	-93.2	-89.6
5G NR FDD n66 (20 MHz)	-94.2	-95.8	-99.6	-95.3
5G NR TDD n41 (100 MHz)	-86.2	-87.2	-91.5	-86.7
5G NR TDD n77 (100 MHz)	-87.7	-85.6	-92.1	-86.3
5G NR TDD n78 (100 MHz)	-87.8	-85.7	-92.3	-86.8

Table 63: RG500U-EB Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Band	RF Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO [12]	
WCDMA B1	-109.2	-109.6	-112.1	-106.7
WCDMA B2	-108.5	-108.5	-111.3	-104.7
WCDMA B5	-109.5	-110.7	-113.0	-104.7
WCDMA B8	-108.8	-110.4	-112.6	-103.7
LTE-FDD B1 (10 MHz)	-97.0	-97.3	-100.3	-96.3
LTE-FDD B2 (10 MHz)	-97.0	-97.3	-100.1	-94.3
LTE-FDD B3 (10 MHz)	-98.1	-98.6	-101.2	-93.3

[12] For the SIMO receiving sensitivity, WCDMA, LTE and 5G n5/n8/n20 bands are tested with 2 Rx antennas, and 5G n1/n3/n7n28//n38/n40/n41/n66/n77/n78 bands are tested with 4 Rx antennas.

LTE-FDD B4 (10 MHz)	-96.6	-96.6	-99.5	-96.3
LTE-FDD B5 (10 MHz)	-97.5	-98.8	-101.2	-94.3
LTE-FDD B7 (10 MHz)	-96.1	-97.6	-99.7	-94.3
LTE-FDD B8 (10 MHz)	-96.7	-98.7	-100.7	-93.3
LTE-FDD B20 (10 MHz)	-98.1	-97.6	-100.8	-93.3
LTE-FDD B28 (10 MHz)	-97.7	-97.9	-100.7	-94.8
LTE-FDD B66 (10 MHz)	-96.4	-96.3	-99.3	-95.8
LTE-TDD B38 (10 MHz)	-96.1	-96.5	-99.2	-96.3
LTE-TDD B40 (10 MHz)	-96.0	-97.2	-99.5	-96.3
LTE-TDD B41 (10 MHz)	-95.8	-96.3	-98.8	-94.3
5G NR FDD n1 (20 MHz)	-94.2	-95.8	-99.9	-95.8
5G NR FDD n3 (20 MHz)	-95.0	-96.2	-99.4	-92.8
5G NR FDD n5 (20MHz)	-94.4	-94.1	-96.7	-90.1
5G NR FDD n7 (20 MHz)	-93.1	-94.7	-99.6	-93.8
5G NR FDD n8 (20 MHz)	-94.7	-94.0	-96.6	-89.3
5G NR FDD n20 (20 MHz)	-92.9	-94.7	-96.4	-89.1
5G NR FDD n28 (20 MHz)	-95.1	-94.9	-99.9	-90.1
5G NR TDD n38 (40 MHz)	-91.3	-91.9	-96.1	-92.7
5G NR TDD n40 (80 MHz)	-88.6	-89.4	-93.3	-89.6
5G NR TDD n41 (100 MHz)	-86.3	-87.0	-91.3	-86.7
5G NR FDD n66 (20 MHz)	-94.3	-95.8	-99.8	-95.3
5G NR TDD n77 (100 MHz)	-88.0	-86.9	-92.7	-86.3
5G NR TDD n78 (100 MHz)	-88.3	-86.7	-93.0	-86.8

Table 64: RG500U-LA Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Band	RF Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO [13]	
WCDMA B2	-110.3	-110.4	-113.8	-104.7
WCDMA B4	-109.1	-108.9	-112.3	-106.7
WCDMA B5	-109.0	-110.2	-113.1	-104.7
LTE-FDD B2 (10 MHz)	-98.3	-98.5	-101.4	-94.3
LTE-FDD B4 (10 MHz)	-97.2	-97.3	-100.3	-96.3
LTE-FDD B5 (10 MHz)	-97.4	-98.6	-101.0	-94.3
LTE-FDD B7 (10 MHz)	-96.5	-97.4	-99.2	-94.3
LTE-FDD B8 (10 MHz)	-96.5	-98.4	-100.5	-93.3
LTE-FDD B26 (10 MHz)	-97.3	-98.5	-100.9	-93.3
LTE-FDD B28 (10 MHz)	-97.4	-97.6	-100.5	-94.8
LTE-FDD B66 (10 MHz)	-97.2	-97.3	-100.3	-96.5
LTE-TDD B38 (10 MHz)	-96.4	-96.3	-98.4	-96.3
LTE-TDD B40 (10 MHz)	-96.9	-97.2	-100.1	-96.3
LTE-FDD B71 (10 MHz)	-97.8	-96.7	-100.3	-93.5
5G NR FDD n2 (20 MHz)	-94.2	-95.3	-99.5	-93.8
5G NR FDD n5 (20MHz)	-93.1	-94.1	-96.0	-90.1
5G NR FDD n7 (20 MHz)	-92.7	-94.1	-99.2	-93.8
5G NR FDD n8 (20 MHz)	-93.8	-93.9	-96.4	-89.3
5G NR FDD n28 (20 MHz)	-94.1	-94.0	-98.5	-77.8
5G NR TDD n38 (40 MHz)	-90.5	-91.9	-96.5	-92.7
5G NR TDD n40 (80 MHz)	-88.0	-88.8	-93.0	-89.6

[13] For the SIMO receiving sensitivity, WCDMA, LTE and 5G n5/n8/n28/n71 bands are tested with 2 Rx antennas, and 5G n2/n7/n38/n40/n41/n66/n77/n78 bands are tested with 4 Rx antennas.

5G NR FDD n66 (20 MHz)	-94.2	-95.3	-99.5	-95.3
5G NR FDD n71 (20 MHz)	-93.2	-92.4	-95.3	-85.3
5G NR TDD n78 (100 MHz)	-88.1	-85.3	-92.3	-86.8

Table 65: RG500U-JO Conducted RF Receiving Sensitivity (Unit: dBm)

Frequency Band	RF Receiving Sensitivity (Typ.)			3GPP (SIMO)
	Primary	Diversity	SIMO [14]	
5G NR TDD n78 (100 MHz)	-88.1	-86.7	-92.5	-86.8

5.8. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 66: Electrostatic Discharge Characteristics (Temperature: 25–30 °C, Humidity: 40 ±5 %)

Tested Interface	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interfaces	±4	±8	kV
Other Interfaces	±0.5	±1	kV

[14] For the SIMO receiving sensitivity, n78 bands are tested with 4 Rx antennas.

5.9. Thermal Dissipation

The module offers the best performance when all internal IC chips are working within their operating temperatures. When the IC chip reaches or exceeds the maximum junction temperature, the module may still work but the performance and function (such as RF output power, data rate.) will be affected to a certain extent. Therefore, the thermal design should be maximally optimized to ensure all internal IC chips always work within the recommended operating temperature range.

The following principles for thermal consideration are provided for reference:

- Keep the module away from heat sources on your PCB, especially high-power components such as processor, power amplifier, and power supply.
- Maintain the integrity of the PCB copper layer and drill as many thermal vias as possible.
- Follow the principles below when the heatsink is necessary:
  - Do not place large size components in the area where the module is mounted on your PCB to reserve enough place for heatsink installation.
  - Attach the heatsink to the shielding cover of the module; In general, the base plate area of the heatsink should be larger than the module area to cover the module completely;
  - Choose the heatsink with adequate fins to dissipate heat;
  - Choose a TIM (Thermal Interface Material) with high thermal conductivity, good softness and good wettability and place it between the heatsink and the module;
  - Fasten the heatsink with four screws to ensure that it is in close contact with the module to prevent the heatsink from falling off during the drop, vibration test, or transportation.

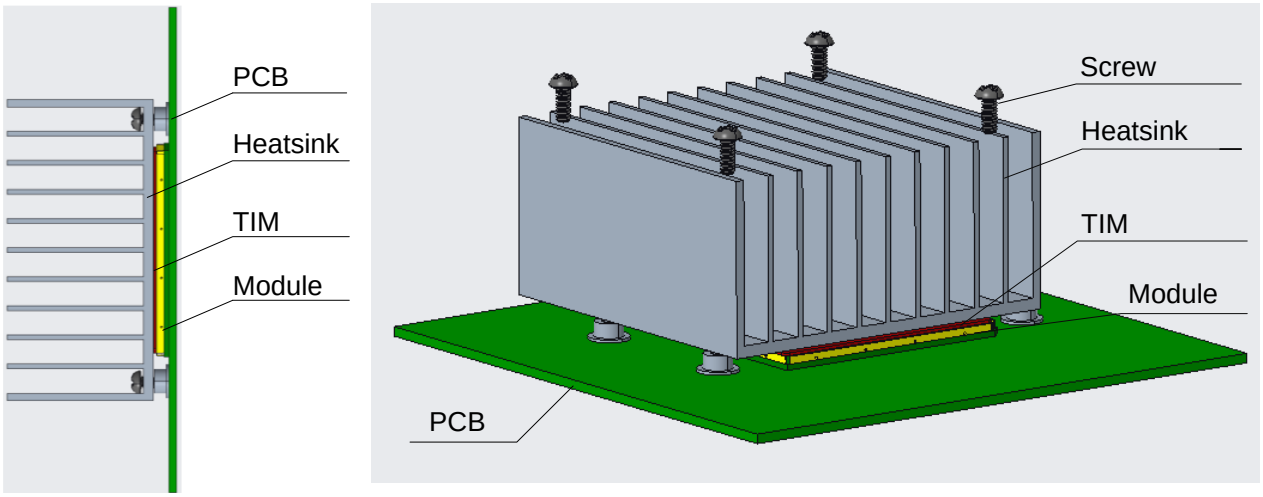


Figure 49: Placement and Fixing of the Heatsink

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm, and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

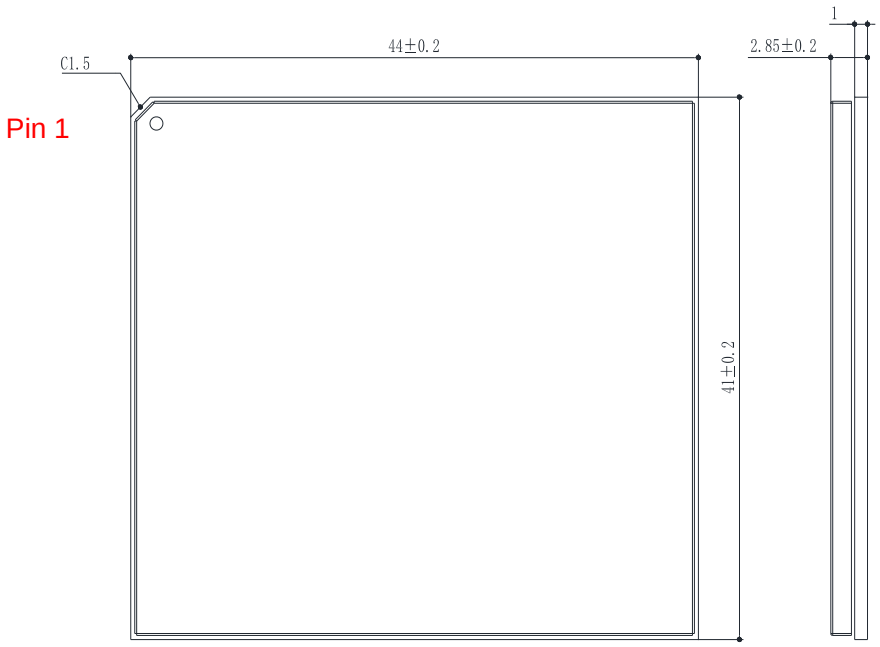


Figure 50: Module Top and Side Dimensions

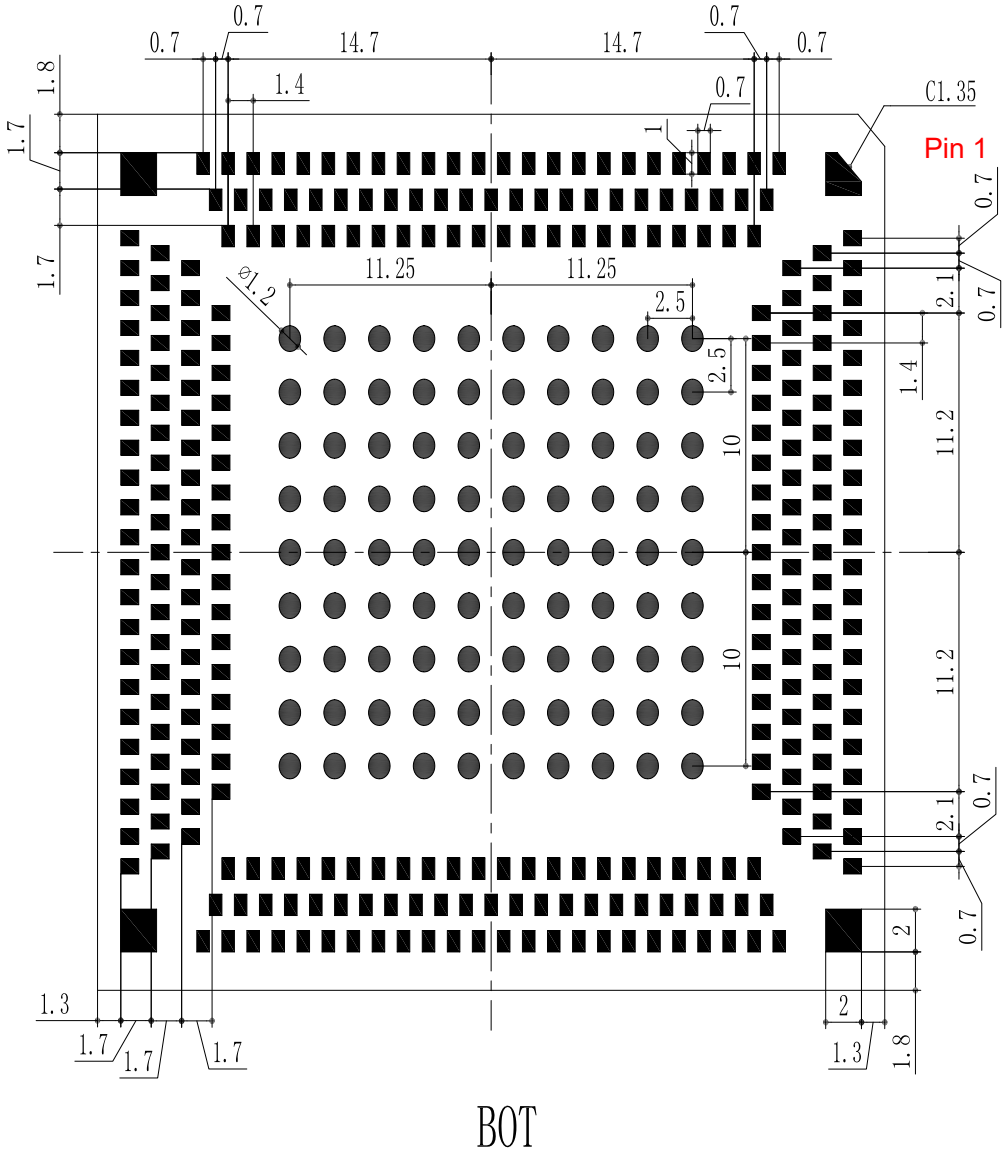


Figure 51: Module Bottom Dimension (Bottom View)

NOTE

The module's coplanarity standard: ≤ 0.13 mm.

6.2. Recommended Footprint

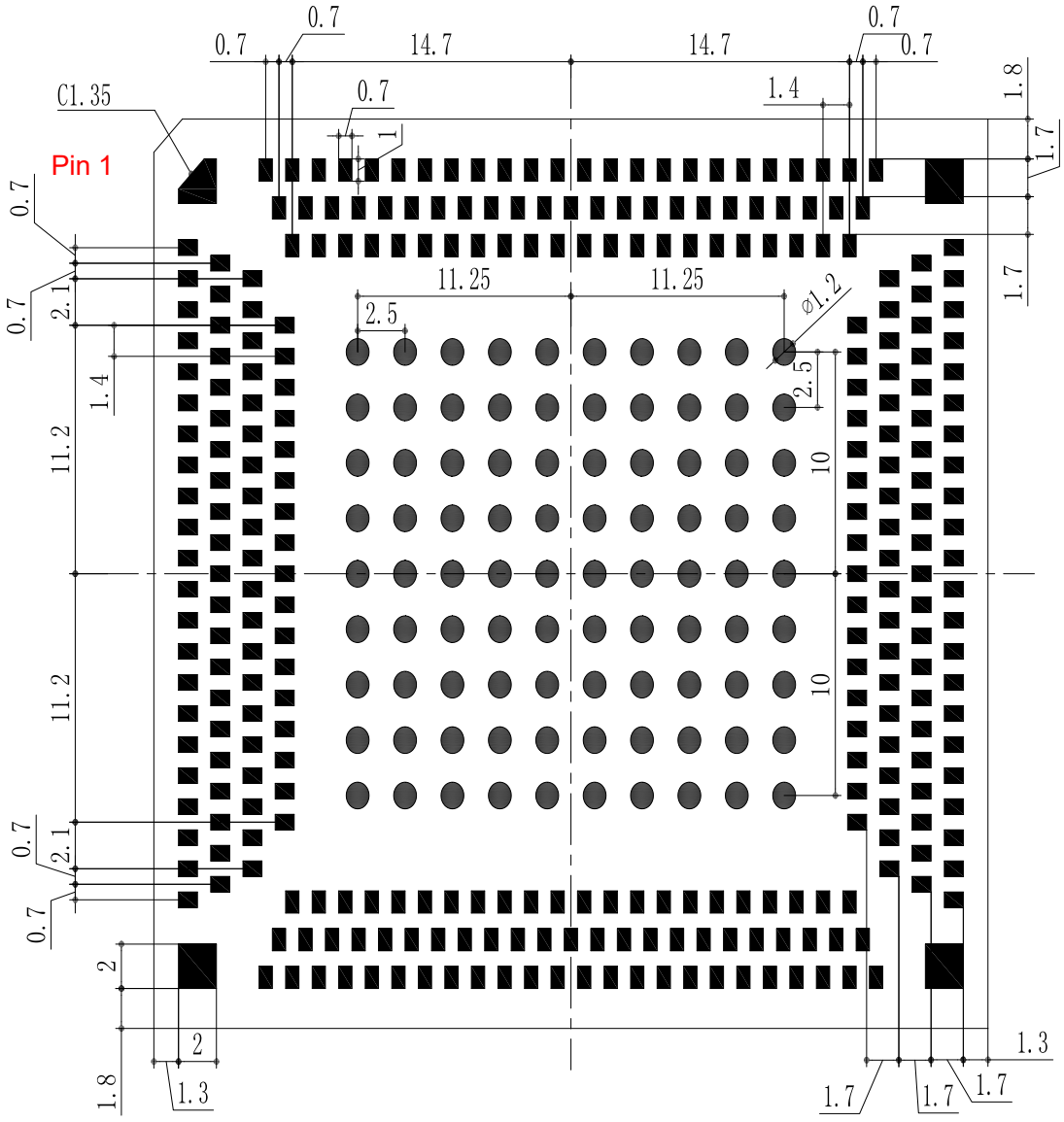


Figure 52: Recommended Footprint

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. To keep the reliability of the mounting and soldering, keep the motherboard thickness as at least 1.2 mm.

6.3. Top and Bottom Views

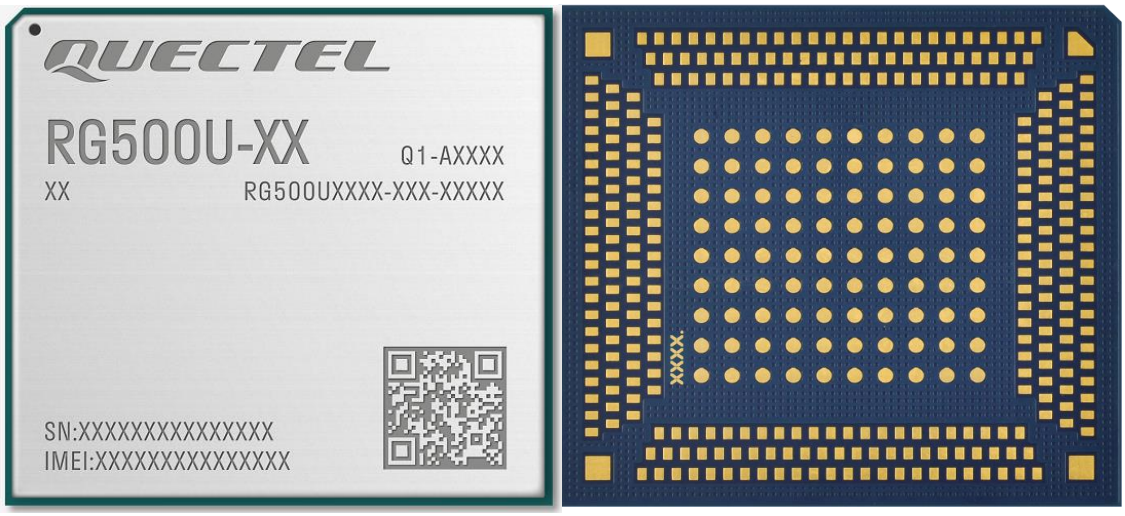


Figure 53: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [15] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[15] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [5]***.

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

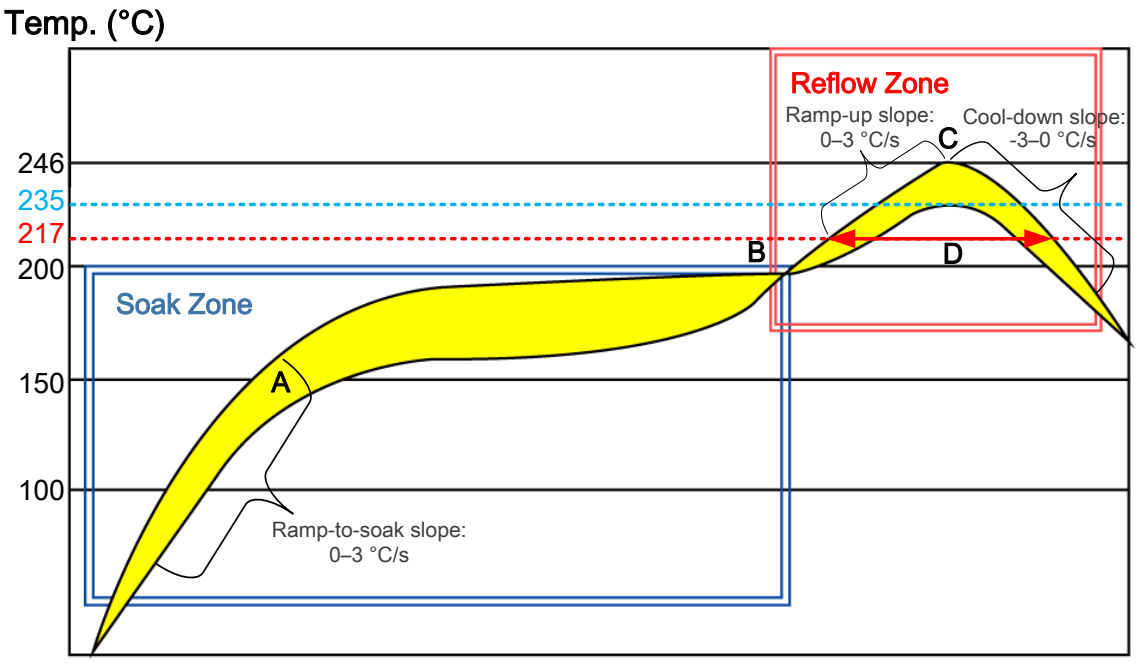


Figure 54: Recommended Reflow Soldering Thermal Profile

Table 67: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak Slope	0–3 °C/s
Soak Time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up Slope	0–3 °C/s
Reflow Time (D: over 217°C)	40–70 s
Max. Temperature	235–246 °C
Cool-down Slope	-3–0 °C/s (refer to NOTE 1 below)
Reflow Cycle	
Max. Reflow Cycle	1

NOTE

1. For large-form-factor modules (that is, minimum side length ≥ 30 mm) with two-piece shielding covers, use a cool-down slope of -1–0 °C/s to reduce the thermal stress, preventing cover lifting. Due to the large-size form factors of such modules, an excessive temperature change may cause excessive thermal deformation of the metal shielding frame and cover. Therefore, reduce the ramp-up and cool-down slopes in the liquid phase of the solder paste to avoid excessive temperature change. If possible, choose a reflow oven with more than 10 temperature zones during production so that there are more temperature zones to set up to meet the optimal temperature curve.
2. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
3. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
4. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
5. Avoid using materials that contain mercury (Hg), such as adhesives, for module processing, even if the materials are RoHS compliant and their mercury content is below 1000 ppm (0.1 %).
6. Corrosive gases may corrode the electronic components inside the module, affecting their reliability and performance, and potentially leading to a shortened service life that fails to meet the designed lifespan. Therefore, do not store or use unprotected modules in environments containing

corrosive gases such as hydrogen sulfide, sulfur dioxide, chlorine, and ammonia.

7. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [6]***.

7.3. Packaging Specification

This chapter outlines the key packaging parameters and processes. All figures below are for reference purposes only, as the actual appearance and structure of packaging materials may vary in delivery

The modules are packed in a tape and reel packaging as specified in the sub-chapters below.

7.3.1. Carrier Tape

Carrier tape dimensions are illustrated in the following figure and table:

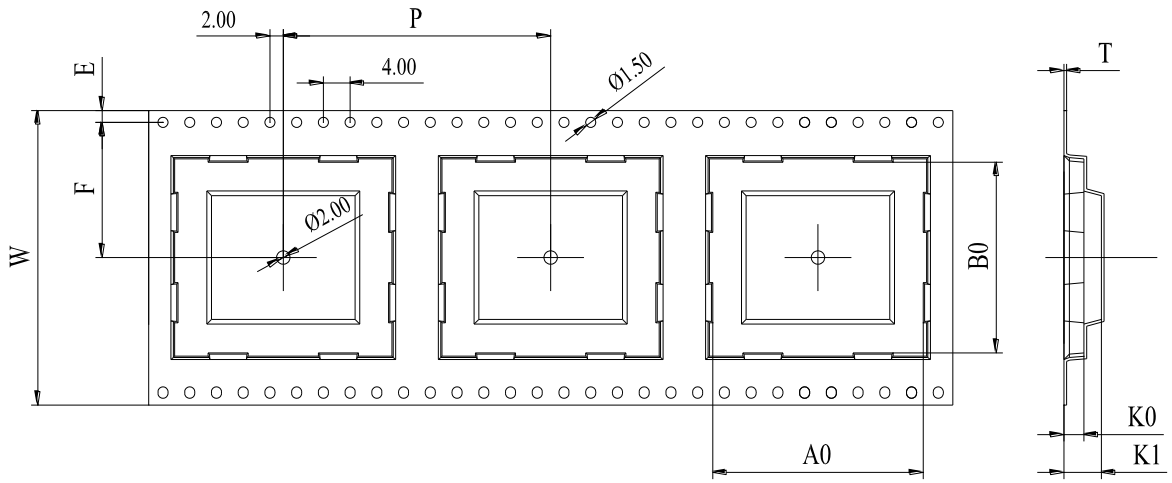


Figure 55: Carrier Tape Dimension Drawing

Table 68: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
72	56	0.4	44.7	41.7	4.2	5.2	34.2	1.75

7.3.2. Plastic Reel

Plastic reel dimensions are illustrated in the following figure and table:

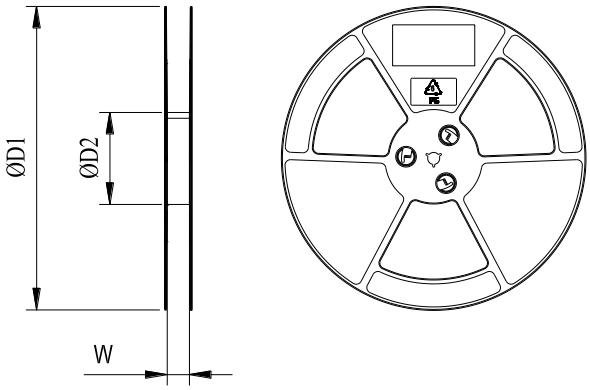


Figure 56: Plastic Reel Dimension Drawing

Table 69: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
380	180	72.5

7.3.3. Mounting Direction

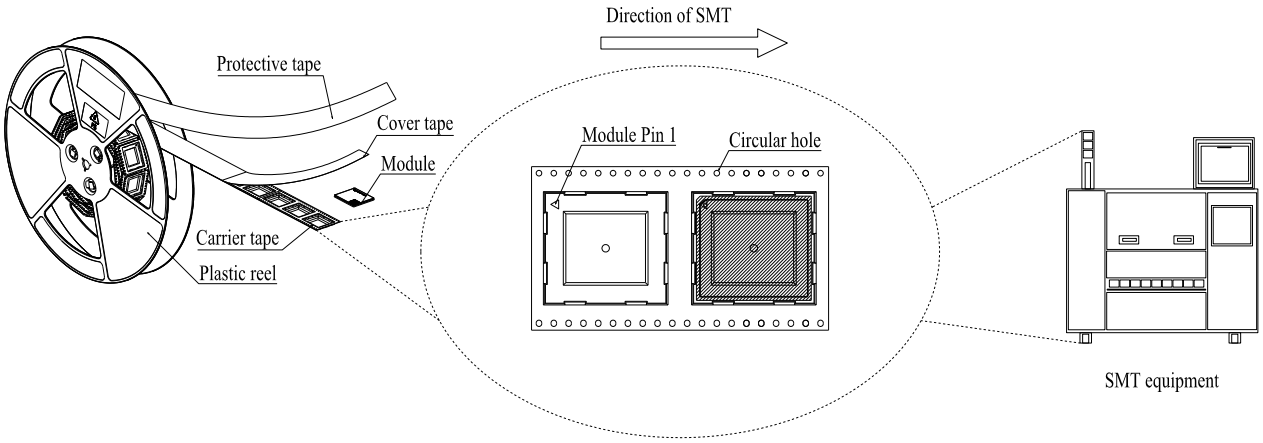
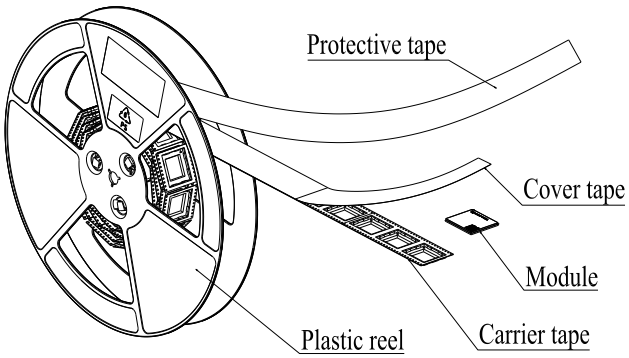


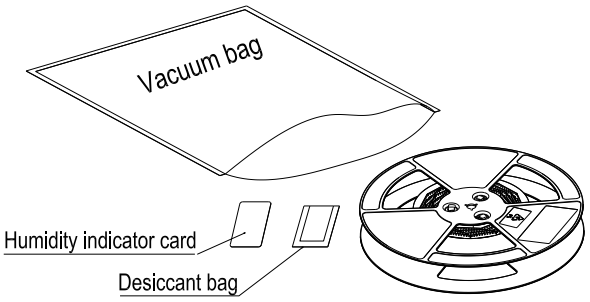
Figure 57: Mounting Direction

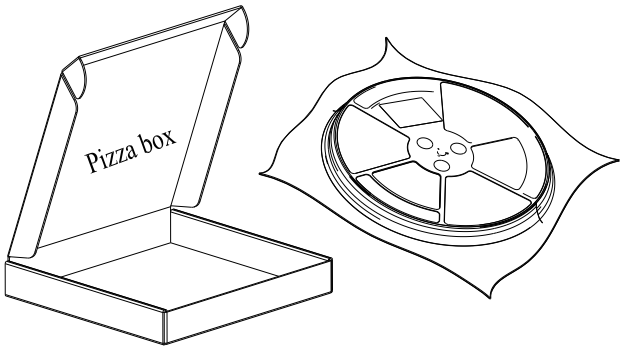
7.3.4. Packaging Process



Place the modules onto the carrier tape cavity and cover them securely with cover tape. Wind the heat-sealed carrier tape onto a plastic reel and apply a protective tape for additional protection. 1 plastic reel can load 200 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag into a vacuum bag, and vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put the 4 packaged pizza boxes into 1 carton and seal it. 1 carton can pack 800 modules.

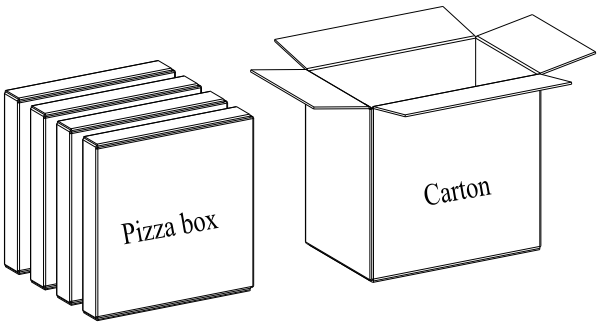


Figure 58: Packaging Process

8 Appendix References

Table 70: Related Documents

Document Name
[1] Quectel_RG500U_Series_CA&EN-DC_Features
[2] Quectel_RG200U&RG500U_Series_5G_EVB_User_Guide
[3] Quectel_RGx00U&RM500U_Series_AT_Commands_Manual
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_Stencil_Design_Requirements
[6] Quectel_Module_SMT_Application_Note

Table 71: Terms and Abbreviations

Abbreviation	Description
2CC	2 Component Carrier
3CC	3 Component Carrier
ADC	Analog-to-Digital Converter
APT	Average Power Tracking
bps	Bits Per Second
CA	Carrier Aggregation
CHAP	Challenge Handshake Authentication Protocol
CMUX	Connection Multiplexing
DL	Downlink

DRX	Discontinuous Reception
DTR	Data Terminal Ready
EP	PCI Express Endpoint Device
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance
FDD	Frequency Division Duplex
FTP	File Transfer Protocol
FTPS	FTP-over-SSL
GRFC	Generic RF Controls
HSDPA	High-Speed Down Link Packet Access
HSPA	High-Speed Packet Access
HSUPA	High-Speed Uplink Packet Access
HTTP	Hypertext Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
LTE	Long Term Evolution
MIMO	Multiple-Input Multiple-Output
MMS	Multimedia Messaging Service
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Level
NAND	NON-AND
NITZ	Network Identity and Time Zone
NTP	Network Time Protocol
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PCIe	Peripheral Component Interconnect Express

PDU	Protocol Data Unit
PING	Packet Internet Groper
PMU	Power Management Unit
PRX	Primary Receive
QAM	Quadrature Amplitude Modulation
QPSK	Quadrature Phase Shift Keying
RF	Radio Frequency
RTC	Real-Time Clock
SCS	Subcarrier Spacing
SIMO	Single Input Multiple Output
SMS	Short Message Service
SMTP	Simple Mail Transfer Protocol
SMTPS	Simple Mail Transfer Protocol Secure
SSL	Secure Sockets Layer
TCP	Transmission Control Protocol
TCXO	Temperature Compensated Crystal Oscillator
TDD	Time Division Duplexing
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UMTS	Universal Mobile Telecommunications System
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
USB	Universal Serial Bus
V_{IH}	High-level Input Voltage

V_{IL}	Low-level Input Voltage
Vmax	Maximum Voltage
Vmin	Minimum Voltage
Vnom	Nominal Voltage
V_{OH}	Low-level Output Voltage
V_{OL}	High-level Input Voltage
VSWR	Voltage Standing Wave Ratio
WCDMA	Wideband Code Division Multiple Access
WLAN	Wireless Local Area Network