An Approach of Nanomagnetic Logic Standard Cells Library

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***Abstract*—For several years, the most used technology was the CMOS(Complementary Metal-Oxide Semiconductor). Due to its physical limitations, other technologies have emerged such as QCA(Quantum-dot Cellular Automata) and NML(Nanomagnetic Logic). Yet, the current placement and routing algorithms are not effective for this technologies due to its clock scheme. Therefore to assist in the development of new placement and routing tools for NML we propose an approach of nanomagnetic logic standard cells library.**

***Index Terms*—component, formatting, style, styling, insert**

I. Introduction

The CMOS (Complementary Metal-Oxide Semiconductor) [1] is the industry-leading technology for the fabrication of semiconductor devices. Over the decades, miniaturization of transistors devices scaled exponentially until the leakage current increase in CMOS technology started imposing several barriers to this shrinking pace [2]. In this direction, researchers have looked for alternative beyond-CMOS technologies to improve the area, speed, and power consumption of future devices. Field-Coupled Nanocomputing (FCN) is a class of these candidate technologies, where there is no transistor and the computation occurs through field interactions among nanoscale basic cell arrangements [3].

In order to keep the progress and overcome the limitations that started to occur, the most studied technologies proposed were the Quantum dot cellular automata, QCA, which can be set in a very high clock rate, and presents low power consumption [4]. Another technology proposed so far can be defined as a magnetic implementation of QCA [3] which is known as Nanomagnetic Logic, NML. It operates at room temperature with ultra-low energy dissipation nanomagnets, presents majority logic and it is nonvolatile, allowing the performance of high density computing systems [5].

In this paper we present a standard cells library for NML, which is a significant precept for the development of more intricate circuits. Standard cells can be reused in many projects easing the designer's work in a certain way. In order to create a standard cells library for Nanomagnetic logic, a clocking scheme is essential. It must integrate with its technology and have a well defined circuit. Thus, for this library we are using the BANCS clock scheme, proposed in previous papers [6].

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An NML circuit relies on the dipolar connection between neighbor cells, and its geometries and positions define their interaction, since the nanomagnets interact through the magnetostatic dipolar coupling [3]. It performs boolean logic operations whereas the magnetic polarization is associated with binary logic states, '0' and '1' [7]. While implementing a circuit that works completely, the correct placement of the magnet is crucial to prevent adverse interactions between neighbor cells [5]. Designing NML circuits demands a simulator, since the physical implementation of huge devices is still an arduous task to achieve.

We organize this paper as follows: Section II provides a background of Nanomagnetic Logic technology while Section III discusses previous works related to NML research. Finally in Section V we present the results and in Section V we show the conclusions.

II. Background

In this section, we present a summary of Nanomagnetic Logic technology. We show how the nanomagnets interact to perform computation. We also show the importance of the clocking system and the standard cells.

A. Nanomagnetic Logic

NML technology is a different way of doing computing. The principle of this technology is in rectangular nanomagnetic of about 200 nm whose magnetic field of one magnet can influence another magnet. When the magnet is north up and south down it is represented with 0, otherwise, is represented with 1. This means that nml technology works in a binary way, which allows applying the computational principles.

When nanomagnets are placed and routed in a controlled manner, they can behave like wires or logic gates. Figure 1 show two possible ways to build wires using NML technology and Figure 2 show a majority gate, a elementary nml cell. This gate can behave as a AND gate or OR gate depending on the value set in one of the inputs as shown in Figure 3. In NML technology is possible change behavior cell changing polarity of one of the nanomagnets.

However, in nanomagnetic wire the small magnetic field generated by the first magnet is not enough to switch the

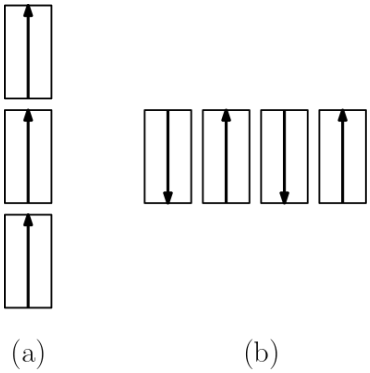

Fig. 1. (a) A ferromagnetic wire. (b) An antiferromagnetic wire.

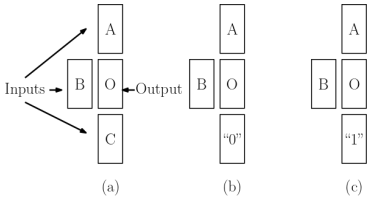

Fig. 2. (a) A NML majority gate (b) AND gate using NML majority gate. (c) OR ggate using NML majority gate

others nanomagnets. Furthermore, long nanomagnetic wires can suffer thermal noise and propagate an incorrect signal.

B. Clocking

A clock scheme is extremely important for the efficiency and effectiveness of an NML circuit [8]. The first problem that makes a clock scheme necessary is the small magnetic field that a nanomagnetic cause. Most of the time, the first nanomagnetic of a NML wire has no power to switch the other nanomagnets, as shown in Figure 3a. To solve this issue, a clock is applied temporarily for neutralize NML wire, allowing the first nanomagnetic to induce the behavior in others nanomagnets[], as shown in Figure 4.

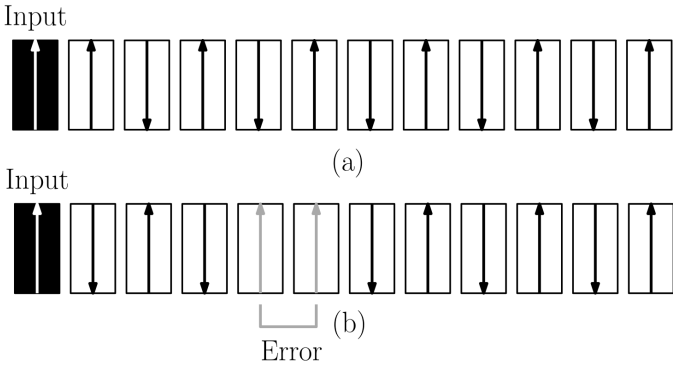

Fig. 3. (a) Small magnetic field can not switching other nanomagnets (b) Thermal noise causes inconsistency of results

Long NML wires can suffer thermal noise and transmit incorrect signals. As explained by Csaba and Porod, wires with more than 5 magnets have a high error rate due to thermal noise [9]. Figure 3c describe this problem. For solved the problem is necessary propagate the signals gradually and it can also be done using a clock scheme[]. Figure 5 show how clock scheme works in NML circuit.

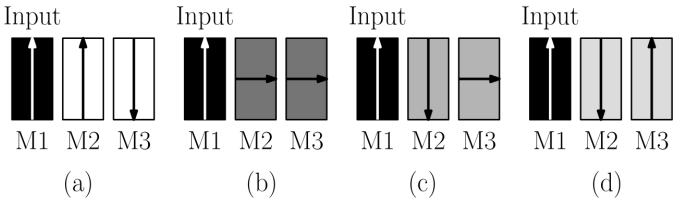

Fig. 4. (a) M1 apply magnetic fiel in M2 but nothing happens (b) Clock neutralize M2 and M3 (c) M1 changes M2 (d) M2 changes M3

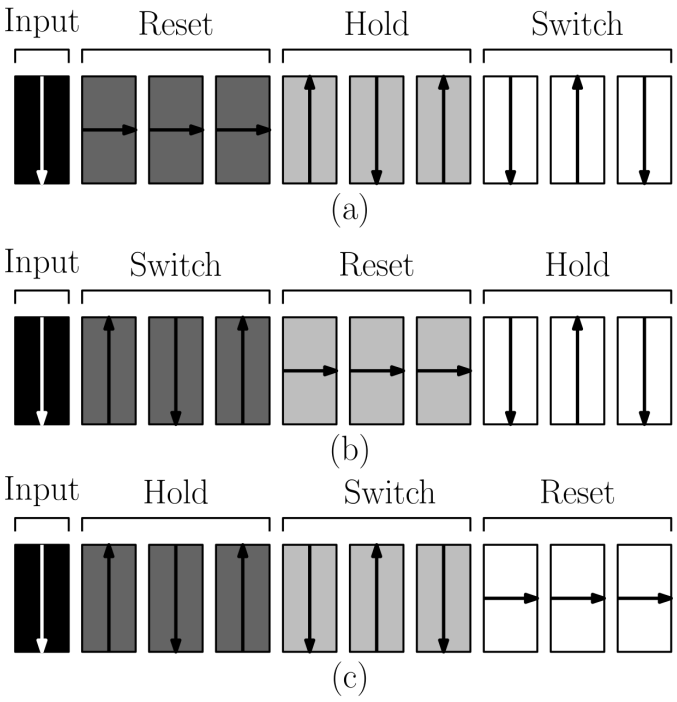

Fig. 5. The image shows how the clock causes the gradual transmission of the signal, avoiding thermal noise errors(a) Dark nanomagnetic switches dark gray nanomagnets (b) Dark gray nanomagnets switches light gray nanomagnets (c) Light gray nanomagnets switches white nanomagnets

As a result of the need for a scheme clock, conventional positioning and routing algorithms have failed to meet the demand for this technology and, therefore, research is needed to enable the creation of new placement and routing tools. To assist in this regard, we created a Nanomagnetic Logic StandardCells Library

III. Related Work

In this section we present an overview of different works related to NML and a standard cells library creation. Some of the works compared here provide a background that we relied on to create our library.

Previous works focused on QCA libraries were the inspiration for our study, especially the QCA cell library ONE,

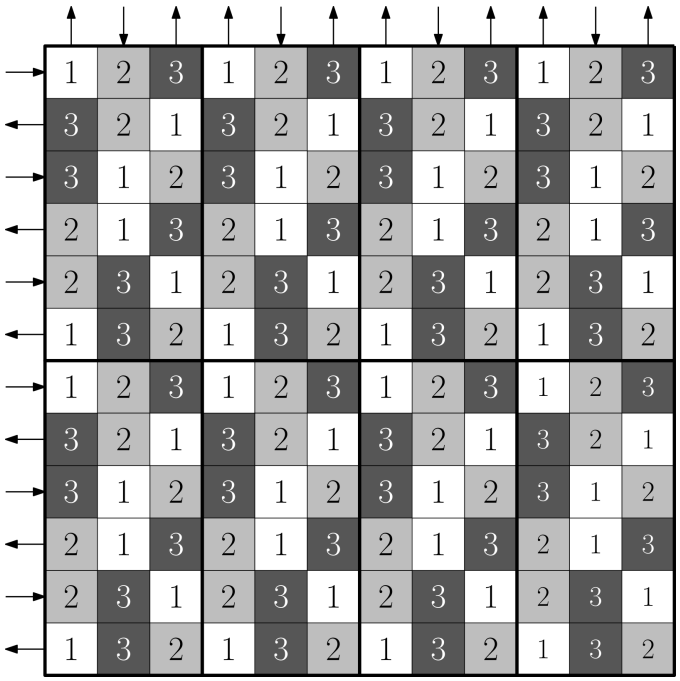

Fig. 6. Clock scheme used to build Nanomagnetic Logic Standard Cells Library

which use the USE clocking scheme, based on the principle that to establish information flow, the clock zones needs to be sequentially arranged [4]. The specifications presented in that paper were the foundation of the rules we followed to create our library. As QCA standard cells consists of a set of cells organized in a way that the desired logic function is achieved, their correct operations depends on its placement and the clocking zones organization. The process of designing the cells it is a similar work in both technologies, affirming even more their relation.

Another standard cell approach proposed for NML circuits was the MagnetoElastic, which differs from ours by using a clock mechanism based on an electric field that effectively forces magnets in the RESET state [10]. Another difference between the libraries is that their cells width and height can vary between three and five nanomagnets, while ours, in each grid of the clocking scheme that is 3x3, it can have nine nanomagnets [6], and as we use this grid to create our cells, its size can oscillate.

A different work that can be compared to ours is a implementation of NML circuits based on the physical structure of Magnetic RAM (M-RAM) which is a well-developed technology and can provide a interface with CMOS. In this paper, the authors adopted a four-phase clock scheme with a difference of 90º in each clock phase. The simulator used was the NANOcom tool that provides the possibility to simulate large architectures without the manual placement of the magnets. However it did not lead to enhanced results from area and power view. Regarding the results obtained by the bonded layout, the free layout was proposed, which is different from the classic M-RAM. As a consequence of not using word lines (except for input magnets located on the circuit border), the process is simplified, since the layer with access transistors can be eliminated, which lead to effective results on area and power [11]. It is important to highlight that this work does not propose a complete standard cells library, it only present a different way to design a cell.

It is also important to highlight another CAD tool that can be use to design NML circuits in it's both ways, iNML (in-plane) and pNML(perpendicular) [12]. The MagCAD tool that, along with ToPoliNano is a framework for design and simulation of circuits, and can be used to compare emerging technologies, fully developed in C++. It presents a tool board of basic blocks allowing the user to design the circuit by dragging and dropping these elements. A VHDL (Very High Speed Integrated Circuits Hardware Description Language) code is generated according to the circuit layout and the technology used. Once the drawing is complete, the user can choose between exporting the layout in a format compatible with ToPoliNano or export the VHDL code associated [13]. However, when exporting to ToPoliNano the user faces a limitation, since in this tool the clock zone is pre-established and it requires a specific library provided in the website, it can limitate the design of cells and circuits [14].

IV. Nanomagnetic logic standard cells library

Regardless of the technology, the cells in a computer circuit are one of its most important components, however, for each technology new ways of building these cells are proposed and, for NML, this is no different. In the same sense, the positioning and route algorithms are very dependent on these cells, as their characteristics are one of the factors responsible for modeling the final circuit. Therefore, in our standard cell library we try to specify the NML cells in the best possible way using the same parameters used in libraries of similar technology, such as the QCA ONE library for QCA technology.

Using majority gates (fundamental logical elements of NML technology) we develop the fundamental cells of boolean logic. For this, we use NMLSim 1.0 tool [5], a simple and reliable tool to validate NML circuits. We also choose BANCS (Bidirectional Alternating Nanomagnetic Clocking Scheme) [6] shown in Figure 6 to design the cells for having a lower average circuit area than other clock schemes. It is important to note that when designing cells for a clock scheme, in this case BANCS, the cells are limited to be used only in the clock scheme used to design them.

To develop the cells, we try to use the smallest possible area, respecting the clock scheme shown in Figure 6 and, therefore, some cells cannot be placed in any region of the clock scheme. Cells with delay 0 as AND, OR, NAND and NOR are not in this rule because they occupy only one region of the clock scheme.

Although fundamentally the AND and OR gates have 2 entrances, in our library these gates have 3 entrances. This is necessary because, due to the behavior of nanomagnets, with

2 inputs, it would never be possible to make a cell behave like a logic gate. As shown in Figure X, if you remove one of the AND gate entries, you will get incorrect results. So, the solution is to keep 3 entries and set one of them to 0 or 1. As shown in Figure Y, if you set one of the cell entries to 0, we will get an AND gate and, if set to 1, we will get an OR gate. The same methodology was adopted for the NAND and NOR gates, as shown in Figure Z. To develop the XOR, MUX2-1 and SR-LATCH cells, we used the fundamental AND, OR, NAND, NOR gates trying to consume the smallest possible area and always respecting the BANCS clock scheme.

A practical example of using the library can be seen in circuit c17 of Figure A and Figure B. One of the circuits was built without the aid of our library and the other uses the standard cell library. The problem with a circuit that was developed without a standard cell library is its low optimization since the logic devices are not obtained in advance, but at the time of placement and route.

To develop a registration form for the cells, we use the QCA ONE article as a reference, which presents a complete and efficient way of characterizing the cells. Figure X shows the specifications of the nml cell AND in our library. The meaning of each parameter of the figure will be detailed in the results section with more examples and the presentation of the standard cells in our library

V. Results

In this section we will present the nanomagnetic logic standard cells and area comparison of circuits using the cells. To understand results is necessary know that down arrows mean 0 and up arrows mean 1 as exemplified in Figure 5.

To specify the cells we using the same pattern as QCA ONE, a Standard Cells Library for QCA technology. The Figure 6 show a exemple of how cells were specify. The name parameter informs csll name; n_input and n_output represents number of inputs and outputs respectively; input and output parameters represents input name and output name respectively; expression mean representation of gate in boolean algebra; zone_dimension informs the width and height of one region in clock grid; width and height means the total area occupied by cell; layer contains necessary number of layers to build the cell; delay_table reports the number of cycles between cell inputs and outputs as shown in figure X; port_location informs the location of the inputs and outputs. Figure X shows how we developed the cell coordinate system.

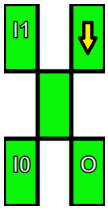

Fig. 7. AND standard cell

```
name: and

n_input: 2
n_output: 1
input: in0 in1
output: out

expression: out = in0 & in1

zone_dimension: 3

width: 3

height: 3

layers: 1

l_reference_zone: #
r_reference_zone: #

delay_table:
/  in0 in1
out 0   0

port_location:
in0 0 0 0
in1 0 2 0
out 2 2 0
```

Fig. 8. AND standard cell specification

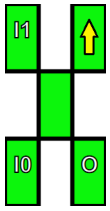

Fig. 9. OR standard cell

```
name: or

n_input: 2
n_output: 1
input: in0 in1
output: out

expression: out = in0 + in1

zone_dimension: 3

width: 3

height: 3

layers: 1

l_reference_zone: #
r_reference_zone: #

delay_table:
/  in0 in1
out 0   0

port_location:
in0 0 0 0
in1 0 2 0
out 2 2 0
```

Fig. 10. OR standard cell specification

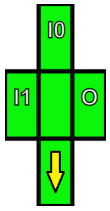

Fig. 11. NAND standard cell

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```
name: and

n_input: 2
n_output: 1
input: in0 in1
output: out

expression: out = -(in0 & in1)

zone_dimension: 3

width: 3

height: 3
```

```
layers: 1

l_reference_zone: #
r_reference_zone: #

delay_table:
/  in0 in1
out 0   0

port_location:
in0 1 2 0
in1 2 1 0
out 2 1 0
```

Fig. 12. NAND standard cell specification

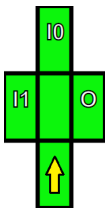

Fig. 13. NOR standard cell

```
name: and

n_input: 2
n_output: 1
input: in0 in1
output: out

expression: out = -(in0 + in1)

zone_dimension: 3

width: 3

height: 3
```

```
layers: 1

l_reference_zone: #
r_reference_zone: #

delay_table:
/  in0 in1
out 0   0

port_location:
in0 1 2 0
in1 2 1 0
out 2 1 0
```

Fig. 14. NAND standard cell specification

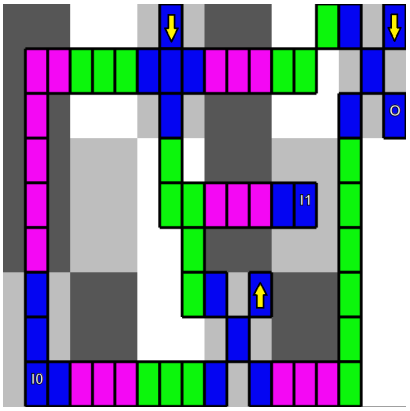

Fig. 15. XOR standard cell

```
name: and

n_input: 2
n_output: 1
input: in0 in1
output: out

expression:
out = -(in0 & in1) + (in0 + in1)

zone_dimension: 3

width: 18

height: 9
```

```
layers: 1

l_reference_zone: #
r_reference_zone: #

delay_table:
/  in0 in1
out 6   6

port_location:
in0 8 1 0
in1 13 4 0
out 18 2 0
```

Fig. 16. XOR standard cell specification

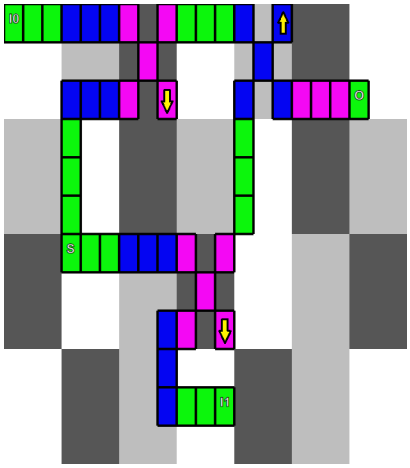

Fig. 17. MUX2-1 standard cell

```
name: mux

n_input: 3
n_output: 1
input: in0 in1 in2
output: out

expression:
out = (in0 & - in2) + (in0 & in1)

zone_dimension: 3

width: 12

height: 9
```

```
layers: 1

l_reference_zone: #
r_reference_zone: #

delay_table:
/  in0 in1 in2
out 2   2   4

port_location:
in0 3 0 0
in1 6 8 0
in2 0 6 0
out 11 2 0
```

Fig. 18. MUX2-1 standard cell specification

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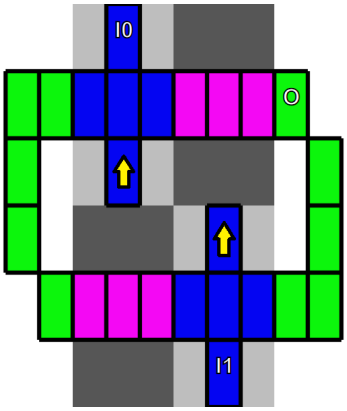

Fig. 19. SR-LATCH standard cell specification

```
name: sr_latch                          layers: 1

n_input: 2                              l_reference_zone: #
n_output: 1                             r_reference_zone: #
input: in0 in1
output: out                             delay_table:
                                        /   in0 in1
expression:                             out 2   5
out[t] = -(in0 + -out[t - 1]) + in1
                                        port_location:
zone_dimension: 3                       in0 3 0 0
                                        in1 6 5 0
width: 12                               out 8 1 0

height: 6
```

Fig. 20. SR-LATCH standard cell specification

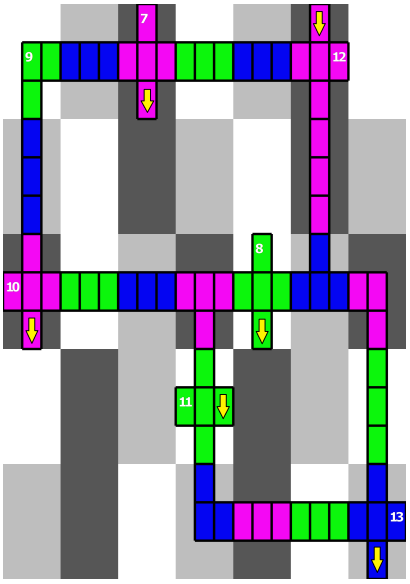

Fig. 21. C17 circuit build with our standard cells

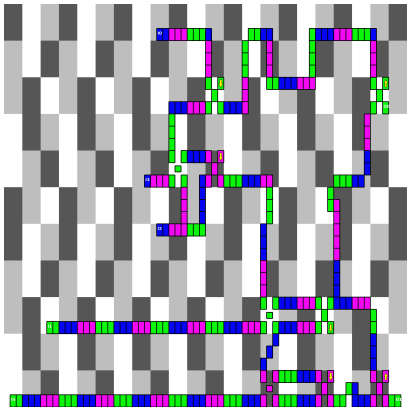

Fig. 22. C17 circuit build without our standard cells

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